

# MCF8316C-Q1 Sensorless Field Oriented Control (FOC) Integrated FET BLDC Driver

## 1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature Grade-1 :  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$
- Three-phase BLDC motor driver with integrated sensorless motor control algorithm
  - Code-free Field Oriented Control (FOC)
  - Offline motor parameters measurement with Motor Parameter Extraction Tool (MPET)
  - 5-point configurable speed profile support
  - Windmilling support through forward resynchronization and reverse drive
  - Analog, PWM, freq. or I<sup>2</sup>C based speed input
  - Configurable motor start-up and stop options
  - Anti-voltage surge (AVS) protection
  - Improved acoustic performance with soft-start, soft-stop and dead time compensation
  - Variable monitoring through DACOUT pins
- 4.5- to 35-V operating voltage (40-V abs max)
- High output current capability: 8-A peak
- Low MOSFET on-state resistance
  - $R_{DS(ON)}$  (HS + LS) at  $T_A = 25^{\circ}\text{C}$  : 95-m $\Omega$  (typ.)
- Low power sleep mode: Refer [Table 7-7](#)
  - 5- $\mu\text{A}$  (maximum) at  $V_{VM} = 24\text{-V}$ ,  $T_A = 25^{\circ}\text{C}$
- Speed loop accuracy: 3% with internal clock and 1% with external clock reference
- Customer-configurable non-volatile memory (EEPROM) to store device configuration
- Supports up to 60-kHz PWM frequency for low inductance motor support
- Does not require external current sense resistors; uses built-in current sensing
- Built-in 3.3-V, 20-mA LDO regulator
- Built-in 3.3-V/5-V, 170-mA buck regulator
- Dedicated DRVOFF pin to disable (Hi-Z) outputs
- Spread spectrum and slew rate for EMI mitigation
- Suite of integrated protection features
  - Supply under voltage lockout (UVLO)
  - Supply over voltage protection (OVP)
  - Motor lock detection (5 different types)
  - Over current protection (OCP)
  - Thermal warning and shutdown (OTW/TSD)
  - Fault condition indication pin (nFAULT)
  - Optional fault diagnostics over I<sup>2</sup>C interface

## 2 Applications

- [Automotive Fan and Blowers](#)
- [Brushless-DC \(BLDC\) Motor Modules](#)
- [Residential and Living Fans](#)
- [Air Purifiers and Humidifier Fans](#)
- [Washer and Dishwashers Pumps](#)
- [CPAP Machines](#)

## 3 Description

The MCF8316C-Q1 provides a single-chip, code-free sensorless FOC device for customers driving speed-controlled 12- to 24-V brushless-DC motors (BLDC) or Permanent Magnet Synchronous motor (PMSM) up to 8-A peak current. The MCF8316C-Q1 integrates three 1/2-bridges with 40-V absolute maximum capability and a very low  $R_{DS(ON)}$  of 95 m $\Omega$  (high-side + low-side FETs). MCF8316C-Q1 integrates power management circuits including an voltage-adjustable buck regulator (3.3 V / 5 V, 170-mA) and LDO (3.3 V / 20 mA) that can be used to power external circuits.

The FOC algorithm configuration can be stored in non-volatile EEPROM, which allows the device to operate stand-alone once the device has been configured. The device receives a speed command through a PWM input, analog voltage, variable frequency square wave or I<sup>2</sup>C command. There are a large number of protection features integrated into the MCF8316C-Q1, intended to protect the device, motor, and system against fault events.

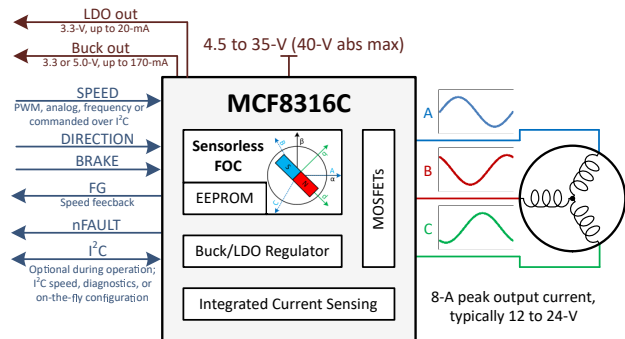
### Device Information<sup>(1)</sup>

| PART NUMBER   | PACKAGE   | BODY SIZE (NOM)   |
|---------------|-----------|-------------------|
| MCF8316C1V-Q1 | VQFN (40) | 7.00 mm x 5.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Documentation for reference:

- Refer [MCF8316C-Q1 tuning guide](#)
- Refer to the [MCF8316C-Q1 EVM GUI](#)



**Simplified Schematic**



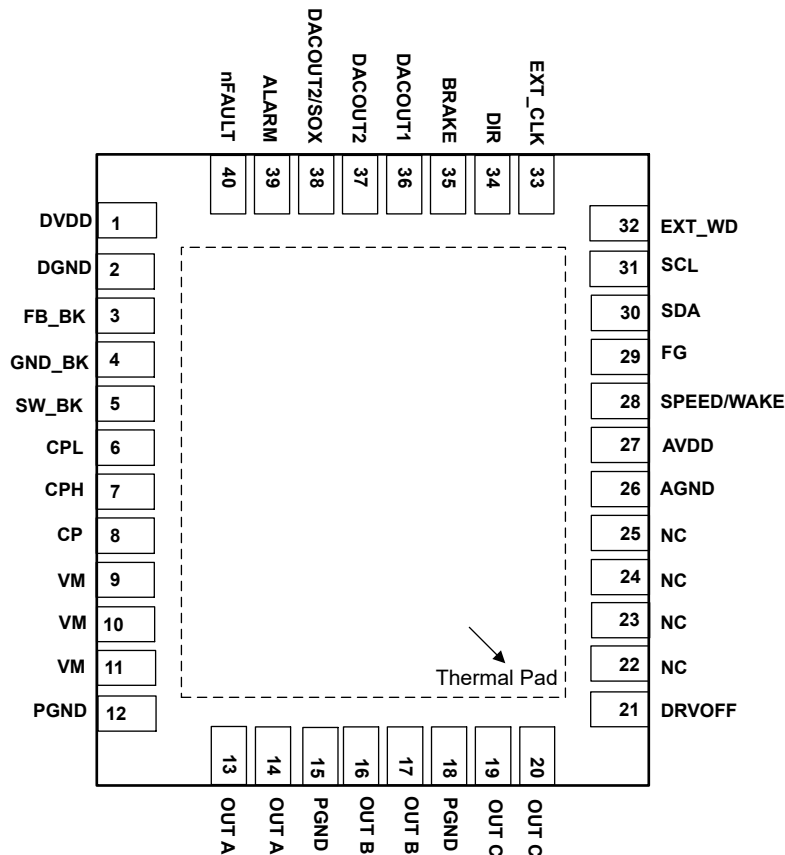
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## 4 Revision History

| DATE        | REVISION | NOTES           |
|-------------|----------|-----------------|
| August 2023 | *        | Initial Release |

## 5 Pin Configuration and Functions



**Figure 5-1. MCF8316C-Q1, 40-Pin VQFN With Exposed Thermal Pad, Top View**

**Table 5-1. Pin Functions**

| PIN     | 40-pin package | TYPE <sup>(1)</sup> | DESCRIPTION   |
|---------|----------------|---------------------|---|
| NAME    | MCF8316C-Q1    |                     |   |
| AGND    | 26             | GND                 | Device analog ground. Refer Layout Guidelines for connection recommendation.  |
| ALARM   | 39             | O                   | Alarm signal: push-pull output. Pulled logic high during fault condition, if enabled. If ALARM pin is not used, leave it floating.  |
| AVDD    | 27             | PWR O               | 3.3-V internal regulator output. Connect a X5R or X7R, 1- $\mu$ F, 6.3-V ceramic capacitor between the AVDD and AGND pins. This regulator can source up to 20 mA for external circuits.   |
| BRAKE   | 35             | I                   | High $\rightarrow$ Brake the motor<br>Low $\rightarrow$ Normal motor operation<br>If BRAKE pin is not used, connect to AGND directly.<br>If BRAKE pin is used to brake the motor, use an (optional) external 10-k $\Omega$ pull-down resistor (to AGND) for better noise rejection. |
| CP      | 8              | PWR                 | Charge pump output. Connect a X5R or X7R, 1- $\mu$ F, 16-V ceramic capacitor between the CP and VM pins.  |
| CPH     | 7              | PWR                 | Charge pump switching node. Connect a X5R or X7R, 47-nF, ceramic capacitor between the CPH and CPL pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.  |
| CPL     | 6              | PWR                 |   |
| DACOUT1 | 36             | O                   | DAC output DACOUT1  |
| DACOUT2 | 37             | O                   | DAC output DACOUT2  |

**Table 5-1. Pin Functions (continued)**

| PIN         | 40-pin package | TYPE <sup>(1)</sup> | DESCRIPTION  |
|-------------|----------------|---------------------|--|
| NAME        | MCF8316C-Q1    |                     |  |
| DACOUT2/SOX | 38             | O                   | Multi-purpose pin:<br>DAC output when configured as DACOUT2<br>CSA output when configured as SOX   |
| DGND        | 2              | GND                 | Device digital ground. Refer Layout Guidelines for connection recommendation.  |
| DIR         | 34             | I                   | Direction of motor spinning;<br>When low, phase driving sequence is OUT A → OUT C → OUT B<br>When high, phase driving sequence is OUT A → OUT B → OUT C<br>If DIR pin is not used, connect to AGND or AVDD directly (depending on phase driving sequence needed).<br>If DIR pin is used for changing motor spin direction, use an (optional) external 10-kΩ pull-down resistor (to AGND) for better noise rejection. |
| DRVOFF      | 21             | I                   | Coast (Hi-Z) all six MOSFETs as long as DRVOFF is high.<br>If DRVOFF pin is not used, connect to AGND directly.<br>If DRVOFF pin is to be used for instantly coasting (Hi-Z) the MOSFETs, use an external 10-kΩ pull-down resistor (to AGND) for better noise rejection.   |
| DVDD        | 1              | PWR                 | 1.5-V internal regulator output. Connect a X5R or X7R, 2.2-μF, 6.3-V ceramic capacitor between the DVDD and DGND pins.   |
| EXT_CLK     | 33             | I                   | External clock reference input in external clock reference mode.   |
| EXT_WD      | 32             | I                   | External watchdog input.   |
| FB_BK       | 3              | PWR I/O             | Feedback for buck regulator output control. Connect to buck regulator output after the inductor/resistor.  |
| FG          | 29             | O                   | Motor speed indicator : open-drain output that requires an external pull-up resistor to 1.8-V to 5.0-V. An optional internal pull-up resistor to AVDD is enabled by setting PULLUP_ENABLE to 1b; no external pull-up resistor should be used when internal pull-up resistor is enabled.  |
| GND_BK      | 4              | GND                 | Buck regulator ground. Refer Layout Guidelines for connection recommendation.  |
| NC          | 22, 23, 24, 25 | -                   | No connection. Leave these pins floating. These pins can also be tied to AGND plane and thermal pad for better heat dissipation.   |
| nFAULT      | 40             | O                   | Fault indicator. Pulled logic-low with fault condition; open-drain output that requires an external pull-up resistor to 1.8-V to 5.0-V. An optional internal pull-up resistor to AVDD is enabled by setting PULLUP_ENABLE to 1b; no external pull-up resistor should be used when internal pull-up resistor is enabled.  |
| OUTA        | 13, 14         | PWR O               | Half-bridge output A   |
| OUTB        | 16, 17         | PWR O               | Half-bridge output B   |
| OUTC        | 19, 20         | PWR O               | Half-bridge output C   |
| PGND        | 12, 15, 18     | GND                 | Device power ground. Refer Layout Guidelines for connection recommendation.  |
| SCL         | 31             | I                   | I <sup>2</sup> C clock input   |
| SDA         | 30             | I/O                 | I <sup>2</sup> C data line   |
| SPEED/WAKE  | 28             | I                   | Device speed input; supports analog, PWM or frequency based speed input. The speed pin input mode can be configured through SPEED_MODE.  |
| SW_BK       | 5              | PWR                 | Buck switch node. Connect this pin to an inductor or resistor.   |
| VM          | 9, 10, 11      | PWR I               | Device and motor power supply. Connect to motor supply voltage; bypass to PGND with one 0.1-μF capacitor plus one bulk capacitor. T1 recommends a capacitor voltage rating at least twice the normal operating voltage of the device.  |
| Thermal pad |                | GND                 | Must be connected to AGND.   |

(1) I = input, O = output, GND = ground, PWR = power, NC = no connect

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

|  | MIN  | MAX                   | UNIT |
|--|------|-----------------------|------|
| Power supply pin voltage (VM)  | -0.3 | 40                    | V    |
| Power supply voltage ramp (VM)   |      | 4                     | V/μs |
| Voltage difference between ground pins (GND_BK, DGND, PGND, AGND)              | -0.3 | 0.3                   | V    |
| Charge pump voltage (CPH, CP)  | -0.3 | V <sub>VM</sub> + 6   | V    |
| Charge pump negative switching pin voltage (CPL)                               | -0.3 | V <sub>VM</sub> + 0.3 | V    |
| Switching regulator pin voltage (FB_BK)  | -0.3 | 6                     | V    |
| Switching node pin voltage (SW_BK)   | -0.3 | V <sub>VM</sub> + 0.3 | V    |
| Analog regulator pin voltage (AVDD)  | -0.3 | 4                     | V    |
| Digital regulator pin voltage (DVDD)   | -0.3 | 1.7                   | V    |
| Logic pin input voltage (BRAKE, DRVOFF, DIR, EXT_CLK, EXT_WD, SCL, SDA, SPEED) | -0.3 | 6                     | V    |
| Open drain pin output voltage (nFAULT, FG)                                     | -0.3 | 6                     | V    |
| Output pin voltage (OUTA, OUTB, OUTC)  | -1   | V <sub>VM</sub> + 1   | V    |
| Ambient temperature, T <sub>A</sub>  | -40  | 125                   | °C   |
| Junction temperature, T <sub>J</sub>   | -40  | 150                   | °C   |
| Storage temperature, T <sub>stg</sub>  | -65  | 150                   | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

### 6.2 ESD Ratings Auto

|                    |                         |   | VALUE       | UNIT |      |
|--------------------|-------------------------|---|-------------|------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 <sup>(1)</sup><br>HBM ESD Classification Level 2 | ±2000       | V    |      |
|                    |                         | Charged device model (CDM), per AEC Q100-011<br>CDM ESD Classification Level C4B          | Corner pins |      | ±750 |
|                    |                         |   | Other pins  |      | ±750 |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

|                                 |                                      |  | MIN  | NOM | MAX | UNIT |
|---------------------------------|--------------------------------------|--|------|-----|-----|------|
| V <sub>VM</sub>                 | Power supply voltage                 | V <sub>VM</sub>                                      | 4.5  | 24  | 35  | V    |
| I <sub>OUT</sub> <sup>(1)</sup> | Peak output winding current          | OUTA, OUTB, OUTC                                     |      |     | 8   | A    |
| V <sub>IN_LOGIC</sub>           | Logic input voltage                  | BRAKE, DRVOFF, DIR, EXT_CLK, EXT_WD, SPEED, SDA, SCL | -0.1 |     | 5.5 | V    |
| V <sub>OD</sub>                 | Open drain pullup voltage            | nFAULT, FG   | -0.1 |     | 5.5 | V    |
| I <sub>OD</sub>                 | Open drain output current capability | nFAULT, FG   |      |     | 5   | mA   |
| T <sub>A</sub>                  | Operating ambient temperature        |  | -40  |     | 125 | °C   |
| T <sub>J</sub>                  | Operating junction temperature       |  | -40  |     | 150 | °C   |

- (1) Power dissipation and thermal limits must be observed

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | MCF8316C-Q1 | UNIT |
|-------------------------------|--|-------------|------|
|                               |  | RGF (VQFN)  |      |
|                               |  | 40 Pins     |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 25.7        | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 15.2        | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 7.3         | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.2         | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 7.2         | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 2.0         | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

at T<sub>J</sub> = –40°C to +150°C, V<sub>VM</sub> = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T<sub>A</sub> = 25°C, V<sub>VM</sub> = 24 V

| PARAMETER             |                                | TEST CONDITIONS  | MIN   | TYP  | MAX   | UNIT |
|-----------------------|--------------------------------|--|-------|------|-------|------|
| <b>POWER SUPPLIES</b> |                                |  |       |      |       |      |
| I <sub>VMQ</sub>      | VM sleep mode current          | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> = 0, T <sub>A</sub> = 25 °C  |       | 3    | 5     | μA   |
|                       |                                | V <sub>SPEED</sub> = 0, T <sub>A</sub> = 125 °C  |       | 3.5  | 7     | μA   |
| I <sub>VMS</sub>      | VM standby mode current        | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> > V <sub>EN_SB</sub> , DRVOFF = High, T <sub>A</sub> = 25 °C, L <sub>BK</sub> = 47 μH, C <sub>BK</sub> = 22 μF                                     |       | 8    | 15    | mA   |
|                       |                                | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> > V <sub>EN_SB</sub> , DRVOFF = High, R <sub>BK</sub> = 22 Ω, C <sub>BK</sub> = 22 μF  |       | 25   | 28    | mA   |
|                       |                                | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> > V <sub>EN_SB</sub> , DRVOFF = High, L <sub>BK</sub> = 47 μH, C <sub>BK</sub> = 22 μF   |       | 8    | 15    | mA   |
|                       |                                | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> > V <sub>EN_SB</sub> , DRVOFF = High, R <sub>BK</sub> = 22 Ω, C <sub>BK</sub> = 22 μF  |       | 25   | 28    | mA   |
| I <sub>VM</sub>       | VM operating mode current      | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> > V <sub>EX_SL</sub> , PWM_FREQ_OUT = 0011b (25 kHz), T <sub>J</sub> = 25 °C, L <sub>BK</sub> = 47 μH, C <sub>BK</sub> = 22 μF, No Motor Connected |       | 11   | 18    | mA   |
|                       |                                | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> > V <sub>EX_SL</sub> , PWM_FREQ_OUT = 0011b (25 kHz), T <sub>J</sub> = 25 °C, R <sub>BK</sub> = 22 Ω, C <sub>BK</sub> = 22 μF, No Motor Connected  |       | 27   | 32    | mA   |
|                       |                                | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> > V <sub>EX_SL</sub> , PWM_FREQ_OUT = 0011b (25 kHz), L <sub>BK</sub> = 47 μH, C <sub>BK</sub> = 22 μF, No Motor Connected                         |       | 11   | 17    | mA   |
|                       |                                | V <sub>VM</sub> > 6 V, V <sub>SPEED</sub> > V <sub>EX_SL</sub> , PWM_FREQ_OUT = 0011b (25 kHz), R <sub>BK</sub> = 22 Ω, C <sub>BK</sub> = 22 μF, No Motor Connected                          |       | 28   | 33    | mA   |
| V <sub>AVDD</sub>     | Analog regulator voltage       | 0 mA ≤ I <sub>AVDD</sub> ≤ 20 mA   | 3.125 | 3.3  | 3.465 | V    |
| I <sub>AVDD</sub>     | External analog regulator load |  |       |      | 20    | mA   |
| V <sub>DVDD</sub>     | Digital regulator voltage      |  | 1.4   | 1.55 | 1.65  | V    |
| V <sub>VCP</sub>      | Charge pump regulator voltage  | VCP with respect to VM   | 4.0   | 4.7  | 5.5   | V    |

at  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{VM} = 4.5$  to  $35\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^\circ\text{C}$ ,  $V_{VM} = 24\text{ V}$

| PARAMETER             |   | TEST CONDITIONS  | MIN  | TYP  | MAX                 | UNIT |
|-----------------------|---|--|------|--|---------------------|------|
| <b>BUCK REGULATOR</b> |   |  |      |  |                     |      |
| $V_{BK}$              | Buck regulator average voltage<br>( $L_{BK} = 47\ \mu\text{H}$ , $C_{BK} = 22\ \mu\text{F}$ ) | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 170\text{ mA}$ ,<br>BUCK_SEL = 00b   | 3.1  | 3.3  | 3.5                 | V    |
|                       |   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 170\text{ mA}$ ,<br>BUCK_SEL = 01b   | 4.6  | 5.0  | 5.4                 | V    |
|                       |   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 170\text{ mA}$ ,<br>BUCK_SEL = 10b   | 3.7  | 4.0  | 4.3                 | V    |
|                       |   | $V_{VM} > 6.7\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 170\text{ mA}$ ,<br>BUCK_SEL = 11b   | 5.2  | 5.7  | 5.8                 | V    |
|                       |   | $V_{VM} < 6.0\text{ V}$ (BUCK_SEL = 00b, 01b,<br>10b, 11b), $0\text{ mA} \leq I_{BK} \leq 170\text{ mA}$   |      | $V_{VM} - I_{BK} \cdot (R_{LBK} + 2)$ <sup>1</sup>   |                     | V    |
| $V_{BK}$              | Buck regulator average voltage<br>( $L_{BK} = 22\ \mu\text{H}$ , $C_{BK} = 22\ \mu\text{F}$ ) | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 20\text{ mA}$ ,<br>BUCK_SEL = 00b  | 3.1  | 3.3  | 3.5                 | V    |
|                       |   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 20\text{ mA}$ ,<br>BUCK_SEL = 01b  | 4.6  | 5.0  | 5.4                 | V    |
|                       |   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 20\text{ mA}$ ,<br>BUCK_SEL = 10b  | 3.7  | 4.0  | 4.3                 | V    |
|                       |   | $V_{VM} > 6.7\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 20\text{ mA}$ ,<br>BUCK_SEL = 11b  | 5.2  | 5.7  | 5.8                 | V    |
|                       |   | $V_{VM} < 6.0\text{ V}$ (BUCK_SEL = 00b, 01b,<br>10b, 11b), $0\text{ mA} \leq I_{BK} \leq 20\text{ mA}$  |      | $V_{VM} - I_{BK} \cdot (R_{LBK} + 2)$ <sup>1</sup>   |                     | V    |
| $V_{BK}$              | Buck regulator average voltage<br>( $R_{BK} = 22\ \Omega$ , $C_{BK} = 22\ \mu\text{F}$ )      | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 10\text{ mA}$ ,<br>BUCK_SEL = 00b  | 3.1  | 3.3  | 3.5                 | V    |
|                       |   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 10\text{ mA}$ ,<br>BUCK_SEL = 01b  | 4.6  | 5.0  | 5.4                 | V    |
|                       |   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 10\text{ mA}$ ,<br>BUCK_SEL = 10b  | 3.7  | 4.0  | 4.3                 | V    |
|                       |   | $V_{VM} > 6.7\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 10\text{ mA}$ ,<br>BUCK_SEL = 11b  | 5.2  | 5.7  | 5.8                 | V    |
|                       |   | $V_{VM} < 6.0\text{ V}$ (BUCK_SEL = 00b, 01b,<br>10b, 11b), $0\text{ mA} \leq I_{BK} \leq 10\text{ mA}$  |      | $V_{VM} - I_{BK} \cdot (R_{LBK} + 2)$ <sup>(1)</sup> |                     | V    |
| $V_{BK\_RIP}$         | Buck regulator ripple voltage   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 170\text{ mA}$ , Buck<br>regulator with inductor, $L_{BK} = 47\ \mu\text{H}$ , $C_{BK}$<br>$= 22\ \mu\text{F}$ | -100 |  | 100                 | mV   |
|                       |   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 20\text{ mA}$ , Buck<br>regulator with inductor, $L_{BK} = 22\ \mu\text{H}$ , $C_{BK}$<br>$= 22\ \mu\text{F}$  | -100 |  | 100                 | mV   |
|                       |   | $V_{VM} > 6\text{ V}$ , $0\text{ mA} \leq I_{BK} \leq 10\text{ mA}$ , Buck<br>regulator with resistor, $R_{BK} = 22\ \Omega$ , $C_{BK} =$<br>$22\ \mu\text{F}$       | -100 |  | 100                 | mV   |
| $I_{BK}$              | External buck regulator load  | $L_{BK} = 47\ \mu\text{H}$ , $C_{BK} = 22\ \mu\text{F}$ ,<br>BUCK_PS_DIS = 1b  |      |  | 170                 | mA   |
|                       |   | $L_{BK} = 47\ \mu\text{H}$ , $C_{BK} = 22\ \mu\text{F}$ ,<br>BUCK_PS_DIS = 0b  |      |  | 170 –<br>$I_{AVDD}$ | mA   |
|                       |   | $L_{BK} = 22\ \mu\text{H}$ , $C_{BK} = 22\ \mu\text{F}$ ,<br>BUCK_PS_DIS = 1b  |      |  | 20                  | mA   |
|                       |   | $L_{BK} = 22\ \mu\text{H}$ , $C_{BK} = 22\ \mu\text{F}$ ,<br>BUCK_PS_DIS = 0b  |      |  | 20 –<br>$I_{AVDD}$  | mA   |
|                       |   | $R_{BK} = 22\ \Omega$ , $C_{BK} = 22\ \mu\text{F}$ ,<br>BUCK_PS_DIS = 1b   |      |  | 10                  | mA   |
|                       |   | $R_{BK} = 22\ \Omega$ , $C_{BK} = 22\ \mu\text{F}$ ,<br>BUCK_PS_DIS = 0b   |      |  | 10 –<br>$I_{AVDD}$  | mA   |

at  $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{VM} = 4.5$  to  $35\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^{\circ}\text{C}$ ,  $V_{VM} = 24\text{ V}$

| PARAMETER                |   | TEST CONDITIONS  | MIN | TYP | MAX  | UNIT             |
|--------------------------|---|--|-----|-----|------|------------------|
| $f_{\text{SW\_BK}}$      | Buck regulator switching frequency                                    | Regulation Mode  | 20  |     | 535  | kHz              |
|                          |   | Linear Mode  | 20  |     | 535  | kHz              |
| $V_{\text{BK\_UV}}$      | Buck regulator undervoltage lockout                                   | $V_{\text{BK}}$ rising, BUCK_SEL = 00b   | 2.7 | 2.8 | 2.95 | V                |
|                          |   | $V_{\text{BK}}$ falling, BUCK_SEL = 00b  | 2.5 | 2.6 | 2.7  | V                |
|                          |   | $V_{\text{BK}}$ rising, BUCK_SEL = 01b   | 4.3 | 4.4 | 4.55 | V                |
|                          |   | $V_{\text{BK}}$ falling, BUCK_SEL = 01b  | 4.1 | 4.2 | 4.38 | V                |
|                          |   | $V_{\text{BK}}$ rising, BUCK_SEL = 10b   | 2.7 | 2.8 | 2.95 | V                |
|                          |   | $V_{\text{BK}}$ falling, BUCK_SEL = 10b  | 2.5 | 2.6 | 2.7  | V                |
|                          |   | $V_{\text{BK}}$ rising, BUCK_SEL = 11b   | 4.3 | 4.4 | 4.55 | V                |
|                          |   | $V_{\text{BK}}$ falling, BUCK_SEL = 11b  | 4.1 | 4.2 | 4.38 | V                |
| $V_{\text{BK\_UV\_HYS}}$ | Buck regulator undervoltage lockout hysteresis                        | Rising to falling threshold, BUCK_SEL = 00b  | 90  | 200 | 400  | mV               |
|                          |   | Rising to falling threshold, BUCK_SEL = 01b  | 90  | 200 | 400  | mV               |
|                          |   | Rising to falling threshold, BUCK_SEL = 10b  | 90  | 200 | 400  | mV               |
|                          |   | Rising to falling threshold, BUCK_SEL = 11b  | 90  | 200 | 400  | mV               |
| $I_{\text{BK\_CL}}$      | Buck regulator current limit threshold                                | BUCK_CL = 0b   | 360 | 600 | 910  | mA               |
|                          |   | BUCK_CL = 1b   | 80  | 150 | 260  | mA               |
| $I_{\text{BK\_OCP}}$     | Buck regulator overcurrent protection trip point                      |  | 2   | 3   | 4    | A                |
| $t_{\text{BK\_RETRY}}$   | Overcurrent protection retry time                                     |  | 0.7 | 1   | 1.3  | ms               |
| <b>DRIVER OUTPUTS</b>    |   |  |     |     |      |                  |
| $R_{\text{DS(ON)}}$      | Total MOSFET on resistance (High-side + Low-side)                     | $V_{\text{VM}} > 6\text{ V}$ , $I_{\text{OUT}} = 1\text{ A}$ , $T_A = 25^{\circ}\text{C}$  |     | 95  | 125  | m $\Omega$       |
|                          |   | $V_{\text{VM}} < 6\text{ V}$ , $I_{\text{OUT}} = 1\text{ A}$ , $T_A = 25^{\circ}\text{C}$  |     | 105 | 130  | m $\Omega$       |
|                          |   | $V_{\text{VM}} > 6\text{ V}$ , $I_{\text{OUT}} = 1\text{ A}$ , $T_J = 150^{\circ}\text{C}$ |     | 140 | 185  | m $\Omega$       |
|                          |   | $V_{\text{VM}} < 6\text{ V}$ , $I_{\text{OUT}} = 1\text{ A}$ , $T_J = 150^{\circ}\text{C}$ |     | 145 | 190  | m $\Omega$       |
| SR                       | Phase pin slew rate switching low to high (Rising from 20 % to 80 %)  | $V_{\text{VM}} = 24\text{ V}$ , SLEW_RATE = 10b  | 80  | 125 | 185  | V/ $\mu\text{s}$ |
|                          |   | $V_{\text{VM}} = 24\text{ V}$ , SLEW_RATE = 11b  | 130 | 200 | 280  | V/ $\mu\text{s}$ |
| SR                       | Phase pin slew rate switching high to low (Falling from 80 % to 20 %) | $V_{\text{VM}} = 24\text{ V}$ , SLEW_RATE = 10b  | 80  | 125 | 185  | V/ $\mu\text{s}$ |
|                          |   | $V_{\text{VM}} = 24\text{ V}$ , SLEW_RATE = 11b  | 110 | 200 | 280  | V/ $\mu\text{s}$ |
| $t_{\text{DEAD}}$        | Output dead time (high to low / low to high)                          | $V_{\text{VM}} = 24\text{ V}$ , SLEW_RATE = 10b  |     | 650 | 1000 | ns               |
|                          |   | $V_{\text{VM}} = 24\text{ V}$ , SLEW_RATE = 11b  |     | 500 | 750  | ns               |



at  $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{VM} = 4.5$  to  $35\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^{\circ}\text{C}$ ,  $V_{VM} = 24\text{ V}$

| PARAMETER                           |  | TEST CONDITIONS   | MIN   | TYP  | MAX   | UNIT          |
|-------------------------------------|--|---|-------|------|-------|---------------|
| <b>SPEED INPUT - PWM MODE</b>       |  |   |       |      |       |               |
| $f_{PWM}$                           | PWM input frequency                                      |   | 0.01  |      | 100   | kHz           |
| $Res_{PWM}$                         | PWM input resolution                                     | $0.01\text{ kHz} \leq f_{PWM} < 0.35\text{ kHz}$  | 11    | 12   | 13    | bits          |
|                                     |  | $0.35\text{ kHz} \leq f_{PWM} < 2\text{ kHz}$   | 12    | 13   | 14    | bits          |
|                                     |  | $2\text{ kHz} \leq f_{PWM} < 3.5\text{ kHz}$  | 11    | 11.5 | 12    | bits          |
|                                     |  | $3.5\text{ kHz} \leq f_{PWM} < 7\text{ kHz}$  | 13    | 13.5 | 14    | bits          |
|                                     |  | $7\text{ kHz} \leq f_{PWM} < 14\text{ kHz}$   | 12    | 12.5 | 13    | bits          |
|                                     |  | $14\text{ kHz} \leq f_{PWM} < 29.3\text{ kHz}$  | 11    | 11.5 | 12    | bits          |
|                                     |  | $29.3\text{ kHz} \leq f_{PWM} < 60\text{ kHz}$  | 10    | 10.5 | 11    | bits          |
|                                     |  | $60\text{ kHz} \leq f_{PWM} \leq 100\text{ kHz}$  | 8     | 9    | 10    | bits          |
| <b>SPEED INPUT - ANALOG MODE</b>    |  |   |       |      |       |               |
| $V_{ANA\_FS}$                       | Analog full-speed voltage                                |   | 2.95  | 3    | 3.05  | V             |
| $V_{ANA\_RES}$                      | Analog voltage resolution                                |   |       | 732  |       | $\mu\text{V}$ |
| <b>SPEED INPUT - FREQUENCY MODE</b> |  |   |       |      |       |               |
| $f_{PWM\_FREQ}$                     | PWM input frequency range                                | Duty cycle = 50%  | 3     |      | 32767 | Hz            |
| <b>SLEEP MODE</b>                   |  |   |       |      |       |               |
| $V_{EN\_SL}$                        | Analog voltage to enter sleep state                      | $SPEED\_MODE = 00b$ (analog mode)   |       |      | 40    | mV            |
| $V_{EX\_SL}$                        | Analog voltage to exit sleep state                       | $SPEED\_MODE = 00b$ (analog mode)   | 2.2   |      |       | V             |
| $t_{DET\_ANA}$                      | Time needed to detect wake-up signal on SPEED pin        | $SPEED\_MODE = 00b$ (analog mode)<br>$V_{SPEED} > V_{EX\_SL}$   | 0.5   | 1    | 1.5   | $\mu\text{s}$ |
| $t_{WAKE}$                          | Wake-up time from sleep state                            | $V_{SPEED} > V_{EX\_SL}$ to DVDD voltage available, $SPEED\_MODE = 01b$ (PWM mode)                          |       | 3    | 5     | ms            |
| $t_{EX\_SL\_DR\_ANA}$               | Time taken to drive motor after wake-up from sleep state | $SPEED\_MODE = 00b$ (analog mode), DVDD voltage available to first output PWM pulse, ISD detection disabled |       |      | 20    | ms            |
| $t_{DET\_PWM}$                      | Time needed to detect wake-up signal on SPEED pin        | $SPEED\_MODE = 01b$ (PWM mode)<br>$V_{SPEED} > V_{IH}$  | 0.5   | 1    | 1.5   | $\mu\text{s}$ |
| $t_{WAKE\_PWM}$                     | Wake-up time from sleep state                            | $V_{SPEED} > V_{IH}$ to DVDD voltage available, $SPEED\_MODE = 01b$ (PWM mode)                              |       | 3    | 5     | ms            |
| $t_{EX\_SL\_DR\_PWM}$               | Time taken to drive motor after wake-up from sleep state | $SPEED\_MODE = 01b$ (PWM mode), DVDD voltage available to first output PWM pulse, ISD detection disabled    |       |      | 20    | ms            |
| $t_{DET\_SL\_ANA}$                  | Time needed to detect sleep command                      | $SPEED\_MODE = 00b$ (analog mode), $V_{SPEED} < V_{EN\_SL}$ , $SLEEP\_ENTRY\_TIME = 00b$                    | 0.035 | 0.05 | 0.065 | ms            |
|                                     |  | $SPEED\_MODE = 00b$ (analog mode), $V_{SPEED} < V_{EN\_SL}$ , $SLEEP\_ENTRY\_TIME = 01b$                    | 0.14  | 0.2  | 0.26  | ms            |
|                                     |  | $SPEED\_MODE = 00b$ (analog mode), $V_{SPEED} < V_{EN\_SL}$ , $SLEEP\_ENTRY\_TIME = 10b$                    | 14    | 20   | 26    | ms            |
|                                     |  | $SPEED\_MODE = 00b$ (analog mode), $V_{SPEED} < V_{EN\_SL}$ , $SLEEP\_ENTRY\_TIME = 11b$                    | 140   | 200  | 260   | ms            |

at  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{VM} = 4.5$  to  $35\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^\circ\text{C}$ ,  $V_{VM} = 24\text{ V}$

| PARAMETER                 |   | TEST CONDITIONS   | MIN   | TYP  | MAX   | UNIT |
|---------------------------|---|---|-------|------|-------|------|
| $t_{\text{DET\_SL\_PWM}}$ | Time needed to detect sleep command                             | SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{\text{SPEED}} < V_{\text{IL}}$ , SLEEP_ENTRY_TIME = 00b  | 0.035 | 0.05 | 0.065 | ms   |
|                           |   | SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{\text{SPEED}} < V_{\text{IL}}$ , SLEEP_ENTRY_TIME = 01b  | 0.14  | 0.2  | 0.26  | ms   |
|                           |   | SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{\text{SPEED}} < V_{\text{IL}}$ , SLEEP_ENTRY_TIME = 10b  | 14    | 20   | 26    | ms   |
|                           |   | SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{\text{SPEED}} < V_{\text{IL}}$ , SLEEP_ENTRY_TIME = 11b  | 140   | 200  | 260   | ms   |
| $t_{\text{EN\_SL}}$       | Time needed to stop driving motor after detecting sleep command | $V_{\text{SPEED}} < V_{\text{EN\_SL}}$ (analog mode) or $V_{\text{SPEED}} < V_{\text{IL}}$ (PWM mode or Frequency mode) or $V_{\text{SPEED}} < V_{\text{IL}}$ and DIGITAL_SPEED_CTRL = 0b (I <sup>2</sup> C mode) |       | 1    | 2     | ms   |

at  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{VM} = 4.5$  to  $35\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^\circ\text{C}$ ,  $V_{VM} = 24\text{ V}$

| PARAMETER  |   | TEST CONDITIONS   | MIN                  | TYP  | MAX                  | UNIT          |
|--|---|---|----------------------|------|----------------------|---------------|
| <b>STANDBY MODE</b>  |   |   |                      |      |                      |               |
| $t_{EX\_SB\_DR\_ANA}$  | Time taken to drive motor after exiting standby state             | SPEED_MODE = 00b (analog mode)<br>$V_{SPEED} > V_{EX\_SB}$ , ISD detection disabled   |                      |      | 6                    | ms            |
| $t_{EX\_SB\_DR\_PWM}$  | Time taken to drive motor after exiting standby state             | SPEED_MODE = 01b (PWM mode)<br>$V_{SPEED} > V_{IH}$ , ISD detection disabled  |                      |      | 6                    | ms            |
| $t_{DET\_SB\_ANA}$   | Time needed to detect standby command                             | SPEED_MODE = 00b (analog mode)<br>$V_{SPEED} < V_{EN\_SB}$  | 0.5                  | 1    | 2                    | ms            |
| $t_{EN\_SB\_PWM}$  | Time needed to detect standby command                             | SPEED_MODE = 01b (PWM mode)<br>$V_{SPEED} < V_{IL}$ , SLEEP_ENTRY_TIME = 00b  | 0.035                | 0.05 | 0.065                | ms            |
|  |   | SPEED_MODE = 01b (PWM mode)<br>$V_{SPEED} < V_{IL}$ , SLEEP_ENTRY_TIME = 01b  | 0.14                 | 0.2  | 0.26                 | ms            |
|  |   | SPEED_MODE = 01b (PWM mode)<br>$V_{SPEED} < V_{IL}$ , SLEEP_ENTRY_TIME = 10b  | 14                   | 20   | 26                   | ms            |
|  |   | SPEED_MODE = 01b (PWM mode)<br>$V_{SPEED} < V_{IL}$ , SLEEP_ENTRY_TIME = 11b  | 140                  | 200  | 260                  | ms            |
| $t_{EN\_SB\_DIG}$  | Time needed to detect standby command                             | SPEED_MODE = 10b (I <sup>2</sup> C mode), DIGITAL_SPEED_CTRL = 0b   |                      | 1    | 2                    | ms            |
| $t_{EN\_SB\_FREQ}$   | Time needed to detect standby command                             | SPEED_MODE = 11b (Frequency mode), $V_{SPEED} < V_{IL}$   |                      | 4000 |                      | ms            |
| $t_{EN\_SB}$   | Time needed to stop driving motor after detecting standby command | $V_{SPEED} < V_{EN\_SL}$ (analog mode) or $V_{SPEED} < V_{IL}$ (PWM or Frequency mode) or DIGITAL_SPEED_CTRL = 0b (I <sup>2</sup> C mode) |                      | 1    | 2                    | ms            |
| <b>LOGIC-LEVEL INPUTS (BRAKE, DIR, EXT_CLK, EXT_WD, SCL, SDA, SPEED)</b> |   |   |                      |      |                      |               |
| $V_{IL}$   | Input logic low voltage   | AVDD = 3 to 3.6 V   |                      |      | $0.25 \cdot AV_{DD}$ | V             |
| $V_{IH}$   | Input logic high voltage  | AVDD = 3 to 3.6 V   |                      |      | $0.65 \cdot AV_{DD}$ | V             |
| $V_{HYS}$  | Input hysteresis  |   | 50                   | 500  | 800                  | mV            |
| $I_{IL}$   | Input logic low current   | AVDD = 3 to 3.6 V   | -0.15                |      | 0.15                 | $\mu\text{A}$ |
| $I_{IH}$   | Input logic high current  | AVDD = 3 to 3.6 V   | -0.4                 |      | 0.15                 | $\mu\text{A}$ |
| $R_{PD\_SPEED}$  | Input pulldown resistance   | SPEED pin To GND  | 0.6                  | 1    | 1.4                  | M $\Omega$    |
| <b>OPEN-DRAIN OUTPUTS (nFAULT, FG)</b>                                   |   |   |                      |      |                      |               |
| $V_{OL}$   | Output logic low voltage  | $I_{OD} = -5\text{ mA}$   |                      |      | 0.4                  | V             |
| $I_{OZ}$   | Output logic high current   | $V_{OD} = 3.3\text{ V}$   | 0                    |      | 0.5                  | $\mu\text{A}$ |
| <b>I<sup>2</sup>C Serial Interface</b>                                   |   |   |                      |      |                      |               |
| $V_{I2C\_L}$   | LOW-level input voltage   |   | -0.5                 |      | $0.3 \cdot AV_{DD}$  | V             |
| $V_{I2C\_H}$   | HIGH-level input voltage  |   | $0.7 \cdot AV_{DD}$  |      | 5.5                  | V             |
| $V_{I2C\_HYS}$   | Hysteresis  |   | $0.05 \cdot AV_{DD}$ |      |                      | V             |
| $V_{I2C\_OL}$  | LOW-level output voltage  | open-drain at 2mA sink current  | 0                    |      | 0.4                  | V             |
| $I_{I2C\_OL}$  | LOW-level output current  | $V_{I2C\_OL} = 0.6\text{ V}$  |                      |      | 6                    | mA            |
| $I_{I2C\_IL}$  | Input current on SDA and SCL                                      |   | $-10^2$              |      | $10^2$               | $\mu\text{A}$ |
| $C_i$  | Capacitance for SDA and SCL                                       |   |                      |      | 10                   | pF            |

at  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{VM} = 4.5$  to  $35\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^\circ\text{C}$ ,  $V_{VM} = 24\text{ V}$

| PARAMETER                  |  | TEST CONDITIONS                          | MIN  | TYP   | MAX              | UNIT          |
|----------------------------|--|--|------|-------|------------------|---------------|
| $t_{of}$                   | Output fall time from $V_{I2C\_H}(\text{min})$ to $V_{I2C\_L}(\text{max})$ | Standard Mode                            |      |       | 250 <sup>3</sup> | ns            |
|                            |  | Fast Mode                                |      |       | 250 <sup>3</sup> | ns            |
| $t_{SP}$                   | Pulse width of spikes that must be suppressed by the input filter          | Fast Mode                                | 0    |       | 50 <sup>4</sup>  | ns            |
| <b>OSCILLATOR</b>          |  |  |      |       |                  |               |
| $f_{OSCREF}$               | External clock reference   | EXT_CLK_CONFIG = 000b                    |      | 8     |                  | kHz           |
|                            |  | EXT_CLK_CONFIG = 001b                    |      | 16    |                  | kHz           |
|                            |  | EXT_CLK_CONFIG = 010b                    |      | 32    |                  | kHz           |
|                            |  | EXT_CLK_CONFIG = 011b                    |      | 64    |                  | kHz           |
|                            |  | EXT_CLK_CONFIG = 100b                    |      | 128   |                  | kHz           |
|                            |  | EXT_CLK_CONFIG = 101b                    |      | 256   |                  | kHz           |
|                            |  | EXT_CLK_CONFIG = 110b                    |      | 512   |                  | kHz           |
|                            |  | EXT_CLK_CONFIG = 111b                    |      | 1024  |                  | kHz           |
| <b>EEPROM</b>              |  |  |      |       |                  |               |
| $EE_{Prog}$                | Programming voltage  |  | 1.35 | 1.5   | 1.65             | V             |
| $EE_{RET}$                 | Retention  | $T_A = 25^\circ\text{C}$                 |      | 100   |                  | Years         |
|                            |  | $T_J = -40$ to $150^\circ\text{C}$       |      | 10    |                  | Years         |
| $EE_{END}$                 | Endurance  | $T_J = -40$ to $150^\circ\text{C}$       |      | 1000  |                  | Cycles        |
|                            |  | $T_J = -40$ to $85^\circ\text{C}$        |      | 20000 |                  | Cycles        |
| <b>PROTECTION CIRCUITS</b> |  |  |      |       |                  |               |
| $V_{UVLO}$                 | Supply undervoltage lockout (UVLO)   | VM rising                                | 4.3  | 4.4   | 4.5              | V             |
|                            |  | VM falling                               | 4.1  | 4.2   | 4.3              | V             |
| $V_{UVLO\_HYS}$            | Supply undervoltage lockout hysteresis                                     | Rising to falling threshold              | 110  | 200   | 350              | mV            |
| $t_{UVLO}$                 | Supply undervoltage deglitch time  |  | 3    | 5     | 7                | $\mu\text{s}$ |
| $V_{OVP}$                  | Supply overvoltage protection (OVP)  | Supply rising, OVP_EN = 1, OVP_SEL = 0   | 32.5 | 34    | 35               | V             |
|                            |  | Supply falling, OVP_EN = 1, OVP_SEL = 0  | 31.8 | 33    | 34.3             | V             |
|                            |  | Supply rising, OVP_EN = 1, OVP_SEL = 1   | 20   | 22    | 23               | V             |
|                            |  | Supply falling, OVP_EN = 1, OVP_SEL = 1  | 19   | 21    | 22               | V             |
| $V_{OVP\_HYS}$             | Supply overvoltage protection (OVP)  | Rising to falling threshold, OVP_SEL = 1 | 0.9  | 1     | 1.1              | V             |
|                            |  | Rising to falling threshold, OVP_SEL = 0 | 0.7  | 0.8   | 0.9              | V             |
| $t_{OVP}$                  | Supply overvoltage deglitch time   |  | 2.5  | 5     | 7                | $\mu\text{s}$ |
| $V_{CPUV}$                 | Charge pump undervoltage lockout (above VM)                                | Supply rising                            | 2.25 | 2.5   | 2.75             | V             |
|                            |  | Supply falling                           | 2.2  | 2.4   | 2.6              | V             |
| $V_{CPUV\_HYS}$            | Charge pump UVLO hysteresis  | Rising to falling threshold              | 65   | 100   | 150              | mV            |
| $V_{AVDD\_UV}$             | Analog regulator undervoltage lockout                                      | Supply rising                            | 2.7  | 2.85  | 3                | V             |
|                            |  | Supply falling                           | 2.5  | 2.65  | 2.8              | V             |
| $V_{AVDD\_UV\_HYS}$        | Analog regulator undervoltage lockout hysteresis                           | Rising to falling threshold              | 180  | 200   | 240              | mV            |
| $I_{OCP}$                  | Overcurrent protection trip point  | OCP_LVL = 0b                             | 9.5  | 16    | 22               | A             |
|                            |  | OCP_LVL = 1b                             | 15   | 24    | 28               | A             |

at  $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{VM} = 4.5$  to  $35\text{ V}$  (unless otherwise noted). Typical limits apply for  $T_A = 25^{\circ}\text{C}$ ,  $V_{VM} = 24\text{ V}$

| PARAMETER                   |                                      | TEST CONDITIONS           | MIN  | TYP | MAX | UNIT               |
|-----------------------------|--------------------------------------|---------------------------|------|-----|-----|--------------------|
| $t_{\text{OCP}}$            | Overcurrent protection deglitch time | OCP_DEG = 00b             | 0.02 | 0.2 | 0.4 | $\mu\text{s}$      |
|                             |                                      | OCP_DEG = 01b             | 0.2  | 0.6 | 1.2 | $\mu\text{s}$      |
|                             |                                      | OCP_DEG = 10b             | 0.5  | 1.2 | 1.8 | $\mu\text{s}$      |
|                             |                                      | OCP_DEG = 11b             | 0.9  | 1.6 | 2.5 | $\mu\text{s}$      |
| $t_{\text{RETRY}}$          | Overcurrent protection retry time    |                           | 425  | 500 | 575 | ms                 |
| $T_{\text{OTW}}$            | Thermal warning temperature          | Die temperature ( $T_J$ ) | 135  | 145 | 155 | $^{\circ}\text{C}$ |
| $T_{\text{OTW\_HYS}}$       | Thermal warning hysteresis           | Die temperature ( $T_J$ ) | 15   | 20  | 25  | $^{\circ}\text{C}$ |
| $T_{\text{TSD\_BUCK}}$      | Thermal shutdown temperature (Buck)  | Die temperature ( $T_J$ ) | 170  | 180 | 190 | $^{\circ}\text{C}$ |
| $T_{\text{TSD\_BUCK\_HYS}}$ | Thermal shutdown hysteresis (Buck)   | Die temperature ( $T_J$ ) | 15   | 20  | 25  | $^{\circ}\text{C}$ |
| $T_{\text{TSD\_FET}}$       | Thermal shutdown temperature (FET)   | Die temperature ( $T_J$ ) | 165  | 175 | 185 | $^{\circ}\text{C}$ |
| $T_{\text{TSD\_FET\_HYS}}$  | Thermal shutdown hysteresis (FET)    | Die temperature ( $T_J$ ) | 20   | 25  | 30  | $^{\circ}\text{C}$ |

- (1)  $R_{\text{LBK}}$  is resistance of inductor  $L_{\text{BK}}$
- (2) If AVDD is switched off, I/O pins must not obstruct the SDA and SCL lines.
- (3) The maximum  $t_f$  for the SDA and SCL bus lines (300 ns) is longer than the specified maximum  $t_{\text{of}}$  for the output stages (250 ns). This allows series protection resistors ( $R_s$ ) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified  $t_f$ .
- (4) Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns

## 6.6 Characteristics of the SDA and SCL bus for Standard and Fast mode

over operating free-air temperature range (unless otherwise noted)

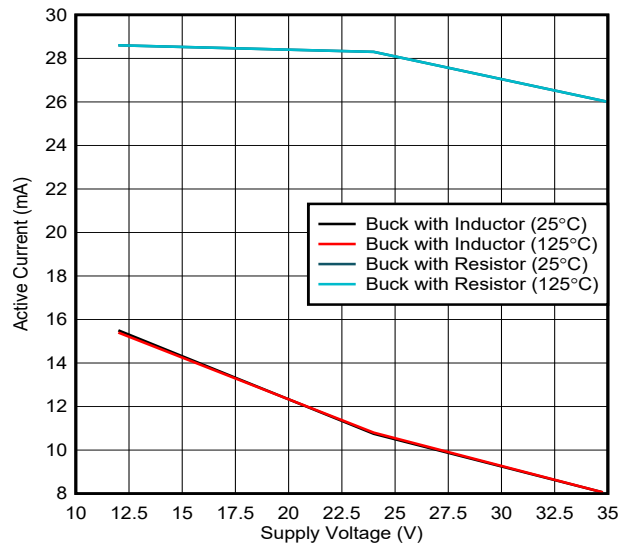
| PARAMETER            |  | TEST CONDITIONS                                       | MIN              | NOM | MAX                 | UNIT          |
|----------------------|--|---|------------------|-----|---------------------|---------------|
| <b>Standard-mode</b> |  |   |                  |     |                     |               |
| $f_{\text{SCL}}$     | SCL clock frequency  |   | 0                |     | 100                 | kHz           |
| $t_{\text{HD\_STA}}$ | Hold time (repeated) START condition   | After this period, the first clock pulse is generated | 4                |     |                     | $\mu\text{s}$ |
| $t_{\text{LOW}}$     | LOW period of the SCL clock  |   | 4.7              |     |                     | $\mu\text{s}$ |
| $t_{\text{HIGH}}$    | HIGH period of the SCL clock   |   | 4                |     |                     | $\mu\text{s}$ |
| $t_{\text{SU\_STA}}$ | Set-up time for a repeated START condition   |   | 4.7              |     |                     | $\mu\text{s}$ |
| $t_{\text{HD\_DAT}}$ | Data hold time <sup>(2)</sup>  | I2C bus devices                                       | 0 <sup>(3)</sup> |     | <sup>(4)</sup>      | $\mu\text{s}$ |
| $t_{\text{SU\_DAT}}$ | Data set-up time   |   | 250              |     |                     | ns            |
| $t_r$                | Rise time for both SDA and SCL signals   |   |                  |     | 1000                | ns            |
| $t_f$                | Fall time of both SDA and SCL signals <sup>(3)</sup><br><sup>(6)</sup> <sup>(7)</sup> <sup>(8)</sup> |   |                  |     | 300                 | ns            |
| $t_{\text{SU\_STO}}$ | Set-up time for STOP condition   |   | 4                |     |                     | $\mu\text{s}$ |
| $t_{\text{BUF}}$     | Bus free time between STOP and START condition   |   | 4.7              |     |                     | $\mu\text{s}$ |
| $C_b$                | Capacitive load for each bus line <sup>(9)</sup>   |   |                  |     | 400                 | pF            |
| $t_{\text{VD\_DAT}}$ | Data valid time <sup>(10)</sup>  |   |                  |     | 3.45 <sup>(4)</sup> | $\mu\text{s}$ |
| $t_{\text{VD\_ACK}}$ | Data valid acknowledge time <sup>(11)</sup>  |   |                  |     | 3.45 <sup>(4)</sup> | $\mu\text{s}$ |
| $V_{\text{nL}}$      | Noise margin at the LOW level  | For each connected device (including hysteresis)      | 0.1*AVD<br>D     |     |                     | V             |
| $V_{\text{nh}}$      | Noise margin at the HIGH level   | For each connected device (including hysteresis)      | 0.2*AVD<br>D     |     |                     | V             |
| <b>Fast-mode</b>     |  |   |                  |     |                     |               |
| $f_{\text{SCL}}$     | SCL clock frequency  |   | 0                |     | 400                 | KHz           |

over operating free-air temperature range (unless otherwise noted)

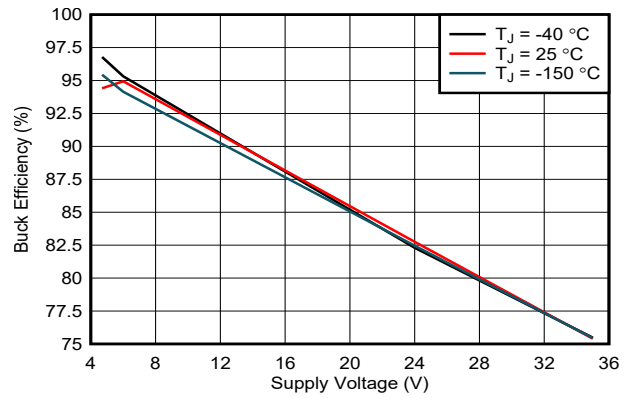
| PARAMETER           |  | TEST CONDITIONS                                       | MIN                     | NOM | MAX                | UNIT |
|---------------------|--|---|-------------------------|-----|--------------------|------|
| t <sub>HD_STA</sub> | Hold time (repeated) START condition   | After this period, the first clock pulse is generated | 0.6                     |     |                    | µs   |
| t <sub>LOW</sub>    | LOW period of the SCL clock  |   | 1.3                     |     |                    | µs   |
| t <sub>HIGH</sub>   | HIGH period of the SCL clock   |   | 0.6                     |     |                    | µs   |
| t <sub>SU_STA</sub> | Set-up time for a repeated START condition   |   | 0.6                     |     |                    | µs   |
| t <sub>HD_DAT</sub> | Data hold time <sup>(2)</sup>  |   | 0 <sup>(3)</sup>        |     | <sup>(4)</sup>     | µs   |
| t <sub>SU_DAT</sub> | Data set-up time   |   | 100 <sup>(5)</sup>      |     |                    | ns   |
| t <sub>r</sub>      | Rise time for both SDA and SCL signals   |   | 20                      |     | 300                | ns   |
| t <sub>f</sub>      | Fall time of both SDA and SCL signals <sup>(3)</sup><br><sup>(6)</sup> <sup>(7)</sup> <sup>(8)</sup> |   | 20 x<br>(AVDD/<br>5.5V) |     | 300                | ns   |
| t <sub>SU_STO</sub> | Set-up time for STOP condition   |   | 0.6                     |     |                    | µs   |
| t <sub>BUF</sub>    | Bus free time between STOP and START condition   |   | 1.3                     |     |                    | µs   |
| C <sub>b</sub>      | Capacitive load for each bus line <sup>(9)</sup>   |   |                         |     | 400                | pF   |
| t <sub>VD_DAT</sub> | Data valid time <sup>(10)</sup>  |   |                         |     | 0.9 <sup>(4)</sup> | µs   |
| t <sub>VD_ACK</sub> | Data valid acknowledge time <sup>(11)</sup>  |   |                         |     | 0.9 <sup>(4)</sup> | µs   |
| V <sub>nL</sub>     | Noise margin at the LOW level  | For each connected device (including hysteresis)      | 0.1*AVD<br>D            |     |                    | V    |
| V <sub>nh</sub>     | Noise margin at the HIGH level   | For each connected device (including hysteresis)      | 0.2*AVD<br>D            |     |                    | V    |

- (1) All values referred to V<sub>IH(min)</sub> and V<sub>IL(max)</sub> levels
- (2) t<sub>HD\_DAT</sub> is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
- (3) A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V<sub>IH(min)</sub> of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- (4) The maximum t<sub>HD\_DAT</sub> could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode, but must be less than the maximum of t<sub>VD\_DAT</sub> or t<sub>VD\_ACK</sub> by a transition time. This maximum must only be met if the device does not stretch the LOW period (t<sub>LOW</sub>) of the SCL signal. If the clock stretched the SCL, the data must be valid by the set-up time before it releases the clock.
- (5) A fast-mode I<sup>2</sup>C-bus device can be used in a standard-mode I<sup>2</sup>C-bus system, but the requirement t<sub>SU\_DAT</sub> 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t<sub>r(max)</sub> + t<sub>SU\_DAT</sub> = 1000 + 250 = 1250 ns (according to the standard-mode I<sup>2</sup>C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.
- (6) If mixed with HS-mode devices, faster fall times according to Table 10 are allowed.
- (7) The maximum t<sub>f</sub> for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t<sub>f</sub> is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t<sub>f</sub>.
- (8) In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
- (9) The maximum bus capacitance allowable may vary from the value depending on the actual operating voltage and frequency of the application.
- (10) t<sub>VD\_DAT</sub> = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
- (11) t<sub>VD\_ACK</sub> = time for acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

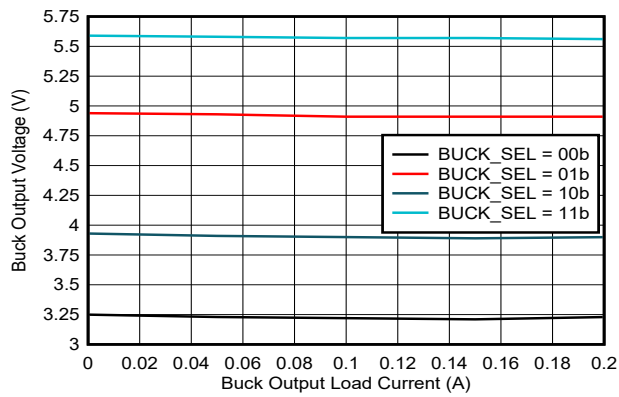
## 6.7 Typical Characteristics



**Figure 6-1. Supply current over supply voltage**



**Figure 6-2. Buck regulator efficiency over supply voltage**



**Figure 6-3. Buck regulator output voltage over load current**

## 7 Detailed Description

### 7.1 Overview

The MCF8316C-Q1 provides a single-chip, code-free sensorless FOC solution for customers driving speed-controlled 12- to 24-V brushless-DC motors requiring up to 8-A peak phase currents.

The MCF8316C-Q1 integrates three  $\frac{1}{2}$ -bridges with 40-V absolute maximum capability and a very low  $R_{DS(ON)}$  of 95-m $\Omega$  (high-side + low-side) to enable high power drive capability. Current is sensed using an integrated current sensing circuit which eliminates the need for external sense resistors. Power management features of an adjustable buck regulator and LDO generate the necessary voltage rails for the device and can also be used to power external circuits.

MCF8316C-Q1 implements sensorless FOC, and so an external microcontroller is not required to spin the brushless-DC motor. The algorithm is implemented in a fixed-function state machine, so no coding is needed. The algorithm is highly configurable through register settings ranging from motor start-up behavior to closed loop operation. Register settings can be stored in non-volatile EEPROM, which allows the device to operate stand-alone once it has been configured. The device receives a speed command through a PWM input, analog voltage, frequency input or I<sup>2</sup>C command.

In-built protection features include power-supply under voltage lockout (UVLO), charge-pump under voltage lockout (CPUV), over current protection (OCP), AVDD under voltage lockout (AVDD\_UV), buck regulator UVLO, motor lock detection and over temperature warning and shutdown (OTW and TSD). Fault events are indicated by the nFAULT pin with detailed fault information available in the registers.

The MCF8316C-Q1 device is available in a 0.5-mm pin pitch, VQFN surface-mount package. The VQFN package size is 7 mm x 5 mm with a height of 1 mm.



## 7.2 Functional Block Diagram

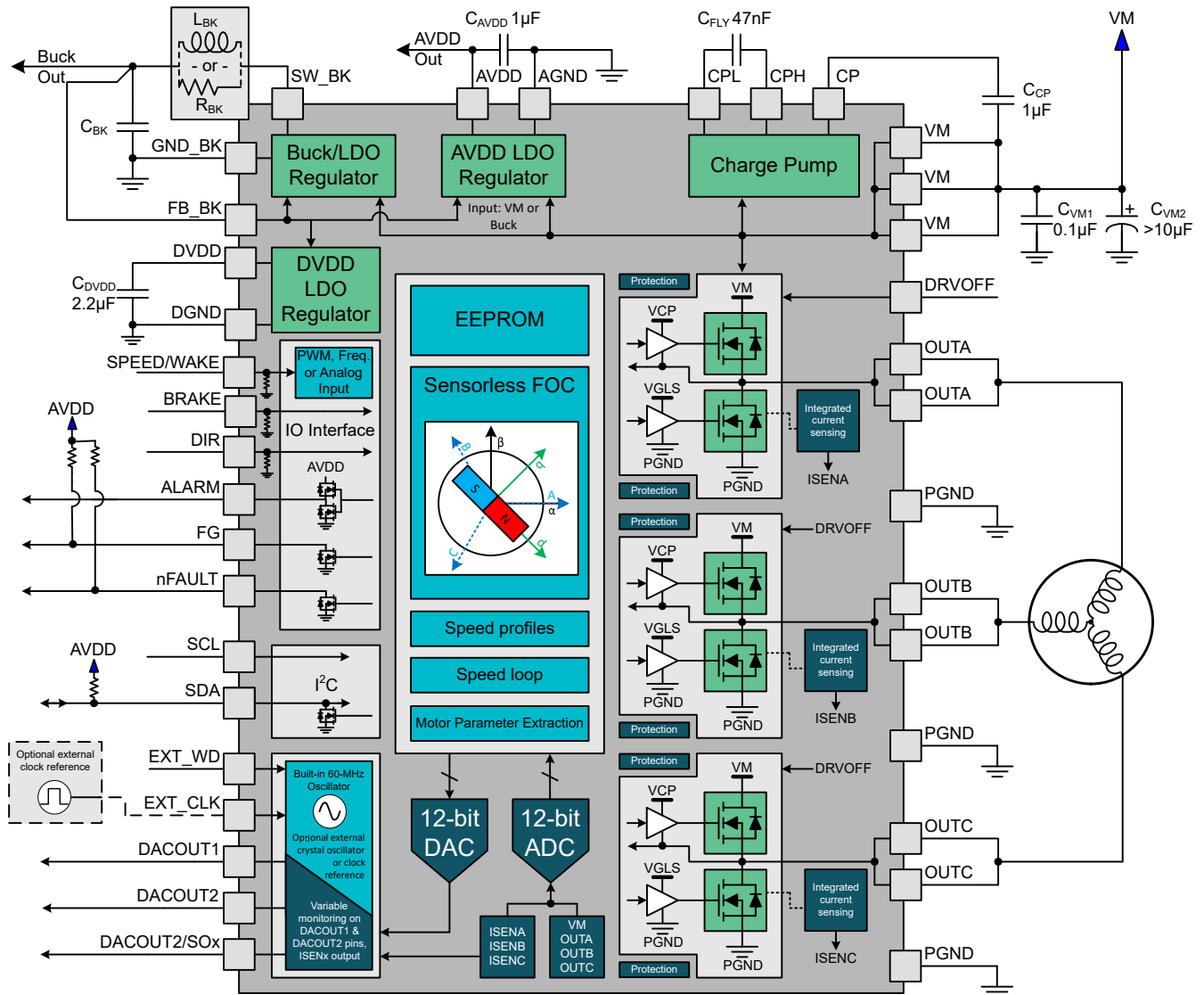


Figure 7-1. MCF8316C-Q1 Functional Block Diagram

## 7.3 Feature Description

### 7.3.1 Output Stage

The MCF8316C-Q1 consists of integrated 95-m $\Omega$  (combined high-side and low-side FETs' on-state resistance) NMOS FETs connected in a three-phase bridge configuration. A doubler charge pump provides the proper gate-bias voltage to the high-side NMOS FETs across a wide operating voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs.

### 7.3.2 Device Interface

The MCF8316C-Q1 supports I<sup>2</sup>C interface to provide end application design with adequate flexibility. MCF8316C-Q1 allows controlling the motor operation and system through BRAKE, DRVOFF, DIR, EXT\_CLK, EXT\_WD and SPEED/WAKE pins. MCF8316C-Q1 also provides different signals for monitoring system variables, speed, fault and phase current feedback through DACOUT1, DACOUT2, FG, nFAULT and SOX pins.

#### 7.3.2.1 Interface - Control and Monitoring

##### Motor Control Signals

- SPEED/WAKE pin is used to control the motor speed and to wake up MCF8316C-Q1 from sleep. SPEED pin can be configured to accept PWM, frequency or analog input signals. It is also used to enter and exit from sleep and standby mode (see [Table 7-7](#)).
- When BRAKE pin is driven 'High', MCF8316C-Q1 enters brake state. Brake state can be configured to either low side brake (see [Low-Side Braking](#)) or align brake (see [Align Braking](#)) through BRAKE\_PIN\_MODE. MCF8316C-Q1 decreases output speed to value defined by BRAKE\_SPEED\_THRESHOLD before entering brake state. As long as BRAKE is driven 'High', MCF8316C-Q1 stays in brake state. Brake pin input can be overwritten by configuring BRAKE\_INPUT over the I<sup>2</sup>C interface.
- The DIR pin decides the direction of motor spin; when driven 'High', the sequence is OUT A → OUT B → OUT C, and when driven 'Low', the sequence is OUT A → OUT C → OUT B. DIR pin input can be overwritten by configuring DIR\_INPUT over the I<sup>2</sup>C interface.
- When DRVOFF pin is driven 'High', MCF8316C-Q1 stops driving the motor by turning OFF (Hi-Z) all MOSFETs (coast state) - this could be accompanied by faults like no motor or abnormal BEMF. When DRVOFF is driven 'Low', MCF8316C-Q1 returns to normal state of operation, as if it was restarting the motor (see [DRVOFF Functionality](#)). DRVOFF does not cause the device to go to sleep or standby mode; the digital core is still active. Entry and exit from sleep or standby condition is controlled by SPEED pin.

##### External Oscillator and Watchdog Signals

- EXT\_CLK pin can be used to provide an external clock reference (see [External Clock Source](#)).
- EXT\_WD pin can be used to provide an external watchdog signal (see [External Watchdog](#)).

##### Output Signals

- DACOUT1 outputs internal variable defined by address in register DACOUT1\_VAR\_ADDR. DACOUT1 is refreshed every PWM cycle (see [DAC outputs](#)).
- DACOUT2 outputs internal variable defined by address in register DACOUT2\_VAR\_ADDR. DACOUT2 is refreshed every PWM cycle (see [DAC outputs](#)).
- FG pin provides pulses which are proportional to motor speed (see [FG Configuration](#)).
- nFAULT (active low) pin provides fault status in device or motor operation.
- ALARM pin, when enabled using ALARM\_PIN\_EN, provides fault status in device or motor operation as an active high signal. When ALARM pin is enabled, report only faults are reported only on ALARM pin (as logic high) and not reported on nFAULT pin (as logic low). When ALARM pin is enabled, actionable faults are reported on ALARM pin (as logic high) as well as on nFAULT pin (as logic low). When ALARM pin is disabled, it is in Hi-Z state and all faults (actionable and report only) are reported on nFAULT as logic low. ALARM pin should be left floating when unused/disabled.
- SOX pin provides the output of one of the current sense amplifiers.

### Note

1. Internal pull-up resistor (to AVDD) for both FG and nFAULT pins can be enabled by configuring PULLUP\_ENABLE to 1b. Any change to this bit needs to be written to EEPROM followed by a power recycle to take effect. When PULLUP\_ENABLE is set to 1b, no external pull-up resistor should be provided.
2. DIR and BRAKE pins each have an internal pull-down resistor of 100-kΩ. When these pins are used, an additional pull-down resistor of 10-kΩ may be added externally for additional noise immunity.
3. SPEED pin has an internal pull-down resistor of 1-MΩ. In analog speed input mode, a suitable R-C filter can be added externally for reducing noise. In PWM speed input mode, SPEED\_PIN\_GLITCH\_FILTER can be appropriately configured for glitch rejection.

### 7.3.2.2 I<sup>2</sup>C Interface

The MCF8316C-Q1 supports an I<sup>2</sup>C serial communication interface that allows an external controller to send and receive data. This I<sup>2</sup>C interface lets the external controller to configure the EEPROM and read detailed fault and motor state information. The pull-down strength of the I<sup>2</sup>C pins can be configured using SLEW\_RATE\_I2C\_PINS. The I<sup>2</sup>C bus is a two-wire interface using the SCL and SDA pins which are described as follows :

- The SCL pin is the clock signal input.
- The SDA pin is the data input and output.

### 7.3.3 Step-Down Mixed-Mode Buck Regulator

The MCF8316C-Q1 has an integrated mixed-mode buck regulator to supply regulated 3.3-V or 5-V power for an external controller or system voltage rail. Additionally, the buck output can also be configured to 4-V or 5.7-V for supporting the extra headroom for an external LDO for generating a 3.3-V or 5-V supplies. The output voltage of the buck is set by BUCK\_SEL.

The buck regulator has a low quiescent current of ~1-2 mA during light loads to prolong battery life. The device improves performance during line and load transients by implementing a pulse-frequency current-mode control scheme which requires less output capacitance and simplifies frequency compensation design.

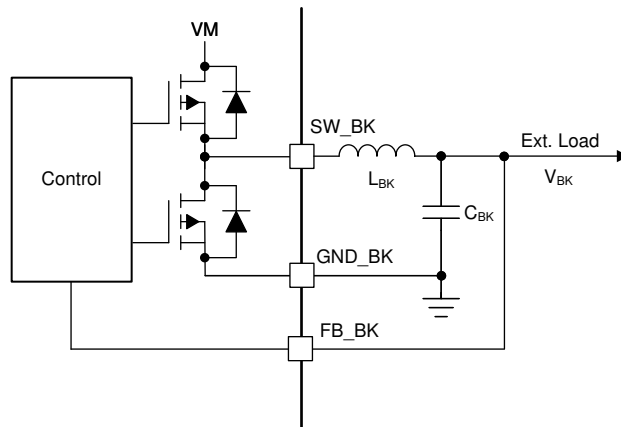
**Table 7-1. Recommended settings for Buck Regulator**

| Buck Mode        | Buck output voltage | Max output current from AVDD (I <sub>AVDD_MAX</sub> ) | Max output current from Buck (I <sub>BK_MAX</sub> ) | Buck current limit    | AVDD power sequencing            |
|------------------|---------------------|---|---|-----------------------|----------------------------------|
| Inductor - 47 μH | 3.3-V or 4-V        | 20 mA   | 170 mA - I <sub>AVDD</sub>                          | 600 mA (BUCK_CL = 0b) | Not supported (BUCK_PS_DIS = 1b) |
| Inductor - 47 μH | 5-V or 5.7-V        | 20 mA   | 170 mA - I <sub>AVDD</sub>                          | 600 mA (BUCK_CL = 0b) | Supported (BUCK_PS_DIS = 0b)     |
| Inductor - 22 μH | 5-V or 5.7-V        | 20 mA   | 20 mA - I <sub>AVDD</sub>                           | 150 mA (BUCK_CL = 1b) | Not supported (BUCK_PS_DIS = 1b) |
| Inductor - 22 μH | 3.3-V or 4-V        | 20 mA   | 20 mA - I <sub>AVDD</sub>                           | 150 mA (BUCK_CL = 1b) | Supported (BUCK_PS_DIS = 0b)     |
| Resistor - 22 Ω  | 5-V or 5.7-V        | 20 mA   | 10 mA - I <sub>AVDD</sub>                           | 150 mA (BUCK_CL = 1b) | Not supported (BUCK_PS_DIS = 1b) |
| Resistor - 22 Ω  | 3.3-V or 4-V        | 20 mA   | 10 mA - I <sub>AVDD</sub>                           | 150 mA (BUCK_CL = 1b) | Supported (BUCK_PS_DIS = 0b)     |

#### 7.3.3.1 Buck in Inductor Mode

The buck regulator in MCF8316C-Q1 is primarily designed to support low inductance of 47-μH and 22-μH. A 47-μH inductor allows the buck regulator to operate up to 170-mA load current support, whereas applications requiring current up to 20-mA can use a 22-μH inductor which saves component size.

Figure 7-2 shows the connection of buck regulator in inductor mode.

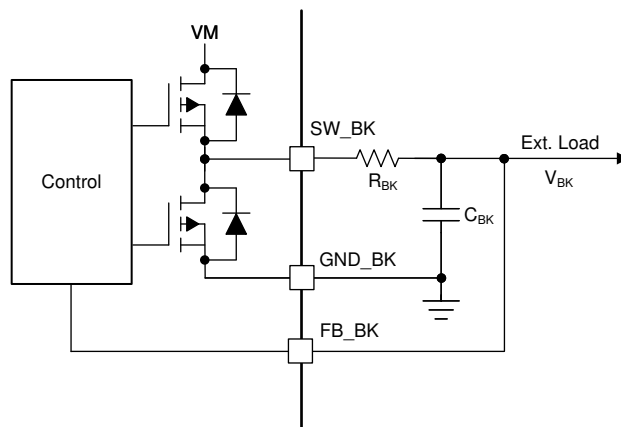


**Figure 7-2. Buck (Inductor Mode)**

### 7.3.3.2 Buck in Resistor mode

If the external load requirement is less than 10-mA, the inductor can be replaced with a resistor. In resistor mode the power is dissipated across the external resistor and the efficiency is lower than buck in inductor mode.

Figure 7-3 shows the connection of buck in resistor mode.



**Figure 7-3. Buck (Resistor Mode)**

### 7.3.3.3 Buck Regulator with External LDO

The buck regulator also supports the voltage requirement to supply an external LDO to generate standard 3.3-V or 5-V output rail with higher accuracies. The buck output voltage should be configured to 4-V or 5.7-V to provide extra headroom to support the external LDO for generating 3.3-V or 5-V rail as shown in Figure 7-4. This allows for a lower-voltage LDO design to save cost and better thermal management due to low drop-out voltage.

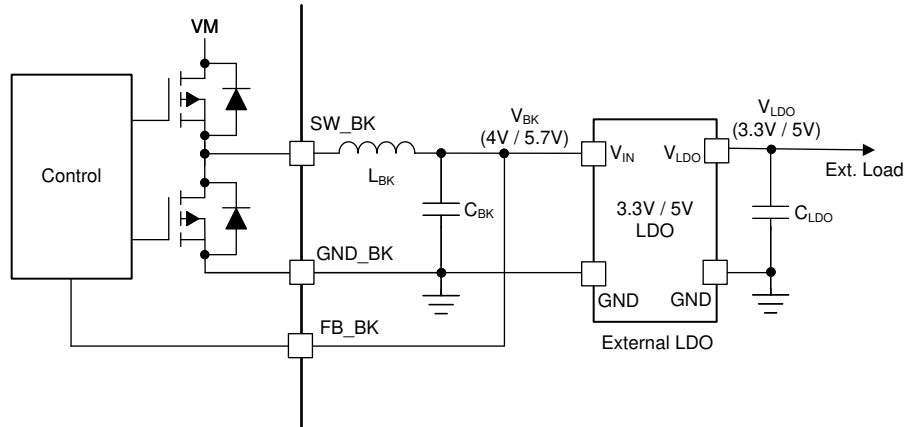


Figure 7-4. Buck Regulator with External LDO

### 7.3.3.4 AVDD Power Sequencing from Buck Regulator

The AVDD LDO has an option of using the power supply from mixed mode buck regulator to reduce the device power dissipation. The power sequencing mode allows on-the-fly changeover of AVDD LDO input from DC mains (VM) to buck output ( $V_{BK}$ ) as shown in Figure 7-5. This sequencing can be configured through the BUCK\_PS\_DIS bit. Power sequencing is supported only when buck output voltage is set to 5-V or 5.7-V.

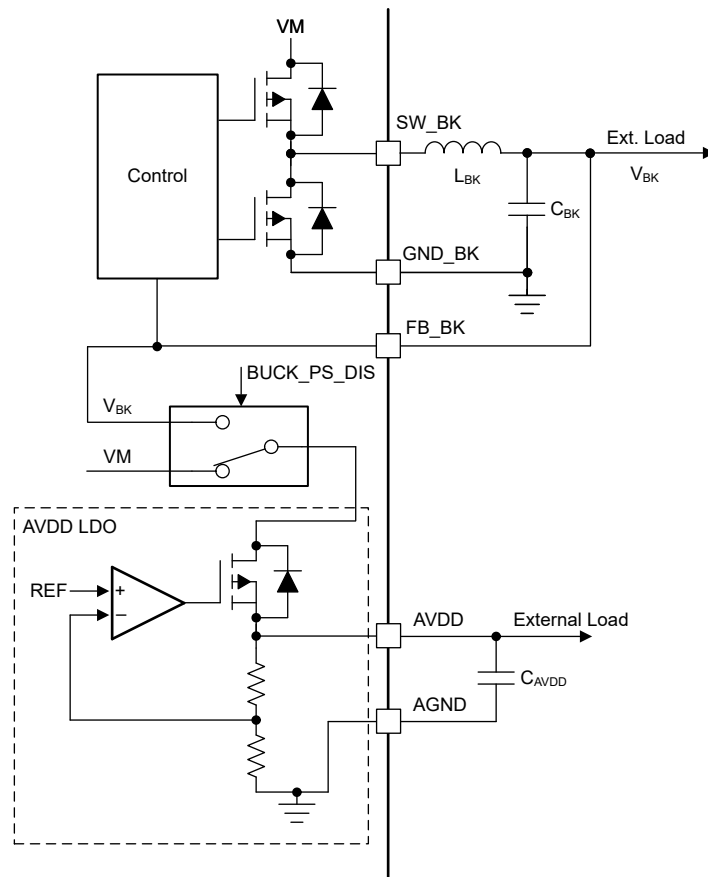


Figure 7-5. AVDD Power Sequencing from Mixed Mode Buck Regulator

### 7.3.3.5 Mixed Mode Buck Operation and Control

The buck regulator implements a pulse frequency modulation (PFM) architecture with peak current mode control. The output voltage of the buck regulator is compared with the internal reference voltage ( $V_{BK\_REF}$ ) which is internally generated depending on the buck output voltage setting (BUCK\_SEL) which constitutes an outer voltage control loop. Depending on the comparator output going high ( $V_{BK} < V_{BK\_REF}$ ) or low ( $V_{BK} > V_{BK\_REF}$ ), the high-side power FET of the buck turns on and off respectively. An independent current control loop monitors the current in high-side power FET ( $I_{BK}$ ) and turns off the high-side FET when the current becomes higher than the buck current limit ( $I_{BK\_CL}$  set by BUCK\_CL) - this implements a current limit control for the buck regulator. Figure 7-6 shows the architecture of the buck and various control/protection loops.

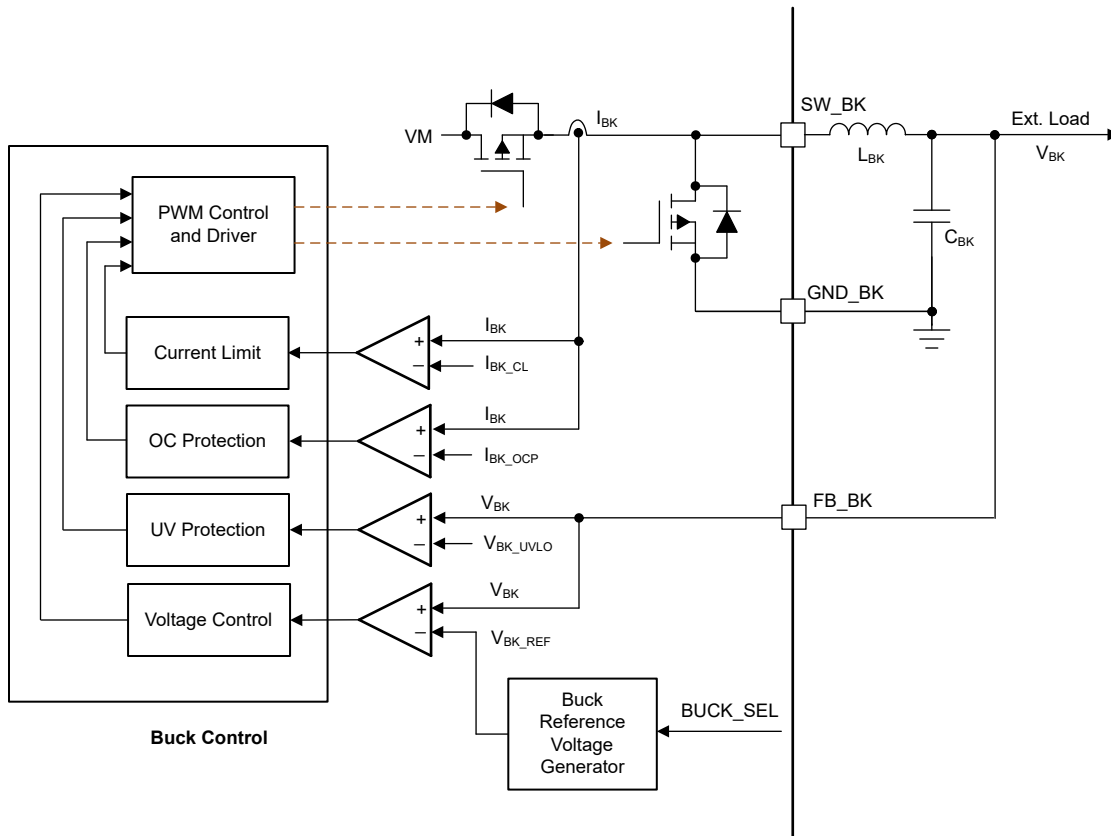
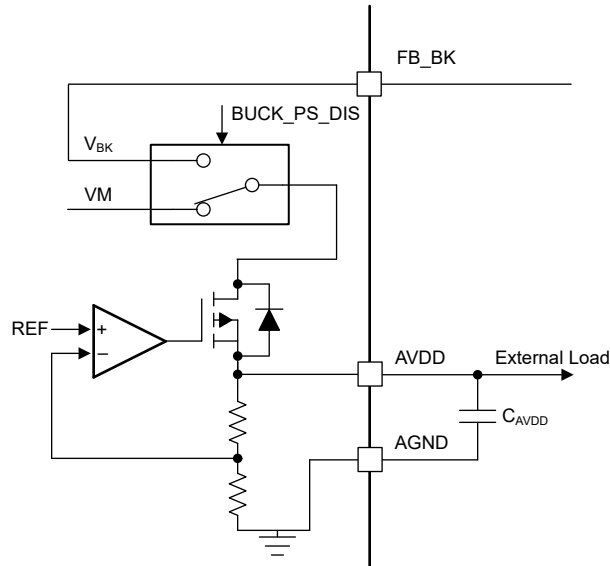


Figure 7-6. Buck Operation and Control Loops

### 7.3.4 AVDD Linear Voltage Regulator

A 3.3-V linear regulator is integrated into MCF8316C-Q1 and is available for use by external circuitry. This AVDD LDO regulator is used for powering up the internal circuitry of the device and additionally, this regulator can also provide the supply voltage for a low-power MCU or other external circuitry supporting up to 20-mA. The output of the AVDD regulator should be bypassed near the AVDD pin with a X5R or X7R, 1- $\mu$ F, 6.3-V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The AVDD nominal, no-load output voltage is 3.3-V.



**Figure 7-7. AVDD Linear Regulator Block Diagram**

Use [Equation 1](#) to calculate the power dissipated in the device by the AVDD linear regulator with VM as supply (BUCK\_PS\_DIS = 1b)

$$P = (V_{VM} - V_{AVDD}) \times I_{AVDD} \quad (1)$$

For example, at a  $V_{VM}$  of 24-V, drawing 20-mA out of AVDD results in a power dissipation as shown in [Equation 2](#).

$$P = (24 \text{ V} - 3.3 \text{ V}) \times 20 \text{ mA} = 414 \text{ mW} \quad (2)$$

Use [Equation 3](#) to calculate the power dissipated in the device by the AVDD linear regulator with buck output as supply (BUCK\_PS\_DIS = 0b)

$$P = (V_{FB\_BK} - V_{AVDD}) \times I_{AVDD} \quad (3)$$

### 7.3.5 Charge Pump

Since the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to turn-on the high-side FETs. The MCF8316C-Q1 integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors ( $C_{CP}$ ,  $C_{FLY}$ ) for operation. See [Figure 7-1](#) and [Table 5-1](#) for details on these capacitors (value, connection, and so forth).

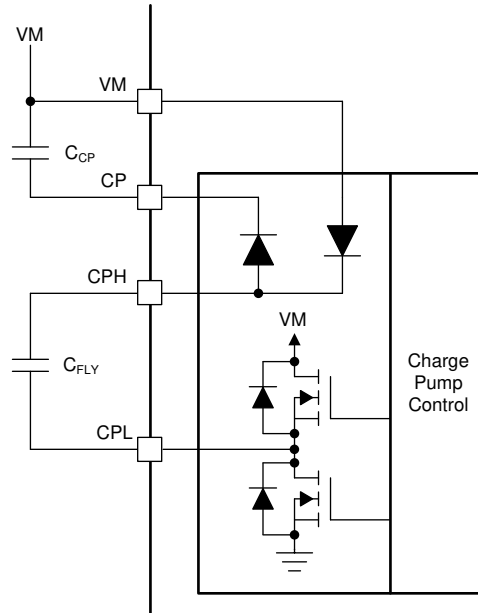


Figure 7-8. Charge Pump

### 7.3.6 Slew Rate Control

An adjustable gate-drive current control is provided for the output stage MOSFETs to achieve configurable slew rate for EMI mitigation. The MOSFET VDS slew rate is a critical factor for optimizing conducted and radiated emissions, total energy and duration of diode recovery spikes and switching voltage transients related to parasitic elements of the PCB. This slew rate is predominantly determined by the control of the internal MOSFET gate current as shown in Figure 7-9.

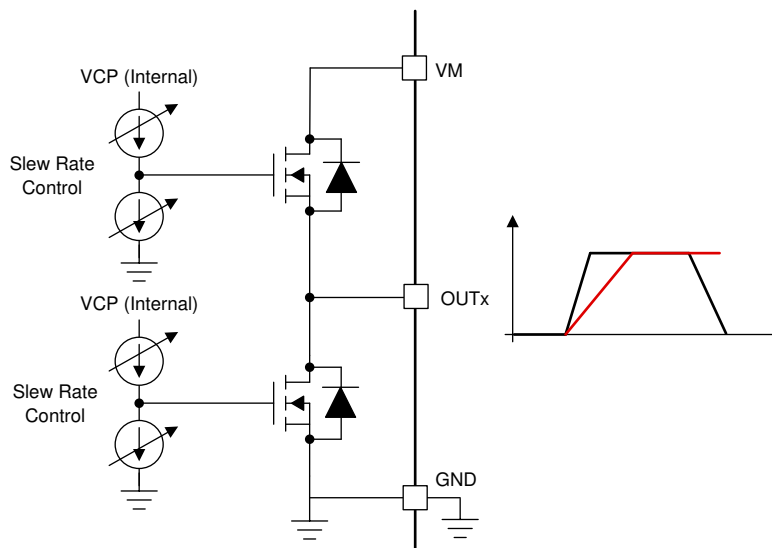
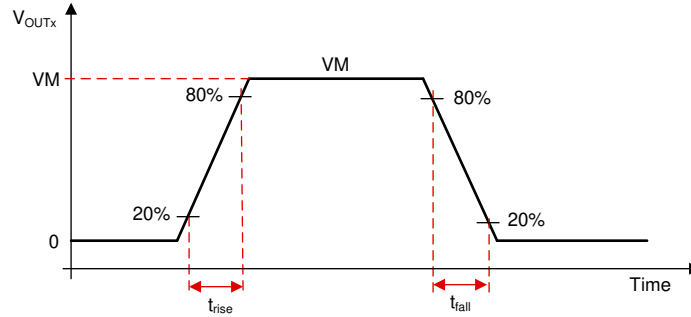


Figure 7-9. Slew Rate Circuit Implementation

The slew rate of each half-bridge can be adjusted through SLEW\_RATE. Slew rate can be configured as either 125-V/ $\mu$ s or 200-V/ $\mu$ s. The slew rate is calculated by the rise-time and fall-time of the voltage on OUTx pin as shown in Figure 7-10.

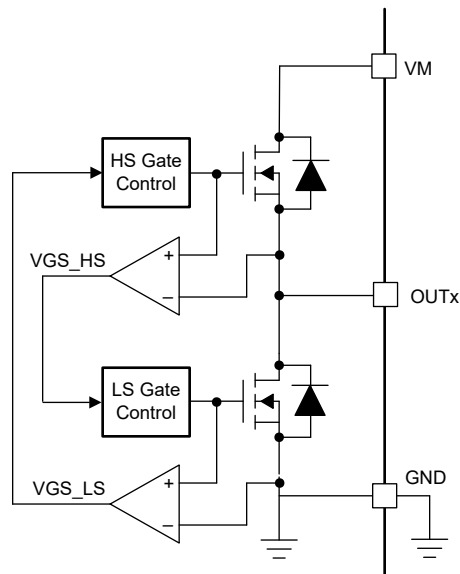




**Figure 7-10. Slew Rate Timings**

### 7.3.7 Cross Conduction (Dead Time)

The device is fully protected against any cross conduction of MOSFETs - during the switching of high-side and low-side MOSFETs, MCF8316C-Q1 avoids shoot-through events by inserting a dead time ( $t_{dead}$ ). This is implemented by sensing the gate-source voltage (VGS) of the high-side and low-side MOSFETs and ensuring that VGS of high-side MOSFET has dropped below turn-off level before switching on the low-side MOSFET of same half-bridge (or vice-versa) as shown in Figure 7-11 and Figure 7-12. The VGS of the high-side and low-side MOSFETs (VGS\_HS and VGS\_LS) shown in Figure 7-12 are internal signals.



**Figure 7-11. Cross Conduction Protection**

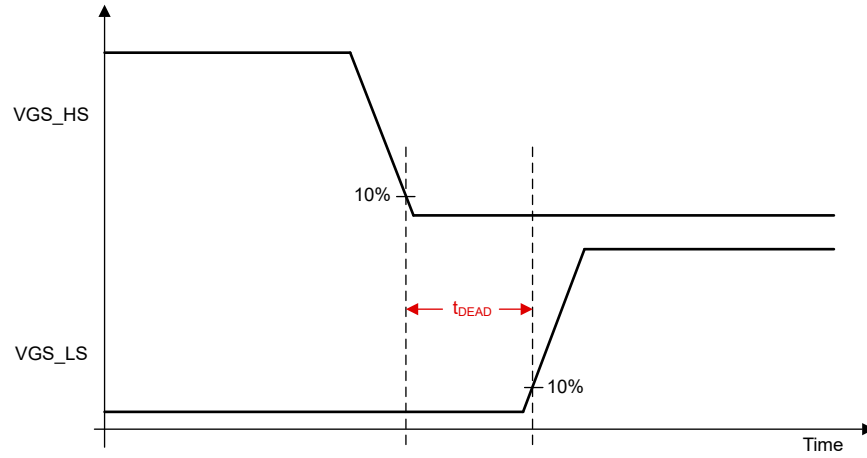


Figure 7-12. Dead Time

### 7.3.8 Motor Control Input Sources

MCF8316C-Q1 provides two modes of controlling the motor based on SPEED\_LOOP\_DIS setting,

1. Speed control: In speed control mode (SPEED\_LOOP\_DIS = 0b), the speed of the motor is controlled according to the input reference using a closed loop PI control .
2. Current control: In current control mode (SPEED\_LOOP\_DIS = 1b), the torque controlling current ( $I_q$ ) is controlled according to the input reference using a closed loop PI control.

MCF8316C-Q1 offers four methods of directly controlling the input reference of the motor. The input reference source is configured by SPEED\_MODE.

The input reference source can be provided in one of the following four ways,

- Analog input on SPEED pin by varying amplitude of input signal (SPEED\_MODE = 00b)
- PWM input on SPEED pin by varying duty cycle of input signal (SPEED\_MODE = 01b)
- Over I<sup>2</sup>C by configuring DIGITAL\_SPEED\_CTRL register (SPEED\_MODE = 10b)
- Frequency input on SPEED pin by varying frequency of input signal (SPEED\_MODE = 11b)

The signal path from SPEED pin input (or I<sup>2</sup>C based speed input) to motor control reference (SPEED\_REF or CURRENT\_REF in Figure 7-32) is as shown in Figure 7-13.

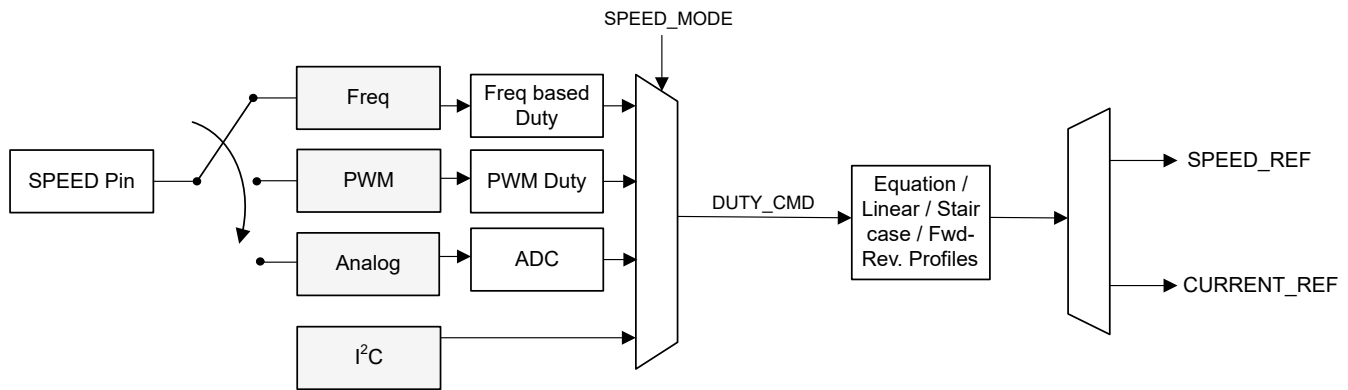
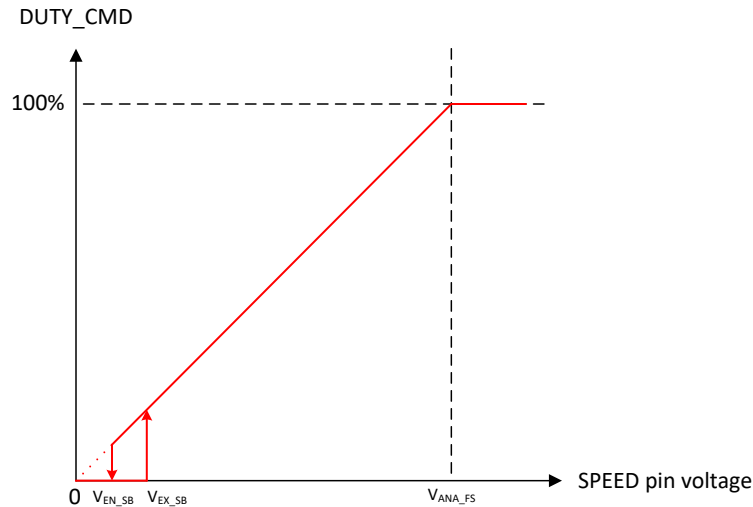


Figure 7-13. Multiplexing the Input Reference Source

#### 7.3.8.1 Analog-Mode Motor Control

Analog input based motor control can be configured by setting SPEED\_MODE to 00b. In this mode, the duty command (DUTY\_CMD) varies with the analog voltage input on the SPEED pin ( $V_{SPEED}$ ). When  $0 \leq V_{SPEED} \leq V_{EN\_SB}$ , DUTY\_CMD is set to zero and the motor is stopped. When  $V_{EX\_SB} \leq V_{SPEED} \leq V_{ANA\_FS}$ , DUTY\_CMD varies linearly with  $V_{SPEED}$  as shown in Figure 7-14.  $V_{EX\_SB}$  and  $V_{EN\_SB}$  are the standby entry and exit thresholds - refer Section 7.4.1.2 for more information on  $V_{EX\_SB}$  and  $V_{EN\_SB}$ . When  $V_{SPEED} > V_{ANA\_FS}$ , DUTY\_CMD is clamped to 100%.



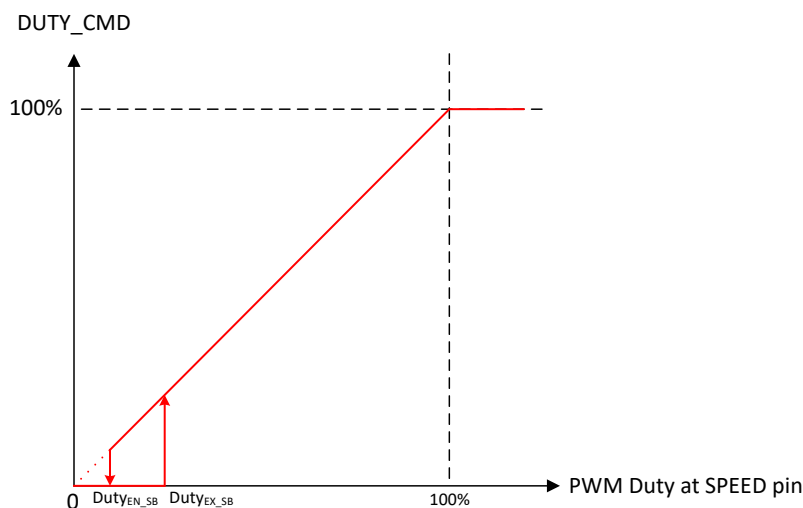
**Figure 7-14. Analog-Mode Motor Control**

### 7.3.8.2 PWM-Mode Motor Control

PWM based motor control can be configured by setting SPEED\_MODE to 01b. In this mode, the PWM duty cycle applied to the SPEED pin can be varied from 0 to 100% and duty command (DUTY\_CMD) varies linearly with the applied PWM duty cycle. When  $0 \leq \text{Duty}_{\text{SPEED}} \leq \text{Duty}_{\text{EN\_SB}}$ , DUTY\_CMD is set to zero and the motor is stopped. When  $\text{Duty}_{\text{EX\_SB}} \leq \text{Duty}_{\text{SPEED}} \leq 100\%$ , DUTY\_CMD varies linearly with  $\text{Duty}_{\text{SPEED}}$  as shown in [Figure 7-15](#).  $\text{Duty}_{\text{EX\_SB}}$  and  $\text{Duty}_{\text{EN\_SB}}$  are the standby entry and exit thresholds - refer [Section 7.4.1.2](#) for more information on  $\text{Duty}_{\text{EX\_SB}}$  and  $\text{Duty}_{\text{EN\_SB}}$ . The frequency of the PWM input signal applied to the SPEED pin is defined as  $f_{\text{PWM}}$  and the range for this frequency can be configured through SPEED\_RANGE\_SEL.

#### Note

1.  $f_{\text{PWM}}$  is the frequency of the PWM signal the device can accept at SPEED pin to control motor speed. It does not correspond to the PWM output frequency that is applied to the motor phases. The PWM output frequency can be configured through PWM\_FREQ\_OUT (see [Section 7.3.16](#)).
2. SLEEP\_ENTRY\_TIME should be set longer than the off time in PWM signal ( $V_{\text{SPEED}} < V_{\text{IL}}$ ) at lowest duty input. For example, if  $f_{\text{PWM}}$  is 10 kHz and lowest duty input is 2%, SLEEP\_ENTRY\_TIME should be more than 98  $\mu\text{s}$  to ensure there is no unintended sleep/standby entry.



**Figure 7-15. PWM-Mode Motor Control**

### 7.3.8.3 I<sup>2</sup>C-based Motor Control

I<sup>2</sup>C based serial interface can be used for motor control by setting SPEED\_MODE to 10b. In this mode, the speed command can be written directly into DIGITAL\_SPEED\_CTRL register. The SPEED pin can be used to control the sleep entry and exit - if SPEED pin input is set to a value lower than V<sub>EN\_SL</sub> after DIGITAL\_SPEED\_CTRL register has been set to 0b for a time longer than SLEEP\_ENTRY\_TIME, MCF8316C-Q1 enters sleep state. When SPEED pin > V<sub>EX\_SL</sub>, MCF8316C-Q1 exits sleep state and speed is controlled through DIGITAL\_SPEED\_CTRL register. If  $0 \leq \text{DIGITAL\_SPEED\_CTRL} \leq \text{DIGITAL\_SPEED\_CTRL}_{\text{EN\_SB}}$  and SPEED pin > V<sub>EX\_SL</sub>, MCF8316C-Q1 is in standby state. The relationship between DUTY\_CMD and DIGITAL\_SPEED\_CTRL register is shown in Figure 7-16. Refer Section 7.4.1.2 for more information on DIGITAL\_SPEED\_CTRL<sub>EN\_SB</sub> and DIGITAL\_SPEED\_CTRL<sub>EN\_SB</sub> EX\_SB.

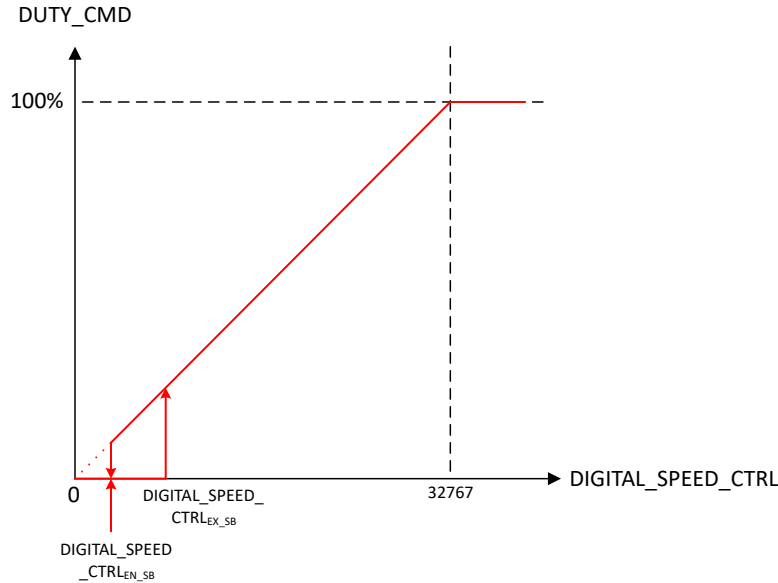
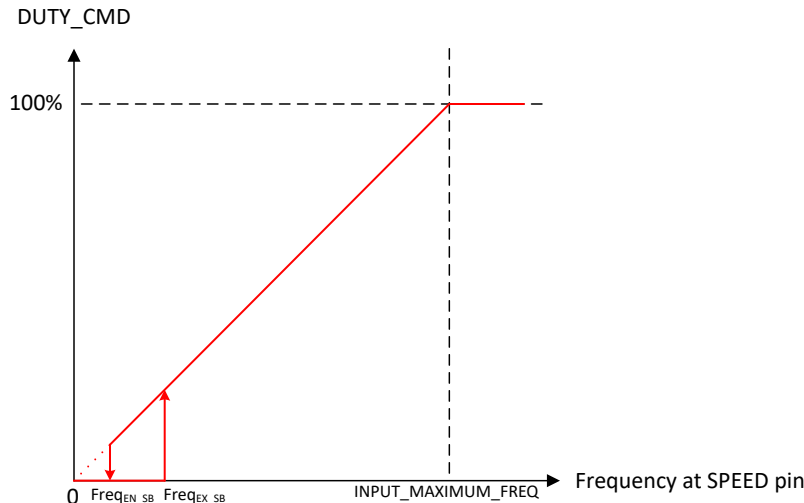


Figure 7-16. I<sup>2</sup>C-Mode Motor Control

### 7.3.8.4 Frequency-Mode Motor Control

Frequency based motor control is configured by setting SPEED\_MODE to 11b. In this mode, duty command varies linearly as a function of the frequency of the square wave input at SPEED pin. When  $0 \leq \text{Freq}_{\text{SPEED}} \leq \text{Freq}_{\text{EN\_SB}}$ , DUTY\_CMD is set to zero and the motor is stopped. When  $\text{Freq}_{\text{EX\_SB}} \leq \text{Freq}_{\text{SPEED}} \leq \text{INPUT\_MAXIMUM\_FREQ}$ , DUTY\_CMD varies linearly with Freq<sub>SPEED</sub> as shown in Figure 7-17. Freq<sub>EX\_SB</sub> and Freq<sub>EN\_SB</sub> are the standby entry and exit thresholds - refer Section 7.4.1.2 for more information on Freq<sub>EX\_SB</sub> and Freq<sub>EN\_SB</sub>. Input frequency greater than INPUT\_MAXIMUM\_FREQ clamps the DUTY\_CMD to 100%.



**Figure 7-17. Frequency-Mode Motor Control**

### 7.3.8.5 Input Reference Profiles

MCF8316C-Q1 supports three different kinds of input reference profiles (linear, staircase, bi-directional) to configure custom reference-duty command transfer function to meet specific application requirements. The input reference profile can be configured through REF\_PROFILE\_CONFIG.

When REF\_PROFILE\_CONFIG is set to 00b, the input reference (SPEED\_REF or CURRENT\_REF) is set by the duty command (DUTY\_CMD) as shown in equations Equation 4 or Equation 5.

$$\text{SPEED\_REF (Hz)} = \text{DUTY\_CMD} \times \text{MAX\_SPEED (when SPEED\_LOOP\_DIS = 0b)} \quad (4)$$

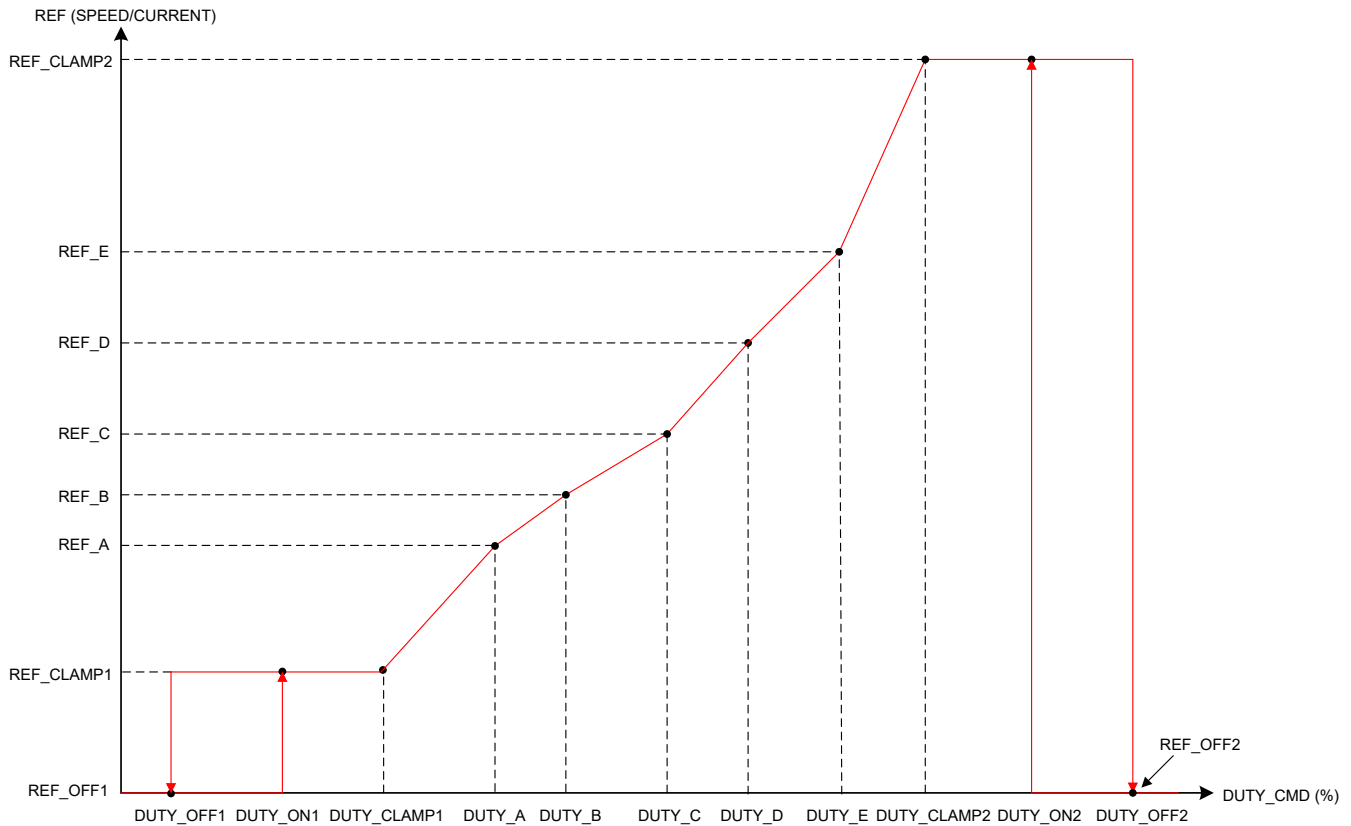
$$\text{CURRENT\_REF (A)} = \text{DUTY\_CMD} \times \text{ILIMIT (when SPEED\_LOOP\_DIS = 1b)} \quad (5)$$

When REF\_PROFILE\_CONFIG is set to 00b, any change in DUTY\_CMD by a value less than DUTY\_HYS does not produce any change in SPEED\_REF or CURRENT\_REF; DUTY\_HYS provides a hysteresis window around DUTY\_CMD for noise immunity.

#### 7.3.8.5.1 Linear Reference Profiles

##### Note

1. For all types of reference profiles, a zero input reference (0-V in analog mode, 0% duty in PWM mode, DIGITAL\_SPEED\_CTRL = 0b I<sup>2</sup>C mode or 0-Hz in frequency mode) stops the motor irrespective of the reference profile configuration.
2. The reference value in Figure 7-18, Figure 7-19, Figure 7-20 is decided by control mode (SPEED\_LOOP\_DIS) as follows,
  - Speed control mode (SPEED\_LOOP\_DIS = 0b): SPEED\_REF (Hz) = (REF\_x/255) x MAX\_SPEED (Hz)
  - Current control mode (SPEED\_LOOP\_DIS = 1b): CURRENT\_REF (A) = (REF\_x/255) x ILIMIT (A)



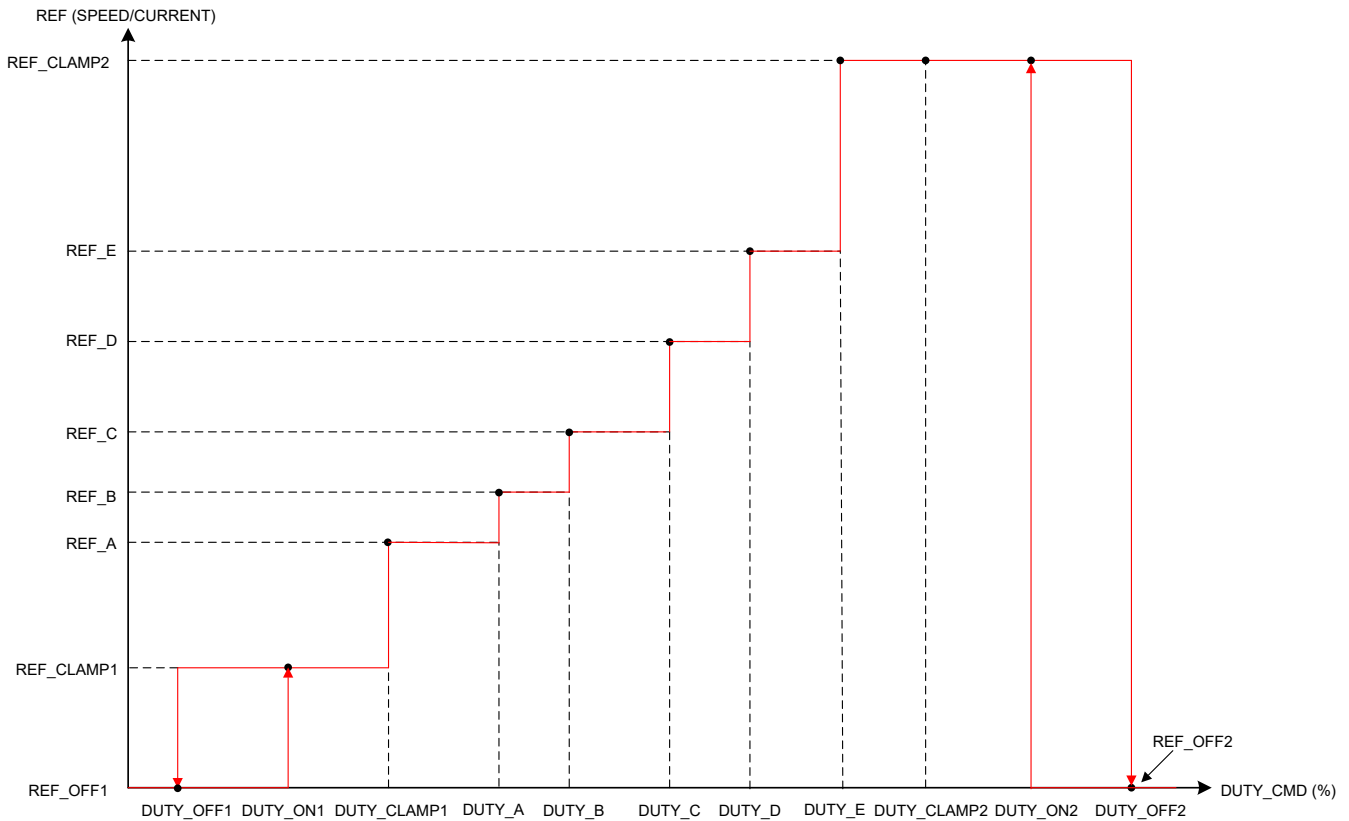
**Figure 7-18. Linear Reference Profile**

Linear reference profiles can be configured by setting REF\_PROFILE\_CONFIG to 01b. Linear profiles feature input references (SPEED\_REF or CURRENT\_REF) which change linearly between REF\_CLAMP1 and REF\_CLAMP2 with different slopes which can be set by configuring DUTY\_x and REF\_x.

- DUTY\_OFF1 configures the duty command below which the reference will be REF\_OFF1.
- DUTY\_OFF1 and DUTY\_ON1 configure a hysteresis between reference levels, REF\_CLAMP1 and REF\_OFF1 as shown in [Figure 7-18](#).
- DUTY\_CLAMP1 configures the duty command till which reference will be constant with a value REF\_CLAMP1. DUTY\_CLAMP1 can be placed anywhere between DUTY\_ON1 and DUTY\_A.
- DUTY\_A configures the duty command for reference REF\_A. The reference changes from REF\_CLAMP1 to REF\_A linearly between DUTY\_CLAMP1 and DUTY\_A. DUTY\_A to DUTY\_E has to be in the same order as shown in [Figure 7-18](#).
- DUTY\_B configures the duty command for reference REF\_B. The reference changes linearly between DUTY\_A and DUTY\_B.
- DUTY\_C configures the duty command for reference REF\_C. The reference changes linearly between DUTY\_B and DUTY\_C.
- DUTY\_D configures the duty command for reference REF\_D. The reference changes linearly between DUTY\_C and DUTY\_D.
- DUTY\_E configures the duty command for reference REF\_E. The reference changes linearly between DUTY\_D and DUTY\_E.
- DUTY\_CLAMP2 configures the duty command above which the reference will be constant at REF\_CLAMP2. REF\_CLAMP2 configures this constant reference between DUTY\_CLAMP2 and DUTY\_OFF2. The reference changes linearly between DUTY\_E and DUTY\_CLAMP2. DUTY\_CLAMP2 can be placed anywhere between DUTY\_E and DUTY\_ON2.
- DUTY\_OFF2 and DUTY\_ON2 configure a hysteresis between reference levels REF\_CLAMP2 and REF\_OFF2 as shown in [Figure 7-18](#).

- DUTY\_OFF2 configures the duty command above which the reference will change from REF\_CLAMP2 to REF\_OFF2.

### 7.3.8.5.2 Staircase Speed Profile



**Figure 7-19. Staircase Reference Profile**

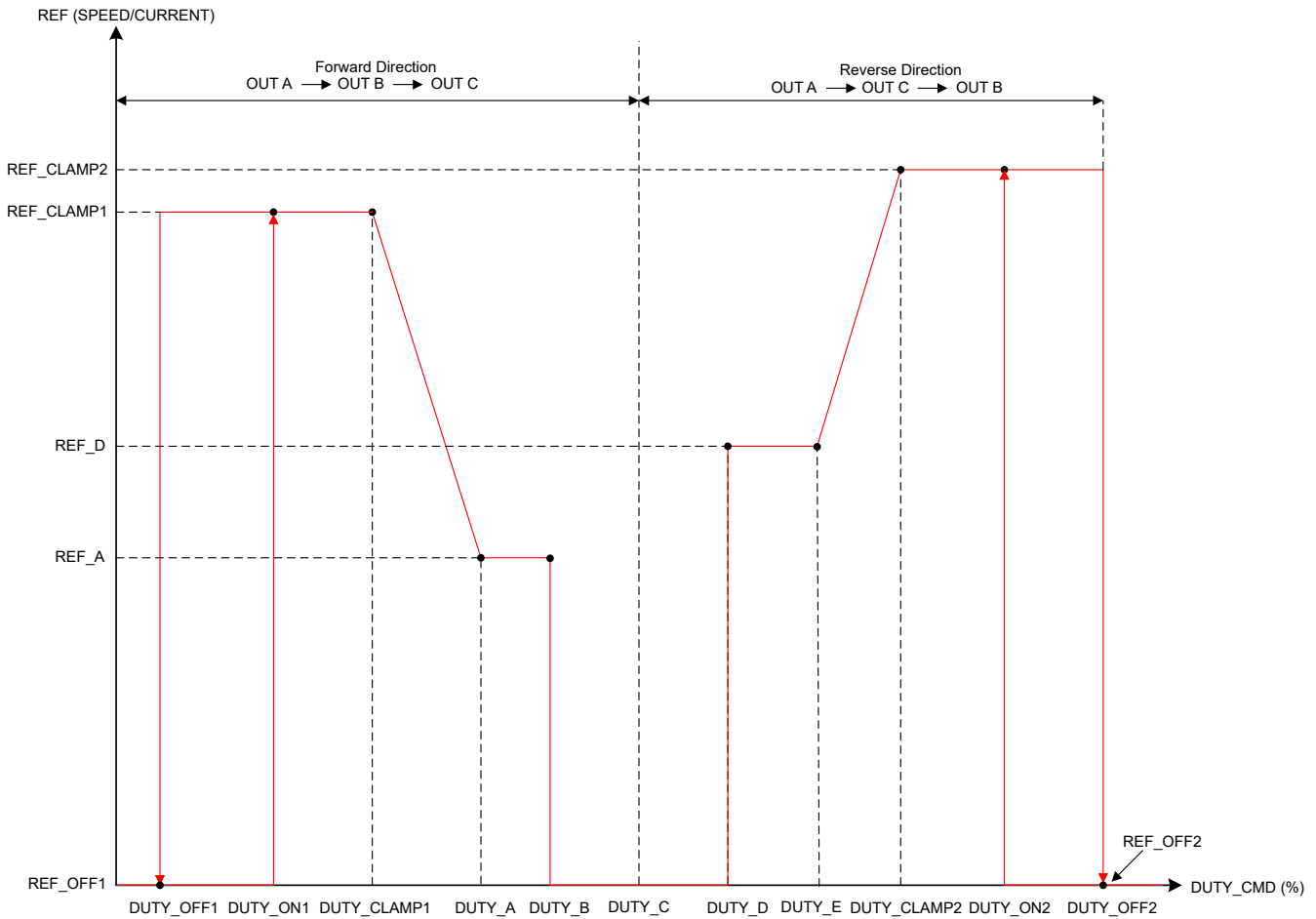
Staircase control profiles can be configured by setting REF\_PROFILE\_CONFIG to 10b. Staircase profiles feature input control reference changes in steps between REF\_CLAMP1 and REF\_CLAMP2, by configuring DUTY\_x and REF\_x.

- DUTY\_OFF1 configures the duty command below which the reference will be REF\_OFF1.
- DUTY\_OFF1 and DUTY\_ON1 configure a hysteresis between reference levels REF\_CLAMP1 and REF\_OFF1 as shown in [Figure 7-19](#).
- DUTY\_CLAMP1 configures the duty command till which reference will be constant. REF\_CLAMP1 configures this constant reference between DUTY\_OFF1 and DUTY\_CLAMP1. DUTY\_CLAMP1 can be placed anywhere between DUTY\_ON1 and DUTY\_A.
- DUTY\_A configures the duty command for reference REF\_A. There is a step change in reference from REF\_CLAMP1 to REF\_A at DUTY\_CLAMP1. DUTY\_A to DUTY\_E has to be in the same order as shown in [Figure 7-19](#).
- DUTY\_B configures the duty command for reference REF\_B. There is a step change in reference from REF\_A to REF\_B at DUTY\_A.
- DUTY\_C configures the duty command for reference REF\_C. There is a step change in reference from REF\_B to REF\_C at DUTY\_B.
- DUTY\_D configures the duty command for reference REF\_D. There is a step change in reference from REF\_C to REF\_D at DUTY\_C.
- DUTY\_E configures the duty command for reference REF\_E. There is a step change in reference from REF\_D to REF\_E at DUTY\_D.



- DUTY\_CLAMP2 configures the duty command above which the reference will be constant at REF\_CLAMP2. REF\_CLAMP2 configures this constant reference between DUTY\_CLAMP2 and DUTY\_OFF2. There is a step change in reference from REF\_E to REF\_CLAMP2 at DUTY\_E. DUTY\_CLAMP2 can be placed anywhere between DUTY\_E and DUTY\_ON2.
- DUTY\_OFF2 and DUTY\_ON2 configure a hysteresis between reference levels REF\_CLAMP2 and REF\_OFF2 as shown in Figure 7-19.
- DUTY\_OFF2 configures the duty command above which the reference will change from REF\_CLAMP2 to REF\_OFF2.

### 7.3.8.5.3 Forward-Reverse Speed Profile



**Figure 7-20. Forward-Reverse Reference Profile**

Forward-Reverse control profiles can be configured by setting REF\_PROFILE\_CONFIG to 11b. Forward-Reverse profiles feature direction change through adjusting the duty command. DUTY\_C configures duty command at which the direction will be changed. The Forward-Reverse speed profile can be used to eliminate the separate signal used to control the motor direction.

**Note**

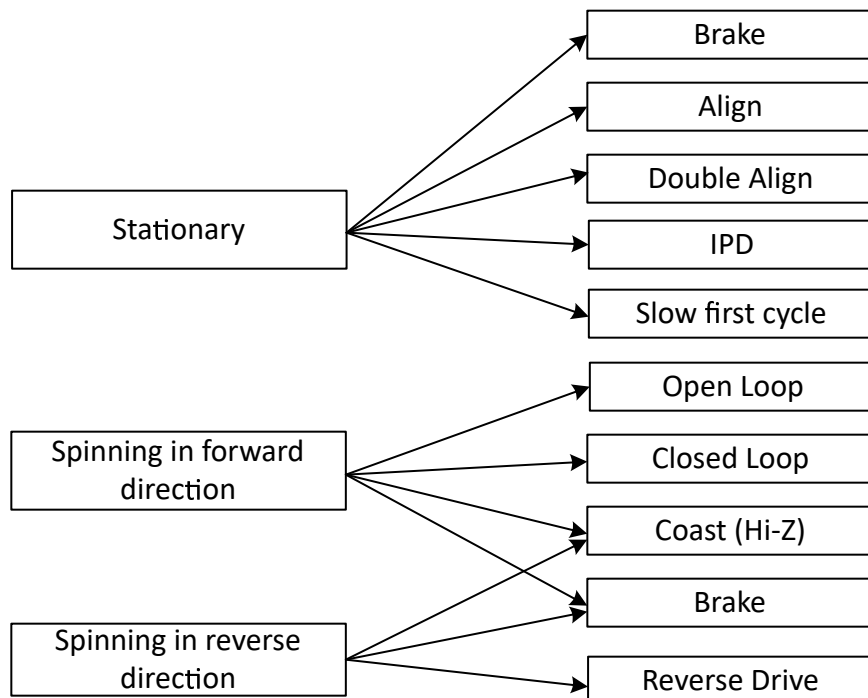
The direction change functionality through DIR pin and DIR\_INPUT bits are disabled in forward reverse profile mode.

- DUTY\_OFF1 configures the duty command below which the reference will be REF\_OFF1.
- DUTY\_OFF1 and DUTY\_ON1 configures a hysteresis between reference levels REF\_CLAMP1 and REF\_OFF1 as shown in Figure 7-20.

- DUTY\_CLAMP1 configures the duty command till which reference will be constant. REF\_CLAMP1 configures this constant reference between DUTY\_OFF1 and DUTY\_CLAMP1. DUTY\_CLAMP1 can be placed anywhere between DUTY\_ON1 and DUTY\_A.
- DUTY\_A configures the duty command for reference REF\_A. The reference changes linearly between DUTY\_CLAMP1 and DUTY\_A. DUTY\_A to DUTY\_E has to be in the same order as shown in [Figure 7-20](#).
- DUTY\_B configures the duty command above which MCF8316C-Q1 will be in idle/off state. The reference remains constant at REF\_A between DUTY\_A and DUTY\_B.
- DUTY\_C configures the duty command at which the direction is changed
- DUTY\_D configures the duty command above which the MCF8316C-Q1 will be in running state in the reverse direction. REF\_D configures constant reference between DUTY\_D and DUTY\_E.
- DUTY\_E configures the duty command above which reference changes linearly between DUTY\_E and DUTY\_CLAMP2.
- DUTY\_CLAMP2 configures the duty command above which the reference will be constant at REF\_CLAMP2. REF\_CLAMP2 configures this constant reference between DUTY\_CLAMP2 and DUTY\_OFF2. DUTY\_CLAMP2 can be placed anywhere between DUTY\_E and DUTY\_ON2.
- DUTY\_OFF2 and DUTY\_ON2 configure a hysteresis between reference levels REF\_CLAMP2 and REF\_OFF2 as shown in [Figure 7-20](#).
- DUTY\_OFF2 configures the duty command above which the reference changes in the reverse direction from REF\_CLAMP2 to REF\_OFF2.

### 7.3.9 Starting the Motor Under Different Initial Conditions

The motor can be in one of three states when MCF8316C-Q1 begins the start-up process. The motor may be stationary, spinning in the forward direction, or spinning in the reverse direction. The MCF8316C-Q1 includes a number of features to allow for reliable motor start-up under all of these conditions. [Figure 7-21](#) shows the motor start-up flow for each of the three initial motor states.



**Figure 7-21. Starting the motor under different initial conditions**

#### Note

"Forward" means "spinning in the same direction as the commanded direction", and "Reverse" means "spinning in the opposite direction as the commanded direction".

### 7.3.9.1 Case 1 – Motor is Stationary

If the motor is stationary, the commutation must be initialized to be in phase with the position of the motor. The MCF8316C-Q1 provides various options to initialize the commutation logic to the motor position and reliably start the motor.

- The align and double align techniques force the motor into alignment by applying a voltage across particular motor phases to force the motor to rotate in alignment with this phase.
- Initial position detect (IPD) determines the position of the motor based on the deterministic inductance variation, which is often present in BLDC motors.
- The slow first cycle method starts the motor by applying a low frequency cycle to align the rotor position to the applied commutation by the end of one electrical rotation.

MCF8316C-Q1 also provides a configurable brake option to ensure the motor is stationary before initiating one of the above start-up methods. Device enters open loop acceleration after going through the configured start-up method.

### 7.3.9.2 Case 2 – Motor is Spinning in the Forward Direction

If the motor is spinning forward (same direction as the commanded direction) with sufficient speed (BEMF), the MCF8316C-Q1 resynchronizes with the spinning motor and continues commutation by going directly to closed loop operation. If the motor speed is too low for closed loop operation, MCF8316C-Q1 enters open loop operation to accelerate the motor till it reaches sufficient speed to enter closed loop operation. By resynchronizing to the spinning motor, the user achieves the fastest possible start-up time for this initial condition. This resynchronization feature can be enabled or disabled through RESYNC\_EN. If resynchronization is disabled, the MCF8316C-Q1 can be configured to wait for the motor to coast to a stop and/or apply a brake. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

### 7.3.9.3 Case 3 – Motor is Spinning in the Reverse Direction

If the motor is spinning in the reverse direction (the opposite direction as the commanded direction), the MCF8316C-Q1 provides several methods to change the direction and drive the motor to the target speed reference in the commanded direction.

The reverse drive method allows the motor to be driven so that it decelerates through zero speed. The motor achieves the shortest possible spin-up time when spinning in the reverse direction.

If reverse drive is not enabled, then the MCF8316C-Q1 can be configured to wait for the motor to coast to a stop and/or apply a brake. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

---

#### Note

Take care when using the reverse drive or brake feature to ensure that the current is limited to an acceptable level and that the supply voltage does not surge as a result of energy being returned to the power supply.

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### 7.3.10 Motor Start Sequence (MSS)

Figure 7-22 shows the motor-start sequence implemented in the MCF8316C-Q1 device.

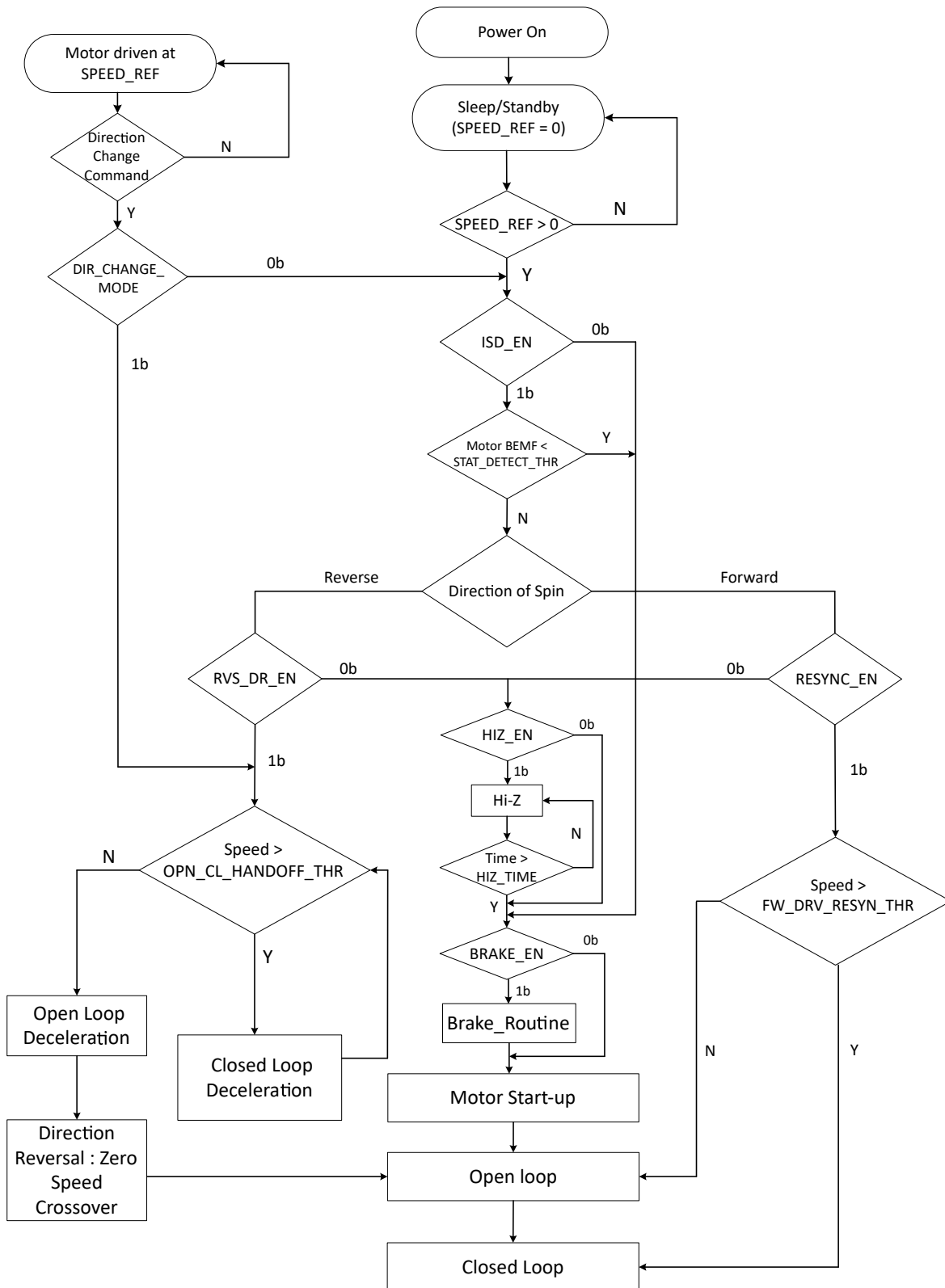


Figure 7-22. Motor Start Sequence

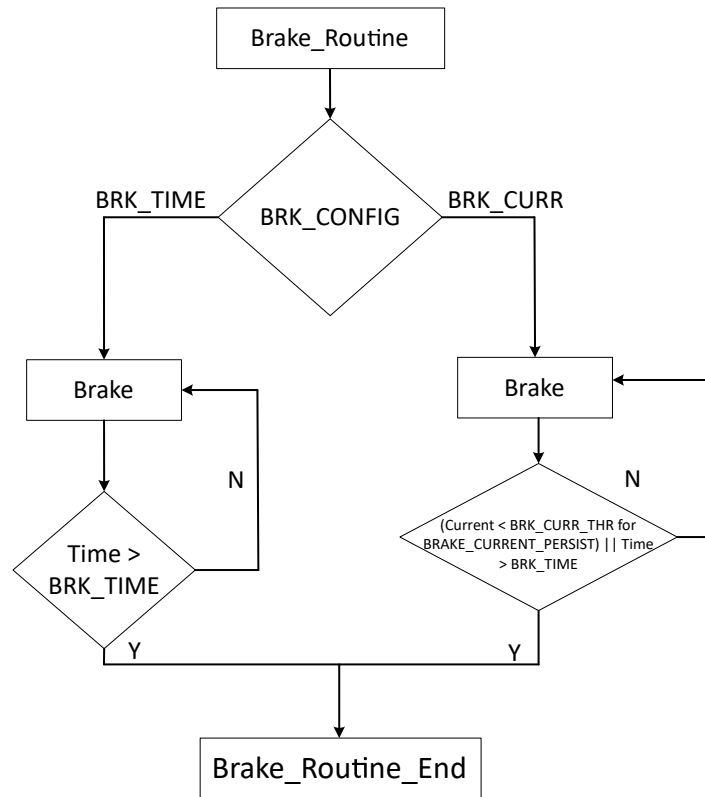


Figure 7-23. Brake Routine

**Power-On State**

This is the initial state of the Motor Start Sequence (MSS) when MCF8316C-Q1 is powered on. In this state, MCF8316C-Q1 configures the peripherals, initializes the algorithm parameters from EEPROM and prepares for driving the motor.

**Sleep/Standby**

In this state, SPEED\_REF is set to zero and MCF8316C-Q1 is either in sleep or standby mode depending on DEV\_MODE and SPEED/WAKE pin voltage.

**SPEED\_REF > 0 Judgement**

When SPEED\_REF is set to greater than zero, MCF8316C-Q1 exits the sleep/standby state and proceeds to ISD\_EN judgement. As long as SPEED\_REF is set to zero, MCF8316C-Q1 stays in sleep/standby state.

**Direction Change Command Judgement**

When a direction change command is received, MCF8316C-Q1 proceeds to DIR\_CHANGE\_MODE judgement.

**DIR\_CHANGE\_MODE Judgement**

If DIR\_CHANGE\_MODE is set to 0b, MCF8316C-Q1 initiates direction change by proceeding to ISD\_EN judgement. Instead, if DIR\_CHANGE\_MODE is set to 1b, MCF8316C-Q1 initiates direction change by proceeding to Speed > OPN\_CL\_HANDOFF\_THR judgement.

**ISD\_EN Judgement**

MCF8316C-Q1 checks to see if the initial speed detect (ISD) function is enabled (ISD\_EN = 1b). If ISD is enabled, MSS proceeds to the BEMF < STAT\_DETECT\_THR judgement. Instead, if ISD is disabled, the MSS proceeds directly to the BRAKE\_EN judgement.

**BEMF < STAT\_DETECT\_THR or BEMF < FG\_BEMF\_THR Judgement**

ISD determines the initial condition (speed, angle, direction of spin) of the motor (see Section 7.3.10.1). If motor is deemed to be stationary (BEMF < STAT\_DETECT\_THR or BEMF < FG\_BEMF\_THR), the MSS proceeds to BRAKE\_EN judgement. If the motor is not stationary, MSS proceeds to verify the direction of spin.

|   |   |
|---|---|
| <b>Direction of spin Judgement</b>  | The MSS determines whether the motor is spinning in the forward or the reverse direction. If the motor is spinning in the forward direction, the MCF8316C-Q1 proceeds to the RESYNC_EN judgement. If the motor is spinning in the reverse direction, the MSS proceeds to the RVS_DR_EN judgement.   |
| <b>RESYNC_EN Judgement</b>  | If RESYNC_EN is set to 1b, MCF8316C-Q1 proceeds to Speed > Open to Closed Loop Handoff (Resync) judgement. If RESYNC_EN is set to 0b, MSS proceeds to HIZ_EN judgement.   |
| <b>Speed &gt;<br/>FW_DRV_RESYN_THR<br/>Judgement</b>                        | If motor speed > FW_DRV_RESYN_THR, MCF8316C-Q1 uses the speed and position information from the ISD to transition to the closed loop state (see <a href="#">Section 7.3.10.2</a> ) directly. If motor speed < FW_DRV_RESYN_THR, MCF8316C-Q1 transitions to open loop state.   |
| <b>RVS_DR_EN Judgement</b>  | The MSS checks to see if the reverse drive function is enabled (RVS_DR_EN = 1b). If it is enabled, the MSS transitions to check speed of the motor in reverse direction. If the reverse drive function is not enabled (RVS_DR_EN = 0b), the MSS advances to the HIZ_EN judgement.   |
| <b>Speed &gt;<br/>OPN_CL_HANDOFF_THR<br/>Judgement</b>                      | The MSS checks to see if the reverse speed is high enough for MCF8316C-Q1 to decelerate in closed loop. Till the speed (in reverse direction) is above OL_CL_HANDOFF_THR, MSS stays in closed loop deceleration. If speed is below OPN_CL_HANDOFF_THR, then the MSS transitions to open loop deceleration.  |
| <b>Reverse Closed Loop, Open Loop Deceleration and Zero Speed Crossover</b> | The MCF8316C-Q1 resynchronizes in the reverse direction, decelerates the motor in closed loop till motor speed falls below the handoff threshold. (see <a href="#">Reverse Drive</a> ). When motor speed in reverse direction is too low, the MCF8316C-Q1 switches to open-loop, decelerates the motor in open-loop, crosses zero speed, and accelerates in the forward direction in open-loop before entering closed loop operation after motor speed is sufficiently high.  |
| <b>HIZ_EN Judgement</b>   | The MSS checks to determine whether the coast (Hi-Z) function is enabled (HIZ_EN = 1b). If the coast function is enabled (HIZ_EN = 1b), the MSS advances to the coast routine. If the coast function is disabled (HIZ_EN = 0b), the MSS advances to the BRAKE_EN judgement.   |
| <b>Coast (Hi-Z) Routine</b>   | The device coasts the motor by turning OFF all six MOSFETs for a certain time configured by HIZ_TIME.   |
| <b>BRAKE_EN Judgement</b>   | The MSS checks to determine whether the brake function is enabled (BRAKE_EN = 1b). If the brake function is enabled (BRAKE_EN = 1b), the MSS advances to the brake routine. If the brake function is disabled (BRAKE_EN = 0b), the MSS advances to the motor start-up state (see <a href="#">Section 7.3.10.4</a> ).  |
| <b>Brake Routine</b>  | MCF8316C-Q1 implements either a time based brake (duration configured by BRK_TIME) or a current based brake (brake applied till phase currents < BRK_CURR_THR for BRAKE_CURRENT_PERSIST) based on BRK_CONFIG. Current based brake has a timeout to ensure brake state ends in case phase currents do not drop below BRK_CURR_THR within BRK_TIME. Time based brake can be applied either using high-side or low-side MOSFETs based on BRK_MODE configuration. Current based brake is applied using low-side MOSFETs only. |
| <b>Closed Loop State</b>  | In this state, the MCF8316C-Q1 drives the motor with sensorless FOC based on rotor angle estimation.  |

### 7.3.10.1 Initial Speed Detect (ISD)

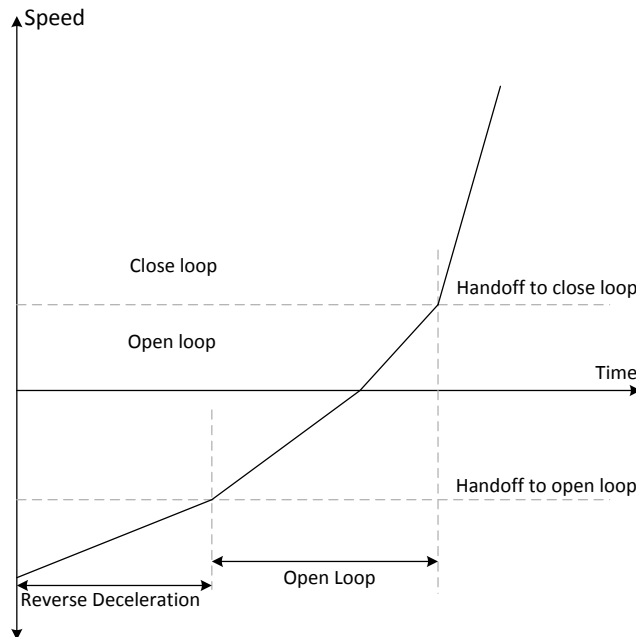
The ISD function is used to identify the initial condition of the motor and is enabled by setting `ISD_EN` to 1b. The initial speed, position and direction is determined by sensing the three phase voltages. ISD can be disabled by setting `ISD_EN` to 0b. If the function is disabled (`ISD_EN` set to 0b), the MCF8316C-Q1 does not perform the initial speed detect function and proceeds to check if the brake routine (`BRAKE_EN`) is enabled.

### 7.3.10.2 Motor Resynchronization

The motor resynchronization function works when the ISD and resynchronization functions are both enabled and the device determines that the initial state of the motor is spinning in the forward direction (same direction as the commanded direction). The speed and position information measured during ISD are used to initialize the drive state of the MCF8316C-Q1, which can transition directly into closed loop (or open loop if motor speed is not sufficient for closed loop operation) state without needing to stop the motor. In the MCF8316C-Q1, motor resynchronization can be enabled/disabled through `RESYNC_EN` bit. If motor resynchronization is disabled, the device proceeds to check if the motor coast (Hi-Z) routine is enabled.

### 7.3.10.3 Reverse Drive

The MCF8316C-Q1 uses the reverse drive function to change the direction of the motor rotation when `ISD_EN` and `RVS_DR_EN` are both set to 1b and the ISD determines the motor spin direction to be opposite to that of the commanded direction. Reverse drive includes synchronizing with the motor speed in the reverse direction, reverse decelerating the motor through zero speed, changing direction, and accelerating in open loop in forward (or commanded) direction until the device transitions into closed loop in forward direction (see [Figure 7-24](#)). MCF8316C-Q1 provides the option of using the forward direction parameters or a separate set of reverse drive parameters by configuring `REV_DRV_CONFIG`.



**Figure 7-24. Reverse Drive Function**

#### 7.3.10.3.1 Reverse Drive Tuning

MCF8316C-Q1 provides the option of tuning the open to closed loop handoff threshold, open loop acceleration (and deceleration) rates and open loop current limit in reverse drive to values different to those used in forward drive operation; the reverse drive specific parameters can be used by setting `REV_DRV_CONFIG` to 1b. If `REV_DRV_CONFIG` is set to 0b, MCF8316C-Q1 uses the equivalent parameters configured for forward drive operation during the reverse drive operation too.

The speed at which motor would enter the open loop in reverse direction can be configured using REV\_DRV\_HANDOFF\_THR. For a smooth transition without jerks or loss of synchronism, user can configure an appropriate current limit when the motor is spinning in open loop during speed reversal using REV\_DRV\_OPEN\_LOOP\_CURRENT. The open loop acceleration rates for the forward direction during speed reversal are defined using REV\_DRV\_OPEN\_LOOP\_ACCEL\_A1 and REV\_DRV\_OPEN\_LOOP\_ACCEL\_A2. The reverse drive open loop deceleration rate, when the motor is decelerating in the opposite direction to zero speed, can be configured as a percentage of reverse drive open loop acceleration using REV\_DRV\_OPEN\_LOOP\_DEC.

#### **7.3.10.4 Motor Start-up**

There are different options available for motor start-up from a stationary position and these options can be configured by MTR\_STARTUP. In align and double align mode, the motor is aligned to a known position by injecting a DC current. In IPD mode, the rotor position is estimated by applying 6 different high-frequency pulses. In slow first cycle mode, the motor is started by applying a low frequency cycle.

##### **7.3.10.4.1 Align**

Align is enabled by configuring MTR\_STARTUP to 00b. The MCF8316C-Q1 aligns the motor by injecting a DC current through a particular phase pattern for a certain time configured by ALIGN\_TIME. The phase pattern during align is generated based on ALIGN\_ANGLE. In the MCF8316C-Q1, the current limit during align is configured through ALIGN\_OR\_SLOW\_CURRENT\_ILIMIT.

A fast change in the phase current may result in a sudden change in the driving torque and this could result in acoustic noise. To avoid this, the MCF8316C-Q1 ramps up the current from 0 to the current limit at a configurable ramp rate set by ALIGN\_SLOW\_RAMP\_RATE. At the end of align routine, the motor will be aligned at the known position.

##### **7.3.10.4.2 Double Align**

Double align is enabled by configuring MTR\_STARTUP to 01b. Single align is not reliable when the initial position of the rotor is 180° out of phase with the applied phase pattern. In this case, it is possible to have start-up failures using single align. In order to improve the reliability of align based start-up, the MCF8316C-Q1 provides the option of double align start-up. In double align start-up, MCF8316C-Q1 uses a phase pattern for the second align that is 90° ahead of the first align phase pattern. In double align, relevant parameters like align time, current limit, ramp rate are the same as in the case of single align - two different phase patterns are applied in succession with the same parameters to ensure that the motor will be aligned to a known position irrespective of initial rotor position.

##### **7.3.10.4.3 Initial Position Detection (IPD)**

Initial Position Detection (IPD) can be enabled by configuring MTR\_STARTUP to 10b. In IPD, inductive sense method is used to determine the initial position of the motor using the spatial variation in the motor inductance.

Align or double align may result in the motor spinning in the reverse direction before starting open loop acceleration. IPD can be used in such applications where reverse rotation of the motor is unacceptable. IPD does not wait for the motor to align with the commutation and therefore can allow for a faster motor start-up sequence. IPD works well when the inductance of the motor varies as a function of position. IPD works by pulsing current in to the motor and hence can generate acoustics which must be taken into account when determining the best start-up method for a particular application.

##### **7.3.10.4.3.1 IPD Operation**

IPD operates by sequentially applying six different phase patterns according to the following sequence: BC-> CB-> AB-> BA-> CA-> AC (see [Figure 7-25](#)). When the current reaches the threshold configured by IPD\_CURR\_THR, the MCF8316C-Q1 stops driving the particular phase pattern and measures the time taken to reach the current threshold from when the particular phase pattern was applied. Thus, the time taken to reach IPD\_CURR\_THR is measured for all six phase patterns - this time varies as a function of the inductance in the motor windings. The state with the shortest time represents the state with the minimum inductance. The minimum inductance is because of the alignment of the north pole of the motor with this particular driving state.



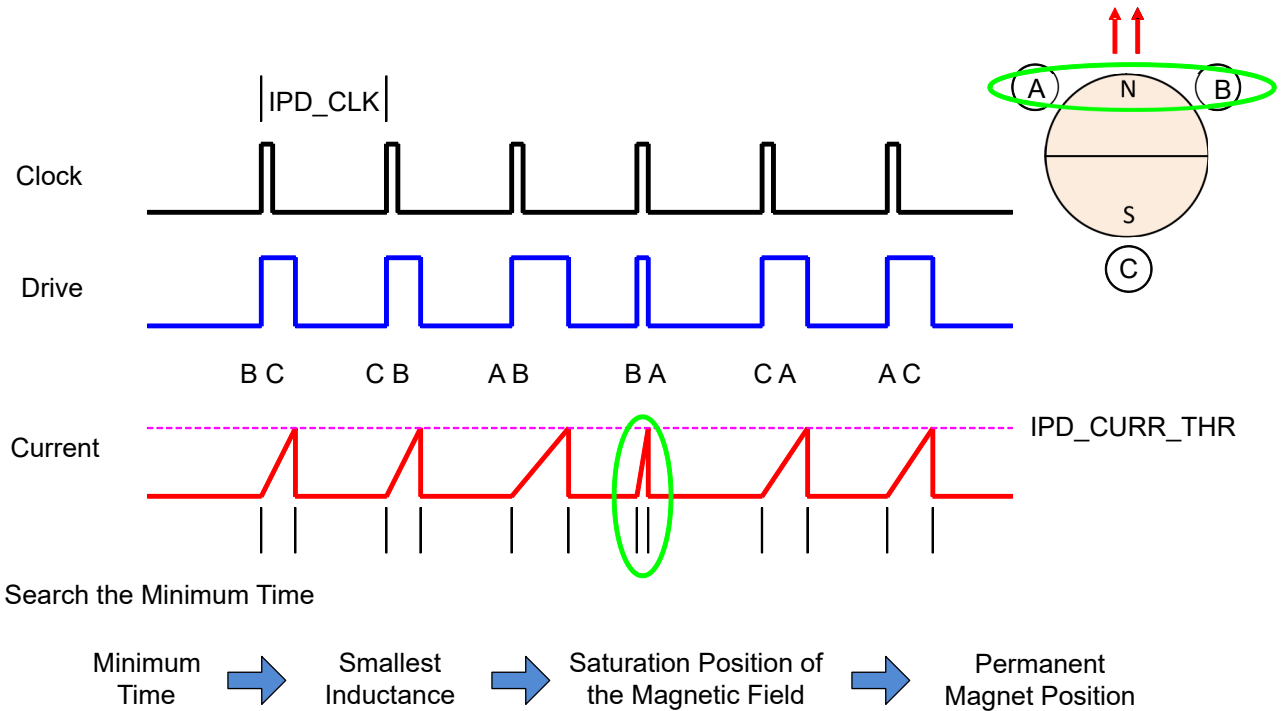


Figure 7-25. IPD Function

#### 7.3.10.4.3.2 IPD Release Mode

Two modes are available for configuring the way the MCF8316C-Q1 stops driving the motor when the current threshold is reached. The recirculate (or brake) mode is selected if  $IPD\_RLS\_MODE = 0b$ . In this configuration, the low-side (LSC) MOSFET remains ON to allow the current to recirculate between the MOSFET (LSC) and body diode (LSA) (see Figure 7-26). Hi-Z mode is selected if  $IPD\_RLS\_MODE = 1b$ . In Hi-Z mode, both the high-side (HSA) and low-side (LSC) MOSFETs are turned OFF and the current recirculates through the body diodes back to the power supply (see Figure 7-27).

In the Hi-Z mode, the phase current has a faster settle-down time, but that can result in a voltage increase on  $V_M$ . The user must manage this with an appropriate selection of either a clamp circuit or by providing sufficient capacitance between  $V_M$  and PGND to absorb the energy. If the voltage surge cannot be contained or if it is unacceptable for the application, recirculate mode must be used. When using the recirculate mode, select the  $IPD\_CLK\_FREQ$  appropriately to give the current in the motor windings enough time to decay to 0-A before the next IPD phase pattern is applied.

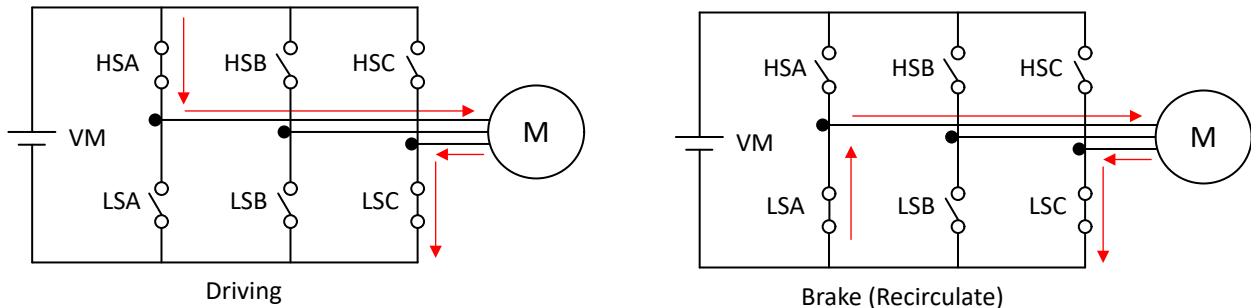
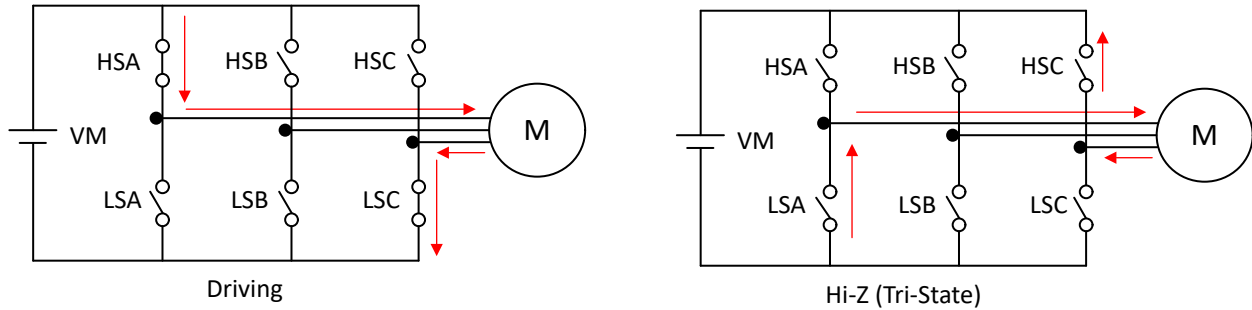


Figure 7-26. IPD Release Mode - Brake (0b)

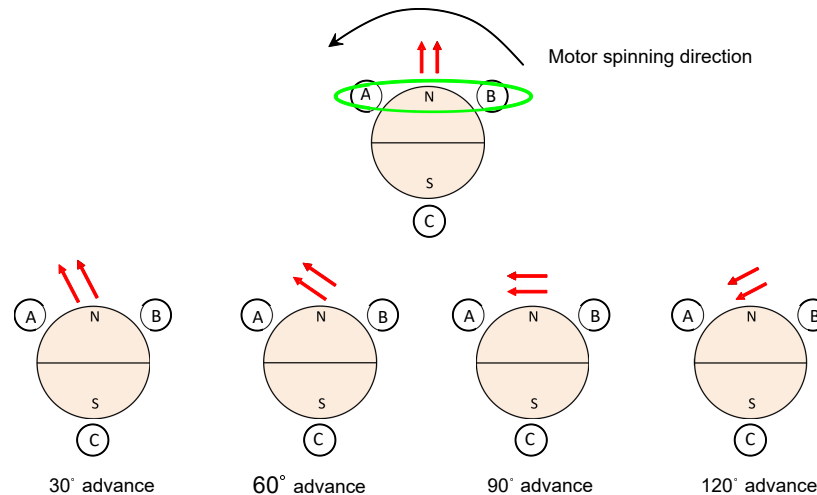


**Figure 7-27. IPD Release Mode - Tristate (1b)**

#### 7.3.10.4.3.3 IPD Advance Angle

After the initial position is detected, the MCF8316C-Q1 begins driving the motor in open loop at an angle specified by IPD\_ADV\_ANGLE.

Advancing the drive angle anywhere from 0° to 180° results in positive torque. Advancing the drive angle by 90° results in maximum initial torque. Applying maximum initial torque could result in uneven acceleration to the rotor. Select the IPD\_ADV\_ANGLE to allow for smooth acceleration in the application (see [Figure 7-28](#)).



**Figure 7-28. IPD Advance Angle**

#### 7.3.10.4.4 Slow First Cycle Startup

Slow First Cycle start-up is enabled by configuring MTR\_STARTUP to 11b. In slow first cycle start-up, the MCF8316C-Q1 starts motor commutation at a frequency defined by SLOW\_FIRST\_CYCLE\_FREQ. The frequency configured is used only for first cycle, and then the motor commutation follows acceleration profile configured by open loop acceleration coefficients A1 and A2. The slow first cycle frequency has to be configured to be slow enough to allow motor to synchronize with the commutation sequence. This mode is useful when fast startup is desired as it significantly reduces the align time.

#### 7.3.10.4.5 Open Loop

Upon completing the motor position initialization with either align, double align, IPD or slow first cycle, the MCF8316C-Q1 begins to accelerate the motor in open loop. In MCF8316C-Q1, the current limit in open loop is set by ILIMIT or OL\_ILIMIT based on the configuration of OL\_ILIMIT\_CONFIG and the speed is increased using this current limit. In open loop, the control PI loops for  $I_q$  and  $I_d$  actively control the currents. The angle during open loop is provided from the ramp generator as shown in [Figure 7-29](#).

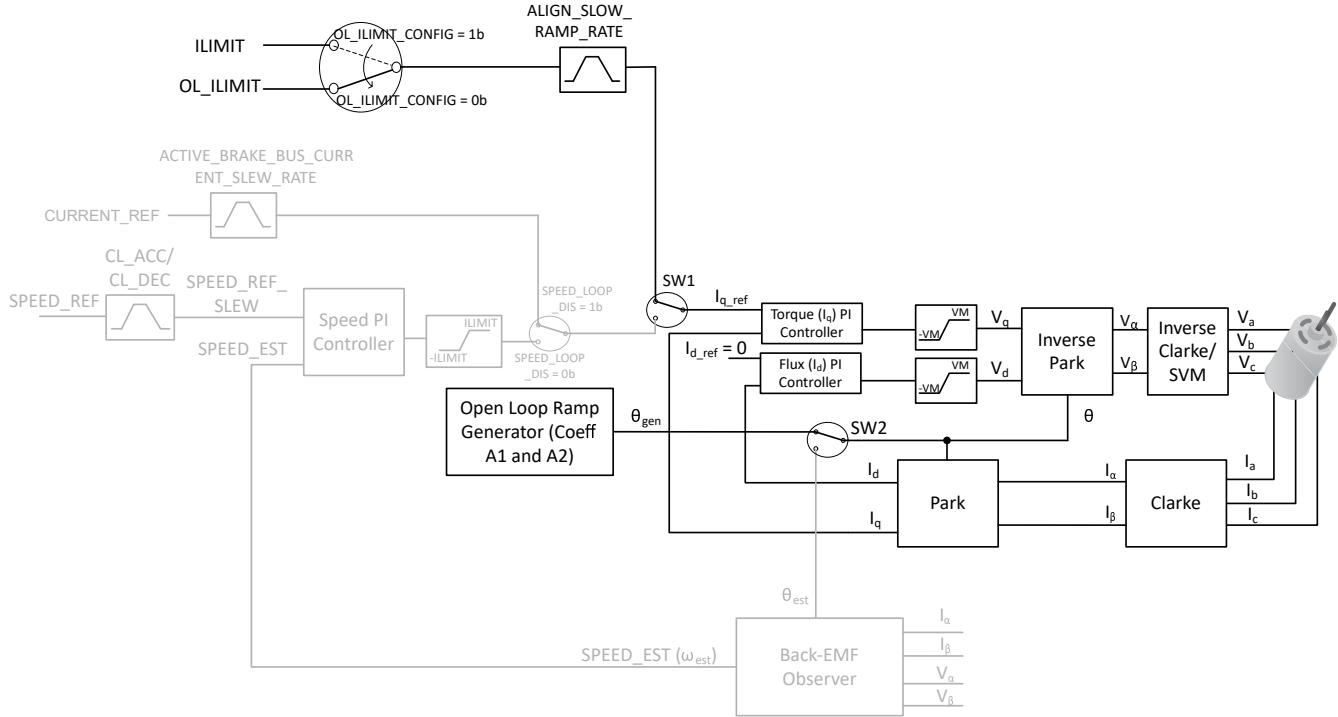


Figure 7-29. Open Loop

The function of the open-loop operation is to drive the motor to a speed at which the motor generates sufficient BEMF to allow the back-EMF observer to accurately detect the position of the rotor. The motor is accelerated in open loop and speed at any given time is determined by Equation 6. In MCF8316C-Q1, open loop acceleration coefficients, A1 and A2 are configured through OL\_ACC\_A1 and OL\_ACC\_A2 respectively.

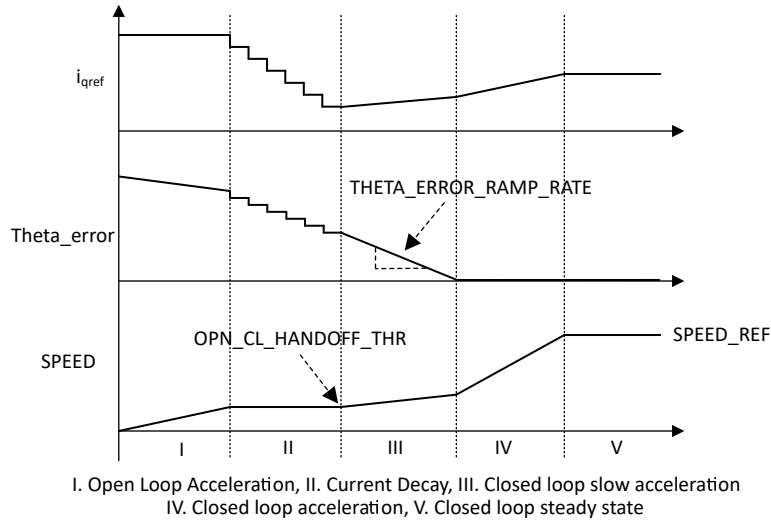
$$\text{Speed}(t) = A1 * t + 0.5 * A2 * t^2 \quad (6)$$

#### 7.3.10.4.6 Transition from Open to Closed Loop

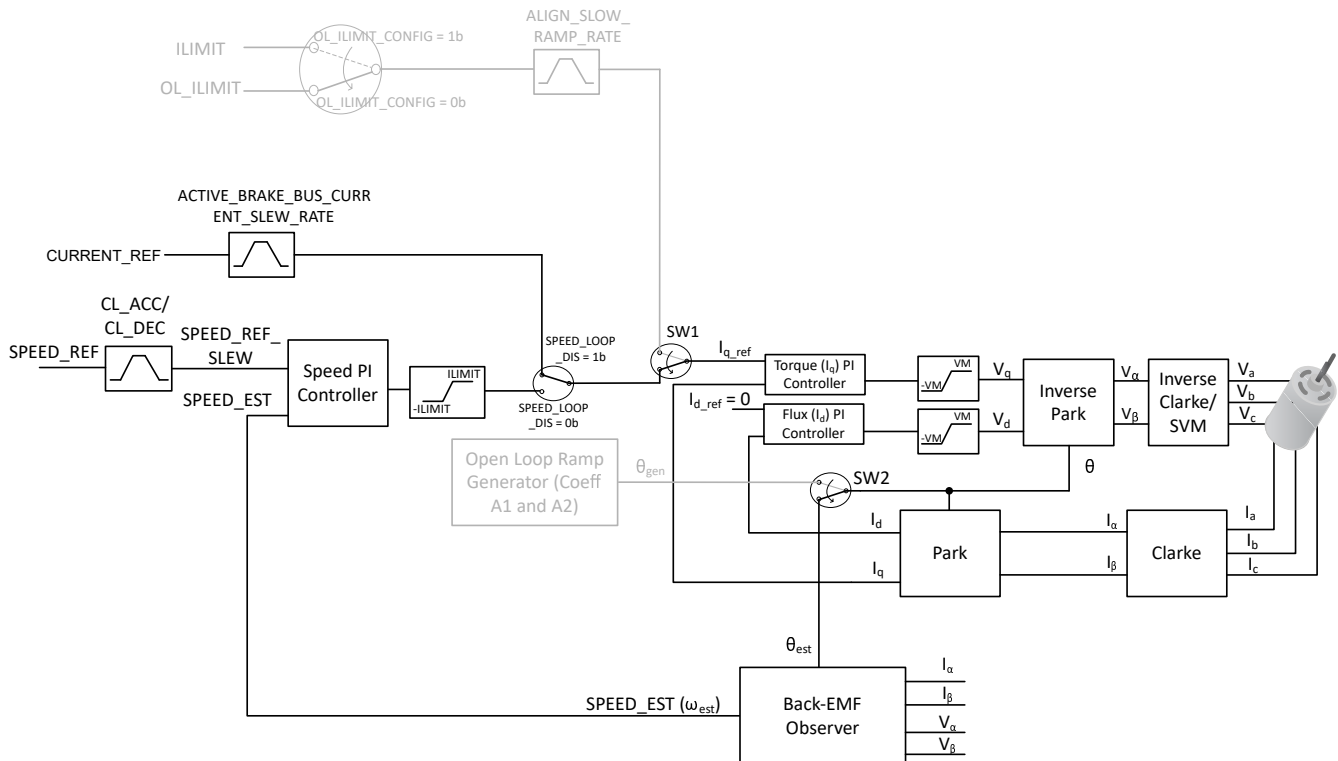
Once the motor has reached a sufficient speed for the back-EMF observer to estimate the angle and speed of the motor, the MCF8316C-Q1 transitions into closed loop state. This handoff speed is automatically determined based on the measured back-EMF and motor speed. Users also have an option to manually set the handoff speed by configuring OPN\_CL\_HANDOFF\_THR and setting AUTO\_HANDOFF\_EN to 0b. In order to have smooth transition and avoid speed transients, the theta error ( $\Theta_{\text{gen}} - \Theta_{\text{est}}$ ) is decreased linearly after transition. The ramp rate of theta error reduction can be configured using THETA\_ERROR\_RAMP\_RATE. If the current limit set during the open loop is high and if it is not reduced before transition to closed loop, the motor speed may momentarily rise to higher values than SPEED\_REF after transition into closed loop. In order to avoid such speed variations, configure the IQ\_RAMP\_EN to 1b, so that  $i_{q\_ref}$  decreases prior to transition into closed loop. However if the final speed reference (SPEED\_REF) is more than two times the open loop to closed loop hand off speed (OPN\_CL\_HANDOFF\_THR), then  $i_{q\_ref}$  is not decreased independent of the IQ\_RAMP\_EN setting, to enable faster motor acceleration.

After hand off to closed loop at a sufficient speed, there could be still some theta error, as the estimators may not be fully aligned. A slow acceleration can be used after the open loop to closed loop transition, ensuring that the theta error reduces to zero. The slow acceleration can be configured using CL\_SLOW\_ACC.

Figure 7-30 shows the control sequence in open to closed loop transition. The current  $i_{q\_ref}$  reduces to a lower value in current decay region, if IQ\_RAMP\_EN is set to 1b. If IQ\_RAMP\_EN is set to 0b, then the current decay region will not be present in the transition sequence.



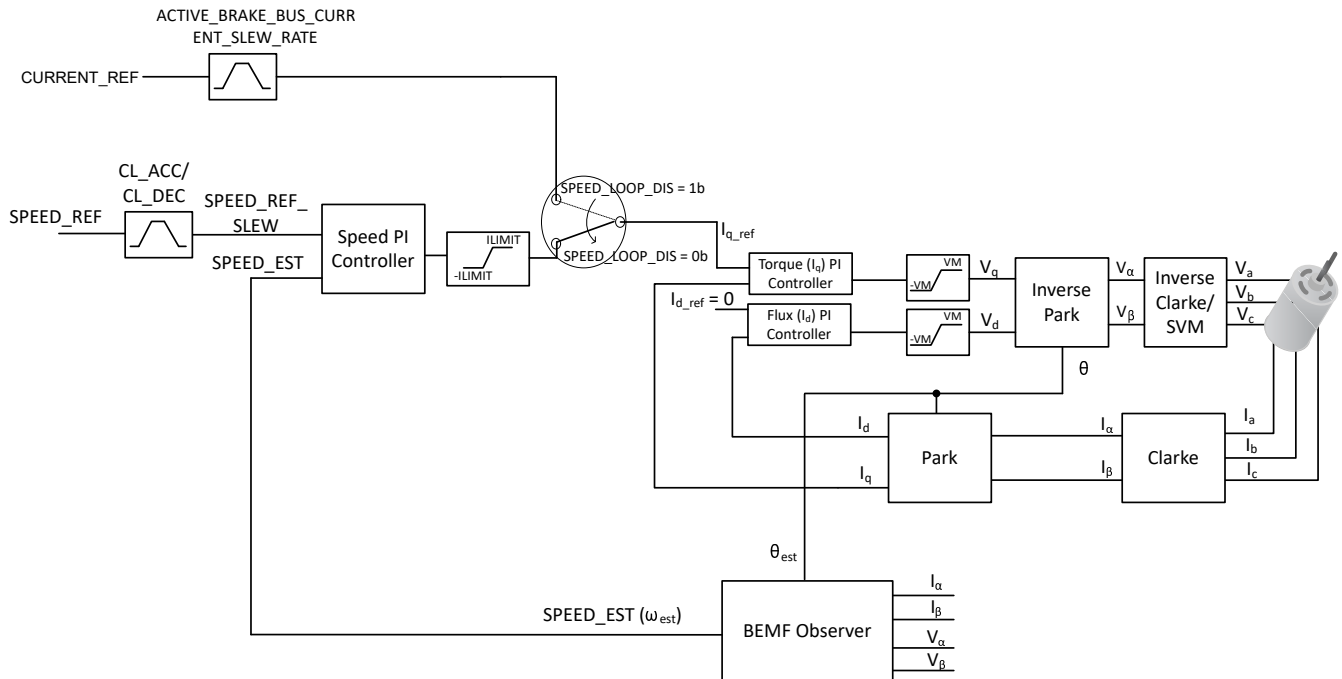
**Figure 7-30. Control Sequence in Open to Closed Loop Transition**



**Figure 7-31. Open to Closed Loop Transition Control Block Diagram**

### 7.3.11 Closed Loop Operation

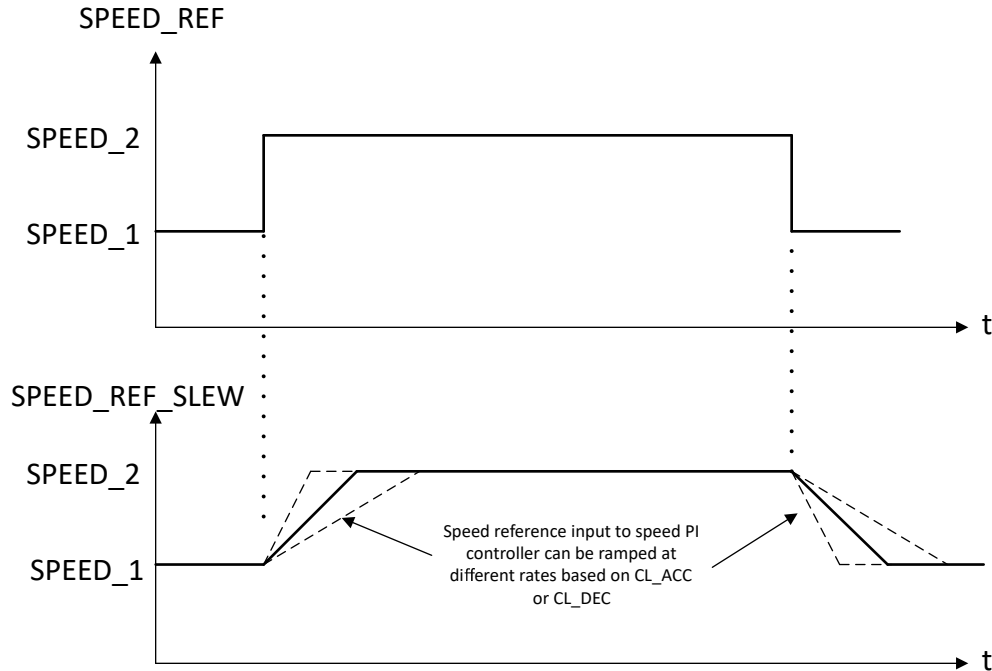
The MCF8316C-Q1 drives the motor using Field Oriented Control (FOC) as shown in [Figure 7-32](#). In closed loop operation, the motor angle ( $\theta_{est}$ ) and speed (Speed\_meas) are estimated using the back-EMF observer. The speed and current regulation are achieved using PI control loop. In order to achieve maximum efficiency, the direct axis current is set to zero ( $I_{d\_ref} = 0$ ), which will ensure that stator and rotor field are orthogonal ( $90^\circ$  out of phase) to each other.



**Figure 7-32. Closed Loop FOC Control**

### 7.3.11.1 Closed Loop Acceleration/Deceleration Slew Rate

During closed loop acceleration/deceleration, MCF8316C-Q1 provides the option of configuring the slew rate of the speed reference input to the speed PI controller (**SPEED\_REF\_SLEW** in Figure 7-32). This allows for a linear change in speed reference input (**SPEED\_REF\_SLEW**) even when there is a step change in speed reference (**SPEED\_REF** from Analog, PWM, Frequency or I<sup>2</sup>C) as seen in Figure 7-33. This slew rate can be configured so as to prevent sudden changes in the torque applied to the motor which could result in acoustic noise. The closed loop acceleration/deceleration slew rate parameter, **CL\_ACC/CL\_DEC**, sets the slew rate of **SPEED\_REF\_SLEW** during acceleration and deceleration (when AVS is not active) respectively.

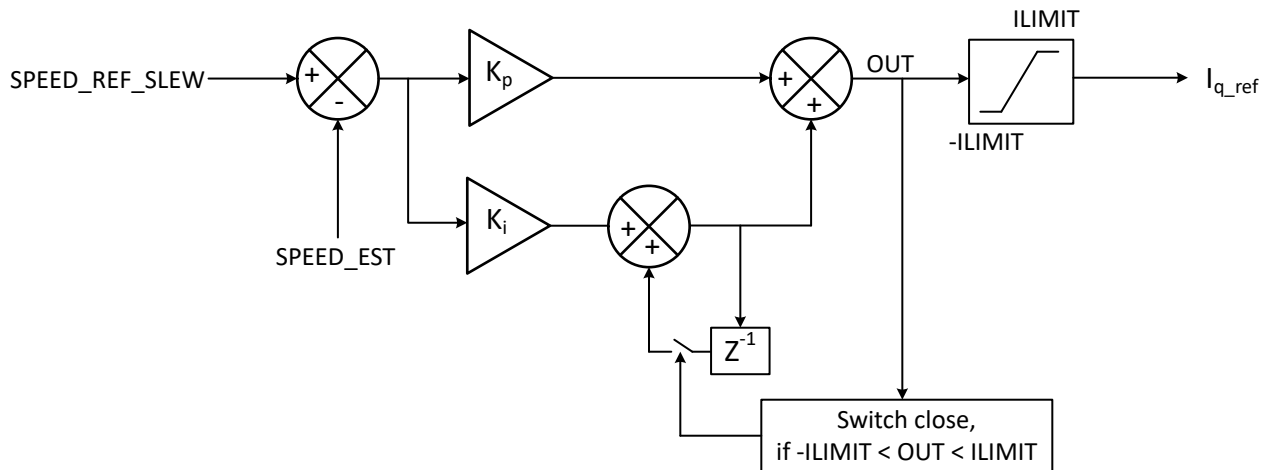


**Figure 7-33. Closed Loop Acceleration/Deceleration Slew Rate**

### 7.3.11.2 Speed PI Control

The integrated speed control loop helps maintain a constant speed over varying operating conditions. The  $K_p$  and  $K_i$  coefficients are configured through SPD\_LOOP\_KP and SPD\_LOOP\_KI. The output of the speed loop is used to generate the current reference for torque control ( $I_{q\_ref}$ ). The output of the speed loop is limited to implement a current limit. The current limit is set by configuring ILIMIT. When output of the speed loop saturates, the integrator is disabled to prevent integral wind-up.

SPEED\_REF\_SLEW is derived from the duty command input, speed profiles and closed loop acceleration/ deceleration rates configured by the user and SPEED\_EST is the estimated speed from the back-EMF observer.



**Figure 7-34. Speed PI Control**

### 7.3.11.3 Current PI Control

The MCF8316C-Q1 has two PI controllers, one each for  $I_d$  and  $I_q$  to control flux and torque separately.  $K_p$  and  $K_i$  coefficients are the same for both PI controllers and are configured through CURR\_LOOP\_KP and CURR\_LOOP\_KI. The outputs of the current control loops are used to generate voltage signals  $V_d$  and  $V_q$  to be

applied to the motor. The outputs of the current loops are clamped to supply voltage  $V_M$ .  $I_d$  current PI loop is executed first and output of  $I_d$  current PI loop  $V_d$  is checked for saturation. When the output of the current loop saturates, the integration is disabled to prevent integral wind-up.

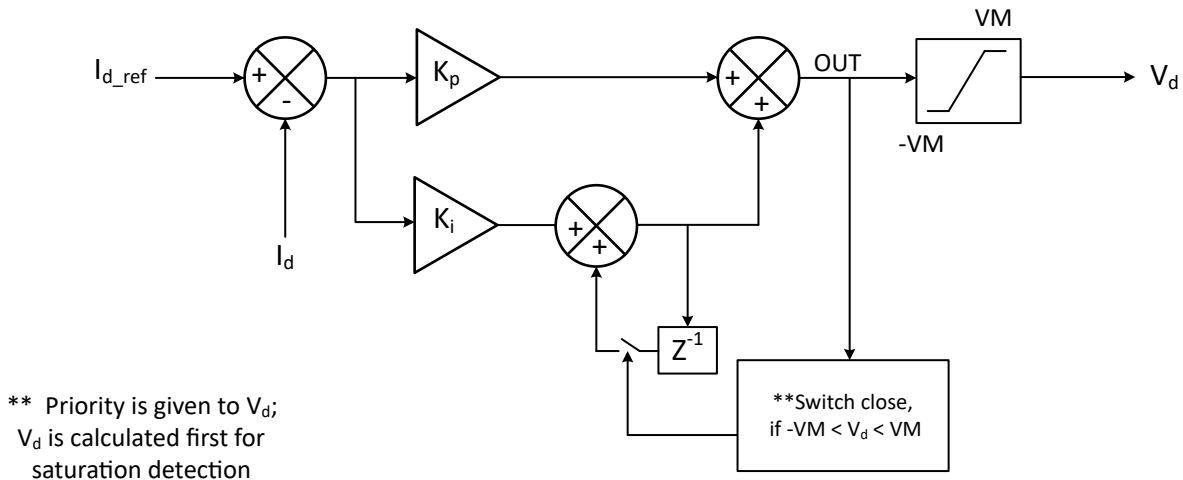


Figure 7-35.  $I_d$  Current PI Control

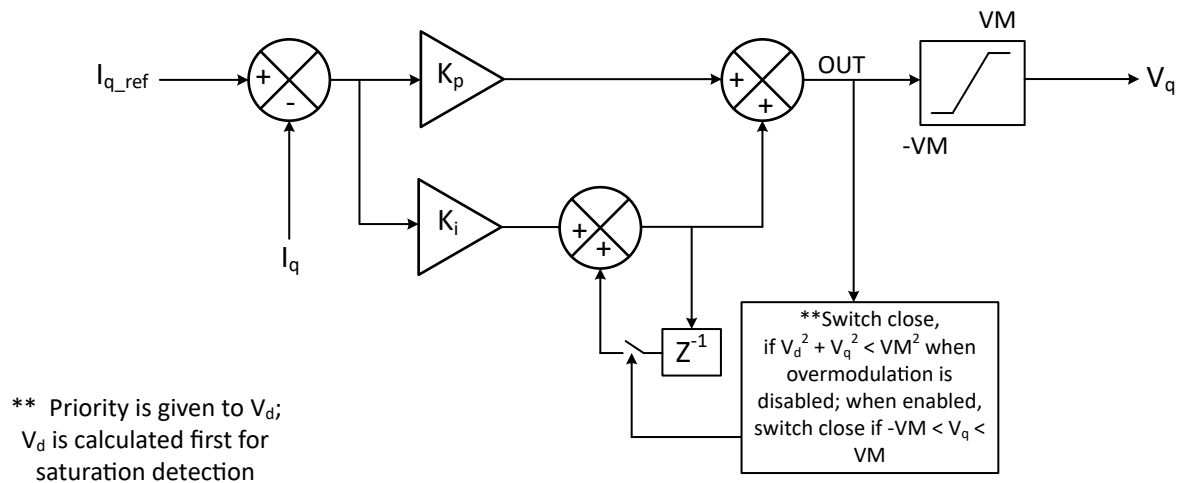


Figure 7-36.  $I_q$  Current PI Control

### 7.3.11.4 Torque Mode

MCF8316C-Q1 provides the option of disabling the speed loop by setting SPEED\_LOOP\_DIS to 1b. In this mode, the q-axis current reference,  $I_{q\_ref}$  is directly set by the product of duty cycle input, DUTY\_CMD (from PWM or I<sup>2</sup>C) and ILIMIT instead of the speed PI loop output as shown in Figure 7-32. Thus, this mode enables torque control through setting  $I_{q\_ref}$  directly and hence can be used for torque mode operation.

### 7.3.11.5 Overmodulation

MCF8316C-Q1 provides an overmodulation option to operate the motor at a higher speed at the same VM voltage by increasing the applied fundamental phase voltage by suitably modifying the applied PWM pattern - the higher fundamental phase voltage is accompanied by an increase in higher order harmonics. This feature can be enabled by setting OVERMODULATION\_ENABLE to 1b.

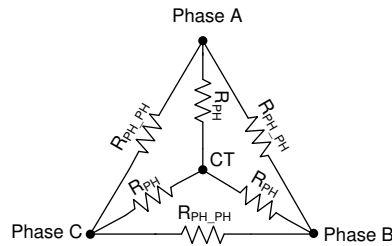
### 7.3.12 Motor Parameters

The MCF8316C-Q1 uses the motor resistance, motor inductance and motor back-EMF constant to estimate motor position when operating in closed loop. The MCF8316C-Q1 has the capability of measuring these

motor parameters in the offline state (see [Motor Parameter Extraction Tool \(MPET\)](#)). Offline measurement of parameters, when enabled, takes place before normal motor operation. The user can also disable the offline measurement and configure motor parameters through EEPROM. This feature of offline motor parameter measurement is useful to account for motor to motor variation during manufacturing.

### 7.3.12.1 Motor Resistance

For a wye-connected motor, the motor phase resistance refers to the resistance from the phase output to the center tap,  $R_{PH}$  (denoted as  $R_{PH}$  in [Figure 7-37](#)). For a delta-connected motor, the motor phase resistance refers to the equivalent phase to center tap in the wye configuration in [Figure 7-37](#).



**Figure 7-37. Motor Resistance**

For both the delta-connected and the wye-connected motor, the easy way to get the equivalent  $R_{PH}$  is to measure the resistance between two phase terminals ( $R_{PH\_PH}$ ), and then divide this value by two,  $R_{PH} = \frac{1}{2} R_{PH\_PH}$ . In wye-connected motor, if user has access to center tap (CT),  $R_{PH}$  can also be measured between center tap (CT) and phase terminal.

Configure the motor resistance ( $R_{PH}$ ) to a nearest value from [Table 7-2](#).

**Table 7-2. Motor Resistance Look-Up Table**

| MOTOR_RES (HEX) | $R_{PH}$ ( $\Omega$ )  | MOTOR_RES (HEX) | $R_{PH}$ ( $\Omega$ ) | MOTOR_RES (HEX) | $R_{PH}$ ( $\Omega$ ) | MOTOR_RES (HEX) | $R_{PH}$ ( $\Omega$ ) |
|-----------------|--|-----------------|-----------------------|-----------------|-----------------------|-----------------|-----------------------|
| 0x00            | Self Measurement (see <a href="#">Motor Parameter Extraction Tool (MPET)</a> ) | 0x40            | 0.145                 | 0x80            | 0.465                 | 0xC0            | 2.1                   |
| 0x01            | 0.006  | 0x41            | 0.150                 | 0x81            | 0.470                 | 0xC1            | 2.2                   |
| 0x02            | 0.007  | 0x42            | 0.155                 | 0x82            | 0.475                 | 0xC2            | 2.3                   |
| 0x03            | 0.008  | 0x43            | 0.160                 | 0x83            | 0.480                 | 0xC3            | 2.4                   |
| 0x04            | 0.009  | 0x44            | 0.165                 | 0x84            | 0.485                 | 0xC4            | 2.5                   |
| 0x05            | 0.010  | 0x45            | 0.170                 | 0x85            | 0.490                 | 0xC5            | 2.6                   |
| 0x06            | 0.011  | 0x46            | 0.175                 | 0x86            | 0.495                 | 0xC6            | 2.7                   |
| 0x07            | 0.012  | 0x47            | 0.180                 | 0x87            | 0.50                  | 0xC7            | 2.8                   |
| 0x08            | 0.013  | 0x48            | 0.185                 | 0x88            | 0.51                  | 0xC8            | 2.9                   |
| 0x09            | 0.014  | 0x49            | 0.190                 | 0x89            | 0.52                  | 0xC9            | 3.0                   |
| 0x0A            | 0.015  | 0x4A            | 0.195                 | 0x8A            | 0.53                  | 0xCA            | 3.2                   |
| 0x0B            | 0.016  | 0x4B            | 0.200                 | 0x8B            | 0.54                  | 0xCB            | 3.4                   |
| 0x0C            | 0.017  | 0x4C            | 0.205                 | 0x8C            | 0.55                  | 0xCC            | 3.6                   |
| 0x0D            | 0.018  | 0x4D            | 0.210                 | 0x8D            | 0.56                  | 0xCD            | 3.8                   |
| 0x0E            | 0.019  | 0x4E            | 0.215                 | 0x8E            | 0.57                  | 0xCE            | 4.0                   |
| 0x0F            | 0.020  | 0x4F            | 0.220                 | 0x8F            | 0.58                  | 0xCF            | 4.2                   |
| 0x10            | 0.022  | 0x50            | 0.225                 | 0x90            | 0.59                  | 0xD0            | 4.4                   |
| 0x11            | 0.024  | 0x51            | 0.230                 | 0x91            | 0.60                  | 0xD1            | 4.6                   |
| 0x12            | 0.026  | 0x52            | 0.235                 | 0x92            | 0.61                  | 0xD2            | 4.8                   |



**Table 7-2. Motor Resistance Look-Up Table (continued)**

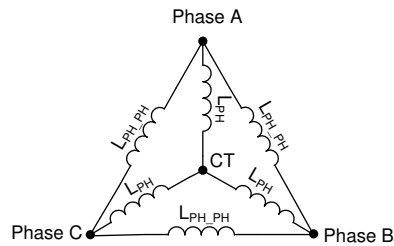
| MOTOR_RES (HEX) | R <sub>PH</sub> (Ω) | MOTOR_RES (HEX) | R <sub>PH</sub> (Ω) | MOTOR_RES (HEX) | R <sub>PH</sub> (Ω) | MOTOR_RES (HEX) | R <sub>PH</sub> (Ω) |
|-----------------|---------------------|-----------------|---------------------|-----------------|---------------------|-----------------|---------------------|
| 0x13            | 0.028               | 0x53            | 0.240               | 0x93            | 0.62                | 0xD3            | 5.0                 |
| 0x14            | 0.030               | 0x54            | 0.245               | 0x94            | 0.63                | 0xD4            | 5.2                 |
| 0x15            | 0.032               | 0x55            | 0.250               | 0x95            | 0.64                | 0xD5            | 5.4                 |
| 0x16            | 0.034               | 0x56            | 0.255               | 0x96            | 0.65                | 0xD6            | 5.6                 |
| 0x17            | 0.036               | 0x57            | 0.260               | 0x97            | 0.66                | 0xD7            | 5.8                 |
| 0x18            | 0.038               | 0x58            | 0.265               | 0x98            | 0.67                | 0xD8            | 6.0                 |
| 0x19            | 0.040               | 0x59            | 0.270               | 0x99            | 0.68                | 0xD9            | 6.2                 |
| 0x1A            | 0.042               | 0x5A            | 0.275               | 0x9A            | 0.69                | 0xDA            | 6.4                 |
| 0x1B            | 0.044               | 0x5B            | 0.280               | 0x9B            | 0.70                | 0xDB            | 6.6                 |
| 0x1C            | 0.046               | 0x5C            | 0.285               | 0x9C            | 0.72                | 0xDC            | 6.8                 |
| 0x1D            | 0.048               | 0x5D            | 0.290               | 0x9D            | 0.74                | 0xDD            | 7.0                 |
| 0x1E            | 0.050               | 0x5E            | 0.295               | 0x9E            | 0.76                | 0xDE            | 7.2                 |
| 0x1F            | 0.052               | 0x5F            | 0.300               | 0x9F            | 0.78                | 0xDF            | 7.4                 |
| 0x20            | 0.054               | 0x60            | 0.305               | 0xA0            | 0.80                | 0xE0            | 7.6                 |
| 0x21            | 0.056               | 0x61            | 0.310               | 0xA1            | 0.82                | 0xE1            | 7.8                 |
| 0x22            | 0.058               | 0x62            | 0.315               | 0xA2            | 0.84                | 0xE2            | 8.0                 |
| 0x23            | 0.060               | 0x63            | 0.320               | 0xA3            | 0.86                | 0xE3            | 8.2                 |
| 0x24            | 0.062               | 0x64            | 0.325               | 0xA4            | 0.88                | 0xE4            | 8.4                 |
| 0x25            | 0.064               | 0x65            | 0.330               | 0xA5            | 0.90                | 0xE5            | 8.6                 |
| 0x26            | 0.066               | 0x66            | 0.335               | 0xA6            | 0.92                | 0xE6            | 8.8                 |
| 0x27            | 0.068               | 0x67            | 0.340               | 0xA7            | 0.94                | 0xE7            | 9                   |
| 0x28            | 0.070               | 0x68            | 0.345               | 0xA8            | 0.96                | 0xE8            | 9.2                 |
| 0x29            | 0.072               | 0x69            | 0.350               | 0xA9            | 0.98                | 0xE9            | 9.4                 |
| 0x2A            | 0.074               | 0x6A            | 0.355               | 0xAA            | 1.00                | 0xEA            | 9.6                 |
| 0x2B            | 0.076               | 0x6B            | 0.360               | 0xAB            | 1.05                | 0xEB            | 9.8                 |
| 0x2C            | 0.078               | 0x6C            | 0.365               | 0xAC            | 1.10                | 0xEC            | 10.0                |
| 0x2D            | 0.080               | 0x6D            | 0.370               | 0xAD            | 1.15                | 0xED            | 10.5                |
| 0x2E            | 0.082               | 0x6E            | 0.375               | 0xAE            | 1.20                | 0xEE            | 11.0                |
| 0x2F            | 0.084               | 0x6F            | 0.380               | 0xAF            | 1.25                | 0xEF            | 11.5                |
| 0x30            | 0.086               | 0x70            | 0.385               | 0xB0            | 1.30                | 0xF0            | 12.0                |
| 0x31            | 0.088               | 0x71            | 0.390               | 0xB1            | 1.35                | 0xF1            | 12.5                |
| 0x32            | 0.090               | 0x72            | 0.395               | 0xB2            | 1.40                | 0xF2            | 13.0                |
| 0x33            | 0.092               | 0x73            | 0.400               | 0xB3            | 1.45                | 0xF3            | 13.5                |
| 0x34            | 0.094               | 0x74            | 0.405               | 0xB4            | 1.50                | 0xF4            | 14.0                |
| 0x35            | 0.096               | 0x75            | 0.410               | 0xB5            | 1.55                | 0xF5            | 14.5                |
| 0x36            | 0.098               | 0x76            | 0.415               | 0xB6            | 1.60                | 0xF6            | 15.0                |
| 0x37            | 0.100               | 0x77            | 0.420               | 0xB7            | 1.65                | 0xF7            | 15.5                |
| 0x38            | 0.105               | 0x78            | 0.425               | 0xB8            | 1.70                | 0xF8            | 16.0                |
| 0x39            | 0.110               | 0x79            | 0.430               | 0xB9            | 1.75                | 0xF9            | 16.5                |
| 0x3A            | 0.115               | 0x7A            | 0.435               | 0xBA            | 1.80                | 0xFA            | 17.0                |
| 0x3B            | 0.120               | 0x7B            | 0.440               | 0xBB            | 1.85                | 0xFB            | 17.5                |
| 0x3C            | 0.125               | 0x7C            | 0.445               | 0xBC            | 1.90                | 0xFC            | 18.0                |
| 0x3D            | 0.130               | 0x7D            | 0.450               | 0xBD            | 1.95                | 0xFD            | 18.5                |
| 0x3E            | 0.135               | 0x7E            | 0.455               | 0xBE            | 2.00                | 0xFE            | 19.0                |

**Table 7-2. Motor Resistance Look-Up Table (continued)**

| MOTOR_RES (HEX) | R <sub>PH</sub> (Ω) | MOTOR_RES (HEX) | R <sub>PH</sub> (Ω) | MOTOR_RES (HEX) | R <sub>PH</sub> (Ω) | MOTOR_RES (HEX) | R <sub>PH</sub> (Ω) |
|-----------------|---------------------|-----------------|---------------------|-----------------|---------------------|-----------------|---------------------|
| 0x3F            | 0.140               | 0x7F            | 0.460               | 0xBF            | 2.05                | 0xFF            | 20.0                |

### 7.3.12.2 Motor Inductance

For a wye-connected motor, the motor phase inductance refers to the inductance from the phase output to the center tap, L<sub>PH</sub> (denoted as L<sub>PH</sub> in Figure 7-38). For a delta-connected motor, the motor phase inductance refers to the equivalent phase to center tap in the wye configuration in Figure 7-38.



**Figure 7-38. Motor Inductance**

For both the delta-connected motor and the wye-connected motor, the easy way to get the equivalent L<sub>PH</sub> is to measure the inductance between two phase terminals (L<sub>PH\_PH</sub>), and then divide this value by two, L<sub>PH</sub> = ½ L<sub>PH\_PH</sub>. In wye-connected motor, if user has access to center tap (CT), L<sub>PH</sub> can also be measured between center tap (CT) and phase terminal.

Configure the motor inductance (L<sub>PH</sub>) to a nearest value from Table 7-3.

**Table 7-3. Motor Inductance Look-Up Table**

| MOTOR_IND (HEX) | L <sub>PH</sub> (mH)  | MOTOR_IND (HEX) | L <sub>PH</sub> (mH) | MOTOR_IND (HEX) | L <sub>PH</sub> (mH) | MOTOR_IND (HEX) | L <sub>PH</sub> (mH) |
|-----------------|---|-----------------|----------------------|-----------------|----------------------|-----------------|----------------------|
| 0x00            | Self Measurement (see Motor Parameter Extraction Tool (MPET)) | 0x40            | 0.145                | 0x80            | 0.465                | 0xC0            | 2.1                  |
| 0x01            | 0.006   | 0x41            | 0.150                | 0x81            | 0.470                | 0xC1            | 2.2                  |
| 0x02            | 0.007   | 0x42            | 0.155                | 0x82            | 0.475                | 0xC2            | 2.3                  |
| 0x03            | 0.008   | 0x43            | 0.160                | 0x83            | 0.480                | 0xC3            | 2.4                  |
| 0x04            | 0.009   | 0x44            | 0.165                | 0x84            | 0.485                | 0xC4            | 2.5                  |
| 0x05            | 0.010   | 0x45            | 0.170                | 0x85            | 0.490                | 0xC5            | 2.6                  |
| 0x06            | 0.011   | 0x46            | 0.175                | 0x86            | 0.495                | 0xC6            | 2.7                  |
| 0x07            | 0.012   | 0x47            | 0.180                | 0x87            | 0.50                 | 0xC7            | 2.8                  |
| 0x08            | 0.013   | 0x48            | 0.185                | 0x88            | 0.51                 | 0xC8            | 2.9                  |
| 0x09            | 0.014   | 0x49            | 0.190                | 0x89            | 0.52                 | 0xC9            | 3.0                  |
| 0x0A            | 0.015   | 0x4A            | 0.195                | 0x8A            | 0.53                 | 0xCA            | 3.2                  |
| 0x0B            | 0.016   | 0x4B            | 0.200                | 0x8B            | 0.54                 | 0xCB            | 3.4                  |
| 0x0C            | 0.017   | 0x4C            | 0.205                | 0x8C            | 0.55                 | 0xCC            | 3.6                  |
| 0x0D            | 0.018   | 0x4D            | 0.210                | 0x8D            | 0.56                 | 0xCD            | 3.8                  |
| 0x0E            | 0.019   | 0x4E            | 0.215                | 0x8E            | 0.57                 | 0xCE            | 4.0                  |
| 0x0F            | 0.020   | 0x4F            | 0.220                | 0x8F            | 0.58                 | 0xCF            | 4.2                  |
| 0x10            | 0.022   | 0x50            | 0.225                | 0x90            | 0.59                 | 0xD0            | 4.4                  |
| 0x11            | 0.024   | 0x51            | 0.230                | 0x91            | 0.60                 | 0xD1            | 4.6                  |
| 0x12            | 0.026   | 0x52            | 0.235                | 0x92            | 0.61                 | 0xD2            | 4.8                  |
| 0x13            | 0.028   | 0x53            | 0.240                | 0x93            | 0.62                 | 0xD3            | 5.0                  |
| 0x14            | 0.030   | 0x54            | 0.245                | 0x94            | 0.63                 | 0xD4            | 5.2                  |
| 0x15            | 0.032   | 0x55            | 0.250                | 0x95            | 0.64                 | 0xD5            | 5.4                  |
| 0x16            | 0.034   | 0x56            | 0.255                | 0x96            | 0.65                 | 0xD6            | 5.6                  |
| 0x17            | 0.036   | 0x57            | 0.260                | 0x97            | 0.66                 | 0xD7            | 5.8                  |
| 0x18            | 0.038   | 0x58            | 0.265                | 0x98            | 0.67                 | 0xD8            | 6.0                  |
| 0x19            | 0.040   | 0x59            | 0.270                | 0x99            | 0.68                 | 0xD9            | 6.2                  |
| 0x1A            | 0.042   | 0x5A            | 0.275                | 0x9A            | 0.69                 | 0xDA            | 6.4                  |
| 0x1B            | 0.044   | 0x5B            | 0.280                | 0x9B            | 0.70                 | 0xDB            | 6.6                  |
| 0x1C            | 0.046   | 0x5C            | 0.285                | 0x9C            | 0.72                 | 0xDC            | 6.8                  |
| 0x1D            | 0.048   | 0x5D            | 0.290                | 0x9D            | 0.74                 | 0xDD            | 7.0                  |
| 0x1E            | 0.050   | 0x5E            | 0.295                | 0x9E            | 0.76                 | 0xDE            | 7.2                  |
| 0x1F            | 0.052   | 0x5F            | 0.300                | 0x9F            | 0.78                 | 0xDF            | 7.4                  |
| 0x20            | 0.054   | 0x60            | 0.305                | 0xA0            | 0.80                 | 0xE0            | 7.6                  |
| 0x21            | 0.056   | 0x61            | 0.310                | 0xA1            | 0.82                 | 0xE1            | 7.8                  |
| 0x22            | 0.058   | 0x62            | 0.315                | 0xA2            | 0.84                 | 0xE2            | 8.0                  |
| 0x23            | 0.060   | 0x63            | 0.320                | 0xA3            | 0.86                 | 0xE3            | 8.2                  |
| 0x24            | 0.062   | 0x64            | 0.325                | 0xA4            | 0.88                 | 0xE4            | 8.4                  |
| 0x25            | 0.064   | 0x65            | 0.330                | 0xA5            | 0.90                 | 0xE5            | 8.6                  |
| 0x26            | 0.066   | 0x66            | 0.335                | 0xA6            | 0.92                 | 0xE6            | 8.8                  |
| 0x27            | 0.068   | 0x67            | 0.340                | 0xA7            | 0.94                 | 0xE7            | 9                    |
| 0x28            | 0.070   | 0x68            | 0.345                | 0xA8            | 0.96                 | 0xE8            | 9.2                  |

**Table 7-3. Motor Inductance Look-Up Table (continued)**

| MOTOR_IND (HEX) | L <sub>PH</sub> (mH) | MOTOR_IND (HEX) | L <sub>PH</sub> (mH) | MOTOR_IND (HEX) | L <sub>PH</sub> (mH) | MOTOR_IND (HEX) | L <sub>PH</sub> (mH) |
|-----------------|----------------------|-----------------|----------------------|-----------------|----------------------|-----------------|----------------------|
| 0x29            | 0.072                | 0x69            | 0.350                | 0xA9            | 0.98                 | 0xE9            | 9.4                  |
| 0x2A            | 0.074                | 0x6A            | 0.355                | 0xAA            | 1.00                 | 0xEA            | 9.6                  |
| 0x2B            | 0.076                | 0x6B            | 0.360                | 0xAB            | 1.05                 | 0xEB            | 9.8                  |
| 0x2C            | 0.078                | 0x6C            | 0.365                | 0xAC            | 1.10                 | 0xEC            | 10.0                 |
| 0x2D            | 0.080                | 0x6D            | 0.370                | 0xAD            | 1.15                 | 0xED            | 10.5                 |
| 0x2E            | 0.082                | 0x6E            | 0.375                | 0xAE            | 1.20                 | 0xEE            | 11.0                 |
| 0x2F            | 0.084                | 0x6F            | 0.380                | 0xAF            | 1.25                 | 0xEF            | 11.5                 |
| 0x30            | 0.086                | 0x70            | 0.385                | 0xB0            | 1.30                 | 0xF0            | 12.0                 |
| 0x31            | 0.088                | 0x71            | 0.390                | 0xB1            | 1.35                 | 0xF1            | 12.5                 |
| 0x32            | 0.090                | 0x72            | 0.395                | 0xB2            | 1.40                 | 0xF2            | 13.0                 |
| 0x33            | 0.092                | 0x73            | 0.400                | 0xB3            | 1.45                 | 0xF3            | 13.5                 |
| 0x34            | 0.094                | 0x74            | 0.405                | 0xB4            | 1.50                 | 0xF4            | 14.0                 |
| 0x35            | 0.096                | 0x75            | 0.410                | 0xB5            | 1.55                 | 0xF5            | 14.5                 |
| 0x36            | 0.098                | 0x76            | 0.415                | 0xB6            | 1.60                 | 0xF6            | 15.0                 |
| 0x37            | 0.100                | 0x77            | 0.420                | 0xB7            | 1.65                 | 0xF7            | 15.5                 |
| 0x38            | 0.105                | 0x78            | 0.425                | 0xB8            | 1.70                 | 0xF8            | 16.0                 |
| 0x39            | 0.110                | 0x79            | 0.430                | 0xB9            | 1.75                 | 0xF9            | 16.5                 |
| 0x3A            | 0.115                | 0x7A            | 0.435                | 0xBA            | 1.80                 | 0xFA            | 17.0                 |
| 0x3B            | 0.120                | 0x7B            | 0.440                | 0xBB            | 1.85                 | 0xFB            | 17.5                 |
| 0x3C            | 0.125                | 0x7C            | 0.445                | 0xBC            | 1.90                 | 0xFC            | 18.0                 |
| 0x3D            | 0.130                | 0x7D            | 0.450                | 0xBD            | 1.95                 | 0xFD            | 18.5                 |
| 0x3E            | 0.135                | 0x7E            | 0.455                | 0xBE            | 2.00                 | 0xFE            | 19.0                 |
| 0x3F            | 0.140                | 0x7F            | 0.460                | 0xBF            | 2.05                 | 0xFF            | 20.0                 |

**7.3.12.3 Motor Back-EMF constant**

The back-EMF constant describes the motor phase-to-neutral back-EMF voltage as a function of the motor speed. For a wye-connected motor, the motor BEMF constant refers to the BEMF as a function of time from the phase output to the center tap,  $K_{t_{PH\_N}}$  (denoted as  $K_{t_{PH\_N}}$  in [Figure 7-39](#)). For a delta-connected motor, the motor BEMF constant refers to the equivalent phase to center tap in the wye configuration in [Figure 7-39](#).

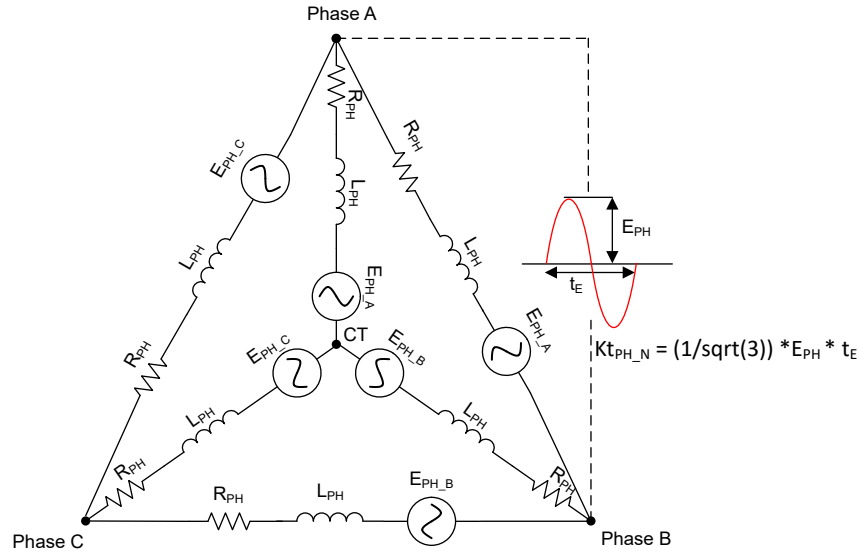


Figure 7-39. Motor back-EMF constant

For both the delta-connected motor and the wye-connected motor, the easy way to get the equivalent  $K_{t_{PH\_N}}$  is to measure the peak value of BEMF on scope for one electrical cycle between two phase terminals ( $E_{PH}$ ), and then multiply by time duration of one electrical cycle and in order to convert from phase-to-phase to phase-to-neutral divide by  $\sqrt{3}$  as shown in Equation 7 .

$$K_{t_{PH\_N}} = \frac{1}{\sqrt{3}} \times E_{PH} \times t_E \quad (7)$$

Configure the motor BEMF constant ( $K_{t_{PH\_N}}$ ) to a nearest value from Table 7-4.

Table 7-4. Motor BEMF constant Look-Up Table

| MOTOR_BEMF_CONST (HEX) | $K_{t_{PH\_N}}$ (mV/Hz)                                       | MOTOR_BEMF_CONST (HEX) | $K_{t_{PH\_N}}$ (mV/Hz) | MOTOR_BEMF_CONST (HEX) | $K_{t_{PH\_N}}$ (mV/Hz) | MOTOR_BEMF_CONST (HEX) | $K_{t_{PH\_N}}$ (mV/Hz) |
|------------------------|---|------------------------|-------------------------|------------------------|-------------------------|------------------------|-------------------------|
| 0x00                   | Self Measurement (see Motor Parameter Extraction Tool (MPET)) | 0x40                   | 14.5                    | 0x80                   | 46.5                    | 0xC0                   | 210                     |
| 0x01                   | 0.6   | 0x41                   | 15.0                    | 0x81                   | 47.0                    | 0xC1                   | 220                     |
| 0x02                   | 0.7   | 0x42                   | 15.5                    | 0x82                   | 47.5                    | 0xC2                   | 230                     |
| 0x03                   | 0.8   | 0x43                   | 16.0                    | 0x83                   | 48.0                    | 0xC3                   | 240                     |
| 0x04                   | 0.9   | 0x44                   | 16.5                    | 0x84                   | 48.5                    | 0xC4                   | 250                     |
| 0x05                   | 1.0   | 0x45                   | 17.0                    | 0x85                   | 49.0                    | 0xC5                   | 260                     |
| 0x06                   | 1.1   | 0x46                   | 17.5                    | 0x86                   | 49.5                    | 0xC6                   | 270                     |
| 0x07                   | 1.2   | 0x47                   | 18.0                    | 0x87                   | 50.0                    | 0xC7                   | 280                     |
| 0x08                   | 1.3   | 0x48                   | 18.5                    | 0x88                   | 51                      | 0xC8                   | 290                     |
| 0x09                   | 1.4   | 0x49                   | 19.0                    | 0x89                   | 52                      | 0xC9                   | 300                     |
| 0x0A                   | 1.5   | 0x4A                   | 19.5                    | 0x8A                   | 53                      | 0xCA                   | 320                     |
| 0x0B                   | 1.6   | 0x4B                   | 20.0                    | 0x8B                   | 54                      | 0xCB                   | 340                     |
| 0x0C                   | 1.7   | 0x4C                   | 20.5                    | 0x8C                   | 55                      | 0xCC                   | 360                     |
| 0x0D                   | 1.8   | 0x4D                   | 21.0                    | 0x8D                   | 56                      | 0xCD                   | 380                     |
| 0x0E                   | 1.9   | 0x4E                   | 21.5                    | 0x8E                   | 57                      | 0xCE                   | 400                     |
| 0x0F                   | 2.0   | 0x4F                   | 22.0                    | 0x8F                   | 58                      | 0xCF                   | 420                     |

**Table 7-4. Motor BEMF constant Look-Up Table (continued)**

| MOTOR_BEMF_ CONST (HEX) | Kt <sub>PH_N</sub> (mV/Hz) | MOTOR_BEMF_ CONST (HEX) | Kt <sub>PH_N</sub> (mV/Hz) | MOTOR_BEMF_ CONST (HEX) | Kt <sub>PH_N</sub> (mV/Hz) | MOTOR_BEMF_ CONST (HEX) | Kt <sub>PH_N</sub> (mV/Hz) |
|-------------------------|----------------------------|-------------------------|----------------------------|-------------------------|----------------------------|-------------------------|----------------------------|
| 0x10                    | 2.2                        | 0x50                    | 22.5                       | 0x90                    | 59                         | 0xD0                    | 440                        |
| 0x11                    | 2.4                        | 0x51                    | 23.0                       | 0x91                    | 60                         | 0xD1                    | 460                        |
| 0x12                    | 2.6                        | 0x52                    | 23.5                       | 0x92                    | 61                         | 0xD2                    | 480                        |
| 0x13                    | 2.8                        | 0x53                    | 24.0                       | 0x93                    | 62                         | 0xD3                    | 500                        |
| 0x14                    | 3.0                        | 0x54                    | 24.5                       | 0x94                    | 63                         | 0xD4                    | 520                        |
| 0x15                    | 3.2                        | 0x55                    | 25.0                       | 0x95                    | 64                         | 0xD5                    | 540                        |
| 0x16                    | 3.4                        | 0x56                    | 25.5                       | 0x96                    | 65                         | 0xD6                    | 560                        |
| 0x17                    | 3.6                        | 0x57                    | 26.0                       | 0x97                    | 66                         | 0xD7                    | 580                        |
| 0x18                    | 3.8                        | 0x58                    | 26.5                       | 0x98                    | 67                         | 0xD8                    | 600                        |
| 0x19                    | 4.0                        | 0x59                    | 27.0                       | 0x99                    | 68                         | 0xD9                    | 620                        |
| 0x1A                    | 4.2                        | 0x5A                    | 27.5                       | 0x9A                    | 69                         | 0xDA                    | 640                        |
| 0x1B                    | 4.4                        | 0x5B                    | 28.0                       | 0x9B                    | 70                         | 0xDB                    | 660                        |
| 0x1C                    | 4.6                        | 0x5C                    | 28.5                       | 0x9C                    | 72                         | 0xDC                    | 680                        |
| 0x1D                    | 4.8                        | 0x5D                    | 29.0                       | 0x9D                    | 74                         | 0xDD                    | 700                        |
| 0x1E                    | 5.0                        | 0x5E                    | 29.5                       | 0x9E                    | 76                         | 0xDE                    | 720                        |
| 0x1F                    | 5.2                        | 0x5F                    | 30.0                       | 0x9F                    | 78                         | 0xDF                    | 740                        |
| 0x20                    | 5.4                        | 0x60                    | 30.5                       | 0xA0                    | 80                         | 0xE0                    | 760                        |
| 0x21                    | 5.6                        | 0x61                    | 31.0                       | 0xA1                    | 82                         | 0xE1                    | 780                        |
| 0x22                    | 5.8                        | 0x62                    | 31.5                       | 0xA2                    | 84                         | 0xE2                    | 800                        |
| 0x23                    | 6.0                        | 0x63                    | 32.0                       | 0xA3                    | 86                         | 0xE3                    | 820                        |
| 0x24                    | 6.2                        | 0x64                    | 32.5                       | 0xA4                    | 88                         | 0xE4                    | 840                        |
| 0x25                    | 6.4                        | 0x65                    | 33.0                       | 0xA5                    | 90                         | 0xE5                    | 860                        |
| 0x26                    | 6.6                        | 0x66                    | 33.5                       | 0xA6                    | 92                         | 0xE6                    | 880                        |
| 0x27                    | 6.8                        | 0x67                    | 34.0                       | 0xA7                    | 94                         | 0xE7                    | 900                        |
| 0x28                    | 7.0                        | 0x68                    | 34.5                       | 0xA8                    | 96                         | 0xE8                    | 920                        |
| 0x29                    | 7.2                        | 0x69                    | 35.0                       | 0xA9                    | 98                         | 0xE9                    | 940                        |
| 0x2A                    | 7.4                        | 0x6A                    | 35.5                       | 0xAA                    | 100                        | 0xEA                    | 960                        |
| 0x2B                    | 7.6                        | 0x6B                    | 36.0                       | 0xAB                    | 105                        | 0xEB                    | 980                        |
| 0x2C                    | 7.8                        | 0x6C                    | 36.5                       | 0xAC                    | 110                        | 0xEC                    | 1000                       |
| 0x2D                    | 8.0                        | 0x6D                    | 37.0                       | 0xAD                    | 115                        | 0xED                    | 1050                       |
| 0x2E                    | 8.2                        | 0x6E                    | 37.5                       | 0xAE                    | 120                        | 0xEE                    | 1100                       |
| 0x2F                    | 8.4                        | 0x6F                    | 38.0                       | 0xAF                    | 125                        | 0xEF                    | 1150                       |
| 0x30                    | 8.6                        | 0x70                    | 38.5                       | 0xB0                    | 130                        | 0xF0                    | 1200                       |
| 0x31                    | 8.8                        | 0x71                    | 39.0                       | 0xB1                    | 135                        | 0xF1                    | 1250                       |
| 0x32                    | 9.0                        | 0x72                    | 39.5                       | 0xB2                    | 140                        | 0xF2                    | 1300                       |
| 0x33                    | 9.2                        | 0x73                    | 40.0                       | 0xB3                    | 145                        | 0xF3                    | 1350                       |
| 0x34                    | 9.4                        | 0x74                    | 40.5                       | 0xB4                    | 150                        | 0xF4                    | 1400                       |
| 0x35                    | 9.6                        | 0x75                    | 41.0                       | 0xB5                    | 155                        | 0xF5                    | 1450                       |
| 0x36                    | 9.8                        | 0x76                    | 41.5                       | 0xB6                    | 160                        | 0xF6                    | 1500                       |
| 0x37                    | 10.0                       | 0x77                    | 42.0                       | 0xB7                    | 165                        | 0xF7                    | 1550                       |
| 0x38                    | 10.5                       | 0x78                    | 42.5                       | 0xB8                    | 170                        | 0xF8                    | 1600                       |
| 0x39                    | 11.0                       | 0x79                    | 43.0                       | 0xB9                    | 175                        | 0xF9                    | 1650                       |
| 0x3A                    | 11.5                       | 0x7A                    | 43.5                       | 0xBA                    | 180                        | 0xFA                    | 1700                       |
| 0x3B                    | 12.0                       | 0x7B                    | 44.0                       | 0xBB                    | 185                        | 0xFB                    | 1750                       |

Table 7-4. Motor BEMF constant Look-Up Table (continued)

| MOTOR_BEMF_CONST (HEX) | Kt <sub>PH_N</sub> (mV/Hz) | MOTOR_BEMF_CONST (HEX) | Kt <sub>PH_N</sub> (mV/Hz) | MOTOR_BEMF_CONST (HEX) | Kt <sub>PH_N</sub> (mV/Hz) | MOTOR_BEMF_CONST (HEX) | Kt <sub>PH_N</sub> (mV/Hz) |
|------------------------|----------------------------|------------------------|----------------------------|------------------------|----------------------------|------------------------|----------------------------|
| 0x3C                   | 12.5                       | 0x7C                   | 44.5                       | 0xBC                   | 190                        | 0xFC                   | 1800                       |
| 0x3D                   | 13.0                       | 0x7D                   | 45.0                       | 0xBD                   | 195                        | 0xFD                   | 1850                       |
| 0x3E                   | 13.5                       | 0x7E                   | 45.5                       | 0xBE                   | 200                        | 0xFE                   | 1900                       |
| 0x3F                   | 14.0                       | 0x7F                   | 46.0                       | 0xBF                   | 205                        | 0xFF                   | 2000                       |

### 7.3.13 Motor Parameter Extraction Tool (MPET)

The MCF8316C-Q1 uses motor winding resistance, motor winding inductance and Back-EMF constant to estimate motor position in closed loop operation. The MCF8316C-Q1 has capability of automatically measuring motor parameters in offline state, rather than having the user enter the values themselves. The MPET routine measures motor winding resistance, inductance, back EMF constant and mechanical load inertia and frictional coefficients. Offline measurement of parameters takes place before normal motor operation. TI recommends to estimate the motor parameters before motor startup to minimize the impact caused due to possible parameter variations.

Figure 7-40 shows the sequence of operation in the MPET routine. The MPET routine is entered when either the MPET\_CMD bit is set to 1b or a non-zero target speed is set. The MPET routine consists of four steps namely, IPD, Open Loop Acceleration, Current Ramp Down and Coasting. Each one of these steps are executed if the condition shown below the step evaluates to TRUE; if the condition evaluates to FALSE, the algorithm bypasses that particular step and moves on to the next step in the sequence. Once all the 4 steps are completed (or bypassed), the algorithm exits the MPET routine. If target speed is set to a non-zero value, the algorithm begins the start-up and acceleration sequence (to target speed reference) once MPET routine is exited.

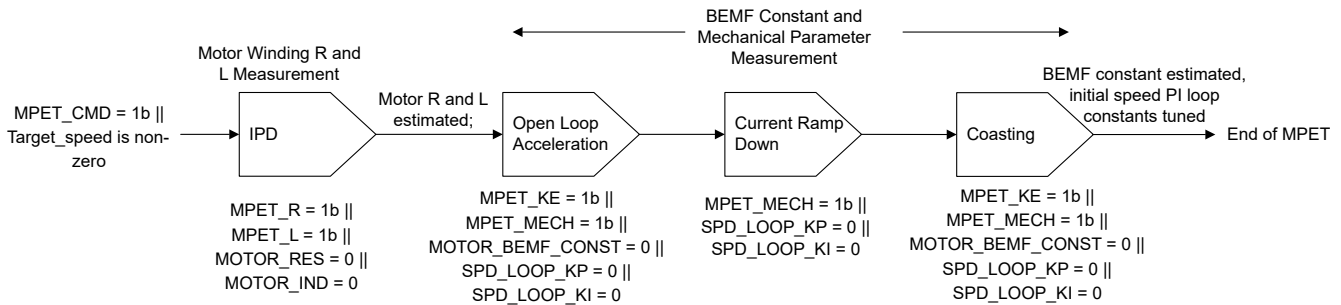


Figure 7-40. MPET Sequence

TI proprietary MPET routine includes following sequence of operation.

- **IPD:** The MPET routine starts with IPD, if the user enables motor winding resistance or inductance measurement by setting MPET\_R = 1b and MPET\_L = 1b or if the user defines MOTOR\_RES = 0 or MOTOR\_IND = 0. The IPD during MPET can be configured using MPET specific configuration parameters or using the normal motor operation IPD configuration parameters. The IPD configuration selection is done using MPET\_IPD\_SELECT. With MPET\_IPD\_SELECT = 1b, the IPD current limit is configured using MPET\_IPD\_CURRENT\_LIMIT and the IPD repeat number is configured using MPET\_IPD\_FREQ. With MPET\_IPD\_SELECT = 0b, the IPD current limit and the repeat number is configured using IPD\_CURR\_THR and IPD\_REPEAT. The IPD timer over flow or the IPD current decay time more than three times the current ramp up time can result in MPET\_IPD\_FAULT. TI recommends to run the MPET multiple times to observe for consistent resistance and inductance reading.

- **Open loop Acceleration:**

After IPD, the MPET routine run align and then open loop acceleration if the back-EMF constant or mechanical parameter measurement are enabled by setting MPET\_KE = 1b and MPET\_MECH = 1b. The MPET routine incorporates the sequences for mechanical parameter

measurement, if the speed loop PI constants are defined as zero, even if MPET\_MECH = 0b. User can configure MPET specific open loop configuration parameters or use normal motor operation open loop configuration parameters. The open loop configuration selection is done using MPET\_KE\_MEAS\_PARAMETER\_SELECT. With MPET\_KE\_MEAS\_PARAMETER\_SELECT = 1b, the speed slew rate is defined using MPET\_OPEN\_LOOP\_SLEW\_RATE, the open loop current reference is defined using MPET\_OPEN\_LOOP\_CURR\_REF and the open loop speed reference is defined using MPET\_OPEN\_LOOP\_SPEED\_REF. With MPET\_KE\_MEAS\_PARAMETER\_SELECT = 0b, the speed slew rate is defined using OL\_ACC\_A1 and OL\_ACC\_A2, 80% of I\_LIMIT for current reference and 50% of MAX\_SPEED for speed reference.

- **Current Ramp Down:** After open loop acceleration, if the mechanical parameter measurement is enabled, then the MPET routine optimizes the motor current to lower value sufficient to support the load. If mechanical parameter measurement is disabled (MPET\_MECH = 0b, or non-zero speed loop PI parameters) then the MPET will not have the current ramp down sequence.
- **Coasting:** MPET routine completes the sequence by allowing the motor to coast by enabling Hi-Z. The motor back EMF and indicative values of mechanical parameters are measured during the motor coasting period. If the motor back EMF is lower than the threshold defined in STAT\_DETECT\_THR, the MPET\_BEMF\_FAULT is generated.

### Selecting the parameters from EEPROM or MPET

The MPET estimated values are available in the MTR\_PARAMS Register. Setting the MPET\_WRITE\_SHADOW bit to 1, writes the MPET estimated values to the shadow registers and the user-configured (from EEPROM) values in MOTOR\_RES, MOTOR\_IND, MOTOR\_BEMF\_CONST, CURR\_LOOP\_KP, CURR\_LOOP\_KI, SPD\_LOOP\_KP and SPD\_LOOP\_KI shadow registers will be overwritten by the estimated values from MPET. If any of the shadow registers are initialized to zero (from EEPROM registers), the MPET estimated values are used for those registers independent of the MPET\_WRITE\_SHADOW setting. The MPET calculates the current loop KP and KI by using the measured resistance and inductance. The MPET does an estimation of the mechanical parameters including the inertia and frictional coefficient at the shaft (includes both motor and shaft coupled load). These values are used to set an initial values speed loop KP and KI. The estimated speed loop KP and KI setting can be used as an initial setting only and TI recommends to tune these parameters on application by the user based on the performance requirement.

#### 7.3.14 Anti-Voltage Surge (AVS)

When a motor is driven, energy is transferred from the power supply into the motor. Some of this energy is stored in the form of inductive and mechanical energy. If the speed command suddenly drops such that the BEMF voltage generated by the motor is greater than the voltage that is applied to the motor, then the mechanical energy of the motor is returned to the power supply and the  $V_M$  voltage surges. The AVS feature works to prevent this voltage surge on  $V_M$  and can be enabled by setting AVS\_EN to 1b. AVS can be disabled by setting AVS\_EN to 0b. When AVS is disabled, the deceleration rate is configured through CL\_DEC\_CONFIG.

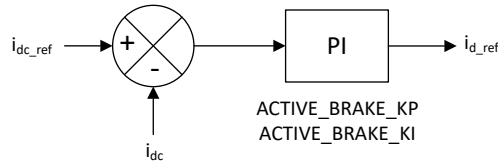
#### 7.3.15 Active Braking

Decelerating the motor quickly requires the motor mechanical energy to be extracted from the rotor in a fast and controlled manner. However, the supply voltage (VM) increases if the motor mechanical energy is returned to the power supply during the deceleration process. MCF8316C-Q1 is capable of decelerating the motor quickly without pumping energy back into the supply voltage by using a novel technique called active braking. ACTIVE\_BRAKE\_EN should be set to 1b to enable active braking and prevent DC bus voltage (VM) spike during fast motor deceleration. Active braking can also be used during reverse drive (see [Reverse Drive](#)) or motor stop (see [Active Spin-Down](#)) to reduce the motor speed quickly without DC bus voltage (VM) spike.

The maximum limit on the current sourced from the DC bus ( $i_{dc\_ref}$ ) during active braking can be configured using ACTIVE\_BRAKE\_CURRENT\_LIMIT. The D-axis current reference ( $i_{d\_ref}$ ) is generated from the error between DC bus current limit ( $i_{dc\_ref}$ ) and the estimated DC bus current ( $i_{dc}$ ) using a PI controller as shown in [Figure 7-41](#). The gain constants of PI controller can be configured using ACTIVE\_BRAKE\_KP and ACTIVE\_BRAKE\_KI. During active braking, the DC bus current limit ( $i_{dc\_ref}$ ) starts



from zero and linearly increases to ACTIVE\_BRAKE\_CURRENT\_LIMIT with current slew rate as defined by ACTIVE\_BRAKE\_BUS\_CURRENT\_SLEW\_RATE.



**Figure 7-41. Active Braking Current Control Loop for  $i_{d\_ref}$**

ACTIVE\_BRAKE\_SPEED\_DELTA\_LIMIT\_ENTRY sets the minimum difference between the initial and target speed above which active braking will be entered. For example, consider ACTIVE\_BRAKE\_SPEED\_DELTA\_LIMIT\_ENTRY is set to 10%; if the initial speed is 100% and target speed is set to 95%, MCF8316C-Q1 uses AVS instead of active braking to reach 95% speed since the difference in commanded speed change (5%) is less than ACTIVE\_BRAKE\_SPEED\_DELTA\_LIMIT\_ENTRY (10%).

ACTIVE\_BRAKE\_SPEED\_DELTA\_LIMIT\_EXIT sets the difference between the current and target speed below which active braking will be exited. For example, consider ACTIVE\_BRAKE\_SPEED\_DELTA\_LIMIT\_EXIT is set to 5%; if the initial motor speed is 100% and target speed is set to 10%, MCF8316C-Q1 uses active braking to reduce the motor speed to 15%; upon reaching 15% speed, MCF8316C-Q1 exits active braking and uses AVS to decelerate the motor speed to 10%.

ACTIVE\_BRAKE\_MOD\_INDEX\_LIMIT sets the modulation index below which active braking will be used. For example, consider ACTIVE\_BRAKE\_MOD\_INDEX\_LIMIT is set to 50%, ACTIVE\_BRAKE\_SPEED\_DELTA\_LIMIT\_ENTRY is set to 5%, ACTIVE\_BRAKE\_SPEED\_DELTA\_LIMIT\_EXIT is set to 2.5%. If the initial motor speed is at 70% (corresponding modulation index is 90%) and target speed is 40% (corresponding modulation index is 60%), MCF8316C-Q1 uses AVS to decelerate the motor till target speed of 40% since the modulation index (60%) corresponding to final speed is higher than ACTIVE\_BRAKE\_MOD\_INDEX\_LIMIT of 50%. In the same case, if final speed command is 10% (corresponding modulation index is 30%), MCF8316C-Q1 uses AVS till 30% speed (corresponding modulation index is 50%), switches to active braking from 30% to 15% speed (final speed of 10% + ACTIVE\_BRAKE\_SPEED\_DELTA\_LIMIT\_EXIT of 5%) and uses AVS again from 15% to 10% speed to complete the active braking. TI recommends starting active braking tuning with ACTIVE\_BRAKE\_MOD\_INDEX\_LIMIT set to 100%; if there is a DC bus voltage (VM) spike observed during active braking, reduce ACTIVE\_BRAKE\_MOD\_INDEX\_LIMIT in steps so as to eliminate this voltage spike. If ACTIVE\_BRAKE\_MOD\_INDEX\_LIMIT is set to 0%, MCF8316C-Q1 decelerates in AVS (even when ACTIVE\_BRAKE\_EN is set to 1b) in the forward direction; in reverse direction (during direction change), ACTIVE\_BRAKE\_MOD\_INDEX\_LIMIT is not applicable and therefore MCF8316C-Q1 decelerates in active braking.

#### Note

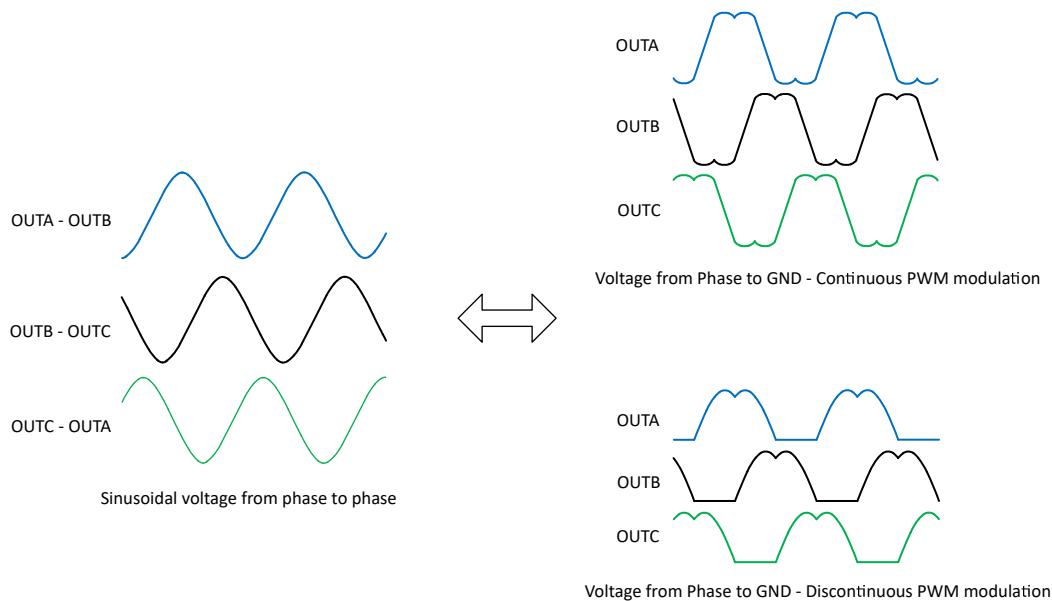
1. ACTIVE\_BRAKE\_SPEED\_DELTA\_LIMIT\_ENTRY, ACTIVE\_BRAKE\_SPEED\_DELTA\_LIMIT\_EXIT and ACTIVE\_BRAKE\_MOD\_INDEX\_LIMIT are applicable only during deceleration in forward direction and not used during direction change.
2. ACTIVE\_BRAKE\_SPEED\_DELTA\_LIMIT\_ENTRY should be set higher than ACTIVE\_BRAKE\_SPEED\_DELTA\_LIMIT\_EXIT for active braking operation.
3. During active (or closed loop) braking,  $i_{q\_ref}$  is clamped to -ILIMIT. This ( $i_{q\_ref}$  being clamped to -ILIMIT) may result in the speed PI loop getting saturated and SPEED\_LOOP\_SATURATION bit getting set to 1b during deceleration. This bit is automatically set to 0b once the deceleration is completed and the speed PI loop is out of saturation. Hence, speed loop saturation fault should be ignored during deceleration.
4. Active braking is not available in torque mode.

### 7.3.16 Output PWM Switching Frequency

MCF8316C-Q1 provides the option to configure the output PWM switching frequency of the MOSFETs through PWM\_FREQ\_OUT. PWM\_FREQ\_OUT has range of 10-60 kHz. In order to select optimal output PWM switching frequency, user has to make tradeoff between the current ripple and the switching losses. Generally, motors having lower L/R ratio require higher PWM switching frequency to reduce current ripple.

### 7.3.17 PWM Modulation Schemes

The MCF8316C-Q1 supports two different modulation schemes, namely, continuous and discontinuous space vector PWM modulation schemes. In continuous PWM modulation, all the three phases switch all the time as per the defined switching frequency. In discontinuous PWM modulation, one of the phases is clamped to ground for 120° electrical period, and the other two phases are pulse width modulated. The modulation scheme is configured using PWM\_MODE. Figure 7-42 shows the modulated average phase voltages for different modulation schemes.



**Figure 7-42. Continuous and Discontinuous PWM Modulation Phase Voltages**

Continuous modulation helps in reducing current ripple for motors having low inductance but it results in higher switching losses because all three phases are switching. Discontinuous modulation has lower switching losses due to only two phases switching at a time, but higher current ripple.

### 7.3.18 Dead Time Compensation

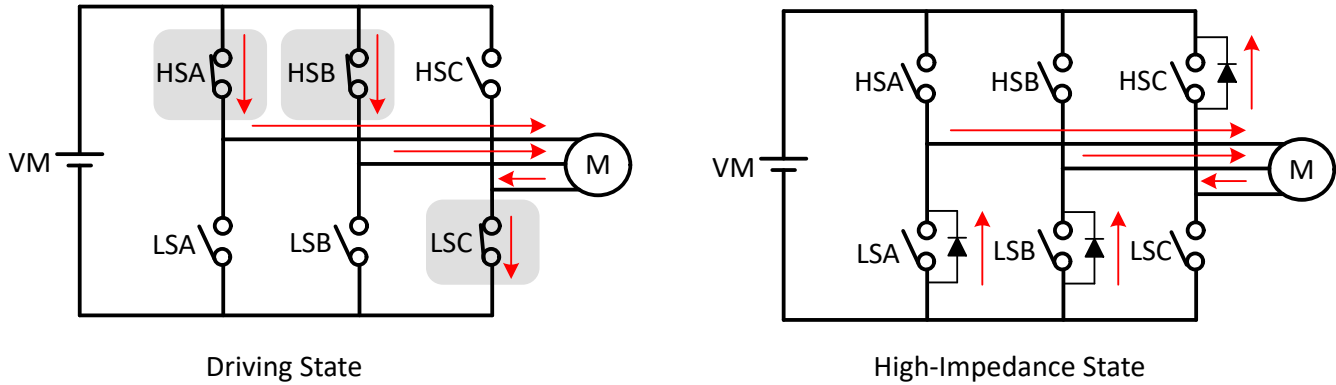
Dead time is inserted between the switching instants of high-side and low-side MOSFETs in a half-bridge leg to avoid shoot-through condition. Due to dead time insertion, the expected voltage and applied voltage at the phase node differ based on the phase current direction. The phase node voltage distortion introduces undesired distortion in the phase current causing audible noise. MCF8316C-Q1 integrates a proprietary dead time compensation technique to remove this phase current distortion and greatly reduce the audible noise, thereby significantly improving the acoustic performance of the FOC in MCF8316C-Q1. This dead time compensation can be enabled or disabled by configuring DEADTIME\_COMP\_EN. Even when DEADTIME\_COMP\_EN is set to 1b (compensation enabled), dead time compensation is disabled when motor electrical frequency exceeds 135-Hz and re-enabled when motor electrical frequency drops below 127-Hz.

### 7.3.19 Motor Stop Options

The MCF8316C-Q1 provides different options for stopping the motor which can be configured by MTR\_STOP.

### 7.3.19.1 Coast (Hi-Z) Mode

Coast (Hi-Z) mode is configured by setting MTR\_STOP to 000b. When motor stop command is received, the MCF8316C-Q1 will transition into a high impedance (Hi-Z) state by turning off all MOSFETs. When the MCF8316C-Q1 transitions from driving the motor into a Hi-Z state, the inductive current in the motor windings continues to flow and the energy returns to the power supply through the body diodes in the MOSFET output stage (see example Figure 7-43).

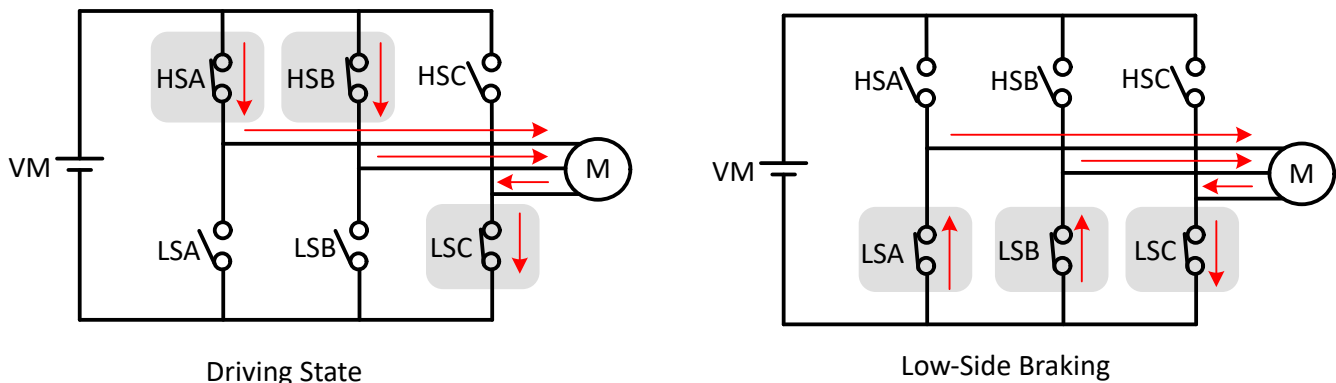


**Figure 7-43. Coast (Hi-Z) Mode**

In this example, current is applied to the motor through the high-side phase-A MOSFET (HSA), high-side phase-B MOSFET (HSB) and returned through the low-side phase-C MOSFET (LSC). When motor stop command is received all 6 MOSFETs transition to Hi-Z state and the inductive energy returns to supply through body diodes of MOSFETs LSA, LSB and HSC.

### 7.3.19.2 Low-Side Braking

Low-side braking mode is configured by setting MTR\_STOP to 010b. When a motor stop command is received, the output speed is reduced to a value defined by BRAKE\_SPEED\_THRESHOLD prior to turning all low-side MOSFETs ON (see example Figure 7-44) for a time configured by MTR\_STOP\_BRK\_TIME. If the motor speed is below BRAKE\_SPEED\_THRESHOLD prior to receiving stop command, then the MCF8316C-Q1 transitions directly into the brake state. After applying the brake for MTR\_STOP\_BRK\_TIME, the MCF8316C-Q1 transitions into the Hi-Z state by turning OFF all MOSFETs.



**Figure 7-44. Low-Side Braking**

The MCF8316C-Q1 can also enter low-side braking through BRAKE pin input. When BRAKE pin is pulled to HIGH state, the output speed is reduced to a value defined by BRAKE\_SPEED\_THRESHOLD prior to turning all low-side MOSFETs ON. In this case, MCF8316C-Q1 stays in low-side brake state till BRAKE pin changes to LOW state.

### 7.3.19.3 High-Side Braking

High-side braking mode is configured by setting MTR\_STOP to 011b. When a motor stop command is received, the output speed is reduced to a value defined by BRAKE\_SPEED\_THRESHOLD prior to turning all high-side MOSFETs ON (see example Figure 7-45) for a time configured by MTR\_STOP\_BRK\_TIME. If the motor speed is below BRAKE\_SPEED\_THRESHOLD prior to receiving stop command, then the MCF8316C-Q1 transitions directly into the brake state. After applying the brake for MTR\_STOP\_BRK\_TIME, the MCF8316C-Q1 transitions into Hi-Z state by turning OFF all MOSFETs.

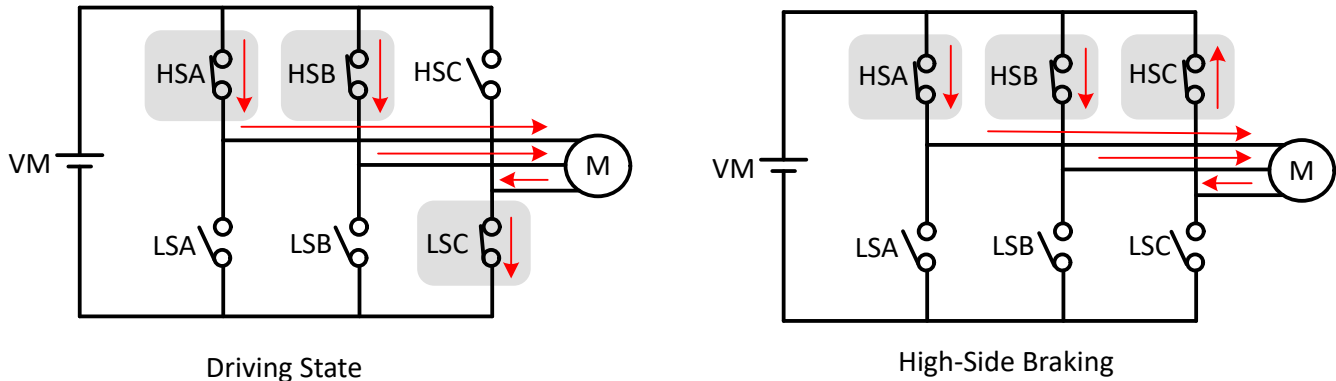


Figure 7-45. High-Side Braking

### 7.3.19.4 Active Spin-Down

Active spin down mode is configured by setting MTR\_STOP to 100b. When a motor stop command is received, the MCF8316C-Q1 reduces SPEED\_REF to ACT\_SPIN\_THR and then transitions to Hi-Z state by turning all MOSFETs OFF. The advantage of this mode is that by reducing SPEED\_REF, the motor is decelerated to lower speed thereby reducing the phase currents before entering Hi-Z. Now, when the motor transitions into Hi-Z state, the energy transfer to the power supply is reduced. The threshold ACT\_SPIN\_THR needs to be configured high enough for MCF8316C-Q1 to not lose synchronization with the motor.

### 7.3.19.5 Align Braking

Align braking based stop mode is configured by setting MTR\_STOP to 101b. In this mode, on receiving the motor stop command, MCF8316C-Q1 reduces the motor speed to a value defined by BRAKE\_SPEED\_THRESHOLD before bringing the motor to align stop by injecting a DC current through a particular phase pattern for a time configured by MTR\_STOP\_BRK\_TIME. The phase pattern during align stop is generated based on the angle at which align needs to be performed and this angle can be configured through ALIGN\_ANGLE or the last commutation angle. ALIGN\_BRAKE\_ANGLE\_SEL can be configured to decide which align angle is to be used by MCF8316C-Q1. The current limit threshold during align braking is configured through ALIGN\_OR\_SLOW\_CURRENT\_ILIMIT.

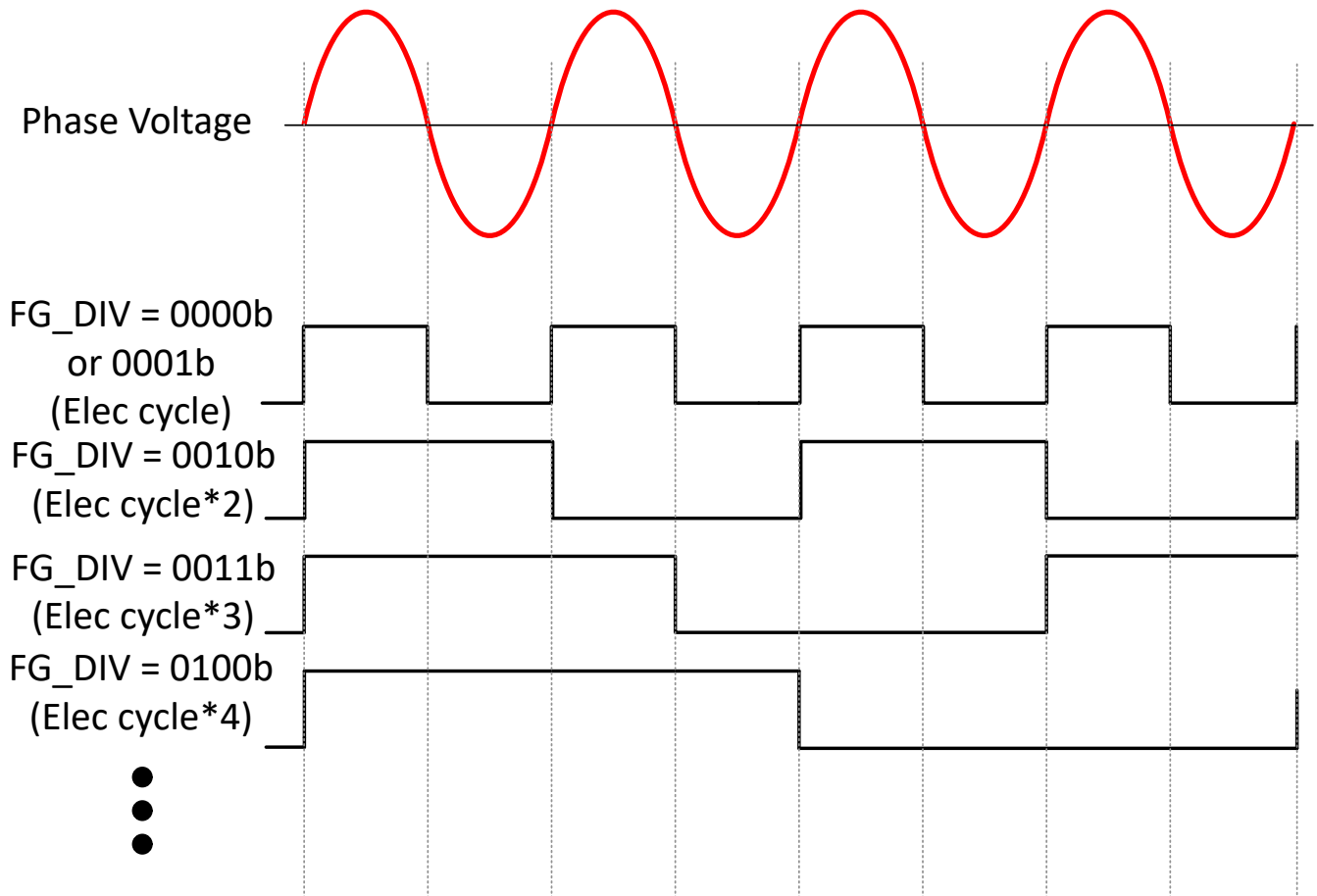
## 7.3.20 FG Configuration

The MCF8316C-Q1 provides information about the motor speed through the Frequency Generate (FG) pin. In MCF8316C-Q1, the FG pin output is configured through FG\_CONFIG. When FG\_CONFIG is configured to 0b, the FG output is active as long as the MCF8316C-Q1 is driving the motor. When FG\_CONFIG is configured to 1b, the MCF8316C-Q1 provides an FG output until the motor back-EMF falls below FG\_BEMF\_THR.

### 7.3.20.1 FG Output Frequency

The FG output frequency can be configured by FG\_DIV. Many applications require the FG output to provide a pulse for every mechanical rotation of the motor. Different FG\_DIV configurations can accomplish this for 2-pole up to 30-pole motors.

Figure 7-46 shows the FG output when MCF8316C-Q1 has been configured to provide FG pulses once every electrical cycle (2 poles), once every two electrical cycle (4 poles), once every three electrical cycles (6 poles), once every four electrical cycles (8 poles), and so on.



**Figure 7-46. FG Frequency Divider**

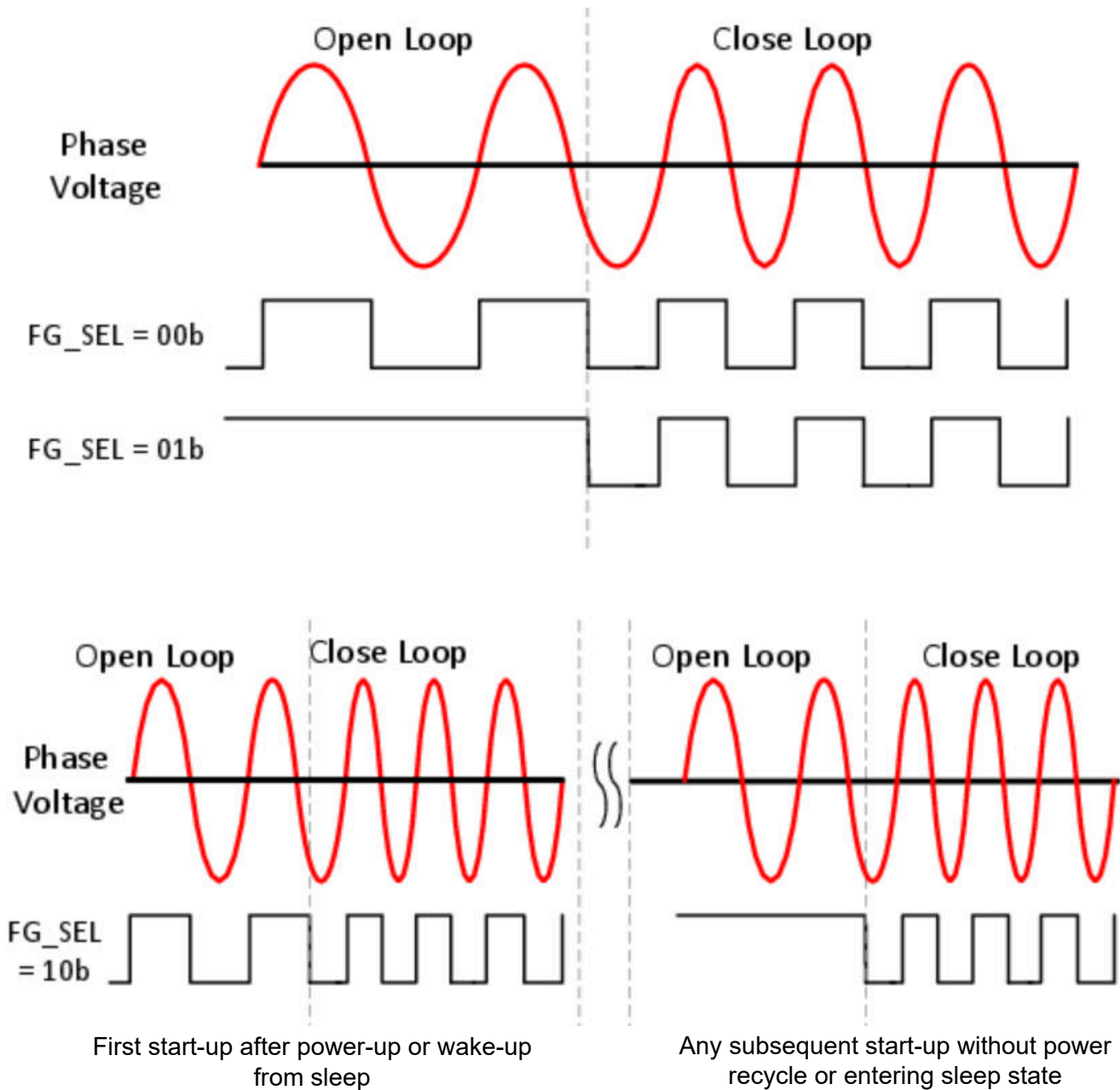
### 7.3.20.2 FG during Open and Closed Loop States

During closed loop operation, the driving speed (FG output frequency) and the actual motor speed are synchronized. During open-loop operation, however, FG may not reflect the actual motor speed.

The MCF8316C-Q1 provides three options for controlling the FG output during open loop, as shown in [Figure 7-47](#). The selection of these options is configured through FG\_SEL.

If FG\_SEL is set to,

- 00b: When in open loop, the FG output is based on the driving frequency.
- 01b: When in open loop, the FG output will be driven high.
- 10b: The FG output will reflect the driving frequency during open loop operation in the first motor start-up cycle after power-on, sleep/standby; FG will be held high during open loop operation in subsequent start-up cycles.



**Figure 7-47. FG Behavior During Open Loop**

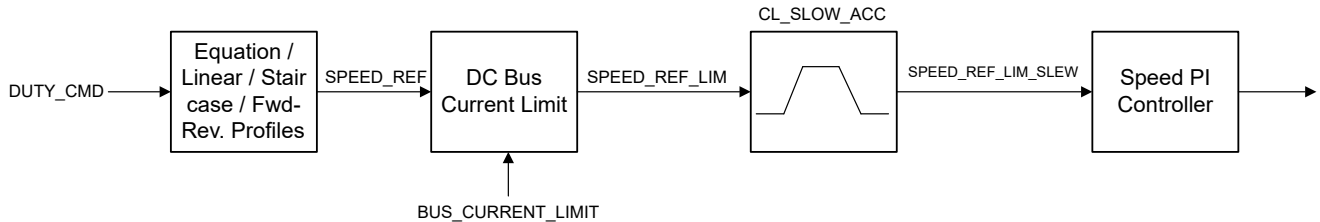
### 7.3.20.3 FG during Fault and Idle States

MCF8316C-Q1 provides the option of configuring FG output during fault and idle (motor stopped due to zero speed command) states. FG output during fault state is configured by FG\_FAULT\_CONFIG and FG output during idle state is configured by FG\_IDLE\_CONFIG - FG can be configured as a low or high signal during fault and can also be configured as a low or high signal during idle state. This allows the use of FG signal to uniquely determine the motor operating condition (fault, idle, spinning). For example, FG output during fault can be configured as a low signal and FG output during idle state can be configured as a high signal and FG during motor spinning can be configured to be at mechanical speed - a low FG output indicates MCF8316C-Q1 encountered a fault condition, a high FG output indicates motor is in idle state and a FG signal at 50% duty indicates motor spinning at a speed equal to FG frequency.

### 7.3.21 DC Bus Current Limit

The DC bus current limit feature can be used to limit the current supplied by the DC input source (VM). This feature can be enabled by setting `BUS_CURRENT_LIMIT_ENABLE` to 1b. The DC bus current limit can be configured using `BUS_CURRENT_LIMIT`. This feature limits the DC bus current by limiting the speed (`SPEED_REF_LIM`)/current (`CURRENT_REF_LIM`) reference as shown in Figure 7-48. Enabling this feature may restrict the speed/phase current of the motor from reaching the set point (`SPEED_REF` or `CURRENT_REF`) in order to limit the DC bus current. The DC bus current limit status is reported on `BUS_CURRENT_LIMIT_STATUS`.

#### Speed Control Mode



#### Current Control Mode

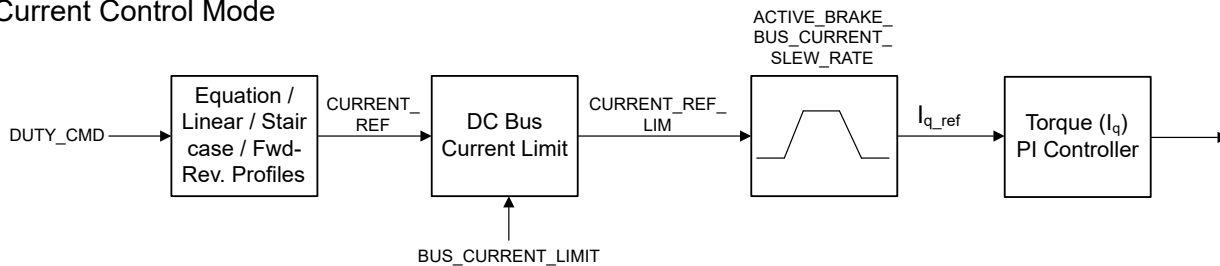


Figure 7-48. DC Bus Current Limit

#### Note

1. DC bus current limit feature is not available when active braking is enabled.
2. MCF8316C-Q1 implements a 5% hysteresis around `BUS_CURRENT_LIMIT` to avoid chattering around this set-point.

### 7.3.22 Protections

The MCF8316C-Q1 is protected from a host of fault events including motor lock, VM undervoltage, AVDD undervoltage, buck undervoltage, charge pump undervoltage, overtemperature and overcurrent events. Table 7-5 summarizes the response, recovery modes, power stage status, reporting mechanism for different faults.

### Note

1. Actionable faults (latched or retry) are always reported on nFAULT pin (as logic low).
2. Actionable faults (latched or retry) are reported on ALARM pin (as logic high) when ALARM\_PIN\_EN is set to 1b.
3. Report only faults are reported on nFAULT (as logic low) only when ALARM\_PIN\_EN is set to 0b. When ALARM\_PIN\_EN is set to 1b, report only faults are reported only on ALARM pin (as logic high) while nFAULT stays high (external or internal pull-up).
4. Priority order for multi-fault scenarios is latched > slower retry time fault > faster retry time fault > report only fault. For example, if a latched and retry fault happen simultaneously, the device stays latched in fault mode until user issues clear fault command by writing 1b to CLR\_FLT. If two retry faults with different retry times happen simultaneously, the device retries only after the longer (slower) retry time lapses.
5. Recovery refers only to state of FETs (Hi-Z or active) after the fault condition is removed. Automatic indicates that the device automatically recovers (and FETs are active) when retry time lapses after the fault condition is removed. Latched indicates that the device waits for clearing of fault condition (by writing 1b to CLR\_FLT bit) to make the FETs active again.
6. Actionable (latched or retry) faults can take up to 200-ms after fault response (FETs in Hi-Z) to be reported on nFAULT pin (as logic low), ALARM pin (as logic high) and fault status registers.
7. Latched faults can take up to 200-ms after CLR\_FLT command is issued (over I<sup>2</sup>C) to be cleared.

**Table 7-5. Fault Action and Response**

| FAULT                                  | CONDITION                           | CONFIGURATION  | REPORT                                       | FETs        | DIGITAL         | RECOVERY   |
|--|-------------------------------------|----------------|--|-------------|-----------------|--|
| VM undervoltage                        | $V_{VM} < V_{UVLO}$ (falling)       | —              | —  | Hi-Z        | Disabled        | Automatic:<br>$V_{VM} > V_{UVLO}$ (rising)       |
| AVDD undervoltage                      | $V_{AVDD} < V_{AVDD\_UV}$ (falling) | —              | —  | Hi-Z        | Disabled        | Automatic:<br>$V_{AVDD} > V_{AVDD\_UV}$ (rising) |
| Buck undervoltage (BUCK_UV)            | $V_{FB\_BK} < V_{BK\_UV}$ (falling) | —              | —  | Active/Hi-Z | Active/Disabled | Automatic:<br>$V_{FB\_BK} > V_{BK\_UV}$ (rising) |
| Charge pump undervoltage (VCP_UV)      | $V_{CP} < V_{CPIUV}$ (falling)      | —              | nFAULT and GATE_DRIVER_FAULT_STATUS register | Hi-Z        | Active          | Automatic:<br>$V_{VCP} > V_{CPIUV}$ (rising)     |
| Over Voltage Protection (OVP)          | $V_{VM} > V_{OVP}$ (rising)         | OVP_EN = 0b    | None   | Active      | Active          | No action  |
|  |                                     | OVP_EN = 1b    | nFAULT and GATE_DRIVER_FAULT_STATUS register | Hi-Z        | Active          | Automatic:<br>$V_{VM} < V_{OVP}$ (falling)       |
| Over Current Protection (OCP)          | $I_{PHASE} > I_{OCP}$               | OCP_MODE = 00b | nFAULT and GATE_DRIVER_FAULT_STATUS register | Hi-Z        | Active          | Latched:<br>CLR_FLT                              |
|  |                                     | OCP_MODE = 01b | nFAULT and GATE_DRIVER_FAULT_STATUS register | Hi-Z        | Active          | Retry:<br>I <sub>RETRY</sub>                     |
| Buck Overcurrent Protection (BUCK_OCP) | $I_{BK} > I_{BK\_OCP}$              | —              | —  | Hi-Z        | Disabled        | Automatic  |



**Table 7-5. Fault Action and Response (continued)**

| FAULT  | CONDITION  | CONFIGURATION                        | REPORT                                      | FETs            | DIGITAL | RECOVERY                   |
|--|--|--------------------------------------|---|-----------------|---------|----------------------------|
| Motor Lock<br>(MTR_LCK )                                 | Motor lock: Abnormal Speed; No Motor Lock; Abnormal BEMF | MTR_LCK_MODE = 0000b or 0001b        | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active  | Latched:<br>CLR_FLT        |
|  |  | MTR_LCK_MODE = 0010b                 | nFAULT and CONTROLLER_FAULT_STATUS register | High side brake | Active  | Latched:<br>CLR_FLT        |
|  |  | MTR_LCK_MODE = 0011b                 | nFAULT and CONTROLLER_FAULT_STATUS register | Low side brake  | Active  | Latched:<br>CLR_FLT        |
|  |  | MTR_LCK_MODE = 0100b or 0101b        | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active  | Retry:<br>$t_{LCK\_RETRY}$ |
|  |  | MTR_LCK_MODE = 0110b                 | nFAULT and CONTROLLER_FAULT_STATUS register | High side brake | Active  | Retry:<br>$t_{LCK\_RETRY}$ |
|  |  | MTR_LCK_MODE = 0111b                 | nFAULT and CONTROLLER_FAULT_STATUS register | Low side brake  | Active  | Retry:<br>$t_{LCK\_RETRY}$ |
|  |  | MTR_LCK_MODE = 1000b                 | nFAULT and CONTROLLER_FAULT_STATUS register | Active          | Active  | No action                  |
|  |  | MTR_LCK_MODE = 1xx1b                 | None  | Active          | Active  | No action                  |
| Hardware Lock-Detection Current Limit<br>(HW_LOCK_LIMIT) | $V_{SOX} > HW\_LOCK\_ILIMIT$                             | HW_LOCK_ILIMIT_MODE = 0000b or 0001b | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active  | Latched:<br>CLR_FLT        |
|  |  | HW_LOCK_ILIMIT_MODE = 0010b          | nFAULT and CONTROLLER_FAULT_STATUS register | High-side brake | Active  | Latched:<br>CLR_FLT        |
|  |  | HW_LOCK_ILIMIT_MODE = 0011b          | nFAULT and CONTROLLER_FAULT_STATUS register | Low-side brake  | Active  | Latched:<br>CLR_FLT        |
|  |  | HW_LOCK_ILIMIT_MODE = 0100b or 0101b | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active  | Retry:<br>$t_{LCK\_RETRY}$ |
|  |  | HW_LOCK_ILIMIT_MODE = 0110b          | nFAULT and CONTROLLER_FAULT_STATUS register | High-side brake | Active  | Retry:<br>$t_{LCK\_RETRY}$ |
|  |  | HW_LOCK_ILIMIT_MODE = 0111b          | nFAULT and CONTROLLER_FAULT_STATUS register | Low-side brake  | Active  | Retry:<br>$t_{LCK\_RETRY}$ |
|  |  | HW_LOCK_ILIMIT_MODE = 1000b          | nFAULT and CONTROLLER_FAULT_STATUS register | Active          | Active  | No action                  |
|  |  | HW_LOCK_ILIMIT_MODE = 1xx1b          | None  | Active          | Active  | No action                  |

**Table 7-5. Fault Action and Response (continued)**

| FAULT   | CONDITION   | CONFIGURATION                     | REPORT                                      | FETs            | DIGITAL | RECOVERY                                       |
|---|---|-----------------------------------|---|-----------------|---------|--|
| Software Lock-Detection Current Limit (LOCK_ILIMIT) | $V_{SOX} > LOCK\_ILIMIT$  | LOCK_ILIMIT_MODE = 0000b or 0001b | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active  | Latched: CLR_FLT                               |
|   |   | LOCK_ILIMIT_MODE = 0010b          | nFAULT and CONTROLLER_FAULT_STATUS register | High-side brake | Active  | Latched: CLR_FLT                               |
|   |   | LOCK_ILIMIT_MODE = 0011b          | nFAULT and CONTROLLER_FAULT_STATUS register | Low-side brake  | Active  | Latched: CLR_FLT                               |
|   |   | LOCK_ILIMIT_MODE = 0100b or 0101b | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active  | Retry: $t_{LCK\_RETRY}$                        |
|   |   | LOCK_ILIMIT_MODE = 0110b          | nFAULT and CONTROLLER_FAULT_STATUS register | High-side brake | Active  | Retry: $t_{LCK\_RETRY}$                        |
|   |   | LOCK_ILIMIT_MODE = 0111b          | nFAULT and CONTROLLER_FAULT_STATUS register | Low-side brake  | Active  | Retry: $t_{LCK\_RETRY}$                        |
|   |   | LOCK_ILIMIT_MODE = 1000b          | nFAULT and CONTROLLER_FAULT_STATUS register | Active          | Active  | No action                                      |
|   |   | LOCK_ILIMIT_MODE = 1xx1b          | None  | Active          | Active  | No action                                      |
| IPD Timeout Fault (IPD_T1_FAULT and IPD_T2_FAULT)   | IPD TIME > 500ms (approx.), during IPD current ramp up or ramp down   | IPD_TIMEOUT_FAULT_EN = 0b         | —   | Active          | Active  | No action                                      |
|   |   | IPD_TIMEOUT_FAULT_EN = 1b         | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active  | Retry: $t_{LCK\_RETRY}$                        |
| IPD Frequency Fault (IPD_FREQ_FAULT)                | IPD pulse before the current decay in previous IPD pulse  | IPD_FREQ_FAULT_EN = 0b            | —   | Active          | Active  | No action                                      |
|   |   | IPD_FREQ_FAULT_EN = 1b            | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active  | Retry: $t_{LCK\_RETRY}$                        |
| MPET IPD Fault (MPET_IPD_FAULT)                     | Same as IPD Timeout Fault during MPET R, L measurement  | —                                 | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active  | Latched: CLR_FLT                               |
| MPET Back-EMF Fault (MPET_BEMF_FAULT)               | Motor Back EMF < STAT_DETECT_THR during MPET Ke and mechanical parameters measurement                                     | —                                 | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active  | Latched: CLR_FLT                               |
| Maximum VM (overvoltage) fault                      | $V_{VM} > MAX\_VM\_MOTOR$ , if $MAX\_VM\_MOTOR \neq 000b$   | MAX_VM_MODE = 0b                  | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active  | Latched: CLR_FLT                               |
|   |   | MAX_VM_MODE = 1b                  | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active  | Automatic: $(V_{VM} < MAX\_VM\_MOTOR - 1)-V$   |
| Minimum VM (undervoltage) fault                     | $V_{VM} < MIN\_VM\_MOTOR$ , if $MIN\_VM\_MOTOR \neq 000b$   | MIN_VM_MODE = 0b                  | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active  | Latched: CLR_FLT                               |
|   |   | MIN_VM_MODE = 1b                  | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active  | Automatic: $(V_{VM} > MIN\_VM\_MOTOR + 0.5)-V$ |
| External Watchdog                                   | Watchdog tickle does not arrive before configured time interval when EXT_WDT_EN = 1b. Refer <a href="#">Section 7.5.5</a> | EXT_WDT_FAULT_MODE = 0b           | nFAULT and CONTROLLER_FAULT_STATUS register | Active          | Active  | No action                                      |
|   |   | EXT_WDT_FAULT_MODE = 1b           | nFAULT and CONTROLLER_FAULT_STATUS register | Hi-Z            | Active  | Latched: CLR_FLT                               |

**Table 7-5. Fault Action and Response (continued)**

| FAULT                          | CONDITION  | CONFIGURATION                 | REPORT                                       | FETs   | DIGITAL | RECOVERY   |
|--------------------------------|--|-------------------------------|--|--|---------|--|
| Bus Current Limit              | $I_{VM} > \text{BUS\_CURRENT\_LIMIT}$ .<br>Refer <a href="#">Section 7.3.21</a>        | BUS_CURRENT_LIMIT_ENABLE = 1b | nFAULT and CONTROLLER_FAULT_STATUS register  | Active; motor speed will be restricted to limit DC bus current | Active  | Automatic: Speed restriction is removed when $I_{VM} < \text{BUS\_CURRENT\_LIMIT}$ |
| Current Loop Saturation        | Indication of current loop saturation due to lower $V_{VM}$                            | SATURATION_FLAGS_EN = 1b      | nFAULT and CONTROLLER_FAULT_STATUS register  | Active; motor speed may not reach speed reference              | Active  | Automatic: motor will reach reference operating point upon exiting saturation      |
| Speed Loop Saturation          | Indication of speed loop saturation due to lower $V_{VM}$ , lower ILIMIT setting etc., | SATURATION_FLAGS_EN = 1b      | nFAULT and CONTROLLER_FAULT_STATUS register  | Active; motor speed may not reach speed reference              | Active  | Automatic: motor will reach reference operating point upon exiting saturation      |
| Thermal warning (OTW)          | $T_J > T_{OTW}$  | OTW_REP = 0b                  | —  | Active   | Active  | No action  |
|                                |  | OTW_REP = 1b                  | nFAULT and GATE_DRIVER_FAULT_STATUS register | Active   | Active  | No action  |
| FET thermal shutdown (TSD_FET) | $T_J > T_{TSD\_FET}$   | —                             | nFAULT and GATE_DRIVER_FAULT_STATUS register | Hi-Z   | Active  | Automatic:<br>$T_J < T_{TSD\_FET} - T_{TSD\_FET\_HYS}$                             |

### 7.3.22.1 VM Supply Undervoltage Lockout

If at any time the input supply voltage on the VM pin falls lower than the  $V_{UVLO}$  threshold (VM UVLO falling threshold), all the integrated FETs, driver charge-pump and digital logic are disabled as shown in Figure 7-49. MCF8316C-Q1 goes into reset state whenever VM UVLO event occurs.

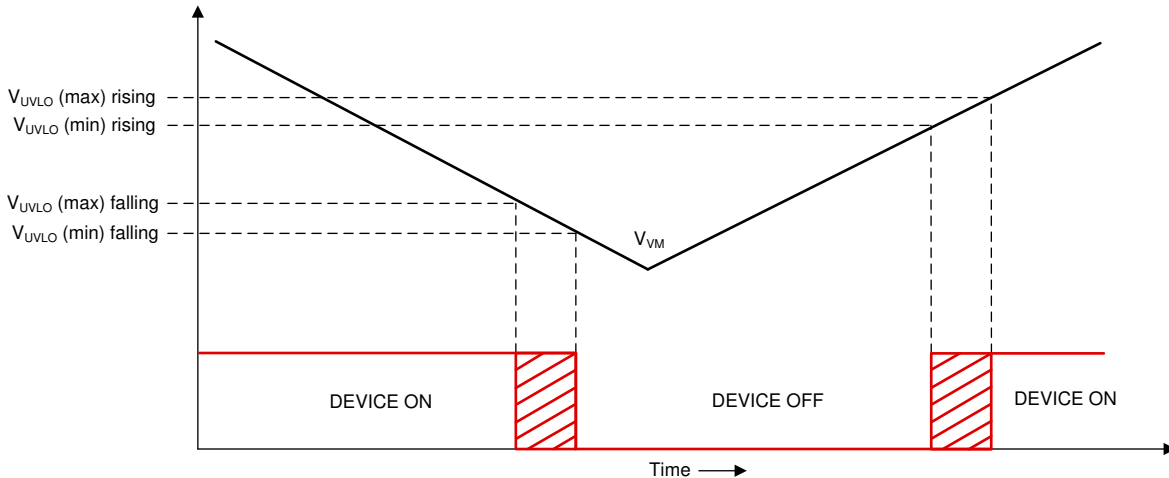


Figure 7-49. VM Supply Undervoltage Lockout

### 7.3.22.2 AVDD Undervoltage Lockout (AVDD\_UV)

If at any time the voltage on the AVDD pin falls lower than the  $V_{AVDD\_UV}$  threshold, all the integrated FETs, driver charge-pump and digital logic controller are disabled. Since internal circuitry in MCF8316C-Q1 is powered through the AVDD regulator, MCF8316C-Q1 goes into reset state whenever AVDD UV event occurs.

### 7.3.22.3 BUCK Under Voltage Lockout (BUCK\_UV)

If at any time the voltage on the FB\_BK pin falls lower than the  $V_{BK\_UVLO}$  threshold, a buck UV fault is recognized - MCF8316C-Q1 continues to attempt regulating the FB\_BK voltage to set value. Since internal circuitry in MCF8316C-Q1 is powered through the buck regulator, MCF8316C-Q1 may go into reset state if FB\_BK voltage drops low enough to trigger UV on the internal circuits.

### 7.3.22.4 VCP Charge Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls lower than the  $V_{CPUV}$  threshold, all the integrated FETs are disabled and the nFAULT pin is driven low. The DRIVER\_FAULT and VCP\_UV bits are set to 1b in the status registers. Normal operation resumes (driver operation and the nFAULT pin is released) when the VCP undervoltage condition clears. The VCP\_UV bit stays set until cleared through the CLR\_FLT bit.

### 7.3.22.5 Overvoltage Protection (OVP)

If at any time input supply voltage on the VM pins rises higher than  $V_{OVP}$ , all the integrated FETs are disabled and the nFAULT pin is driven low. The DRIVER\_FAULT and OVP bits are set to 1b in the status registers. Normal operation resumes (driver operation and the nFAULT pin is released) when the OVP condition clears. The OVP bit stays set until cleared through the CLR\_FLT bit. Setting the OVP\_EN to 0b disables this protection feature.

The OVP threshold can be set to 22-V or 34-V based on the OVP\_SEL bit.

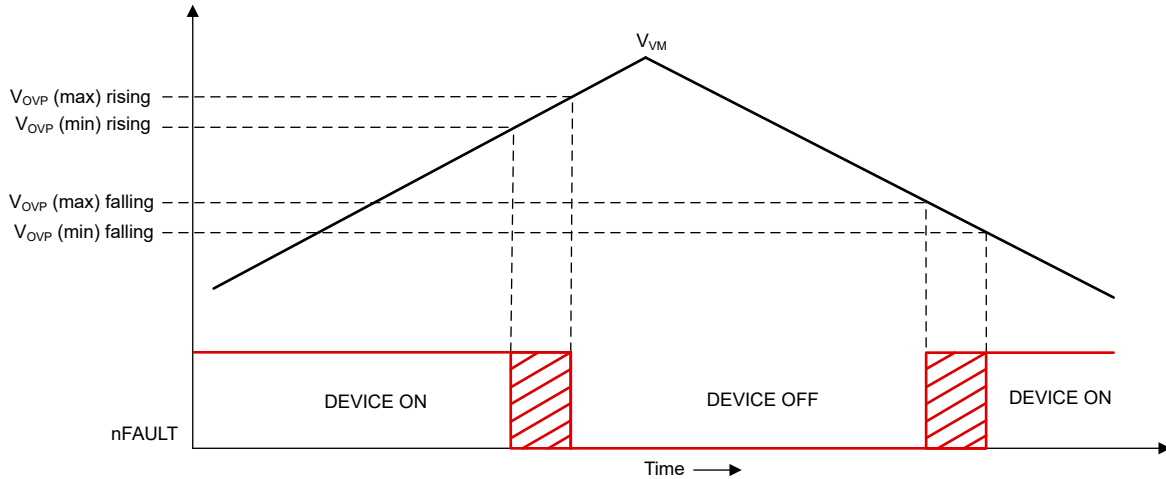


Figure 7-50. Over Voltage Protection

### 7.3.22.6 Overcurrent Protection (OCP)

MOSFET overcurrent event is sensed by monitoring the current flowing through the FETs. If the current across a FET exceeds the  $I_{OCP}$  threshold for longer than the deglitch time  $t_{OCP}$ , an OCP event is recognized and action is taken according to OCP\_MODE. The  $I_{OCP}$  threshold is set through the OCP\_LVL,  $t_{OCP}$  is set through OCP\_DEG and the OCP\_MODE can be configured in four different modes: latched shutdown, automatic retry, report only and disabled.

#### 7.3.22.6.1 OCP Latched Shutdown (OCP\_MODE = 00b)

When an OCP event happens in this mode, all MOSFETs are disabled and the nFAULT pin is driven low. The DRIVER\_FAULT, OCP and corresponding FET's OCP bits are set to 1b in the status registers. Normal operation resumes (driver operation and the nFAULT pin is released) when the OCP condition clears and a clear fault command is issued through the CLR\_FLT bit.

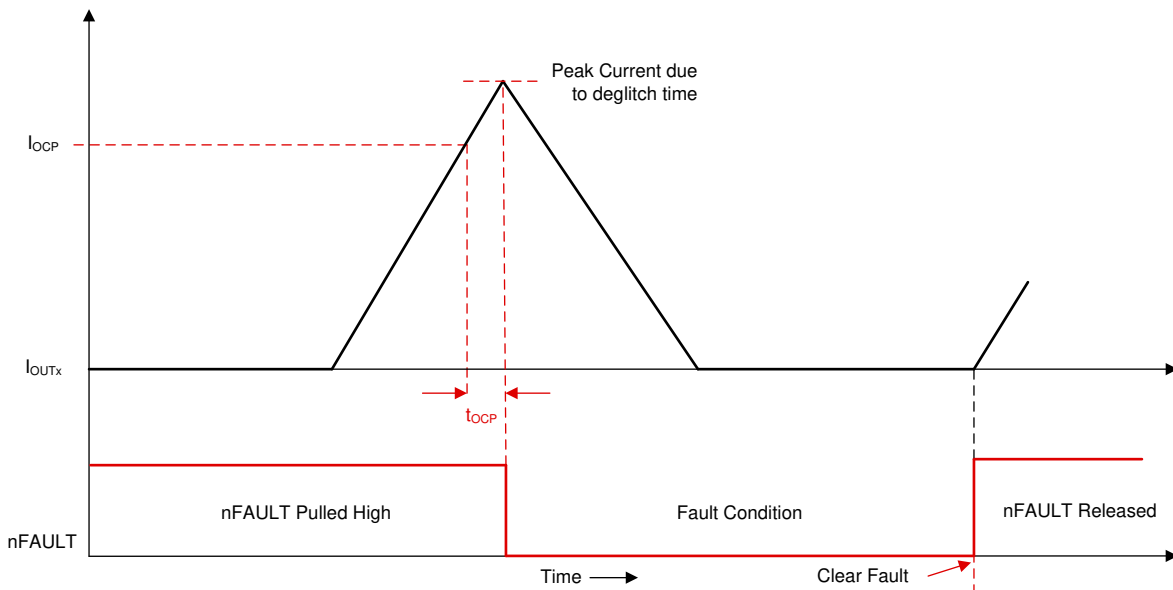


Figure 7-51. Overcurrent Protection - Latched Shutdown Mode

### 7.3.22.6.2 OCP Automatic Retry (OCP\_MODE = 01b)

When an OCP event happens in this mode, all the FETs are disabled and the nFAULT pin is driven low. The DRIVER\_FAULT, OCP and corresponding FET's OCP bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the  $t_{RETRY}$  (T\_RETRY) time elapses. The DRIVER\_FAULT bit is reset to 0b after the  $t_{RETRY}$  period expires. The OCP and corresponding FET's OCP bits are set to 1b until cleared through the CLR\_FLT bit.

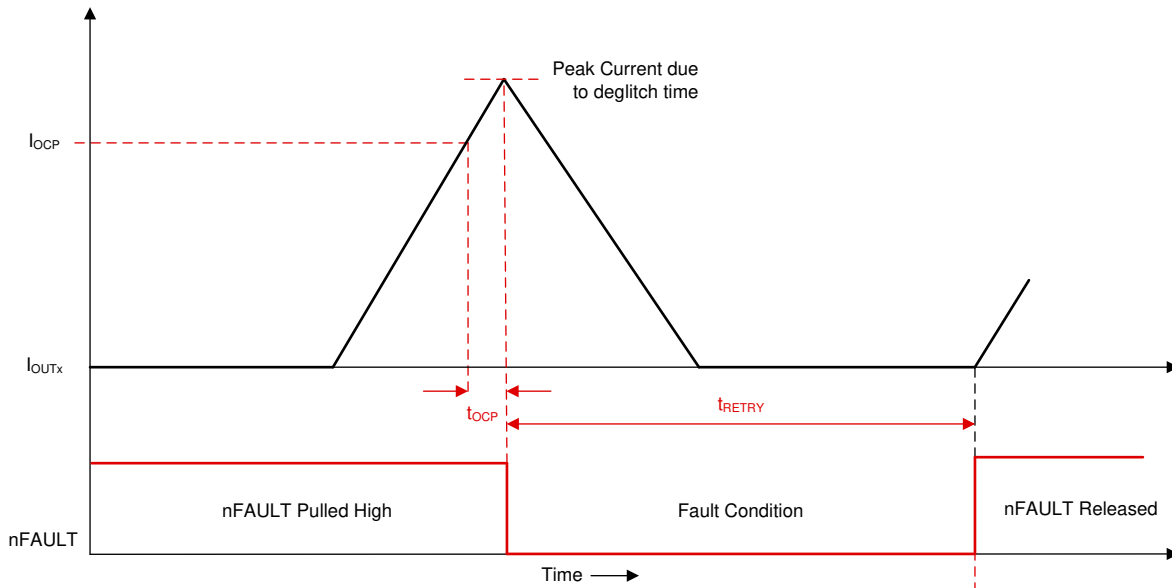


Figure 7-52. Overcurrent Protection - Automatic Retry Mode

### 7.3.22.7 Buck Overcurrent Protection

The buck overcurrent event is sensed by monitoring the current flowing through high-side MOSFET of the buck regulator. If the current through the high-side MOSFET exceeds the  $I_{BK\_OCP}$  threshold for a time longer than the deglitch time ( $t_{OCP}$ ), a buck OCP event is recognized and the buck regulator MOSFETs are disabled (Hi-Z). MCF8316C-Q1 goes into reset state whenever buck OCP event occurs, since the internal circuitry in MCF8316C-Q1 is powered from the buck regulator output.

### 7.3.22.8 Hardware Lock Detection Current Limit (HW\_LOCK\_ILIMIT)

The hardware lock detection current limit function provides a configurable threshold for limiting the current to prevent damage to the system. The MCF8316C-Q1 continuously motor phase currents are using comparators. If at any time, any phase current exceeds HW\_LOCK\_ILIMIT threshold for a time longer than  $t_{HW\_LOCK\_ILIMIT}$ , a HW\_LOCK\_ILIMIT event is recognized and action is taken according to the HW\_LOCK\_ILIMIT\_MODE. The current threshold is set by HW\_LOCK\_ILIMIT and the deglitch time,  $t_{HW\_LOCK\_ILIMIT}$  is set by HW\_LOCK\_ILIMIT\_DEG. HW\_LOCK\_ILIMIT\_MODE can be set in four different modes: HW\_LOCK\_ILIMIT latched shutdown, HW\_LOCK\_ILIMIT automatic retry, HW\_LOCK\_ILIMIT report only, and HW\_LOCK\_ILIMIT disabled.

#### 7.3.22.8.1 HW\_LOCK\_ILIMIT Latched Shutdown (HW\_LOCK\_ILIMIT\_MODE = 00xxb)

When a HW\_LOCK\_ILIMIT event happens in this mode, the status of MOSFET will be configured by HW\_LOCK\_ILIMIT\_MODE and nFAULT is driven low. Status of MOSFETs during HW\_LOCK\_ILIMIT:

- HW\_LOCK\_ILIMIT\_MODE = 0000b or 0001b: All MOSFETs are turned OFF.
- HW\_LOCK\_ILIMIT\_MODE = 0010b: All-high side MOSFETs are turned ON.
- HW\_LOCK\_ILIMIT\_MODE = 0011b: All-low side MOSFETs are turned ON.

The CONTROLLER\_FAULT and HW\_LOCK\_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the HW\_LOCK\_ILIMIT condition clears and a clear fault command is issued through the CLR\_FLT bit.

#### 7.3.22.8.2 HW\_LOCK\_ILIMIT Automatic recovery (HW\_LOCK\_ILIMIT\_MODE = 01xxb)

When a HW\_LOCK\_ILIMIT event happens in this mode, the status of MOSFET will be configured by HW\_LOCK\_ILIMIT\_MODE and nFAULT is driven low. Status of MOSFET during HW\_LOCK\_ILIMIT:

- HW\_LOCK\_ILIMIT\_MODE = 0100b or 0101b: All MOSFETs are turned OFF.
- HW\_LOCK\_ILIMIT\_MODE = 0110b: All high-side MOSFETs are turned ON
- HW\_LOCK\_ILIMIT\_MODE = 0111b: All low-side MOSFETs are turned ON

The CONTROLLER\_FAULT and HW\_LOCK\_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the  $t_{LCK\_RETRY}$  (configured by LCK\_RETRY) time lapses. The CONTROLLER\_FAULT and HW\_LOCK\_ILIMIT bits are reset to 0b after the  $t_{LCK\_RETRY}$  period expires.

#### 7.3.22.8.3 HW\_LOCK\_ILIMIT Report Only (HW\_LOCK\_ILIMIT\_MODE = 1000b)

No protective action is taken when a HW\_LOCK\_ILIMIT event happens in this mode. The hardware lock detection current limit event is reported by setting the CONTROLLER\_FAULT and HW\_LOCK\_ILIMIT bits to 1b in the fault status registers. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the HW\_LOCK\_ILIMIT condition clears and a clear fault command is issued through the CLR\_FLT bit.

#### 7.3.22.8.4 HW\_LOCK\_ILIMIT Disabled (HW\_LOCK\_ILIMIT\_MODE= 1xx1b)

No action is taken when a HW\_LOCK\_ILIMIT event happens in this mode.

#### 7.3.22.9 Lock Detection Current Limit (LOCK\_ILIMIT)

The lock detection current limit function provides a configurable threshold for limiting the current to prevent damage to the system. The MCF8316C-Q1 continuously monitors the motor phase currents through the ADC. If at any time, any phase current exceeds LOCK\_ILIMIT for a time longer than  $t_{LCK\_ILIMIT}$ , a LOCK\_ILIMIT event is recognized and action is taken according to LOCK\_ILIMIT\_MODE. The current threshold is set by LOCK\_ILIMIT and the deglitch time,  $t_{LCK\_ILIMIT\_DEG}$  is set by LOCK\_ILIMIT\_DEG. LOCK\_ILIMIT\_MODE can be set in four different modes: LOCK\_ILIMIT latched shutdown, LOCK\_ILIMIT automatic retry, LOCK\_ILIMIT report only and LOCK\_ILIMIT disabled.

##### 7.3.22.9.1 LOCK\_ILIMIT Latched Shutdown (LOCK\_ILIMIT\_MODE = 00xxb)

When a LOCK\_ILIMIT event happens in this mode, the status of MOSFETs will be configured by LOCK\_ILIMIT\_MODE and nFAULT is driven low. Status of MOSFETs during LOCK\_ILIMIT:

- LOCK\_ILIMIT\_MODE = 0000b or 0001b: All MOSFETs are turned OFF.
- LOCK\_ILIMIT\_MODE = 0010b: All high-side MOSFETs are turned ON.
- LOCK\_ILIMIT\_MODE = 0011b: All low-side MOSFETs are turned ON.

The CONTROLLER\_FAULT and LOCK\_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the LOCK\_ILIMIT condition clears and a clear fault command is issued through the CLR\_FLT bit.

##### 7.3.22.9.2 LOCK\_ILIMIT Automatic Recovery (LOCK\_ILIMIT\_MODE = 01xxb)

When a LOCK\_ILIMIT event happens in this mode, the status of MOSFETs will be configured by LOCK\_ILIMIT\_MODE and nFAULT is driven low. Status of MOSFETs during LOCK\_ILIMIT:

- LOCK\_ILIMIT\_MODE = 0100b or 0101b: All MOSFETs are turned OFF.
- LOCK\_ILIMIT\_MODE = 0110b: All high-side MOSFETs are turned ON
- LOCK\_ILIMIT\_MODE = 0111b: All low-side MOSFETs are turned ON

The CONTROLLER\_FAULT and LOCK\_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the  $t_{LCK\_RETRY}$  (configured

by LCK\_RETRY) time lapses. The CONTROLLER\_FAULT and LOCK\_ILIMIT bits are reset to 0b after the  $t_{LCK\_RETRY}$  period expires.

#### 7.3.22.9.3 LOCK\_ILIMIT Report Only (LOCK\_ILIMIT\_MODE = 1000b)

No protective action is taken when a LOCK\_ILIMIT event happens in this mode. The lock detection current limit event is reported by setting the CONTROLLER\_FAULT and LOCK\_ILIMIT bits to 1b in the fault status registers. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the LOCK\_ILIMIT condition clears and a clear fault command is issued through the CLR\_FLT bit.

#### 7.3.22.9.4 LOCK\_ILIMIT Disabled (LOCK\_ILIMIT\_MODE = 1xx1b)

No action is taken when a LOCK\_ILIMIT event happens in this mode.

#### 7.3.22.10 FET Thermal Warning (OTW)

If the FET temperature exceeds the FET thermal warning limit ( $T_{OTW}$ ), nFAULT is pulled low and the OT and OTW bits in the gate driver status register are set to 1b. The reporting of OTW (on nFAULT and status bits) can be enabled by setting OTW\_REP to 1b. The device performs no additional action and continues to function. The nFAULT pin is pulled low and OTW bit remains set until cleared through the CLR\_FLT bit and the die temperature is lower than thermal warning limit. ( $T_{OTW} - T_{OTW\_HYS}$ ).

#### 7.3.22.11 FET Thermal Shutdown (TSD\_FET)

If the FET temperature exceeds the FET thermal shutdown limit ( $T_{TSD\_FET}$ ), all the FETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the DRIVER\_FAULT, OT and OTS bit in the status register are set to 1b. Normal operation resumes (driver operation and the nFAULT pin is released) when the die temperature decreases below the hysteresis point of the thermal shutdown limit ( $T_{TSD\_FET} - T_{TSD\_FET\_HYS}$ ). The OTS bit stays latched high indicating that a thermal event occurred until a clear fault command is issued through the CLR\_FLT bit. This protection feature cannot be disabled.

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#### Note

If die temperature increases to  $T_{TSD\_BUCK}$ , MCF8316C-Q1 will undergo a reset and all fault status bits in this case will be reset to 0b.

---

#### 7.3.22.12 Motor Lock (MTR\_LCK)

The MCF8316C-Q1 continuously checks for different motor lock conditions (see [Motor Lock Detection](#)) during motor operation. When one of the enabled lock condition happens, a MTR\_LCK event is recognized and action is taken according to the MTR\_LCK\_MODE.

All locks can be enabled or disabled individually and retry times can be configured through LCK\_RETRY. MTR\_LCK\_MODE bit can operate in four different modes: MTR\_LCK latched shutdown, MTR\_LCK automatic retry, MTR\_LCK report only and MTR\_LCK disabled.

##### 7.3.22.12.1 MTR\_LCK Latched Shutdown (MTR\_LCK\_MODE = 00xxb)

When a MTR\_LCK event happens in this mode, the status of MOSFETs will be configured by MTR\_LCK\_MODE and nFAULT is driven low. Status of MOSFETs during MTR\_LCK:

- MTR\_LCK\_MODE = 0000b or 0001b: All MOSFETs are turned OFF.
- MTR\_LCK\_MODE = 0010b: All high-side MOSFETs are turned ON.
- MTR\_LCK\_MODE = 0011b: All low-side MOSFETs are turned ON.

The CONTROLLER\_FAULT, MTR\_LCK and respective motor lock condition bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the MTR\_LCK condition clears and a clear fault command is issued through the CLR\_FLT bit.

##### 7.3.22.12.2 MTR\_LCK Automatic Recovery (MTR\_LCK\_MODE= 01xxb)

When a MTR\_LCK event happens in this mode, the status of MOSFETs will be configured by MTR\_LCK\_MODE and nFAULT is driven low. Status of MOSFETs during MTR\_LCK:



- MTR\_LCK\_MODE = 0100b or 0101b: All MOSFETs are turned OFF.
- MTR\_LCK\_MODE = 0110b: All high-side MOSFETs are turned ON.
- MTR\_LCK\_MODE = 0111b: All low-side MOSFETs are turned ON.

The CONTROLLER\_FAULT, MTR\_LCK and respective motor lock condition bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the  $t_{LCK\_RETRY}$  (configured by LCK\_RETRY) time lapses. The CONTROLLER\_FAULT, MTR\_LCK and respective motor lock condition bits are reset to 0b after the  $t_{LCK\_RETRY}$  period expires.

#### 7.3.22.12.3 MTR\_LCK Report Only (MTR\_LCK\_MODE = 1000b)

No protective action is taken when a MTR\_LCK event happens in this mode. The motor lock event is reported by setting the CONTROLLER\_FAULT, MTR\_LCK and respective motor lock condition bits to 1b in the fault status registers. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the MTR\_LCK condition clears and a clear fault command is issued through the CLR\_FLT bit.

#### 7.3.22.12.4 MTR\_LCK Disabled (MTR\_LCK\_MODE = 1xx1b)

No action is taken when a MTR\_LCK event happens in this mode.

### 7.3.22.13 Motor Lock Detection

The MCF8316C-Q1 provides different lock detect mechanisms to determine if the motor is in a locked state. Multiple detection mechanisms work together to ensure the lock condition is detected quickly and reliably. In addition to detecting if there is a locked motor condition, the MCF8316C-Q1 can also identify and take action if there is no motor connected to the system. Each of the lock detect mechanisms and the no-motor detection can be disabled by their respective register bits (LOCK1/2/3\_EN).

#### 7.3.22.13.1 Lock 1: Abnormal Speed (ABN\_SPEED)

MCF8316C-Q1 monitors the speed continuously and at any time the speed exceeds LOCK\_ABN\_SPEED, an ABN\_SPEED lock event is recognized and action is taken according to the MTR\_LCK\_MODE. The threshold is set through the LOCK\_ABN\_SPEED register. ABN\_SPEED lock can be enabled/disabled by LOCK1\_EN.

#### 7.3.22.13.2 Lock 2: Abnormal BEMF (ABN\_BEMF)

MCF8316C-Q1 estimates back-EMF in order to run motor optimally in closed loop. This estimated back-EMF is compared against the expected back-EMF calculated using the estimated speed and the BEMF constant. Whenever motor is stalled the estimated back-EMF is inaccurate due to lower back-EMF at low speed. When the difference between estimated and expected back-EMF exceeds ABNORMAL\_BEMF\_THR, an abnormal BEMF fault is triggered and action is taken according to the MTR\_LCK\_MODE.

ABN\_BEMF lock can be enabled/disabled by LOCK2\_EN.

#### 7.3.22.13.3 Lock3: No-Motor Fault (NO\_MTR)

The MCF8316C-Q1 continuously monitors phase currents on all three phases; if any phase current stays below NO\_MTR\_THR for 500ms, a NO\_MTR event is recognized. The response to the NO\_MTR event is configured through MTR\_LCK\_MODE. NO\_MTR lock can be enabled/disabled by LOCK3\_EN.

### 7.3.22.14 MPET Faults

An error during resistance and inductance measurement is reported using MPET\_IPD\_FAULT. The MPET\_IPD\_FAULT gets triggered when the IPD timer overflows due to unsuccessful attempt to ramp up the current to the threshold value, same as explained in [Section 7.3.22.15](#). The fault typically gets triggered when there is no motor connected to MCF8316C-Q1 or when the MPET IPD current threshold is set high for motors with high resistance.

An error during BEMF constant measurement is reported using MPET\_BEMF\_FAULT. This fault gets triggered when the measured back EMF is less than the threshold set in STAT\_DETECT\_THR. One example of such fault scenario can be the motor stall while running in open loop due to incorrect open loop configuration used.

### 7.3.22.15 IPD Faults

The MCF8316C-Q1 uses 12-bit timers to estimate the time during the current ramp up and ramp down during IPD, when the motor start-up is configured as IPD (MTR\_STARTUP is set to 10b). During IPD, the algorithm checks for a successful current ramp-up to IPD\_CURR\_THR, starting with an IPD clock of 10MHz; if unsuccessful (timer overflow before current reaches IPD\_CURR\_THR), IPD is repeated with lower frequency clocks of 1MHz, 100kHz, and 10kHz sequentially. If the IPD timer overflows (current does not reach IPD\_CURR\_THR) with all the four clock frequencies, then the IPD\_T1\_FAULT gets triggered. Similarly the algorithm checks for a successful current decay to zero during IPD current ramp down using all the mentioned IPD clock frequencies. If the IPD timer overflows (current does not ramp down to zero) in all the four attempts, then the IPD\_T2\_FAULT gets triggered. The user can enable IPD timeout (IPD timer overflow) by setting IPD\_TIMEOUT\_FAULT\_EN to 1b.

IPD gives incorrect results if the next IPD pulse is commanded before the complete decay of current due to present IPD pulse. The MCF8316C-Q1 can generate a fault called IPD\_FREQ\_FAULT during such a scenario by setting IPD\_FREQ\_FAULT\_EN to 1b. The IPD\_FREQ\_FAULT maybe triggered if the IPD frequency is too high for the IPD current limit and the IPD release mode or if the motor inductance is too high for the IPD frequency, IPD current limit and IPD release mode.

On the occurrence of any IPD fault, MCF8316C-Q1 stops the IPD based start-up process and FETs are in Hi-Z. MCF8316C-Q1 automatically retries IPD based start-up after  $t_{LCK\_RETRY}$  elapses.

## 7.4 Device Functional Modes

### 7.4.1 Functional Modes

#### 7.4.1.1 Sleep Mode

In sleep mode, the MOSFETs, sense amplifiers, buck regulator, charge pump, AVDD LDO regulator and the I<sup>2</sup>C bus are disabled. The device can be configured to enter sleep (instead of standby) mode by configuring DEV\_MODE to 1b. SPEED pin and I<sup>2</sup>C speed command determine entry and exit from sleep state as described in [Table 7-7](#).

#### 7.4.1.2 Standby Mode

The device can be configured to operate as a standby device by setting DEV\_MODE to 0b. In standby mode, the charge pump, AVDD LDO, buck regulator and I<sup>2</sup>C bus are active while the motor is in stopped state waiting for a suitable non-zero speed command. SPEED pin (analog, PWM or frequency based speed input) or I<sup>2</sup>C speed command (I<sup>2</sup>C based speed input) determines entry and exit from standby state as described in [Table 7-7](#).

The thresholds for entering and exiting standby mode in different input modes are as follows,

**Table 7-6. Standby Mode Entry/Exit Thresholds**

| Input Source (SPEED_MODE) | Standby entry/exit thresholds             | REF_PROFILE_CONFIG = 00b   | REF_PROFILE_CONFIG # 00b |
|---------------------------|---|--|--------------------------|
| Analog (00b)              | V <sub>EN_SB</sub>                        | 1% x V <sub>ANA_FS</sub>   | 1% x V <sub>ANA_FS</sub> |
|                           | V <sub>EX_SB</sub>                        | 5% x V <sub>ANA_FS</sub>   | 5% x V <sub>ANA_FS</sub> |
| PWM (01b)                 | Duty <sub>EX_SB/EN_SB</sub>               | Maximum of (1%, DUTY_HYS)  | 0%                       |
| I <sup>2</sup> C (10b)    | DIGITAL_SPEED_CTRL <sub>EX_SB/EN_SB</sub> | Maximum of (1%, DUTY_HYS) x 32767  | 0                        |
| Frequency (11b)           | Freq <sub>EX_SB/EN_SB</sub>               | Maximum of (1%, DUTY_HYS) x INPUT_MAXIMUM_FREQ (subject to minimum of 3Hz) | < 3Hz                    |

**Table 7-7. Conditions to Enter or Exit Sleep/Standby Modes**

| SPEED COMMAND MODE | ENTER STANDBY CONDITION                                  | EXIT FROM STANDBY CONDITION                              | ENTER SLEEP CONDITION   | EXIT FROM SLEEP CONDITION  |
|--------------------|--|--|---|--|
| Analog             | V <sub>SPEED</sub> < V <sub>EN_SB</sub>                  | V <sub>SPEED</sub> > V <sub>EX_SB</sub>                  | V <sub>SPEED</sub> < V <sub>EN_SL</sub> for t <sub>DET_SL_ANA</sub>                           | V <sub>SPEED</sub> > V <sub>EX_SL</sub> for t <sub>DET_ANA</sub> |
| PWM                | Duty <sub>SPEED</sub> < Duty <sub>EN_SB</sub>            | Duty <sub>SPEED</sub> > Duty <sub>EX_SB</sub>            | V <sub>SPEED</sub> < V <sub>IL</sub> for t <sub>DET_SL_PWM</sub>                              | V <sub>SPEED</sub> > V <sub>IH</sub> for t <sub>DET_PWM</sub>    |
| I <sup>2</sup> C   | DIGITAL_SPEED_CTRL < DIGITAL_SPEED_CTRL <sub>EN_SB</sub> | DIGITAL_SPEED_CTRL > DIGITAL_SPEED_CTRL <sub>EX_SB</sub> | DIGITAL_SPEED_CTRL is set to 0b for SLEEP_ENTRY_TIME and V <sub>SPEED</sub> < V <sub>IL</sub> | V <sub>SPEED</sub> > V <sub>IH</sub> for t <sub>DET_PWM</sub>    |
| Frequency          | Freq <sub>SPEED</sub> < Freq <sub>EN_SB</sub>            | Freq <sub>SPEED</sub> > Freq <sub>EX_SB</sub>            | V <sub>SPEED</sub> < V <sub>IL</sub> for t <sub>DET_SL_PWM</sub>                              | V <sub>SPEED</sub> > V <sub>IH</sub> for t <sub>DET_PWM</sub>    |

#### Note

V<sub>SPEED</sub> : SPEED pin input voltage, Duty<sub>SPEED</sub> : SPEED pin input PWM duty, Freq<sub>SPEED</sub> : SPEED pin input frequency

#### 7.4.1.3 Fault Reset (CLR\_FLT)

In the case of latched faults, the device goes into a partial shutdown state to help protect the power MOSFETs and system. When the fault condition clears, the device can go to the operating state again by setting the CLR\_FLT to 1b.

## 7.5 External Interface

### 7.5.1 DRVOFF Functionality

When DRVOFF pin is driven high, all six MOSFETs are put in Hi-Z state, irrespective of speed command. If motor speed command is non-zero when DRVOFF is driven high, device may encounter a fault like no motor or abnormal BEMF. Whenever DRVOFF is driven high, it should be held high for a minimum of 10s for safe operation.

### 7.5.2 DAC outputs

MCF8316C-Q1 has two 12-bit DACs which output analog voltage equivalent of digital variables on the DACOUT1 and DACOUT2 pins. The maximum DAC output voltage is 3-V. Signals available on DACOUT pins are useful in tracking internal variables in real-time and can be used for tuning speed controller or motor acceleration time. The address for variables to be tracked on DACOUT1 and DACOUT2 are configured using DACOUT1\_VAR\_ADDR and DACOUT2\_VAR\_ADDR respectively. DACOUT1 is available on pin 36 and DACOUT2 can be configured on pin 38 by setting DAC\_SOx\_SEL to 00b. DACOUT2 is also available on pin 37. DAC\_ENABLE should be configured to 1b for pins 36, 37 to function as DAC outputs.

### 7.5.3 Current Sense Output

MCF8316C-Q1 can provide the built-in current sense amplifiers' output on the SOX pin. SOX output is available on pin 38 and can be configured by DAC\_SOx\_SEL.

### 7.5.4 Oscillator Source

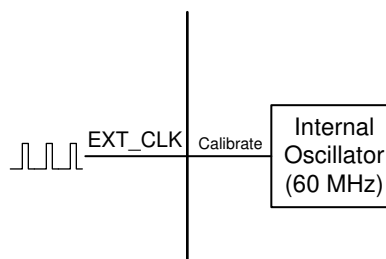
MCF8316C-Q1 has a built-in oscillator that is used as the clock source for all digital peripherals and timing measurements. Default configuration for MCF8316C-Q1 is to use the internal oscillator and it is sufficient to drive the motor without need for any external crystal or clock sources.

In case MCF8316C-Q1 does not meet accuracy requirements of timing measurement or speed loop, then MCF8316C-Q1 has an option to support an external clock reference.

In order to improve EMI performance, MCF8316C-Q1 provides the option of modulating the clock frequency by enabling Spread Spectrum Modulation (SSM) through SPREAD\_SPECTRUM\_MODULATION\_DIS.

#### 7.5.4.1 External Clock Source

Speed loop accuracy of MCF8316C-Q1 over the operating temperature range can be improved by providing a more accurate clock reference on EXT\_CLK pin as shown in [Figure 7-53](#). EXT\_CLK will be used to calibrate the internal clock oscillator - this will help match the accuracy of the internal clock oscillator to that of the external clock. External clock source can be selected by configuring CLK\_SEL to 11b and setting EXT\_CLK\_EN to 1b. The external clock source frequency can be configured through EXT\_CLK\_CONFIG.



**Figure 7-53. External Clock Reference**

#### Note

External clock is optional and can be used when higher clock accuracy is needed. MCF8316C-Q1 will always power up using the internal oscillator in all modes.

### 7.5.5 External Watchdog

MCF8316C-Q1 provides an external watchdog feature - EXT\_WDT\_EN bit should be set to 1b to enable the external watchdog. When this feature is enabled, the device waits for a tickle (low to high transition in EXT\_WD pin, WATCHDOG\_TICKLE set to 1b in I<sup>2</sup>C mode) from the external watchdog input for a configured time interval; if the time interval between two consecutive tickles is higher than the configured time, a watchdog fault is triggered. The watchdog fault response can be configured using EXT\_WDT\_FAULT\_MODE either as a report only fault or as a latched fault with MOSFETs in Hi-Z state. The latched fault can be cleared by writing 1b to CLR\_FLT. When a watchdog timeout occurs, WATCHDOG\_FAULT bit is set to 1b. In case, the next tickle arrives before the configured time interval elapses, the watchdog timer is reset and it begins to wait for the next tickle. This can be used to continuously monitor the health of an external MCU (which is the external watchdog input) and put the MCF8316C-Q1 MOSFETs in Hi-Z, in case the external MCU is in a fault/hang state.

The external watchdog input is selected using EXT\_WDT\_INPUT\_MODE and can either be the EXT\_WD pin or the I<sup>2</sup>C interface. The time interval between two tickles to trigger a watchdog fault is configured by EXT\_WDT\_CONFIG; there are 4 time settings - 100, 200, 500 and 1000ms for the EXT\_WD pin based watchdog and 4 time settings - 1, 2, 5 and 10s for the I<sup>2</sup>C based watchdog.

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#### **Note**

Watchdog should be disabled by setting EXT\_WDT\_EN to 0b before changing EXT\_WDT\_CONFIG configuration.

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## 7.6 EEPROM access and I<sup>2</sup>C interface

### 7.6.1 EEPROM Access

MCF8316C-Q1 has 1024 bits (16 rows of 64 bits each) of EEPROM, which are used to store the motor configuration parameters. Erase operations are row-wise (all 64 bits are erased in a single erase operation), but 32-bit write and read operations are supported. EEPROM can be written and read using the I<sup>2</sup>C serial interface but erase cannot be performed using I<sup>2</sup>C serial interface. The shadow registers corresponding to the EEPROM are located at addresses 0x000080-0x0000AE.

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#### Note

MCF8316C-Q1 allows EEPROM write and read operations only when the motor is not spinning.

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#### 7.6.1.1 EEPROM Write

In MCF8316C-Q1, EEPROM write procedure is as follows,

1. Write register 0x000080 (ISD\_CONFIG) with ISD and reverse drive configuration like resync enable, reverse drive enable, stationary detect threshold, reverse drive handoff threshold etc.
2. Write register 0x000082 (REV\_DRIVE\_CONFIG) with reverse drive and active brake configuration like reverse drive open loop acceleration, active brake current limit, Kp, Ki values etc.
3. Write register 0x000084 (MOTOR\_STARTUP1) with motor start-up configuration like start-up method, IPD parameters, align parameters etc.
4. Write register 0x000086 (MOTOR\_STARTUP2) with motor start-up configuration like open loop acceleration, open loop current limit, first cycle frequency etc.
5. Write register 0x000088 (CLOSED\_LOOP1) with motor control configuration like closed loop acceleration, overmodulation enable, PWM frequency, FG signal parameters etc.
6. Write register 0x00008A (CLOSED\_LOOP2) with motor control configuration like motor winding resistance and inductance, motor stop options, brake speed threshold etc.
7. Write register 0x00008C (CLOSED\_LOOP3) with motor control configuration like motor BEMF constant, current loop Kp, Ki etc.
8. Write register 0x00008E (CLOSED\_LOOP4) with motor control configuration like speed loop Kp, Ki and maximum speed.
9. Write register 0x000090 (FAULT\_CONFIG1) with fault control configuration software and hardware current limits, lock current limit and actions, retry times etc.
10. Write register 0x000092 (FAULT\_CONFIG2) with fault control configuration like hardware current limit actions, OV, UV limits and actions, abnormal speed level, no motor threshold etc.
11. Write registers 0x000094 – 0x00009E (SPEED\_PROFILES1-6) with speed profile configuration like profile type, duty cycle, speed clamp level, duty cycle clamp level etc.
12. Write register 0x0000A0 (INT\_ALGO\_1) with miscellaneous configuration like ISD run time and timeout, MPET parameters etc.
13. Write register 0x0000A2 (INT\_ALGO\_2) with miscellaneous configuration like additional MPET parameters, IPD high resolution enable, active brake current slew rate, closed loop slow acceleration etc.
14. Write registers 0x0000A4 (PIN\_CONFIG1) with pin configuration for speed input mode (analog or PWM), BRAKE pin mode etc.
15. Write registers 0x0000A6 and 0x0000A8 (DEVICE\_CONFIG1 and DEVICE\_CONFIG2) with device configuration like pins 36, 37 configuration, pin 38 configuration, dynamic CSA gain enable, dynamic voltage gain enable, clock source select, speed range select etc.
16. Write register 0x0000AA (PERI\_CONFIG1) with peripheral configuration like dead time, bus current limit, DIR input, SSM enable etc.
17. Write registers 0x0000AC and 0x0000AE (GD\_CONFIG1 and GD\_CONFIG2) with gate driver configuration like slew rate, CSA gain, OCP level, mode, OVP enable, level, buck voltage level, buck current limit etc.
18. Write 0x8A500000 into register 0x0000EA to write the shadow register(0x000080-0x0000AE) values into the EEPROM.
19. Wait for 300ms for the EEPROM write operation to complete

Steps 1-17 can be selectively executed based on registers/parameters that need to be modified. After all shadow registers have been updated with the required values, step 18 should be executed to copy the contents of the shadow registers into the EEPROM.

### 7.6.1.2 EEPROM Read

In MCF8316C-Q1, EEPROM read procedure is as follows,

1. Write 0x40000000 into register 0x0000EA to read the EEPROM data into the shadow registers (0x000080-0x0000AE).
2. Wait for 100ms for the EEPROM read operation to complete.
3. Read the shadow register values, 1 or 2 registers at a time, using the I<sup>2</sup>C read command as explained in [Section 7.6.2](#). Shadow register addresses are in the range of 0x000080-0x0000AE. Register address increases in steps of 2 for 32-bit read operation (since each address is a 16-bit location).

### 7.6.2 I<sup>2</sup>C Serial Interface

MCF8316C-Q1 interfaces with an external MCU over an I<sup>2</sup>C serial interface. MCF8316C-Q1 is an I<sup>2</sup>C target to be interfaced with a controller. External MCU can use this interface to read/write from/to any non-reserved register in MCF8316C-Q1.

#### Note

For reliable communication, a 100- $\mu$ s delay should be used between every byte transferred over the I<sup>2</sup>C bus.

#### 7.6.2.1 I<sup>2</sup>C Data Word

The I<sup>2</sup>C data word format is shown in [Table 7-8](#).

**Table 7-8. I<sup>2</sup>C Data Word Format**

| TARGET_ID | R/W | CONTROL WORD | DATA                | CRC-8   |
|-----------|-----|--------------|---------------------|---------|
| A6 - A0   | W0  | CW23 - CW0   | D15 / D31/ D63 - D0 | C7 - C0 |

**Target ID and R/W Bit:** The first byte includes the 7-bit I<sup>2</sup>C target ID, followed by the read/write command bit. Every packet in MCF8316C-Q1 the communication protocol starts with writing a 24-bit control word and hence the R/W bit is always 0.

**24-bit Control Word:** The Target Address is followed by a 24-bit control bit. The control word format is shown in [Table 7-9](#).

**Table 7-9. 24-bit Control Word Format**

| OP_R/W | CRC_EN | DLEN       | MEM_SEC     | MEM_PAGE    | MEM_ADDR   |
|--------|--------|------------|-------------|-------------|------------|
| CW23   | CW22   | CW21- CW20 | CW19 - CW16 | CW15 - CW12 | CW11 - CW0 |

Each field in the control word is explained in detail below.

**OP\_R/W – Read/Write:** R/W bit gives information on whether this is a read (1b) operation or write (0b) operation. For write operation, MCF8316C-Q1 will expect data bytes to be sent after the 24-bit control word. For read operation, MCF8316C-Q1 will expect an I<sup>2</sup>C read request with repeated start or normal start after the 24-bit control word.

**CRC\_EN – Cyclic Redundancy Check(CRC) Enable:** MCF8316C-Q1 supports CRC to verify the data integrity. This bit controls whether the CRC feature is enabled or not.

**DLEN – Data Length:** DLEN field determines the length of the data that will be sent by external MCU to MCF8316C-Q1. MCF8316C-Q1 protocol supports three data lengths: 16-bit, 32-bit and 64-bit.

**Table 7-10. Data Length Configuration**

| DLEN Value | Data Length |
|------------|-------------|
| 00b        | 16-bit      |

**Table 7-10. Data Length Configuration (continued)**

| DLEN Value | Data Length |
|------------|-------------|
| 01b        | 32-bit      |
| 10b        | 64-bit      |
| 11b        | Reserved    |

**MEM\_SEC – Memory Section:** Each memory location in MCF8316C-Q1 is addressed using three separate entities in the control word – Memory Section, Memory Page, Memory Address. Memory Section is a 4-bit field which denotes the memory section to which the memory location belongs like RAM, ROM etc.

**MEM\_PAGE – Memory Page:** Memory page is a 4-bit field which denotes the memory page to which the memory location belongs.

**MEM\_ADDR – Memory Address:** Memory address is the last 12-bits of the address. The complete 22-bit address is constructed internally by MCF8316C-Q1 using all three fields – Memory Section, Memory Page, Memory Address. For memory locations 0x000000-0x000800, memory section is 0x0, memory page is 0x0 and memory address is the lowest 12 bits(0x000 for 0x000000, 0x080 for 0x000080 and 0x800 for 0x000800). All relevant memory locations (EEPROM and RAM variables) have MEM\_SEC and MEM\_PAGE values both corresponding to 0x0. All other MEM\_SEC, MEM\_PAGE values are reserved and not for external use.

**Data Bytes:** For a write operation to MCF8316C-Q1, the 24-bit control word is followed by data bytes. The DLEN field in the control word should correspond with the number of bytes sent in this section. In case of mismatch between number of data bytes and DLEN, the write operation is discarded.

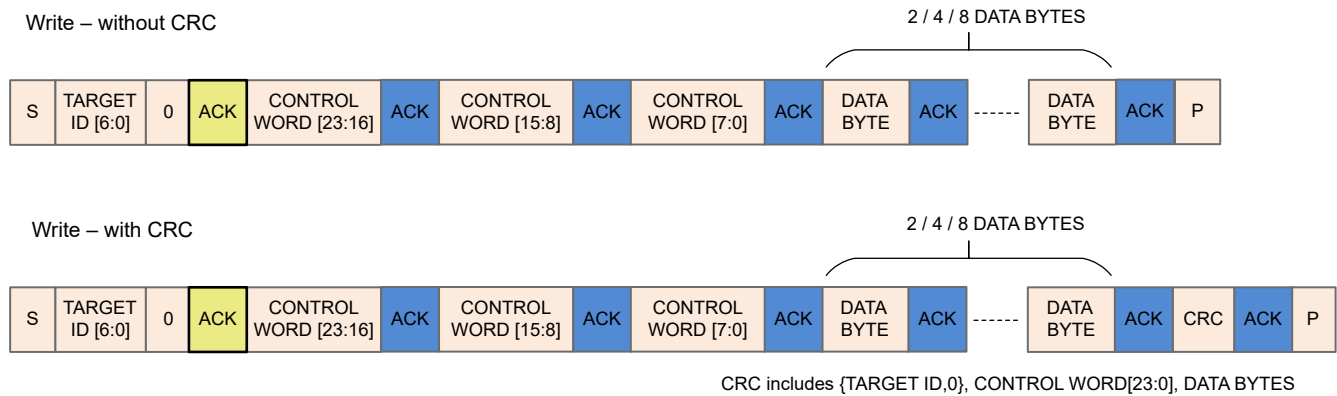
**CRC Byte:** If the CRC feature is enabled in the control word, CRC byte has to be sent at the end of a write transaction. Refer to [Section 7.6.2.6](#) for detailed information on CRC byte calculation.

#### 7.6.2.2 I<sup>2</sup>C Write Transaction

MCF8316C-Q1 write transaction over I<sup>2</sup>C involves the following sequence (see [Figure 7-54](#)).

1. I<sup>2</sup>C start condition.
2. Start is followed by the I<sup>2</sup>C target ID byte, made up of 7-bit target ID along with the R/W bit set to 0b. ACK in yellow box indicates that MCF8316C-Q1 has processed the received target ID which has matched with its I<sup>2</sup>C target ID and therefore will proceed with this transaction. If target ID received does not match with the I<sup>2</sup>C ID of MCF8316C-Q1, then the transaction is ignored. and no ACK is sent by MCF8316C-Q1.
3. The target ID byte is followed by the 24-bit control word sent one byte at a time. Bit 23 in the control word is 0b as it is a write transaction. ACK in blue boxes correspond to acknowledgements sent by MCF8316C-Q1 to the controller that the previous byte (of control word) has been received and next byte can be sent.
4. The 24-bit control word is then followed by the data bytes. The number of data bytes sent by the controller depends on the DLEN field in the control word.
  - a. While sending data bytes, the LSB byte is sent first. Refer to [Section 7.6.2.4](#) for more details.
  - b. 16-bit/32-bit write – The data sent is written to the address mentioned in control word.
  - c. 64-bit Write – 64-bit is treated as two successive 32-bit writes. The address mentioned in control word is taken as Addr\_1. Addr\_2 is internally calculated by MCF8316C-Q1 by incrementing Addr\_1 by 0x2. A total of 8 data bytes are sent. The first 4 bytes (sent in LSB first) are written to Addr\_1 and the next 4 bytes are written to Addr\_2.
  - d. ACK in blue boxes (after every data byte) correspond to the acknowledgement sent by MCF8316C-Q1 to the controller that the previous data byte has been received and next data byte can be sent.
5. If CRC is enabled, the packet ends with a CRC byte. CRC is calculated for the entire packet (Target ID + W bit, Control Word, Data Bytes). MCF8316C-Q1 will send an ACK on receiving the CRC byte.
6. I<sup>2</sup>C Stop condition from the controller to terminate the transaction.



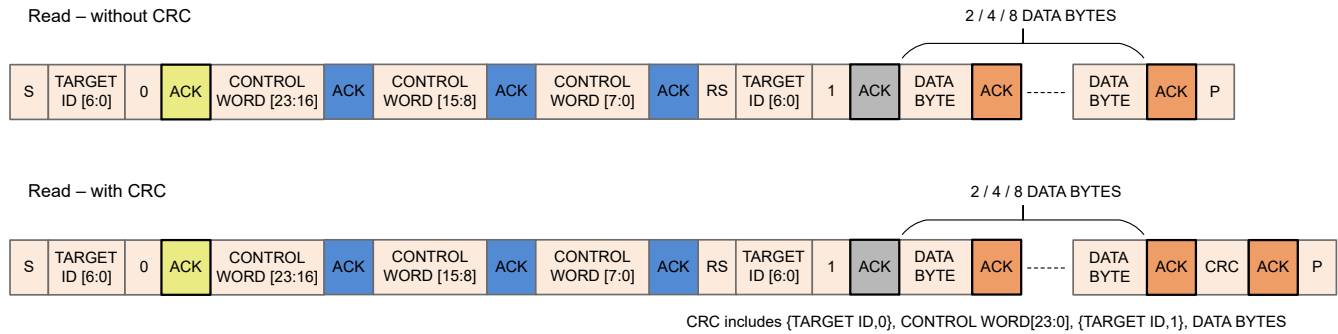


**Figure 7-54. I<sup>2</sup>C Write Transaction Sequence**

### 7.6.2.3 I<sup>2</sup>C Read Transaction

MCF8316C-Q1 read transaction over I<sup>2</sup>C involves the following sequence (see [Figure 7-55](#)).

1. I<sup>2</sup>C Start condition from the controller to initiate the transaction.
2. Start is followed by the I<sup>2</sup>C target ID byte, made up of 7-bit target ID along with the R/W bit set to 0b. ACK (in yellow box) indicates that MCF8316C-Q1 has processed the received target ID which has matched with its I<sup>2</sup>C target ID and therefore will proceed with this transaction. If target ID received does not match with the I<sup>2</sup>C ID of MCF8316C-Q1, then the transaction is ignored and no ACK is sent by MCF8316C-Q1.
3. The target ID byte is followed by the 24-bit control word sent one byte at a time. Bit 23 in the control word is set to 1b as it is a read transaction. ACK (in blue boxes) correspond to acknowledgements sent by MCF8316C-Q1 to the controller that the previous byte (of control word) has been received and next byte can be sent.
4. The control word is followed by a Repeated Start (RS, start without a preceding stop) or normal Start (P followed by S) to initiate the data (to be read back) transfer from MCF8316C-Q1 to I<sup>2</sup>C controller. RS or S is followed by the 7-bit target ID along with R/W bit set to 1b to initiate the read transaction. MCF8316C-Q1 sends an ACK (in grey box after RS) to the controller to acknowledge the receipt of read transaction request.
5. Post acknowledgement of read transaction request, MCF8316C-Q1 sends the data bytes on SDA one byte at a time. The number of data bytes sent by MCF8316C-Q1 depends on the DLEN field in the control word.
  - a. While sending data bytes, the LSB byte is sent first. Refer the examples in [Section 7.6.2.4](#) for more details.
  - b. 16-bit/32-bit Read – The data from the address mentioned in control word is sent back to the controller.
  - c. 64-bit Read – 64-bit is treated as two successive 32-bit reads. The address mentioned in control word is taken as Addr\_1. Addr\_2 is internally calculated by MCF8316C-Q1 by incrementing Addr\_1 by 0x2. A total of 8 data bytes are sent by MCF8316C-Q1. The first 4 bytes (sent in LSB first) are read from Addr\_1 and the next 4 bytes are read from Addr\_2.
  - d. ACK in orange boxes correspond to acknowledgements sent by the controller to MCF8316C-Q1 that the previous byte has been received and next byte can be sent.
6. If CRC is enabled in the control word, then MCF8316C-Q1 sends an additional CRC byte at the end. Controller has to read the CRC byte and then send the last ACK (in orange). CRC is calculated for the entire packet (Target ID + W bit, Control Word, Target ID + R bit, Data Bytes).
7. I<sup>2</sup>C Stop condition from the controller to terminate the transaction.



**Figure 7-55. I<sup>2</sup>C Read Transaction Sequence**

**7.6.2.4 I<sup>2</sup>C Communication Protocol Packet Examples**

All values used in this example section are in hex format. I<sup>2</sup>C target ID used in the examples is 0x60.

**Example for 32-bit Write Operation:** Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

**Table 7-11. Example for 32-bit Write Operation Packet**

| Start Byte |                        | Control Word 0 |        |           |           | Control Word 1 |          |          | Control Word 2 | Data Bytes |       |       |          | CRC |
|------------|------------------------|----------------|--------|-----------|-----------|----------------|----------|----------|----------------|------------|-------|-------|----------|-----|
| Target ID  | I <sup>2</sup> C Write | OP_R/W         | CRC_EN | DLEN      | MEM_SEC   | MEM_PAGE       | MEM_ADDR | MEM_ADDR | DB0            | DB1        | DB2   | DB3   | CRC Byte |     |
| A6-A0      | W0                     | CW23           | CW22   | CW21-CW20 | CW19-CW16 | CW15-CW12      | CW11-CW8 | CW7-CW0  | D7-D0          | D7-D0      | D7-D0 | D7-D0 | C7-C0    |     |
| 0x60       | 0x0                    | 0x0            | 0x1    | 0x1       | 0x0       | 0x0            | 0x0      | 0x80     | 0xCD           | 0xAB       | 0x34  | 0x12  | 0x45     |     |
| 0xC0       |                        | 0x50           |        |           |           | 0x00           |          | 0x80     | 0xCD           | 0xAB       | 0x34  | 0x12  | 0x45     |     |

**Example for 64-bit Write Operation:** Address - 0x00000080, Data Address 0x00000080 - Data 0x01234567, Data Address 0x00000082 – Data 0x89ABCDEF, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

**Table 7-12. Example for 64-bit Write Operation Packet**

| Start Byte |                        | Control Word 0 |        |           |           | Control Word 1 |          |          | Control Word 2    | Data Bytes | CRC |
|------------|------------------------|----------------|--------|-----------|-----------|----------------|----------|----------|-------------------|------------|-----|
| Target ID  | I <sup>2</sup> C Write | OP_R/W         | CRC_EN | DLEN      | MEM_SEC   | MEM_PAGE       | MEM_ADDR | MEM_ADDR | DB0 - DB7         | CRC Byte   |     |
| A6-A0      | W0                     | CW23           | CW22   | CW21-CW20 | CW19-CW16 | CW15-CW12      | CW11-CW8 | CW7-CW0  | [D7-D0] x 8       | C7-C0      |     |
| 0x60       | 0x0                    | 0x0            | 0x1    | 0x2       | 0x0       | 0x0            | 0x0      | 0x80     | 0x67452301EFCDA89 | 0x45       |     |
| 0xC0       |                        | 0x60           |        |           |           | 0x00           |          | 0x80     | 0x67452301EFCDA89 | 0x45       |     |

**Example for 32-bit Read Operation:** Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x56 (Sample value; does not match with the actual CRC calculation)

**Table 7-13. Example for 32-bit Read Operation Packet**

| Start Byte |                        | Control Word 0 |        |           |           | Control Word 1 | Control Word 2 | Start Byte | Byte 0                | Byte 1 | Byte 2 | Byte 3 | Byte 4 |          |       |
|------------|------------------------|----------------|--------|-----------|-----------|----------------|----------------|------------|-----------------------|--------|--------|--------|--------|----------|-------|
| Target ID  | I <sup>2</sup> C Write | R/W            | CRC_EN | DLEN      | MEM_SEC   | MEM_PAGE       | MEM_ADDR       | Target ID  | I <sup>2</sup> C Read | DB0    | DB1    | DB2    | DB3    | CRC Byte |       |
| A6-A0      | W0                     | CW23           | CW22   | CW21-CW20 | CW19-CW16 | CW15-CW12      | CW11-CW8       | CW7-CW0    | A6-A0                 | W0     | D7-D0  | D7-D0  | D7-D0  | D7-D0    | C7-C0 |
| 0x60       | 0x0                    | 0x1            | 0x1    | 0x1       | 0x0       | 0x0            | 0x0            | 0x80       | 0x60                  | 0x1    | 0xCD   | 0xAB   | 0x34   | 0x12     | 0x56  |
| 0xC0       |                        | 0xD0           |        |           |           | 0x00           |                | 0x80       | 0xC1                  |        | 0xCD   | 0xAB   | 0x34   | 0x12     | 0x56  |

### 7.6.2.5 I<sup>2</sup>C Clock Stretching

The I<sup>2</sup>C peripheral in MCF8316C-Q1 implements clock stretching under certain conditions when there are pending I<sup>2</sup>C interrupts waiting to be processed. During clock stretching, MCF8316C-Q1 pulls SCL low and the I<sup>2</sup>C bus is unavailable for use by other devices. The following is a list of conditions under which clock stretching can occur:

1. **Start interrupt pending:** There are two scenarios when a start interrupt can result in clock stretching,
  - a. When target ID is a match, I<sup>2</sup>C peripheral in MCF8316C-Q1 raises a start interrupt request. Until this start interrupt request is processed, clock is stretched. Upon processing this request, clock is released and an ACK (marked in yellow or grey in [Figure 7-54](#) and [Figure 7-55](#)) is sent to the controller for continuing with the transaction.
  - b. If Start (followed by target ID match) for a new transaction is received when a receive interrupt from previous transaction is yet to be processed, clock is stretched until both the receive interrupt and start interrupt are processed in chronological order. This process ensures that previous transaction is executed correctly before initiating the next transaction.
2. **Receive interrupt pending:** When a receive interrupt is waiting to be processed and the receive register is full which occurs when two successive bytes (data or control) have been received by MCF8316C-Q1 (separated by one ACK shown as blue boxes in [Figure 7-54](#) and [Figure 7-55](#)) without the receive interrupt generated by the first byte being processed. Upon receive of second byte, clock is stretched until receive interrupt generated by the first byte is processed.
3. **Transmit buffer is empty:** In case of a transmit interrupt pending (to send data back to controller), if the transmit buffer is waiting to be populated with data to be read back to the controller, clock stretching is done until the transmit buffer is populated with requested data. After the buffer is populated, clock is released and data is sent to controller.

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#### Note

I<sup>2</sup>C clock stretching is timed out after 5 ms by MCF8316C-Q1 to allow I<sup>2</sup>C bus access for other devices on the same bus.

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### 7.6.2.6 CRC Byte Calculation

An 8-bit CCIT polynomial ( $x^8 + x^2 + x + 1$ ) and CRC initial value 0xFF is used for CRC computation.

**CRC Calculation in Write Operation:** When the external MCU writes to MCF8316C-Q1, if the CRC is enabled, the external MCU has to compute an 8-bit CRC byte and add the CRC byte at the end of the data. MCF8316C-Q1 will compute CRC using the same polynomial internally and if there is a mismatch, the write request is discarded. Input data for CRC calculation by external MCU for write operation are listed below:

1. Target ID + write bit.
2. Control word – 3 bytes
3. Data bytes – 2/4/8 bytes

**CRC Calculation in Read Operation:** When the external MCU reads from MCF8316C-Q1, if the CRC is enabled, MCF8316C-Q1 sends the CRC byte at the end of the data. The CRC computation in read operation involves the start byte, control words sent by external MCU along with data bytes sent by MCF8316C-Q1. Input data for CRC calculation by external MCU to verify the data sent by MCF8316C-Q1 are listed below :

1. Target ID + write bit
2. Control word – 3 bytes
3. Target ID + read bit
4. Data bytes – 2/4/8 bytes

## 7.7 EEPROM (Non-Volatile) Register Map

### 7.7.1 Algorithm\_Configuration Registers

Table 7-14 lists the memory-mapped registers for the Algorithm\_Configuration registers. All register offset addresses not listed in Table 7-14 should be considered as reserved locations and the register contents should not be modified.

**Table 7-14. ALGORITHM\_CONFIGURATION Registers**

| Offset | Acronym          | Register Name                    | Section            |
|--------|------------------|----------------------------------|--------------------|
| 80h    | ISD_CONFIG       | ISD Configuration                | <a href="#">Go</a> |
| 82h    | REV_DRIVE_CONFIG | Reverse Drive Configuration      | <a href="#">Go</a> |
| 84h    | MOTOR_STARTUP1   | Motor Startup Configuration1     | <a href="#">Go</a> |
| 86h    | MOTOR_STARTUP2   | Motor Startup Configuration2     | <a href="#">Go</a> |
| 88h    | CLOSED_LOOP1     | Close Loop Configuration 1       | <a href="#">Go</a> |
| 8Ah    | CLOSED_LOOP2     | Close Loop Configuration2        | <a href="#">Go</a> |
| 8Ch    | CLOSED_LOOP3     | Close Loop Configuration3        | <a href="#">Go</a> |
| 8Eh    | CLOSED_LOOP4     | Close Loop Configuration4        | <a href="#">Go</a> |
| 94h    | REF_PROFILES1    | Reference Profile Configuration1 | <a href="#">Go</a> |
| 96h    | REF_PROFILES2    | Reference Profile Configuration2 | <a href="#">Go</a> |
| 98h    | REF_PROFILES3    | Reference Profile Configuration3 | <a href="#">Go</a> |
| 9Ah    | REF_PROFILES4    | Reference Profile Configuration4 | <a href="#">Go</a> |
| 9Ch    | REF_PROFILES5    | Reference Profile Configuration5 | <a href="#">Go</a> |
| 9Eh    | REF_PROFILES6    | Reference Profile Configuration6 | <a href="#">Go</a> |

Complex bit access types are encoded to fit into small table cells. Table 7-15 shows the codes that are used for access types in this section.

**Table 7-15. Algorithm\_Configuration Access Type Codes**

| Access Type            | Code | Description                            |
|------------------------|------|--|
| Read Type              |      |  |
| R                      | R    | Read                                   |
| Write Type             |      |  |
| W                      | W    | Write                                  |
| Reset or Default Value |      |  |
| -n                     |      | Value after reset or the default value |

### 7.7.1.1 ISD\_CONFIG Register (Offset = 80h) [Reset = 0000000h]

ISD\_CONFIG is shown in [Figure 7-56](#) and described in [Table 7-16](#).

Return to the [Summary Table](#).

Register to configure initial speed detect settings

**Figure 7-56. ISD\_CONFIG Register**

|                  |        |                     |            |              |           |                           |                 |
|------------------|--------|---------------------|------------|--------------|-----------|---------------------------|-----------------|
| 31               | 30     | 29                  | 28         | 27           | 26        | 25                        | 24              |
| RESERVED         | ISD_EN | BRAKE_EN            | HIZ_EN     | RVS_DR_EN    | RESYNC_EN | FW_DRV_RESYN_THR          |                 |
| R/W-0h           | R/W-0h | R/W-0h              | R/W-0h     | R/W-0h       | R/W-0h    | R/W-0h                    |                 |
| 23               | 22     | 21                  | 20         | 19           | 18        | 17                        | 16              |
| FW_DRV_RESYN_THR |        | BRK_MODE            | BRK_CONFIG | BRK_CURR_THR |           |                           | BRK_TIME        |
| R/W-0h           |        | R/W-0h              | R/W-0h     | R/W-0h       |           |                           | R/W-0h          |
| 15               | 14     | 13                  | 12         | 11           | 10        | 9                         | 8               |
| BRK_TIME         |        |                     | HIZ_TIME   |              |           |                           | STAT_DETECT_THR |
| R/W-0h           |        |                     | R/W-0h     |              |           |                           | R/W-0h          |
| 7                | 6      | 5                   | 4          | 3            | 2         | 1                         | 0               |
| STAT_DETECT_THR  |        | REV_DRV_HANDOFF_THR |            |              |           | REV_DRV_OPEN_LOOP_CURRENT |                 |
| R/W-0h           |        | R/W-0h              |            |              |           | R/W-0h                    |                 |

**Table 7-16. ISD\_CONFIG Register Field Descriptions**

| Bit | Field     | Type | Reset | Description   |
|-----|-----------|------|-------|---|
| 31  | RESERVED  | R/W  | 0h    | Reserved  |
| 30  | ISD_EN    | R/W  | 0h    | ISD Enable<br>0h = Disable<br>1h = Enable               |
| 29  | BRAKE_EN  | R/W  | 0h    | Brake enable<br>0h = Disable<br>1h = Enable             |
| 28  | HIZ_EN    | R/W  | 0h    | Hi-Z enable<br>0h = Disable<br>1h = Enable              |
| 27  | RVS_DR_EN | R/W  | 0h    | Reverse Drive Enable<br>0h = Disable<br>1h = Enable     |
| 26  | RESYNC_EN | R/W  | 0h    | Resynchronization Enable<br>0h = Disable<br>1h = Enable |

**Table 7-16. ISD\_CONFIG Register Field Descriptions (continued)**

| Bit   | Field            | Type | Reset | Description   |
|-------|------------------|------|-------|---|
| 25-22 | FW_DRV_RESYN_THR | R/W  | 0h    | Minimum Speed threshold to resynchronize to close loop (% of MAX_SPEED)<br>0h = 5%<br>1h = 10%<br>2h = 15%<br>3h = 20%<br>4h = 25%<br>5h = 30%<br>6h = 35%<br>7h = 40%<br>8h = 45%<br>9h = 50%<br>Ah = 55%<br>Bh = 60%<br>Ch = 70%<br>Dh = 80%<br>Eh = 90%<br>Fh = 100% |
| 21    | BRK_MODE         | R/W  | 0h    | Brake mode<br>0h = All three high side FETs turned ON<br>1h = All three low side FETs turned ON   |
| 20    | BRK_CONFIG       | R/W  | 0h    | Brake configuration<br>0h = Brake time is used to exit Brake state<br>1h = Brake current threshold and Brake time are used to exit Brake state  |
| 19-17 | BRK_CURR_THR     | R/W  | 0h    | Brake current threshold<br>0h = 0.1 A<br>1h = 0.2 A<br>2h = 0.3 A<br>3h = 0.5 A<br>4h = 1.0 A<br>5h = 2.0 A<br>6h = 4.0 A<br>7h = 8.0 A   |
| 16-13 | BRK_TIME         | R/W  | 0h    | Brake time<br>0h = 10 ms<br>1h = 50 ms<br>2h = 100 ms<br>3h = 200 ms<br>4h = 300 ms<br>5h = 400 ms<br>6h = 500 ms<br>7h = 750 ms<br>8h = 1 s<br>9h = 2 s<br>Ah = 3 s<br>Bh = 4 s<br>Ch = 5 s<br>Dh = 7.5 s<br>Eh = 10 s<br>Fh = 15 s                                    |

**Table 7-16. ISD\_CONFIG Register Field Descriptions (continued)**

| Bit  | Field                     | Type | Reset | Description   |
|------|---------------------------|------|-------|---|
| 12-9 | HIZ_TIME                  | R/W  | 0h    | Hi-Z time<br>0h = 10 ms<br>1h = 50 ms<br>2h = 100 ms<br>3h = 200 ms<br>4h = 300 ms<br>5h = 400 ms<br>6h = 500 ms<br>7h = 750 ms<br>8h = 1 s<br>9h = 2 s<br>Ah = 3 s<br>Bh = 4 s<br>Ch = 5 s<br>Dh = 7.5 s<br>Eh = 10 s<br>Fh = 15 s   |
| 8-6  | STAT_DETECT_THR           | R/W  | 0h    | BEMF threshold to detect if motor is stationary<br>0h = 50 mV<br>1h = 75 mV<br>2h = 100 mV<br>3h = 250 mV<br>4h = 500 mV<br>5h = 750 mV<br>6h = 1000 mV<br>7h = 1500 mV   |
| 5-2  | REV_DRV_HANDOFF_THR       | R/W  | 0h    | Speed threshold used to transition to open loop during reverse drive (% of MAX_SPEED)<br>0h = 2.5%<br>1h = 5%<br>2h = 7.5%<br>3h = 10%<br>4h = 12.5%<br>5h = 15%<br>6h = 20%<br>7h = 25%<br>8h = 30%<br>9h = 40%<br>Ah = 50%<br>Bh = 60%<br>Ch = 70%<br>Dh = 80%<br>Eh = 90%<br>Fh = 100% |
| 1-0  | REV_DRV_OPEN_LOOP_CURRENT | R/W  | 0h    | Open loop current limit during reverse drive<br>0h = 1.5 A<br>1h = 2.5 A<br>2h = 3.5 A<br>3h = 5.0 A  |

### 7.7.1.2 REV\_DRIVE\_CONFIG Register (Offset = 82h) [Reset = 0000000h]

REV\_DRIVE\_CONFIG is shown in [Figure 7-57](#) and described in [Table 7-17](#).

Return to the [Summary Table](#).

Register to configure reverse drive settings

**Figure 7-57. REV\_DRIVE\_CONFIG Register**

|                            |                            |        |    |        |                            |                 |    |
|----------------------------|----------------------------|--------|----|--------|----------------------------|-----------------|----|
| 31                         | 30                         | 29     | 28 | 27     | 26                         | 25              | 24 |
| RESERVED                   | REV_DRV_OPEN_LOOP_ACCEL_A1 |        |    |        | REV_DRV_OPEN_LOOP_ACCEL_A2 |                 |    |
| R/W-0h                     |                            | R/W-0h |    |        |                            | R/W-0h          |    |
| 23                         | 22                         | 21     | 20 | 19     | 18                         | 17              | 16 |
| REV_DRV_OPEN_LOOP_ACCEL_A2 | ACTIVE_BRAKE_CURRENT_LIMIT |        |    |        | ACTIVE_BRAKE_KP            |                 |    |
| R/W-0h                     |                            | R/W-0h |    |        |                            | R/W-0h          |    |
| 15                         | 14                         | 13     | 12 | 11     | 10                         | 9               | 8  |
| ACTIVE_BRAKE_KP            |                            |        |    |        |                            | ACTIVE_BRAKE_KI |    |
| R/W-0h                     |                            |        |    | R/W-0h |                            |                 |    |
| 7                          | 6                          | 5      | 4  | 3      | 2                          | 1               | 0  |
| ACTIVE_BRAKE_KI            |                            |        |    |        |                            |                 |    |
| R/W-0h                     |                            |        |    |        |                            |                 |    |

**Table 7-17. REV\_DRIVE\_CONFIG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description  |
|-------|----------------------------|------|-------|--|
| 31    | RESERVED                   | R/W  | 0h    | Reserved   |
| 30-27 | REV_DRV_OPEN_LOOP_ACCEL_A1 | R/W  | 0h    | Open loop acceleration coefficient A1 during reverse drive<br>0h = 0.01 Hz/s<br>1h = 0.05 Hz/s<br>2h = 1 Hz/s<br>3h = 2.5 Hz/s<br>4h = 5 Hz/s<br>5h = 10 Hz/s<br>6h = 25 Hz/s<br>7h = 50 Hz/s<br>8h = 75 Hz/s<br>9h = 100 Hz/s<br>Ah = 250 Hz/s<br>Bh = 500 Hz/s<br>Ch = 750 Hz/s<br>Dh = 1000 Hz/s<br>Eh = 5000 Hz/s<br>Fh = 10000 Hz/s |



**Table 7-17. REV\_DRIVE\_CONFIG Register Field Descriptions (continued)**

| Bit   | Field                      | Type | Reset | Description   |
|-------|----------------------------|------|-------|---|
| 26-23 | REV_DRV_OPEN_LOOP_ACCEL_A2 | R/W  | 0h    | Open loop acceleration coefficient A2 during reverse drive<br>0h = 0.0 Hz/s <sup>2</sup><br>1h = 0.05 Hz/s <sup>2</sup><br>2h = 1 Hz/s <sup>2</sup><br>3h = 2.5 Hz/s <sup>2</sup><br>4h = 5 Hz/s <sup>2</sup><br>5h = 10 Hz/s <sup>2</sup><br>6h = 25 Hz/s <sup>2</sup><br>7h = 50 Hz/s <sup>2</sup><br>8h = 75 Hz/s <sup>2</sup><br>9h = 100 Hz/s <sup>2</sup><br>Ah = 250 Hz/s <sup>2</sup><br>Bh = 500 Hz/s <sup>2</sup><br>Ch = 750 Hz/s <sup>2</sup><br>Dh = 1000 Hz/s <sup>2</sup><br>Eh = 5000 Hz/s <sup>2</sup><br>Fh = 10000 Hz/s <sup>2</sup> |
| 22-20 | ACTIVE_BRAKE_CURRENT_LIMIT | R/W  | 0h    | Bus current limit during active braking<br>0h = 0.5 A<br>1h = 1 A<br>2h = 2 A<br>3h = 3 A<br>4h = 4 A<br>5h = 5 A<br>6h = 6 A<br>7h = 7 A   |
| 19-10 | ACTIVE_BRAKE_KP            | R/W  | 0h    | 10-bit value for active braking loop Kp. $K_p = \text{ACTIVE\_BRAKE\_KP} / 2^7$   |
| 9-0   | ACTIVE_BRAKE_KI            | R/W  | 0h    | 10-bit value for active braking loop Ki. $K_i = \text{ACTIVE\_BRAKE\_KI} / 2^9$   |

### 7.7.1.3 MOTOR\_STARTUP1 Register (Offset = 84h) [Reset = 0000000h]

MOTOR\_STARTUP1 is shown in [Figure 7-58](#) and described in [Table 7-18](#).

Return to the [Summary Table](#).

Register to configure motor startup settings<sup>1</sup>

**Figure 7-58. MOTOR\_STARTUP1 Register**

|               |             |              |                              |                  |            |                 |                |
|---------------|-------------|--------------|------------------------------|------------------|------------|-----------------|----------------|
| 31            | 30          | 29           | 28                           | 27               | 26         | 25              | 24             |
| RESERVED      | MTR_STARTUP |              | ALIGN_SLOW_RAMP_RATE         |                  |            | ALIGN_TIME      |                |
| R/W-0h        | R/W-0h      |              | R/W-0h                       |                  |            | R/W-0h          |                |
| 23            | 22          | 21           | 20                           | 19               | 18         | 17              | 16             |
| ALIGN_TIME    |             |              | ALIGN_OR_SLOW_CURRENT_ILIMIT |                  |            | IPD_CLK_FREQ    |                |
| R/W-0h        |             |              | R/W-0h                       |                  |            | R/W-0h          |                |
| 15            | 14          | 13           | 12                           | 11               | 10         | 9               | 8              |
| IPD_CLK_FREQ  |             | IPD_CURR_THR |                              |                  |            | IPD_RLS_MODE    |                |
| R/W-0h        |             | R/W-0h       |                              |                  |            | R/W-0h          |                |
| 7             | 6           | 5            | 4                            | 3                | 2          | 1               | 0              |
| IPD_ADV_ANGLE |             | IPD_REPEAT   |                              | OL_ILIMIT_CONFIG | IQ_RAMP_EN | ACTIVE_BRAKE_EN | REV_DRV_CONFIG |
| R/W-0h        |             | R/W-0h       |                              | R/W-0h           | R/W-0h     | R/W-0h          | R/W-0h         |

**Table 7-18. MOTOR\_STARTUP1 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description   |
|-------|----------------------|------|-------|---|
| 31    | RESERVED             | R/W  | 0h    | Reserved  |
| 30-29 | MTR_STARTUP          | R/W  | 0h    | Motor start-up method<br>0h = Align<br>1h = Double Align<br>2h = IPD<br>3h = Slow first cycle   |
| 28-25 | ALIGN_SLOW_RAMP_RATE | R/W  | 0h    | Align, slow first cycle and open loop current ramp rate<br>0h = 0.1 A/s<br>1h = 1 A/s<br>2h = 5 A/s<br>3h = 10 A/s<br>4h = 15 A/s<br>5h = 25 A/s<br>6h = 50 A/s<br>7h = 100 A/s<br>8h = 150 A/s<br>9h = 200 A/s<br>Ah = 250 A/s<br>Bh = 500 A/s<br>Ch = 1000 A/s<br>Dh = 2000 A/s<br>Eh = 5000 A/s<br>Fh = No Limit A/s |

**Table 7-18. MOTOR\_STARTUP1 Register Field Descriptions (continued)**

| Bit   | Field                            | Type | Reset | Description  |
|-------|----------------------------------|------|-------|--|
| 24-21 | ALIGN_TIME                       | R/W  | 0h    | Align time<br>0h = 10 ms<br>1h = 50 ms<br>2h = 100 ms<br>3h = 200 ms<br>4h = 300 ms<br>5h = 400 ms<br>6h = 500 ms<br>7h = 750 ms<br>8h = 1 s<br>9h = 1.5 s<br>Ah = 2 s<br>Bh = 3 s<br>Ch = 4 s<br>Dh = 5 s<br>Eh = 7.5 s<br>Fh = 10 s                                      |
| 20-17 | ALIGN_OR_SLOW_CUR<br>RENT_ILIMIT | R/W  | 0h    | Align or slow first cycle current limit<br>0h = 0.125 A<br>1h = 0.25 A<br>2h = 0.5 A<br>3h = 1.0 A<br>4h = 1.5 A<br>5h = 2.0 A<br>6h = 2.5 A<br>7h = 3.0 A<br>8h = 3.5 A<br>9h = 4.0 A<br>Ah = 4.5 A<br>Bh = 5.0 A<br>Ch = 5.5 A<br>Dh = 6.0 A<br>Eh = 7.0 A<br>Fh = 8.0 A |
| 16-14 | IPD_CLK_FREQ                     | R/W  | 0h    | IPD Clock Frequency<br>0h = 50 Hz<br>1h = 100 Hz<br>2h = 250 Hz<br>3h = 500 Hz<br>4h = 1000 Hz<br>5h = 2000 Hz<br>6h = 5000 Hz<br>7h = 10000 Hz  |

**Table 7-18. MOTOR\_STARTUP1 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description  |
|------|------------------|------|-------|--|
| 13-9 | IPD_CURR_THR     | R/W  | 0h    | IPD Current Threshold<br>0h = 0.25 A<br>1h = 0.5 A<br>2h = 0.75 A<br>3h = 1.0 A<br>4h = 1.25 A<br>5h = 1.5 A<br>6h = 2.0 A<br>7h = 2.5 A<br>8h = 3.0 A<br>9h = 3.667 A<br>Ah = 4.0 A<br>Bh = 4.667 A<br>Ch = 5.0 A<br>Dh = 5.333 A<br>Eh = 6.0 A<br>Fh = 6.667 A<br>10h = 7.333 A<br>11h = 8.0 A<br>12h = Not Applicable<br>13h = Not Applicable<br>14h = Not Applicable<br>15h = Not Applicable<br>16h = Not Applicable<br>17h = Not Applicable<br>18h = Not Applicable<br>19h = Not Applicable<br>1Ah = Not Applicable<br>1Bh = Not Applicable<br>1Ch = Not Applicable<br>1Dh = Not Applicable<br>1Eh = Not Applicable<br>1Fh = Not Applicable |
| 8    | IPD_RLS_MODE     | R/W  | 0h    | IPD release mode<br>0h = Brake<br>1h = Tristate  |
| 7-6  | IPD_ADV_ANGLE    | R/W  | 0h    | IPD advance angle<br>0h = 0°<br>1h = 30°<br>2h = 60°<br>3h = 90°   |
| 5-4  | IPD_REPEAT       | R/W  | 0h    | Number of times IPD is executed<br>0h = 1 time<br>1h = 2 times<br>2h = 3 times<br>3h = 4 times   |
| 3    | OL_ILIMIT_CONFIG | R/W  | 0h    | Open loop current limit configuration<br>0h = Open loop current limit defined by OL_ILIMIT<br>1h = Open loop current limit defined by ILIMIT   |
| 2    | IQ_RAMP_EN       | R/W  | 0h    | Iq ramp down for transition from open loop to closed loop<br>0h = Disable Iq ramp down<br>1h = Enable Iq ramp down   |
| 1    | ACTIVE_BRAKE_EN  | R/W  | 0h    | Enables active braking during deceleration<br>0h = Disable Active Brake<br>1h = Enable Active Brake  |
| 0    | REV_DRV_CONFIG   | R/W  | 0h    | Choose between forward and reverse drive setting for reverse drive<br>0h = Open loop current, A1, A2 based on forward drive<br>1h = Open loop current, A1, A2 based on reverse drive   |

### 7.7.1.4 MOTOR\_STARTUP2 Register (Offset = 86h) [Reset = 0000000h]

MOTOR\_STARTUP2 is shown in [Figure 7-59](#) and described in [Table 7-19](#).

Return to the [Summary Table](#).

Register to configure motor startup settings2

**Figure 7-59. MOTOR\_STARTUP2 Register**

|                         |           |        |    |                          |                           |                        |    |
|-------------------------|-----------|--------|----|--------------------------|---------------------------|------------------------|----|
| 31                      | 30        | 29     | 28 | 27                       | 26                        | 25                     | 24 |
| RESERVED                | OL_ILIMIT |        |    |                          | OL_ACC_A1                 |                        |    |
| R/W-0h                  |           | R/W-0h |    |                          |                           | R/W-0h                 |    |
| 23                      | 22        | 21     | 20 | 19                       | 18                        | 17                     | 16 |
| OL_ACC_A1               | OL_ACC_A2 |        |    |                          | AUTO_HAN<br>DO_FF_EN      | OPN_CL_HAN<br>DOFF_THR |    |
| R/W-0h                  |           | R/W-0h |    |                          |                           | R/W-0h                 |    |
| 15                      | 14        | 13     | 12 | 11                       | 10                        | 9                      | 8  |
| OPN_CL_HAN<br>DOFF_THR  |           |        |    | ALIGN_ANGLE              |                           |                        |    |
| R/W-0h                  |           |        |    | R/W-0h                   |                           |                        |    |
| 7                       | 6         | 5      | 4  | 3                        | 2                         | 1                      | 0  |
| SLOW_FIRST_C<br>YC_FREQ |           |        |    | FIRST_CYCLE<br>_FREQ_SEL | THETA_ERROR_R<br>AMP_RATE |                        |    |
| R/W-0h                  |           |        |    | R/W-0h                   |                           | R/W-0h                 |    |

**Table 7-19. MOTOR\_STARTUP2 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description  |
|-------|-----------|------|-------|--|
| 31    | RESERVED  | R/W  | 0h    | Reserved   |
| 30-27 | OL_ILIMIT | R/W  | 0h    | Open Loop current limit<br>0h = 0.125 A<br>1h = 0.25 A<br>2h = 0.5 A<br>3h = 1.0 A<br>4h = 1.5 A<br>5h = 2.0 A<br>6h = 2.5 A<br>7h = 3.0 A<br>8h = 3.5 A<br>9h = 4.0 A<br>Ah = 4.5 A<br>Bh = 5.0 A<br>Ch = 5.5 A<br>Dh = 6.0 A<br>Eh = 7.0 A<br>Fh = 8.0 A |

**Table 7-19. MOTOR\_STARTUP2 Register Field Descriptions (continued)**

| Bit   | Field           | Type | Reset | Description  |
|-------|-----------------|------|-------|--|
| 26-23 | OL_ACC_A1       | R/W  | 0h    | Open loop acceleration coefficient A1<br>0h = 0.01 Hz/s<br>1h = 0.05 Hz/s<br>2h = 1 Hz/s<br>3h = 2.5 Hz/s<br>4h = 5 Hz/s<br>5h = 10 Hz/s<br>6h = 25 Hz/s<br>7h = 50 Hz/s<br>8h = 75 Hz/s<br>9h = 100 Hz/s<br>Ah = 250 Hz/s<br>Bh = 500 Hz/s<br>Ch = 750 Hz/s<br>Dh = 1000 Hz/s<br>Eh = 5000 Hz/s<br>Fh = 10000 Hz/s  |
| 22-19 | OL_ACC_A2       | R/W  | 0h    | Open loop acceleration coefficient A2<br>0h = 0.0 Hz/s <sup>2</sup><br>1h = 0.05 Hz/s <sup>2</sup><br>2h = 1 Hz/s <sup>2</sup><br>3h = 2.5 Hz/s <sup>2</sup><br>4h = 5 Hz/s <sup>2</sup><br>5h = 10 Hz/s <sup>2</sup><br>6h = 25 Hz/s <sup>2</sup><br>7h = 50 Hz/s <sup>2</sup><br>8h = 75 Hz/s <sup>2</sup><br>9h = 100 Hz/s <sup>2</sup><br>Ah = 250 Hz/s <sup>2</sup><br>Bh = 500 Hz/s <sup>2</sup><br>Ch = 750 Hz/s <sup>2</sup><br>Dh = 1000 Hz/s <sup>2</sup><br>Eh = 5000 Hz/s <sup>2</sup><br>Fh = 10000 Hz/s <sup>2</sup> |
| 18    | AUTO_HANDOFF_EN | R/W  | 0h    | Auto Handoff Enable<br>0h = Disable Auto Handoff (and use OPN_CL_HANDOFF_THR)<br>1h = Enable Auto Handoff  |

**Table 7-19. MOTOR\_STARTUP2 Register Field Descriptions (continued)**

| Bit   | Field              | Type | Reset | Description   |
|-------|--------------------|------|-------|---|
| 17-13 | OPN_CL_HANDOFF_THR | R/W  | 0h    | Open to closed loop handoff threshold (% of MAX_SPEED)<br>0h = 1%<br>1h = 2%<br>2h = 3%<br>3h = 4%<br>4h = 5%<br>5h = 6%<br>6h = 7%<br>7h = 8%<br>8h = 9%<br>9h = 10%<br>Ah = 11%<br>Bh = 12%<br>Ch = 13%<br>Dh = 14%<br>Eh = 15%<br>Fh = 16%<br>10h = 17%<br>11h = 18%<br>12h = 19%<br>13h = 20%<br>14h = 22.5%<br>15h = 25%<br>16h = 27.5%<br>17h = 30%<br>18h = 32.5%<br>19h = 35%<br>1Ah = 37.5%<br>1Bh = 40%<br>1Ch = 42.5%<br>1Dh = 45%<br>1Eh = 47.5%<br>1Fh = 50% |

**Table 7-19. MOTOR\_STARTUP2 Register Field Descriptions (continued)**

| Bit  | Field                    | Type | Reset | Description  |
|------|--------------------------|------|-------|--|
| 12-8 | ALIGN_ANGLE              | R/W  | 0h    | Align angle<br>0h = 0 deg<br>1h = 10 deg<br>2h = 20 deg<br>3h = 30 deg<br>4h = 45 deg<br>5h = 60 deg<br>6h = 70 deg<br>7h = 80 deg<br>8h = 90 deg<br>9h = 110 deg<br>Ah = 120 deg<br>Bh = 135 deg<br>Ch = 150 deg<br>Dh = 160 deg<br>Eh = 170 deg<br>Fh = 180 deg<br>10h = 190 deg<br>11h = 210 deg<br>12h = 225 deg<br>13h = 240 deg<br>14h = 250 deg<br>15h = 260 deg<br>16h = 270 deg<br>17h = 280 deg<br>18h = 290 deg<br>19h = 315 deg<br>1Ah = 330 deg<br>1Bh = 340 deg<br>1Ch = 350 deg<br>1Dh = Reserved<br>1Eh = Reserved<br>1Fh = Reserved |
| 7-4  | SLOW_FIRST_CYC_FREQ<br>Q | R/W  | 0h    | Frequency of first cycle during start-up (% of MAX_SPEED)<br>0h = 1%<br>1h = 2%<br>2h = 3%<br>3h = 5%<br>4h = 7.5%<br>5h = 10%<br>6h = 12.5%<br>7h = 15%<br>8h = 17.5%<br>9h = 20%<br>Ah = 25%<br>Bh = 30%<br>Ch = 35%<br>Dh = 40%<br>Eh = 45%<br>Fh = 50%   |
| 3    | FIRST_CYCLE_FREQ_S<br>EL | R/W  | 0h    | First cycle frequency in open loop for align, double align and IPD start-up<br>0h = 0 Hz<br>1h = Defined by SLOW_FIRST_CYC_FREQ  |



**Table 7-19. MOTOR\_STARTUP2 Register Field Descriptions (continued)**

| Bit | Field                 | Type | Reset | Description  |
|-----|-----------------------|------|-------|--|
| 2-0 | THETA_ERROR_RAMP_RATE | R/W  | 0h    | Ramp rate for reducing difference between estimated theta and open loop theta<br>0h = 0.01 deg/ms<br>1h = 0.05 deg/ms<br>2h = 0.1 deg/ms<br>3h = 0.15 deg/ms<br>4h = 0.2 deg / ms<br>5h = 0.5 deg/ms<br>6h = 1 deg/ms<br>7h = 2 deg/ms |

### 7.7.1.5 CLOSED\_LOOP1 Register (Offset = 88h) [Reset = 0000000h]

CLOSED\_LOOP1 is shown in [Figure 7-60](#) and described in [Table 7-20](#).

Return to the [Summary Table](#).

Register to configure close loop settings1

**Figure 7-60. CLOSED\_LOOP1 Register**

|              |  |                       |  |        |  |    |  |              |  |                  |  |                |  |          |  |
|--------------|--|-----------------------|--|--------|--|----|--|--------------|--|------------------|--|----------------|--|----------|--|
| 31           |  | 30                    |  | 29     |  | 28 |  | 27           |  | 26               |  | 25             |  | 24       |  |
| RESERVED     |  | OVERMODULATION_ENABLE |  | CL_ACC |  |    |  |              |  |                  |  | CL_DEC_CONFIG  |  |          |  |
| R/W-0h       |  | R/W-0h                |  | R/W-0h |  |    |  |              |  |                  |  | R/W-0h         |  |          |  |
| 23           |  | 22                    |  | 21     |  | 20 |  | 19           |  | 18               |  | 17             |  | 16       |  |
| CL_DEC       |  |                       |  |        |  |    |  | PWM_FREQ_OUT |  |                  |  |                |  |          |  |
| R/W-0h       |  |                       |  |        |  |    |  | R/W-0h       |  |                  |  |                |  |          |  |
| 15           |  | 14                    |  | 13     |  | 12 |  | 11           |  | 10               |  | 9              |  | 8        |  |
| PWM_FREQ_OUT |  | PWM_MODE              |  | FG_SEL |  |    |  | FG_DIV       |  |                  |  |                |  |          |  |
| R/W-0h       |  | R/W-0h                |  | R/W-0h |  |    |  | R/W-0h       |  |                  |  |                |  |          |  |
| 7            |  | 6                     |  | 5      |  | 4  |  | 3            |  | 2                |  | 1              |  | 0        |  |
| FG_CONFIG    |  | FG_BEMF_THR           |  |        |  |    |  | AVS_EN       |  | DEADTIME_COMP_EN |  | SPEED_LOOP_DIS |  | RESERVED |  |
| R/W-0h       |  | R/W-0h                |  |        |  |    |  | R/W-0h       |  | R/W-0h           |  | R/W-0h         |  | R/W-0h   |  |

**Table 7-20. CLOSED\_LOOP1 Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description  |
|-----|-----------------------|------|-------|--|
| 31  | RESERVED              | R/W  | 0h    | Reserved   |
| 30  | OVERMODULATION_ENABLE | R/W  | 0h    | Enable overmodulation<br>0h = Disable overmodulation<br>1h = Enable overmodulation |

**Table 7-20. CLOSED\_LOOP1 Register Field Descriptions (continued)**

| Bit   | Field         | Type | Reset | Description  |
|-------|---------------|------|-------|--|
| 29-25 | CL_ACC        | R/W  | 0h    | Closed loop acceleration<br>0h = 0.5 Hz/s<br>1h = 1 Hz/s<br>2h = 2.5 Hz/s<br>3h = 5 Hz/s<br>4h = 7.5 Hz/s<br>5h = 10 Hz/s<br>6h = 20 Hz/s<br>7h = 40 Hz/s<br>8h = 60 Hz/s<br>9h = 80 Hz/s<br>Ah = 100 Hz/s<br>Bh = 200 Hz/s<br>Ch = 300 Hz/s<br>Dh = 400 Hz/s<br>Eh = 500 Hz/s<br>Fh = 600 Hz/s<br>10h = 700 Hz/s<br>11h = 800 Hz/s<br>12h = 900 Hz/s<br>13h = 1000 Hz/s<br>14h = 2000 Hz/s<br>15h = 4000 Hz/s<br>16h = 6000 Hz/s<br>17h = 8000 Hz/s<br>18h = 10000 Hz/s<br>19h = 20000 Hz/s<br>1Ah = 30000 Hz/s<br>1Bh = 40000 Hz/s<br>1Ch = 50000 Hz/s<br>1Dh = 60000 Hz/s<br>1Eh = 70000 Hz/s<br>1Fh = No limit |
| 24    | CL_DEC_CONFIG | R/W  | 0h    | Closed loop deceleration configuration<br>0h = Closed loop deceleration defined by CL_DEC<br>1h = Closed loop deceleration defined by CL_ACC   |

**Table 7-20. CLOSED\_LOOP1 Register Field Descriptions (continued)**

| Bit   | Field        | Type | Reset | Description  |
|-------|--------------|------|-------|--|
| 23-19 | CL_DEC       | R/W  | 0h    | <p>Closed loop deceleration. This setting is used only if AVS is disabled and CL_DEC_CONFIG is set to 0b</p> <p>0h = 0.5 Hz/s<br/>                     1h = 1 Hz/s<br/>                     2h = 2.5 Hz/s<br/>                     3h = 5 Hz/s<br/>                     4h = 7.5 Hz/s<br/>                     5h = 10 Hz/s<br/>                     6h = 20 Hz/s<br/>                     7h = 40 Hz/s<br/>                     8h = 60 Hz/s<br/>                     9h = 80 Hz/s<br/>                     Ah = 100 Hz/s<br/>                     Bh = 200 Hz/s<br/>                     Ch = 300 Hz/s<br/>                     Dh = 400 Hz/s<br/>                     Eh = 500 Hz/s<br/>                     Fh = 600 Hz/s<br/>                     10h = 700 Hz/s<br/>                     11h = 800 Hz/s<br/>                     12h = 900 Hz/s<br/>                     13h = 1000 Hz/s<br/>                     14h = 2000 Hz/s<br/>                     15h = 4000 Hz/s<br/>                     16h = 6000 Hz/s<br/>                     17h = 8000 Hz/s<br/>                     18h = 10000 Hz/s<br/>                     19h = 20000 Hz/s<br/>                     1Ah = 30000 Hz/s<br/>                     1Bh = 40000 Hz/s<br/>                     1Ch = 50000 Hz/s<br/>                     1Dh = 60000 Hz/s<br/>                     1Eh = 70000 Hz/s<br/>                     1Fh = No limit</p> |
| 18-15 | PWM_FREQ_OUT | R/W  | 0h    | <p>PWM output frequency</p> <p>0h = 10 kHz<br/>                     1h = 15 kHz<br/>                     2h = 20 kHz<br/>                     3h = 25 kHz<br/>                     4h = 30 kHz<br/>                     5h = 35 kHz<br/>                     6h = 40 kHz<br/>                     7h = 45 kHz<br/>                     8h = 50 kHz<br/>                     9h = 55 kHz<br/>                     Ah = 60 kHz<br/>                     Bh = Not Applicable<br/>                     Ch = Not Applicable<br/>                     Dh = Not Applicable<br/>                     Eh = Not Applicable<br/>                     Fh = Not Applicable</p>  |
| 14    | PWM_MODE     | R/W  | 0h    | <p>PWM modulation</p> <p>0h = Continuous Space Vector Modulation<br/>                     1h = Discontinuous Space Vector Modulation</p>   |
| 13-12 | FG_SEL       | R/W  | 0h    | <p>FG select</p> <p>0h = Output FG in open loop and closed loop<br/>                     1h = Output FG in only closed loop<br/>                     2h = Output FG in open loop for the first motor run after power-up/wake-up<br/>                     3h = Not Applicable</p>   |

**Table 7-20. CLOSED\_LOOP1 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description  |
|------|------------------|------|-------|--|
| 11-8 | FG_DIV           | R/W  | 0h    | FG Division factor<br>0h = Divide by 1 (2-pole motor mechanical speed)<br>1h = Divide by 1 (2-pole motor mechanical speed)<br>2h = Divide by 2 (4-pole motor mechanical speed)<br>3h = Divide by 3 (6-pole motor mechanical speed)<br>4h = Divide by 4 (8-pole motor mechanical speed) ...<br>Fh = Divide by 15 (30-pole motor mechanical speed) |
| 7    | FG_CONFIG        | R/W  | 0h    | FG output configuration<br>0h = FG active as long as motor is driven<br>1h = FG active till BEMF drops below BEMF threshold defined by FG_BEMF_THR   |
| 6-4  | FG_BEMF_THR      | R/W  | 0h    | FG output BEMF threshold<br>0h = +/- 1mV<br>1h = +/- 2mV<br>2h = +/- 5mV<br>3h = +/- 10mV<br>4h = +/- 20mV<br>5h = +/- 30mV<br>6h = Not Applicable<br>7h = Not Applicable  |
| 3    | AVS_EN           | R/W  | 0h    | AVS enable<br>0h = Disable<br>1h = Enable  |
| 2    | DEADTIME_COMP_EN | R/W  | 0h    | Deadtime compensation enable<br>0h = Disable<br>1h = Enable  |
| 1    | SPEED_LOOP_DIS   | R/W  | 0h    | Speed loop disable (or torque mode enable)<br>0h = Speed loop enable (Torque mode disable)<br>1h = Speed loop disable (Torque mode enable)   |
| 0    | RESERVED         | R/W  | 0h    | Reserved   |

### 7.7.1.6 CLOSED\_LOOP2 Register (Offset = 8Ah) [Reset = 0000000h]

CLOSED\_LOOP2 is shown in [Figure 7-61](#) and described in [Table 7-21](#).

Return to the [Summary Table](#).

Register to configure close loop settings2

**Figure 7-61. CLOSED\_LOOP2 Register**

|              |          |        |    |                       |        |    |    |
|--------------|----------|--------|----|-----------------------|--------|----|----|
| 31           | 30       | 29     | 28 | 27                    | 26     | 25 | 24 |
| RESERVED     | MTR_STOP |        |    | MTR_STOP_BRK_TIME     |        |    |    |
| R/W-0h       |          | R/W-0h |    |                       | R/W-0h |    |    |
| 23           | 22       | 21     | 20 | 19                    | 18     | 17 | 16 |
| ACT_SPIN_THR |          |        |    | BRAKE_SPEED_THRESHOLD |        |    |    |
| R/W-0h       |          |        |    | R/W-0h                |        |    |    |
| 15           | 14       | 13     | 12 | 11                    | 10     | 9  | 8  |
| MOTOR_RES    |          |        |    |                       |        |    |    |
| R/W-0h       |          |        |    |                       |        |    |    |
| 7            | 6        | 5      | 4  | 3                     | 2      | 1  | 0  |
| MOTOR_IND    |          |        |    |                       |        |    |    |
| R/W-0h       |          |        |    |                       |        |    |    |

**Table 7-21. CLOSED\_LOOP2 Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description   |
|-------|-------------------|------|-------|---|
| 31    | RESERVED          | R/W  | 0h    | Reserved  |
| 30-28 | MTR_STOP          | R/W  | 0h    | Motor stop options<br>0h = Hi-Z<br>1h = Not Applicable<br>2h = Low side braking<br>3h = High side braking<br>4h = Active spin down<br>5h = Align braking<br>6h = Not Defined<br>7h = Not Defined  |
| 27-24 | MTR_STOP_BRK_TIME | R/W  | 0h    | Brake time during motor stop<br>0h = 1 ms<br>1h = 1 ms<br>2h = 1 ms<br>3h = 1 ms<br>4h = 1 ms<br>5h = 5 ms<br>6h = 10 ms<br>7h = 50 ms<br>8h = 100 ms<br>9h = 250 ms<br>Ah = 500 ms<br>Bh = 1000 ms<br>Ch = 2500 ms<br>Dh = 5000 ms<br>Eh = 10000 ms<br>Fh = 15000 ms |

**Table 7-21. CLOSED\_LOOP2 Register Field Descriptions (continued)**

| Bit   | Field                     | Type | Reset | Description  |
|-------|---------------------------|------|-------|--|
| 23-20 | ACT_SPIN_THR              | R/W  | 0h    | Speed threshold for active spin down (% of MAX_SPEED)<br>0h = 100 %<br>1h = 90 %<br>2h = 80 %<br>3h = 70 %<br>4h = 60%<br>5h = 50 %<br>6h = 45 %<br>7h = 40 %<br>8h = 35 %<br>9h = 30 %<br>Ah = 25 %<br>Bh = 20 %<br>Ch = 15 %<br>Dh = 10 %<br>Eh = 5 %<br>Fh = 2.5 %  |
| 19-16 | BRAKE_SPEED_THRES<br>HOLD | R/W  | 0h    | Speed threshold for BRAKE pin and motor stop options (Low side Braking or High Side Braking or Align Braking) (% of MAX_SPEED)<br>0h = 100 %<br>1h = 90 %<br>2h = 80 %<br>3h = 70 %<br>4h = 60%<br>5h = 50 %<br>6h = 45 %<br>7h = 40 %<br>8h = 35 %<br>9h = 30 %<br>Ah = 25 %<br>Bh = 20 %<br>Ch = 15 %<br>Dh = 10 %<br>Eh = 5 %<br>Fh = 2.5 % |
| 15-8  | MOTOR_RES                 | R/W  | 0h    | 8-bit values for motor phase resistance See <a href="#">Table 7-2</a> for values of phase resistance   |
| 7-0   | MOTOR_IND                 | R/W  | 0h    | 8-bit values for motor phase inductance See <a href="#">Table 7-3</a> for values of phase inductance   |

### 7.7.1.7 CLOSED\_LOOP3 Register (Offset = 8Ch) [Reset = 0000000h]

CLOSED\_LOOP3 is shown in [Figure 7-62](#) and described in [Table 7-22](#).

Return to the [Summary Table](#).

Register to configure close loop settings3

**Figure 7-62. CLOSED\_LOOP3 Register**

|                  |    |                  |              |             |    |    |    |
|------------------|----|------------------|--------------|-------------|----|----|----|
| 31               | 30 | 29               | 28           | 27          | 26 | 25 | 24 |
| RESERVED         |    | MOTOR_BEMF_CONST |              |             |    |    |    |
| R/W-0h           |    | R/W-0h           |              |             |    |    |    |
| 23               | 22 | 21               | 20           | 19          | 18 | 17 | 16 |
| MOTOR_BEMF_CONST |    | CURR_LOOP_KP     |              |             |    |    |    |
| R/W-0h           |    | R/W-0h           |              |             |    |    |    |
| 15               | 14 | 13               | 12           | 11          | 10 | 9  | 8  |
| CURR_LOOP_KP     |    |                  | CURR_LOOP_KI |             |    |    |    |
| R/W-0h           |    |                  | R/W-0h       |             |    |    |    |
| 7                | 6  | 5                | 4            | 3           | 2  | 1  | 0  |
| CURR_LOOP_KI     |    |                  |              | SPD_LOOP_KP |    |    |    |
| R/W-0h           |    |                  |              | R/W-0h      |    |    |    |

**Table 7-22. CLOSED\_LOOP3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description   |
|-------|------------------|------|-------|---|
| 31    | RESERVED         | R/W  | 0h    | Reserved  |
| 30-23 | MOTOR_BEMF_CONST | R/W  | 0h    | 8-bit values for motor BEMF Constant See <a href="#">Table 7-4</a> for values of BEMF constant  |
| 22-13 | CURR_LOOP_KP     | R/W  | 0h    | 10-bit value for current Iq and Id loop Kp. CURR_LOOP_KP is divided in 2 sections, SCALE(9:8) and VALUE(7:0). $K_p = \text{VALUE} / 10^{\text{SCALE}}$ . Please set to 0 for auto calculation of current Kp and Ki        |
| 12-3  | CURR_LOOP_KI     | R/W  | 0h    | 10-bit value for current Iq and Id loop Ki. CURR_LOOP_KI is divided in 2 sections, SCALE(9:8) and VALUE(7:0). $K_i = 1000 * \text{VALUE} / 10^{\text{SCALE}}$ . Please set to 0 for auto calculation of current Kp and Ki |
| 2-0   | SPD_LOOP_KP      | R/W  | 0h    | 3 MSB bits for speed loop Kp. SPD_LOOP_KP is divided in 2 sections, SCALE(9:8) and VALUE(7:0). $K_p = 0.01 * \text{VALUE} / 10^{\text{SCALE}}$ .  |



### 7.7.1.8 CLOSED\_LOOP4 Register (Offset = 8Eh) [Reset = 0000000h]

CLOSED\_LOOP4 is shown in [Figure 7-63](#) and described in [Table 7-23](#).

Return to the [Summary Table](#).

Register to configure close loop settings4

**Figure 7-63. CLOSED\_LOOP4 Register**

|             |    |             |    |    |    |    |    |
|-------------|----|-------------|----|----|----|----|----|
| 31          | 30 | 29          | 28 | 27 | 26 | 25 | 24 |
| RESERVED    |    | SPD_LOOP_KP |    |    |    |    |    |
| R/W-0h      |    | R/W-0h      |    |    |    |    |    |
| 23          | 22 | 21          | 20 | 19 | 18 | 17 | 16 |
| SPD_LOOP_KI |    |             |    |    |    |    |    |
| R/W-0h      |    |             |    |    |    |    |    |
| 15          | 14 | 13          | 12 | 11 | 10 | 9  | 8  |
| SPD_LOOP_KI |    | MAX_SPEED   |    |    |    |    |    |
| R/W-0h      |    | R/W-0h      |    |    |    |    |    |
| 7           | 6  | 5           | 4  | 3  | 2  | 1  | 0  |
| MAX_SPEED   |    |             |    |    |    |    |    |
| R/W-0h      |    |             |    |    |    |    |    |

**Table 7-23. CLOSED\_LOOP4 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description   |
|-------|-------------|------|-------|---|
| 31    | RESERVED    | R/W  | 0h    | Reserved  |
| 30-24 | SPD_LOOP_KP | R/W  | 0h    | 7 LSB bits for speed loop Kp. SPD_LOOP_KP is divided in 2 sections, SCALE(10:9) and VALUE(8:0). $K_p = 0.01 * VALUE / 10^{SCALE}$ .   |
| 23-14 | SPD_LOOP_KI | R/W  | 0h    | 10 bit value for speed loop Ki. SPD_LOOP_KI is divided in 2 sections, SCALE(9:8) and VALUE(7:0). $K_i = 0.1 * VALUE / 10^{SCALE}$ .   |
| 13-0  | MAX_SPEED   | R/W  | 0h    | 14-bit value for setting maximum value of speed in electrical Hz<br>Maximum motor electrical speed (Hz): {MOTOR_SPEED/6} For example: if MOTOR_SPEED is 0x2710, then maximum motor speed (Hz) = 10000(0x2710)/6 = 1666 Hz |

### 7.7.1.9 REF\_PROFILES1 Register (Offset = 94h) [Reset = 0000000h]

REF\_PROFILES1 is shown in [Figure 7-64](#) and described in [Table 7-24](#).

Return to the [Summary Table](#).

Register to configure reference profile1

**Figure 7-64. REF\_PROFILES1 Register**

|             |                    |        |             |          |        |    |    |  |
|-------------|--------------------|--------|-------------|----------|--------|----|----|--|
| 31          | 30                 | 29     | 28          | 27       | 26     | 25 | 24 |  |
| RESERVED    | REF_PROFILE_CONFIG |        |             | DUTY_ON1 |        |    |    |  |
| R/W-0h      |                    | R/W-0h |             |          | R/W-0h |    |    |  |
| 23          | 22                 | 21     | 20          | 19       | 18     | 17 | 16 |  |
| DUTY_ON1    |                    |        | DUTY_OFF1   |          |        |    |    |  |
| R/W-0h      |                    |        | R/W-0h      |          |        |    |    |  |
| 15          | 14                 | 13     | 12          | 11       | 10     | 9  | 8  |  |
| DUTY_OFF1   |                    |        | DUTY_CLAMP1 |          |        |    |    |  |
| R/W-0h      |                    |        | R/W-0h      |          |        |    |    |  |
| 7           | 6                  | 5      | 4           | 3        | 2      | 1  | 0  |  |
| DUTY_CLAMP1 |                    |        | DUTY_A      |          |        |    |    |  |
| R/W-0h      |                    |        | R/W-0h      |          |        |    |    |  |

**Table 7-24. REF\_PROFILES1 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description  |
|-------|--------------------|------|-------|--|
| 31    | RESERVED           | R/W  | 0h    | Reserved   |
| 30-29 | REF_PROFILE_CONFIG | R/W  | 0h    | Configuration for Reference profiles<br>0h = Reference/Equation<br>1h = Linear Profile<br>2h = Staircase Profile<br>3h = Forward-Reverse Profile |
| 28-21 | DUTY_ON1           | R/W  | 0h    | Turn On Duty Cycle (%) = $\{(DUTY\_ON1/255)*100\}$   |
| 20-13 | DUTY_OFF1          | R/W  | 0h    | Turn Off Duty Cycle (%) = $\{(DUTY\_OFF1/255)*100\}$   |
| 12-5  | DUTY_CLAMP1        | R/W  | 0h    | Duty Cycle for clamping Duty Input (%) = $\{(DUTY\_CLAMP1/255)*100\}$  |
| 4-0   | DUTY_A             | R/W  | 0h    | 5 MSB bits for Duty Cycle A  |

### 7.7.1.10 REF\_PROFILES2 Register (Offset = 96h) [Reset = 0000000h]

REF\_PROFILES2 is shown in [Figure 7-65](#) and described in [Table 7-25](#).

Return to the [Summary Table](#).

Register to configure reference profile2

**Figure 7-65. REF\_PROFILES2 Register**

|          |        |        |    |        |        |    |    |  |
|----------|--------|--------|----|--------|--------|----|----|--|
| 31       | 30     | 29     | 28 | 27     | 26     | 25 | 24 |  |
| RESERVED | DUTY_A |        |    | DUTY_B |        |    |    |  |
| R/W-0h   |        | R/W-0h |    |        | R/W-0h |    |    |  |
| 23       | 22     | 21     | 20 | 19     | 18     | 17 | 16 |  |
| DUTY_B   |        |        |    | DUTY_C |        |    |    |  |
| R/W-0h   |        |        |    | R/W-0h |        |    |    |  |
| 15       | 14     | 13     | 12 | 11     | 10     | 9  | 8  |  |
| DUTY_C   |        |        |    | DUTY_D |        |    |    |  |
| R/W-0h   |        |        |    | R/W-0h |        |    |    |  |
| 7        | 6      | 5      | 4  | 3      | 2      | 1  | 0  |  |
| DUTY_D   |        |        |    | DUTY_E |        |    |    |  |
| R/W-0h   |        |        |    | R/W-0h |        |    |    |  |

**Table 7-25. REF\_PROFILES2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---|
| 31    | RESERVED | R/W  | 0h    | Reserved  |
| 30-28 | DUTY_A   | R/W  | 0h    | 3 LSB bits for Duty Cycle A. Duty Cycle A (%) = $\{(DUTY\_A/255)*100\}$ |
| 27-20 | DUTY_B   | R/W  | 0h    | Duty Cycle B (%) = $\{(DUTY\_B/255)*100\}$                              |
| 19-12 | DUTY_C   | R/W  | 0h    | Duty Cycle C (%) = $\{(DUTY\_C/255)*100\}$                              |
| 11-4  | DUTY_D   | R/W  | 0h    | Duty Cycle D (%) = $\{(DUTY\_D/255)*100\}$                              |
| 3-0   | DUTY_E   | R/W  | 0h    | 4 MSB bits for Duty Cycle E   |

### 7.7.1.11 REF\_PROFILES3 Register (Offset = 98h) [Reset = 0000000h]

REF\_PROFILES3 is shown in [Figure 7-66](#) and described in [Table 7-26](#).

Return to the [Summary Table](#).

Register to configure reference profile3

**Figure 7-66. REF\_PROFILES3 Register**

|             |        |    |    |             |          |          |        |
|-------------|--------|----|----|-------------|----------|----------|--------|
| 31          | 30     | 29 | 28 | 27          | 26       | 25       | 24     |
| RESERVED    | DUTY_E |    |    |             | DUTY_ON2 |          |        |
| R/W-0h      |        |    |    | R/W-0h      |          |          | R/W-0h |
| 23          | 22     | 21 | 20 | 19          | 18       | 17       | 16     |
| DUTY_ON2    |        |    |    | DUTY_OFF2   |          |          |        |
| R/W-0h      |        |    |    | R/W-0h      |          |          |        |
| 15          | 14     | 13 | 12 | 11          | 10       | 9        | 8      |
| DUTY_OFF2   |        |    |    | DUTY_CLAMP2 |          |          |        |
| R/W-0h      |        |    |    | R/W-0h      |          |          |        |
| 7           | 6      | 5  | 4  | 3           | 2        | 1        | 0      |
| DUTY_CLAMP2 |        |    |    | DUTY_HYS    |          | RESERVED |        |
| R/W-0h      |        |    |    | R/W-0h      |          | R/W-0h   |        |

**Table 7-26. REF\_PROFILES3 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description  |
|-------|-------------|------|-------|--|
| 31    | RESERVED    | R/W  | 0h    | Reserved   |
| 30-27 | DUTY_E      | R/W  | 0h    | 4 LSB bits for Duty Cycle E. Duty_E Configuration Duty Cycle E (%) = $\{(DUTY\_E/255)*100\}$ |
| 26-19 | DUTY_ON2    | R/W  | 0h    | Turn On Duty Cycle (%) = $\{(DUTY\_ON2/255)*100\}$   |
| 18-11 | DUTY_OFF2   | R/W  | 0h    | Turn Off Duty Cycle (%) = $\{(DUTY\_OFF2/255)*100\}$   |
| 10-3  | DUTY_CLAMP2 | R/W  | 0h    | Duty Cycle for clamping Duty Input(%) = $\{(DUTY\_CLAMP1/255)*100\}$                         |
| 2-1   | DUTY_HYS    | R/W  | 0h    | Duty hysteresis<br>0h = 0%<br>1h = 0.5%<br>2h = 1%<br>3h = 2%                                |
| 0     | RESERVED    | R/W  | 0h    | Reserved   |

### 7.7.1.12 REF\_PROFILES4 Register (Offset = 9Ah) [Reset = 0000000h]

REF\_PROFILES4 is shown in [Figure 7-67](#) and described in [Table 7-27](#).

Return to the [Summary Table](#).

Register to configure reference profile4

**Figure 7-67. REF\_PROFILES4 Register**

|            |            |    |    |        |    |    |    |
|------------|------------|----|----|--------|----|----|----|
| 31         | 30         | 29 | 28 | 27     | 26 | 25 | 24 |
| RESERVED   | REF_OFF1   |    |    |        |    |    |    |
| R/W-0h     |            |    |    | R/W-0h |    |    |    |
| 23         | 22         | 21 | 20 | 19     | 18 | 17 | 16 |
| REF_OFF1   | REF_CLAMP1 |    |    |        |    |    |    |
| R/W-0h     |            |    |    | R/W-0h |    |    |    |
| 15         | 14         | 13 | 12 | 11     | 10 | 9  | 8  |
| REF_CLAMP1 | REF_A      |    |    |        |    |    |    |
| R/W-0h     |            |    |    | R/W-0h |    |    |    |
| 7          | 6          | 5  | 4  | 3      | 2  | 1  | 0  |
| REF_A      | REF_B      |    |    |        |    |    |    |
| R/W-0h     |            |    |    | R/W-0h |    |    |    |

**Table 7-27. REF\_PROFILES4 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description   |
|-------|------------|------|-------|---|
| 31    | RESERVED   | R/W  | 0h    | Reserved  |
| 30-23 | REF_OFF1   | R/W  | 0h    | Turn off reference (% of Maximum Reference) = $\{(REF\_OFF1/255)*100\}$ |
| 22-15 | REF_CLAMP1 | R/W  | 0h    | Clamp Ref 1 (% of Maximum Reference) = $\{(REF\_CLAMP1/255)*100\}$      |
| 14-7  | REF_A      | R/W  | 0h    | Ref A (% of Maximum Reference) = $\{(REF\_A/255)*100\}$                 |
| 6-0   | REF_B      | R/W  | 0h    | 7 MSB of REF_B configuration  |

### 7.7.1.13 REF\_PROFILES5 Register (Offset = 9Ch) [Reset = 0000000h]

REF\_PROFILES5 is shown in [Figure 7-68](#) and described in [Table 7-28](#).

Return to the [Summary Table](#).

Register to configure reference profile5

**Figure 7-68. REF\_PROFILES5 Register**

|          |        |          |    |    |    |        |    |  |
|----------|--------|----------|----|----|----|--------|----|--|
| 31       | 30     | 29       | 28 | 27 | 26 | 25     | 24 |  |
| RESERVED | REF_B  |          |    |    |    | REF_C  |    |  |
| R/W-0h   | R/W-0h |          |    |    |    | R/W-0h |    |  |
| 23       | 22     | 21       | 20 | 19 | 18 | 17     | 16 |  |
| REF_C    |        |          |    |    |    | REF_D  |    |  |
| R/W-0h   |        |          |    |    |    | R/W-0h |    |  |
| 15       | 14     | 13       | 12 | 11 | 10 | 9      | 8  |  |
| REF_D    |        |          |    |    |    | REF_E  |    |  |
| R/W-0h   |        |          |    |    |    | R/W-0h |    |  |
| 7        | 6      | 5        | 4  | 3  | 2  | 1      | 0  |  |
| REF_E    |        | RESERVED |    |    |    |        |    |  |
| R/W-0h   |        | R/W-0h   |    |    |    |        |    |  |

**Table 7-28. REF\_PROFILES5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--|
| 31    | RESERVED | R/W  | 0h    | Reserved   |
| 30    | REF_B    | R/W  | 0h    | 1 LSB of REF_B configuration. Ref B(% of Maximum Reference) = $\{(REF\_B/255)*100\}$ |
| 29-22 | REF_C    | R/W  | 0h    | Ref C (% of Maximum Reference) = $\{(REF\_C/255)*100\}$                              |
| 21-14 | REF_D    | R/W  | 0h    | Ref D (% of Maximum Reference) = $\{(REF\_D/255)*100\}$                              |
| 13-6  | REF_E    | R/W  | 0h    | Ref E(% of Maximum Reference) = $\{(REF\_E/255)*100\}$                               |
| 5-0   | RESERVED | R/W  | 0h    | Reserved   |

### 7.7.1.14 REF\_PROFILES6 Register (Offset = 9Eh) [Reset = 0000000h]

REF\_PROFILES6 is shown in [Figure 7-69](#) and described in [Table 7-29](#).

Return to the [Summary Table](#).

Register to configure reference profile6

**Figure 7-69. REF\_PROFILES6 Register**

|            |    |            |    |    |    |    |    |
|------------|----|------------|----|----|----|----|----|
| 31         | 30 | 29         | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    | REF_OFF2   |    |    |    |    |    |
| R/W-0h     |    | R/W-0h     |    |    |    |    |    |
| 23         | 22 | 21         | 20 | 19 | 18 | 17 | 16 |
| REF_OFF2   |    | REF_CLAMP2 |    |    |    |    |    |
| R/W-0h     |    | R/W-0h     |    |    |    |    |    |
| 15         | 14 | 13         | 12 | 11 | 10 | 9  | 8  |
| REF_CLAMP2 |    | RESERVED   |    |    |    |    |    |
| R/W-0h     |    | R/W-0h     |    |    |    |    |    |
| 7          | 6  | 5          | 4  | 3  | 2  | 1  | 0  |
| RESERVED   |    |            |    |    |    |    |    |
| R/W-0h     |    |            |    |    |    |    |    |

**Table 7-29. REF\_PROFILES6 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description  |
|-------|------------|------|-------|--|
| 31    | RESERVED   | R/W  | 0h    | Reserved   |
| 30-23 | REF_OFF2   | R/W  | 0h    | Turn off Ref (% of Maximum Reference) = $\{(REF\_OFF2/255)*100\}$  |
| 22-15 | REF_CLAMP2 | R/W  | 0h    | Clamp Ref 2 (% of Maximum Reference) = $\{(REF\_CLAMP2/255)*100\}$ |
| 14-0  | RESERVED   | R/W  | 0h    | Reserved   |

### 7.7.2 Fault\_Configuration Registers

[Table 7-30](#) lists the memory-mapped registers for the Fault\_Configuration registers. All register offset addresses not listed in [Table 7-30](#) should be considered as reserved locations and the register contents should not be modified.

**Table 7-30. FAULT\_CONFIGURATION Registers**

| Offset | Acronym       | Register Name        | Section            |
|--------|---------------|----------------------|--------------------|
| 90h    | FAULT_CONFIG1 | Fault Configuration1 | <a href="#">Go</a> |
| 92h    | FAULT_CONFIG2 | Fault Configuration2 | <a href="#">Go</a> |

Complex bit access types are encoded to fit into small table cells. [Table 7-31](#) shows the codes that are used for access types in this section.

**Table 7-31. Fault\_Configuration Access Type Codes**

| Access Type            | Code | Description |
|------------------------|------|-------------|
| Read Type              |      |             |
| R                      | R    | Read        |
| Write Type             |      |             |
| W                      | W    | Write       |
| Reset or Default Value |      |             |

**Table 7-31. Fault\_Configuration Access Type Codes  
(continued)**

| Access Type | Code | Description                            |
|-------------|------|--|
| <i>-n</i>   |      | Value after reset or the default value |



### 7.7.2.1 FAULT\_CONFIG1 Register (Offset = 90h) [Reset = 0000000h]

FAULT\_CONFIG1 is shown in [Figure 7-70](#) and described in [Table 7-32](#).

Return to the [Summary Table](#).

Register to configure fault settings1

**Figure 7-70. FAULT\_CONFIG1 Register**

|                  |                 |        |    |        |                      |                   |                     |
|------------------|-----------------|--------|----|--------|----------------------|-------------------|---------------------|
| 31               | 30              | 29     | 28 | 27     | 26                   | 25                | 24                  |
| RESERVED         | ILIMIT          |        |    |        | HW_LOCK_ILIMIT       |                   |                     |
| R/W-0h           |                 | R/W-0h |    |        |                      | R/W-0h            |                     |
| 23               | 22              | 21     | 20 | 19     | 18                   | 17                | 16                  |
| HW_LOCK_ILIMIT   | LOCK_ILIMIT     |        |    |        | LOCK_ILIMIT_MODE     |                   |                     |
| R/W-0h           |                 | R/W-0h |    |        |                      | R/W-0h            |                     |
| 15               | 14              | 13     | 12 | 11     | 10                   | 9                 | 8                   |
| LOCK_ILIMIT_MODE | LOCK_ILIMIT_DEG |        |    |        | LCK_RETRY            |                   |                     |
| R/W-0h           |                 | R/W-0h |    |        |                      | R/W-0h            |                     |
| 7                | 6               | 5      | 4  | 3      | 2                    | 1                 | 0                   |
| LCK_RETRY        | MTR_LCK_MODE    |        |    |        | IPD_TIMEOUT_FAULT_EN | IPD_FREQ_FAULT_EN | SATURATION_FLAGS_EN |
| R/W-0h           |                 | R/W-0h |    | R/W-0h |                      | R/W-0h            | R/W-0h              |

**Table 7-32. FAULT\_CONFIG1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--|
| 31    | RESERVED | R/W  | 0h    | Reserved   |
| 30-27 | ILIMIT   | R/W  | 0h    | Current limit for Iq axis (torque) current reference in closed loop<br>0h = 0.125 A<br>1h = 0.25 A<br>2h = 0.5 A<br>3h = 1.0 A<br>4h = 1.5 A<br>5h = 2.0 A<br>6h = 2.5 A<br>7h = 3.0 A<br>8h = 3.5 A<br>9h = 4.0 A<br>Ah = 4.5 A<br>Bh = 5.0 A<br>Ch = 5.5 A<br>Dh = 6.0 A<br>Eh = 7.0 A<br>Fh = 8.0 A |

**Table 7-32. FAULT\_CONFIG1 Register Field Descriptions (continued)**

| Bit   | Field          | Type | Reset | Description  |
|-------|----------------|------|-------|--|
| 26-23 | HW_LOCK_ILIMIT | R/W  | 0h    | Comparator based lock detection current threshold<br>0h = 0.125 A<br>1h = 0.25 A<br>2h = 0.5 A<br>3h = 1.0 A<br>4h = 1.5 A<br>5h = 2.0 A<br>6h = 2.5 A<br>7h = 3.0 A<br>8h = 3.5 A<br>9h = 4.0 A<br>Ah = 4.5 A<br>Bh = 5.0 A<br>Ch = 5.5 A<br>Dh = 6.0 A<br>Eh = 7.0 A<br>Fh = 8.0 A |
| 22-19 | LOCK_ILIMIT    | R/W  | 0h    | ADC based lock detection current threshold<br>0h = 0.125 A<br>1h = 0.25 A<br>2h = 0.5 A<br>3h = 1.0 A<br>4h = 1.5 A<br>5h = 2.0 A<br>6h = 2.5 A<br>7h = 3.0 A<br>8h = 3.5 A<br>9h = 4.0 A<br>Ah = 4.5 A<br>Bh = 5.0 A<br>Ch = 5.5 A<br>Dh = 6.0 A<br>Eh = 7.0 A<br>Fh = 8.0 A        |

**Table 7-32. FAULT\_CONFIG1 Register Field Descriptions (continued)**

| Bit   | Field            | Type | Reset | Description  |
|-------|------------------|------|-------|--|
| 18-15 | LOCK_ILIMIT_MODE | R/W  | 0h    | <p>Lock current limit mode</p> <p>0h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is tristated</p> <p>1h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is tristated</p> <p>2h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in high side brake mode (All high side FETs are turned ON)</p> <p>3h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in low side brake mode (All low side FETs are turned ON)</p> <p>4h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active</p> <p>5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active</p> <p>6h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in high side brake mode (All high side FETs are turned ON); nFAULT active</p> <p>7h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low side brake mode (All low side FETs are turned ON); nFAULT active</p> <p>8h = Ilimit lock detection current limit is in report only but no action is taken; nFAULT active</p> <p>9h = ILIMIT LOCK is disabled</p> <p>Ah = ILIMIT LOCK is disabled</p> <p>Bh = ILIMIT LOCK is disabled</p> <p>Ch = ILIMIT LOCK is disabled</p> <p>Dh = ILIMIT LOCK is disabled</p> <p>Eh = ILIMIT LOCK is disabled</p> <p>Fh = ILIMIT LOCK is disabled</p> |
| 14-11 | LOCK_ILIMIT_DEG  | R/W  | 0h    | <p>Lock detection current limit deglitch time</p> <p>0h = Not Applicable</p> <p>1h = Not Applicable</p> <p>2h = 0.2 ms</p> <p>3h = 0.5 ms</p> <p>4h = 1 ms</p> <p>5h = 2.5 ms</p> <p>6h = 5 ms</p> <p>7h = 7.5 ms</p> <p>8h = 10 ms</p> <p>9h = 25 ms</p> <p>Ah = 50 ms</p> <p>Bh = 75 ms</p> <p>Ch = 100 ms</p> <p>Dh = 200 ms</p> <p>Eh = 500 ms</p> <p>Fh = 1000 ms</p>   |

**Table 7-32. FAULT\_CONFIG1 Register Field Descriptions (continued)**

| Bit  | Field                | Type | Reset | Description   |
|------|----------------------|------|-------|---|
| 10-7 | LCK_RETRY            | R/W  | 0h    | Lock detection retry time<br>0h = 300 ms<br>1h = 500 ms<br>2h = 1 s<br>3h = 2 s<br>4h = 3 s<br>5h = 4 s<br>6h = 5 s<br>7h = 6 s<br>8h = 7 s<br>9h = 8 s<br>Ah = 9 s<br>Bh = 10 s<br>Ch = 11 s<br>Dh = 12 s<br>Eh = 13 s<br>Fh = 14 s  |
| 6-3  | MTR_LCK_MODE         | R/W  | 0h    | Motor Lock Mode<br>0h = Motor lock detection causes latched fault; nFAULT active; Gate driver is tristated<br>1h = Motor lock detection causes latched fault; nFAULT active; Gate driver is tristated<br>2h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in high side brake mode (All high side FETs are turned ON)<br>3h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in low side brake mode (All low side FETs are turned ON)<br>4h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active<br>5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active<br>6h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in high side brake mode (All high side FETs are turned ON); nFAULT active<br>7h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low side brake mode (All low side FETs are turned ON); nFAULT active<br>8h = Motor lock detection current limit is in report only but no action is taken; nFAULT active<br>9h = Motor lock detection is disabled<br>Ah = Motor lock detection is disabled<br>Bh = Motor lock detection is disabled<br>Ch = Motor lock detection is disabled<br>Dh = Motor lock detection is disabled<br>Eh = Motor lock detection is disabled<br>Fh = Motor lock detection is disabled |
| 2    | IPD_TIMEOUT_FAULT_EN | R/W  | 0h    | IPD timeout fault enable<br>0h = Disable<br>1h = Enable   |
| 1    | IPD_FREQ_FAULT_EN    | R/W  | 0h    | IPD frequency fault enable<br>0h = Disable<br>1h = Enable   |
| 0    | SATURATION_FLAGS_EN  | R/W  | 0h    | Enables indication of current loop and speed loop saturation<br>0h = Disable<br>1h = Enable   |

### 7.7.2.2 FAULT\_CONFIG2 Register (Offset = 92h) [Reset = 0000000h]

FAULT\_CONFIG2 is shown in [Figure 7-71](#) and described in [Table 7-33](#).

Return to the [Summary Table](#).

Register to configure fault settings2

**Figure 7-71. FAULT\_CONFIG2 Register**

|                     |                    |            |          |                |                     |                   |    |
|---------------------|--------------------|------------|----------|----------------|---------------------|-------------------|----|
| 31                  | 30                 | 29         | 28       | 27             | 26                  | 25                | 24 |
| RESERVED            | LOCK1_EN           | LOCK2_EN   | LOCK3_EN | LOCK_ABN_SPEED |                     | ABNORMAL_BEMF_THR |    |
| R/W-0h              | R/W-0h             | R/W-0h     | R/W-0h   | R/W-0h         |                     | R/W-0h            |    |
| 23                  | 22                 | 21         | 20       | 19             | 18                  | 17                | 16 |
| ABNORMAL_BEMF_THR   |                    | NO_MTR_THR |          |                | HW_LOCK_ILIMIT_MODE |                   |    |
| R/W-0h              |                    | R/W-0h     |          |                | R/W-0h              |                   |    |
| 15                  | 14                 | 13         | 12       | 11             | 10                  | 9                 | 8  |
| HW_LOCK_ILIMIT_MODE | HW_LOCK_ILIMIT_DEG |            |          | RESERVED       | MIN_VM_MOTOR        |                   |    |
| R/W-0h              | R/W-0h             |            |          | R/W-0h         | R/W-0h              |                   |    |
| 7                   | 6                  | 5          | 4        | 3              | 2                   | 1                 | 0  |
| MIN_VM_MODE         | MAX_VM_MOTOR       |            |          | MAX_VM_MODE    | AUTO_RETRY_TIMES    |                   |    |
| R/W-0h              | R/W-0h             |            |          | R/W-0h         | R/W-0h              |                   |    |

**Table 7-33. FAULT\_CONFIG2 Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description  |
|-------|-------------------|------|-------|--|
| 31    | RESERVED          | R/W  | 0h    | Reserved   |
| 30    | LOCK1_EN          | R/W  | 0h    | Lock 1 (Abnormal Speed) Enable<br>0h = Disable<br>1h = Enable  |
| 29    | LOCK2_EN          | R/W  | 0h    | Lock 2 (Abnormal BEMF) Enable<br>0h = Disable<br>1h = Enable   |
| 28    | LOCK3_EN          | R/W  | 0h    | Lock 3 (No Motor) Enable<br>0h = Disable<br>1h = Enable  |
| 27-25 | LOCK_ABN_SPEED    | R/W  | 0h    | Abnormal speed lock threshold (% of MAX_SPEED)<br>0h = 130%<br>1h = 140%<br>2h = 150%<br>3h = 160%<br>4h = 170%<br>5h = 180%<br>6h = 190%<br>7h = 200% |
| 24-22 | ABNORMAL_BEMF_THR | R/W  | 0h    | Abnormal BEMF lock threshold (% of expected BEMF)<br>0h = 40%<br>1h = 45%<br>2h = 50%<br>3h = 55%<br>4h = 60%<br>5h = 65%<br>6h = 67.5%<br>7h = 70%    |

**Table 7-33. FAULT\_CONFIG2 Register Field Descriptions (continued)**

| Bit   | Field               | Type | Reset | Description   |
|-------|---------------------|------|-------|---|
| 21-19 | NO_MTR_THR          | R/W  | 0h    | No motor lock threshold<br>0h = 0.075 A<br>1h = 0.075 A<br>2h = 0.1A<br>3h = 0.125 A<br>4h = 0.25 A<br>5h = 0.5 A<br>6h = 0.75 A<br>7h = 1.0 A  |
| 18-15 | HW_LOCK_ILIMIT_MODE | R/W  | 0h    | Hardware lock detection current mode<br>0h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is tristated<br>1h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is tristated<br>2h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in high side brake mode (All high side FETs are turned ON)<br>3h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in low side brake mode (All low side FETs are turned ON)<br>4h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active<br>5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active<br>6h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in high side brake mode (All high side FETs are turned ON); nFAULT active<br>7h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low side brake mode (All low side FETs are turned ON); nFAULT active<br>8h = Hardware ILIMIT lock detection is in report only but no action is taken<br>9h = Hardware ILIMIT lock detection is disabled<br>Ah = Hardware ILIMIT lock detection is disabled<br>Bh = Hardware ILIMIT lock detection is disabled<br>Ch = Hardware ILIMIT lock detection is disabled<br>Dh = Hardware ILIMIT lock detection is disabled<br>Eh = Hardware ILIMIT lock detection is disabled<br>Fh = Hardware ILIMIT lock detection is disabled |
| 14-12 | HW_LOCK_ILIMIT_DEG  | R/W  | 0h    | Hardware lock detection current limit deglitch time<br>0h = No deglitch<br>1h = 1 $\mu$ s<br>2h = 2 $\mu$ s<br>3h = 3 $\mu$ s<br>4h = 4 $\mu$ s<br>5h = 5 $\mu$ s<br>6h = 6 $\mu$ s<br>7h = 7 $\mu$ s   |
| 11    | RESERVED            | R/W  | 0h    | Reserved  |
| 10-8  | MIN_VM_MOTOR        | R/W  | 0h    | Minimum DC Bus voltage for running motor (V)<br>0h = No Limit<br>1h = 4.5 V<br>2h = 5 V<br>3h = 5.5 V<br>4h = 6 V<br>5h = 7.5 V<br>6h = 10 V<br>7h = 12.5 V   |

**Table 7-33. FAULT\_CONFIG2 Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description  |
|-----|------------------|------|-------|--|
| 7   | MIN_VM_MODE      | R/W  | 0h    | DC Bus Undervoltage Fault Recovery Mode<br>0h = Latch on undervoltage<br>1h = Automatic clear if voltage in bounds   |
| 6-4 | MAX_VM_MOTOR     | R/W  | 0h    | Maximum DC Bus voltage for running motor<br>0h = No Limit<br>1h = 20 V<br>2h = 22.5 V<br>3h = 25 V<br>4h = 27.5 V<br>5h = 30 V<br>6h = 32.5 V<br>7h = 35 V |
| 3   | MAX_VM_MODE      | R/W  | 0h    | DC Bus Overvoltage Fault Recovery Mode<br>0h = Latch on overvoltage<br>1h = Automatic clear if voltage in bounds   |
| 2-0 | AUTO_RETRY_TIMES | R/W  | 0h    | Automatic retry attempts<br>0h = No Limit<br>1h = 2<br>2h = 3<br>3h = 5<br>4h = 7<br>5h = 10<br>6h = 15<br>7h = 20   |

### 7.7.3 Hardware\_Configuration Registers

Table 7-34 lists the memory-mapped registers for the Hardware\_Configuration registers. All register offset addresses not listed in Table 7-34 should be considered as reserved locations and the register contents should not be modified.

**Table 7-34. HARDWARE\_CONFIGURTION Registers**

| Offset | Acronym        | Register Name              | Section            |
|--------|----------------|----------------------------|--------------------|
| A4h    | PIN_CONFIG     | Hardware Pin Configuration | <a href="#">Go</a> |
| A6h    | DEVICE_CONFIG1 | Device configuration1      | <a href="#">Go</a> |
| A8h    | DEVICE_CONFIG2 | Device configuration2      | <a href="#">Go</a> |
| AAh    | PERI_CONFIG1   | Peripheral Configuration1  | <a href="#">Go</a> |
| ACH    | GD_CONFIG1     | Gate Driver Configuration1 | <a href="#">Go</a> |
| Aeh    | GD_CONFIG2     | Gate Driver Configuration2 | <a href="#">Go</a> |

Complex bit access types are encoded to fit into small table cells. Table 7-35 shows the codes that are used for access types in this section.

**Table 7-35. Hardware\_Configuration Access Type Codes**

| Access Type            | Code    | Description         |
|------------------------|---------|---------------------|
| Read Type              |         |                     |
| R                      | R       | Read                |
| Write Type             |         |                     |
| W                      | W       | Write               |
| W1C                    | W<br>1C | Write<br>1 to clear |
| Reset or Default Value |         |                     |

**Table 7-35. Hardware\_Configuration Access Type  
Codes (continued)**

| Access Type | Code | Description                            |
|-------------|------|--|
| <i>-n</i>   |      | Value after reset or the default value |



### 7.7.3.1 PIN\_CONFIG Register (Offset = A4h) [Reset = 0000000h]

PIN\_CONFIG is shown in [Figure 7-72](#) and described in [Table 7-36](#).

Return to the [Summary Table](#).

Register to configure hardware pins

**Figure 7-72. PIN\_CONFIG Register**

|                 |              |                |                       |                  |                |            |                 |
|-----------------|--------------|----------------|-----------------------|------------------|----------------|------------|-----------------|
| 31              | 30           | 29             | 28                    | 27               | 26             | 25         | 24              |
| RESERVED        | RESERVED     |                |                       | VdcFilterDisable | RESERVED       |            |                 |
| R/W-0h          | R/W-0h       |                |                       | R/W-0h           | R/W-0h         |            |                 |
| 23              | 22           | 21             | 20                    | 19               | 18             | 17         | 16              |
| RESERVED        |              |                |                       |                  |                |            |                 |
| R/W-0h          |              |                |                       |                  |                |            |                 |
| 15              | 14           | 13             | 12                    | 11               | 10             | 9          | 8               |
| RESERVED        |              |                | RESERVED              |                  | FG_IDLE_CONFIG |            | FG_FAULT_CONFIG |
| R/W-0h          |              |                | R/W-0h                |                  | R/W-0h         |            | R/W-0h          |
| 7               | 6            | 5              | 4                     | 3                | 2              | 1          | 0               |
| FG_FAULT_CONFIG | ALARM_PIN_EN | BRAKE_PIN_MODE | ALIGN_BRAKE_ANGLE_SEL | BRAKE_INPUT      |                | SPEED_MODE |                 |
| R/W-0h          | R/W-0h       | R/W-0h         | R/W-0h                | R/W-0h           |                | R/W-0h     |                 |

**Table 7-36. PIN\_CONFIG Register Field Descriptions**

| Bit   | Field                 | Type | Reset | Description   |
|-------|-----------------------|------|-------|---|
| 31    | RESERVED              | R/W  | 0h    | Reserved  |
| 30-28 | RESERVED              | R/W  | 0h    | Reserved  |
| 27    | VdcFilterDisable      | R/W  | 0h    | Vdc (VM) filter disable<br>0h = Vdc filter Enable<br>1h = Vdc filter Disable  |
| 26-13 | RESERVED              | R/W  | 0h    | Reserved  |
| 12-11 | RESERVED              | R/W  | 0h    | Reserved  |
| 10-9  | FG_IDLE_CONFIG        | R/W  | 0h    | FG configuration during stop<br>0h = FG state decided by FG_CONFIG<br>1h = FG is pulled to High<br>2h = FG is pulled to Low<br>3h = FG is pulled to High                                  |
| 8-7   | FG_FAULT_CONFIG       | R/W  | 0h    | FG configuration during fault<br>0h = Use last FG Signal when motor is driven before fault<br>1h = FG is pulled to High<br>2h = FG is pulled to Low<br>3h = FG state decided by FG_CONFIG |
| 6     | ALARM_PIN_EN          | R/W  | 0h    | Alarm pin enable<br>0h = Disable<br>1h = Enable   |
| 5     | BRAKE_PIN_MODE        | R/W  | 0h    | Brake pin mode<br>0h = Low side brake<br>1h = Align brake   |
| 4     | ALIGN_BRAKE_ANGLE_SEL | R/W  | 0h    | Align brake angle select<br>0h = Use last commutation angle before entering align braking<br>1h = Use ALIGN_ANGLE configuration for align braking   |

**Table 7-36. PIN\_CONFIG Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description  |
|-----|-------------|------|-------|--|
| 3-2 | BRAKE_INPUT | R/W  | 0h    | Brake pin override<br>0h = Hardware Pin BRAKE<br>1h = Override pin and brake/align according to BRAKE_PIN_MODE<br>2h = Override pin and do not brake/align<br>3h = Hardware Pin BRAKE  |
| 1-0 | SPEED_MODE  | R/W  | 0h    | Configure motor control input source<br>0h = Controlled by analog voltage on SPEED pin<br>1h = Controlled by duty cycle (PWM) on SPEED pin<br>2h = Controlled by DIGITAL_SPEED_CTRL value (I2C)<br>3h = Controlled by frequency on SPEED pin |

### 7.7.3.2 DEVICE\_CONFIG1 Register (Offset = A6h) [Reset = 0000000h]

DEVICE\_CONFIG1 is shown in [Figure 7-73](#) and described in [Table 7-37](#).

Return to the [Summary Table](#).

Register to configure device

**Figure 7-73. DEVICE\_CONFIG1 Register**

|                 |          |             |                    |            |                 |          |    |
|-----------------|----------|-------------|--------------------|------------|-----------------|----------|----|
| 31              | 30       | 29          | 28                 | 27         | 26              | 25       | 24 |
| RESERVED        | RESERVED | DAC_SOx_SEL |                    | DAC_ENABLE | I2C_TARGET_ADDR |          |    |
| R/W-0h          | R/W-0h   | R/W-0h      |                    | R/W-0h     | R/W-0h          |          |    |
| 23              | 22       | 21          | 20                 | 19         | 18              | 17       | 16 |
| I2C_TARGET_ADDR |          |             |                    | RESERVED   |                 |          |    |
| R/W-0h          |          |             |                    | R/W-0h     |                 |          |    |
| 15              | 14       | 13          | 12                 | 11         | 10              | 9        | 8  |
| RESERVED        |          |             |                    |            |                 |          |    |
| R/W-0h          |          |             |                    |            |                 |          |    |
| 7               | 6        | 5           | 4                  | 3          | 2               | 1        | 0  |
| RESERVED        |          |             | SLEW_RATE_I2C_PINS |            | PULLUP_ENABLE   | BUS_VOLT |    |
| R/W-0h          |          |             | R/W-0h             |            | R/W-0h          | R/W-0h   |    |

**Table 7-37. DEVICE\_CONFIG1 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description  |
|-------|--------------------|------|-------|--|
| 31    | RESERVED           | R/W  | 0h    | Reserved   |
| 30    | RESERVED           | R/W  | 0h    | Reserved   |
| 29-28 | DAC_SOx_SEL        | R/W  | 0h    | Selects between DAC2 and SOx channels<br>0h = DACOUT2<br>1h = SOA<br>2h = SOB<br>3h = SOC  |
| 27    | DAC_ENABLE         | R/W  | 0h    | DAC1 and DAC2 enables<br>0h = DACOUT1 and DACOUT2 on dedicated DAC pins disabled<br>1h = DACOUT1 and DACOUT2 on dedicated DAC pins enabled |
| 26-20 | I2C_TARGET_ADDR    | R/W  | 0h    | I2C target address   |
| 19-5  | RESERVED           | R/W  | 0h    | Reserved   |
| 4-3   | SLEW_RATE_I2C_PINS | R/W  | 0h    | Slew rate control for I2C pins<br>0h = 4.8 mA<br>1h = 3.9 mA<br>2h = 1.86 mA<br>3h = 30.8 mA   |
| 2     | PULLUP_ENABLE      | R/W  | 0h    | Pull-up enable for nFAULT and FG pins<br>0h = Disable<br>1h = Enable   |
| 1-0   | BUS_VOLT           | R/W  | 0h    | Maximum DC bus voltage configuration<br>0h = 15 V<br>1h = 30 V<br>2h = 60 V<br>3h = Not defined  |

### 7.7.3.3 DEVICE\_CONFIG2 Register (Offset = A8h) [Reset = 0000000h]

DEVICE\_CONFIG2 is shown in [Figure 7-74](#) and described in [Table 7-38](#).

Return to the [Summary Table](#).

Register to configure device

**Figure 7-74. DEVICE\_CONFIG2 Register**

|                    |    |                     |                         |                |         |                    |                    |
|--------------------|----|---------------------|-------------------------|----------------|---------|--------------------|--------------------|
| 31                 | 30 | 29                  | 28                      | 27             | 26      | 25                 | 24                 |
| RESERVED           |    | INPUT_MAXIMUM_FREQ  |                         |                |         |                    |                    |
| R/W-0h             |    | R/W-0h              |                         |                |         |                    |                    |
| 23                 | 22 | 21                  | 20                      | 19             | 18      | 17                 | 16                 |
| INPUT_MAXIMUM_FREQ |    |                     |                         |                |         |                    |                    |
| R/W-0h             |    |                     |                         |                |         |                    |                    |
| 15                 | 14 | 13                  | 12                      | 11             | 10      | 9                  | 8                  |
| SLEEP_ENTRY_TIME   |    | DYNAMIC_CSA_GAIN_EN | DYNAMIC_VOLTAGE_GAIN_EN | DEV_MODE       | CLK_SEL |                    | EXT_CLK_EN         |
| R/W-0h             |    | R/W-0h              | R/W-0h                  | R/W-0h         | R/W-0h  |                    | R/W-0h             |
| 7                  | 6  | 5                   | 4                       | 3              | 2       | 1                  | 0                  |
| EXT_CLK_CONFIG     |    |                     | EXT_WDT_EN              | EXT_WDT_CONFIG |         | EXT_WDT_INPUT_MODE | EXT_WDT_FAULT_MODE |
| R/W-0h             |    |                     | R/W-0h                  | R/W-0h         |         | R/W-0h             | R/W-0h             |

**Table 7-38. DEVICE\_CONFIG2 Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description   |
|-------|-------------------------|------|-------|---|
| 31    | RESERVED                | R/W  | 0h    | Reserved  |
| 30-16 | INPUT_MAXIMUM_FREQ      | R/W  | 0h    | Input frequency on speed pin for frequency based motor control that corresponds to 100% duty cycle. Input duty cycle = Input frequency / INPUT_MAXIMUM_FREQ   |
| 15-14 | SLEEP_ENTRY_TIME        | R/W  | 0h    | Device enters sleep mode when input source is held at or below the sleep entry threshold for SLEEP_ENTRY_TIME<br>0h = Sleep entry when SPEED pin remains low for 50µs<br>1h = Sleep entry when SPEED pin remains low for 200µs<br>2h = Sleep entry when SPEED pin remains low for 20ms<br>3h = Sleep entry when SPEED pin remains low for 200ms |
| 13    | DYNAMIC_CSA_GAIN_EN     | R/W  | 0h    | Adjust CSA gain dynamically for optimal resolution across current levels<br>0h = Dynamic CSA gain is disabled<br>1h = Dynamic CSA gain is enabled   |
| 12    | DYNAMIC_VOLTAGE_GAIN_EN | R/W  | 0h    | Adjust voltage gain dynamically for optimal voltage resolution across voltage levels<br>0h = Dynamic voltage gain is disabled<br>1h = Dynamic voltage gain is enabled   |
| 11    | DEV_MODE                | R/W  | 0h    | Device mode select<br>0h = Standby Mode<br>1h = Sleep Mode  |
| 10-9  | CLK_SEL                 | R/W  | 0h    | Clock source<br>0h = Internal Oscillator<br>1h = Crude Oscillator - WDT<br>2h = Not Applicable<br>3h = External Clock input   |
| 8     | EXT_CLK_EN              | R/W  | 0h    | Enable external clock mode<br>0h = Disable<br>1h = Enable   |

**Table 7-38. DEVICE\_CONFIG2 Register Field Descriptions (continued)**

| Bit | Field              | Type | Reset | Description  |
|-----|--------------------|------|-------|--|
| 7-5 | EXT_CLK_CONFIG     | R/W  | 0h    | External clock configuration<br>0h = 8 kHz<br>1h = 16 kHz<br>2h = 32 kHz<br>3h = 64 kHz<br>4h = 128 kHz<br>5h = 256 kHz<br>6h = 512 kHz<br>7h = 1024 kHz |
| 4   | EXT_WDT_EN         | R/W  | 0h    | Enable external watchdog<br>0h = Disable<br>1h = Enable  |
| 3-2 | EXT_WDT_CONFIG     | R/W  | 0h    | Time between watchdog tickles (GPIO/I2C)<br>0h = 100ms/1s<br>1h = 200ms/2s<br>2h = 500ms/5s<br>3h = 1000ms/10s   |
| 1   | EXT_WDT_INPUT_MODE | R/W  | 0h    | External watchdog input mode<br>0h = Watchdog tickle over I2C<br>1h = Watchdog tickle over GPIO  |
| 0   | EXT_WDT_FAULT_MODE | R/W  | 0h    | External watchdog fault mode<br>0h = Report Only<br>1h = Latch with FETs in Hi-Z   |

### 7.7.3.4 PERI\_CONFIG1 Register (Offset = AAh) [Reset = 0000000h]

PERI\_CONFIG1 is shown in [Figure 7-75](#) and described in [Table 7-39](#).

Return to the [Summary Table](#).

Register to peripheral1

**Figure 7-75. PERI\_CONFIG1 Register**

|                                      |  |                                |  |                              |  |                 |  |                  |  |                                      |  |                   |  |    |  |
|--------------------------------------|--|--------------------------------|--|------------------------------|--|-----------------|--|------------------|--|--------------------------------------|--|-------------------|--|----|--|
| 31                                   |  | 30                             |  | 29                           |  | 28              |  | 27               |  | 26                                   |  | 25                |  | 24 |  |
| RESERVED                             |  | SPREAD_SPECTRUM_MODULATION_DIS |  | RESERVED                     |  |                 |  |                  |  |                                      |  | BUS_CURRENT_LIMIT |  |    |  |
| R/W-0h                               |  | R/W-1h                         |  | R/W-0h                       |  |                 |  |                  |  |                                      |  | R/W-0h            |  |    |  |
| 23                                   |  | 22                             |  | 21                           |  | 20              |  | 19               |  | 18                                   |  | 17                |  | 16 |  |
| BUS_CURRENT_LIMIT                    |  | BUS_CURRENT_LIMIT_ENABLE       |  | DIR_INPUT                    |  | DIR_CHANGE_MODE |  | SELF_TEST_ENABLE |  | ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY |  |                   |  |    |  |
| R/W-0h                               |  | R/W-0h                         |  | R/W-0h                       |  | R/W-0h          |  | R/W-0h           |  | R/W-0h                               |  | R/W-0h            |  |    |  |
| 15                                   |  | 14                             |  | 13                           |  | 12              |  | 11               |  | 10                                   |  | 9                 |  | 8  |  |
| ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY |  |                                |  | ACTIVE_BRAKE_MOD_INDEX_LIMIT |  |                 |  | SPEED_RANGE_SEL  |  | RESERVED                             |  |                   |  |    |  |
| R/W-0h                               |  |                                |  | R/W-0h                       |  |                 |  | R/W-0h           |  | R/W-0h                               |  |                   |  |    |  |
| 7                                    |  | 6                              |  | 5                            |  | 4               |  | 3                |  | 2                                    |  | 1                 |  | 0  |  |
| RESERVED                             |  |                                |  |                              |  |                 |  |                  |  |                                      |  |                   |  |    |  |
| R/W-0h                               |  |                                |  |                              |  |                 |  |                  |  |                                      |  |                   |  |    |  |

**Table 7-39. PERI\_CONFIG1 Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description  |
|-------|--------------------------------|------|-------|--|
| 31    | RESERVED                       | R/W  | 0h    | Reserved   |
| 30    | SPREAD_SPECTRUM_MODULATION_DIS | R/W  | 1h    | Spread Spectrum Modulation disable<br>0h = SSM is Enabled<br>1h = SSM is Disabled  |
| 29-26 | RESERVED                       | R/W  | 0h    | Reserved   |
| 25-22 | BUS_CURRENT_LIMIT              | R/W  | 0h    | Bus current limit<br>0h = 0.125 A<br>1h = 0.25 A<br>2h = 0.5 A<br>3h = 1.0 A<br>4h = 1.5 A<br>5h = 2.0 A<br>6h = 2.5 A<br>7h = 3.0 A<br>8h = 3.5 A<br>9h = 4.0 A<br>Ah = 4.5 A<br>Bh = 5.0 A<br>Ch = 5.5 A<br>Dh = 6.0 A<br>Eh = 7.0 A<br>Fh = 8.0 A |
| 21    | BUS_CURRENT_LIMIT_ENABLE       | R/W  | 0h    | Bus current limit enable<br>0h = Disable<br>1h = Enable  |

**Table 7-39. PERI\_CONFIG1 Register Field Descriptions (continued)**

| Bit   | Field                                | Type | Reset | Description  |
|-------|--------------------------------------|------|-------|--|
| 20-19 | DIR_INPUT                            | R/W  | 0h    | DIR pin override<br>0h = Hardware Pin DIR<br>1h = Override DIR pin with clockwise rotation OUTA-OUTB-OUTC<br>2h = Override DIR pin with counter clockwise rotation OUTA-OUTC-OUTB<br>3h = Hardware Pin DIR   |
| 18    | DIR_CHANGE_MODE                      | R/W  | 0h    | Response to change of DIR pin status<br>0h = Follow motor stop options and ISD routine on detecting DIR change<br>1h = Change the direction through Reverse Drive while continuously driving the motor   |
| 17    | SELF_TEST_ENABLE                     | R/W  | 0h    | Enables self-test on power up<br>0h = STL is disabled<br>1h = STL is enabled   |
| 16-13 | ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY | R/W  | 0h    | Difference between final speed and present speed below which active braking will be applied<br>0h = Not Applicable<br>1h = 5%<br>2h = 10%<br>3h = 15%<br>4h = 20%<br>5h = 25%<br>6h = 30%<br>7h = 35%<br>8h = 40%<br>9h = 45%<br>Ah = 50%<br>Bh = 60%<br>Ch = 70%<br>Dh = 80%<br>Eh = 90%<br>Fh = 100% |
| 12-10 | ACTIVE_BRAKE_MOD_INDEX_LIMIT         | R/W  | 0h    | Modulation Index limit below which active braking will be applied<br>0h = 0%<br>1h = 40%<br>2h = 50%<br>3h = 60%<br>4h = 70%<br>5h = 80%<br>6h = 90%<br>7h = 100%  |
| 9     | SPEED_RANGE_SEL                      | R/W  | 0h    | Frequency range selection for PWM/duty based motor control input<br>0h = 325Hz to 100kHz<br>1h = 10Hz to 325Hz   |
| 8     | RESERVED                             | R/W  | 0h    | Reserved   |
| 7-0   | RESERVED                             | R/W  | 0h    | Reserved   |

### 7.7.3.5 GD\_CONFIG1 Register (Offset = ACh) [Reset = 0000000h]

GD\_CONFIG1 is shown in Figure 7-76 and described in Table 7-40.

Return to the [Summary Table](#).

Register to configure gated driver settings1

**Figure 7-76. GD\_CONFIG1 Register**

|          |          |          |          |           |          |          |         |
|----------|----------|----------|----------|-----------|----------|----------|---------|
| 31       | 30       | 29       | 28       | 27        | 26       | 25       | 24      |
| PARITY   | RESERVED |          | RESERVED | SLEW_RATE |          | RESERVED |         |
| R/W-0h   | R/W-0h   |          | R/W-1h   | R/W-0h    |          | R/W-0h   |         |
| 23       | 22       | 21       | 20       | 19        | 18       | 17       | 16      |
| RESERVED | RESERVED | RESERVED | RESERVED | OVP_SEL   | OVP_EN   | RESERVED | OTW_REP |
| R/W-0h   | R/W-0h   | R/W-1h   | R/W-0h   | R/W-0h    | R/W-0h   | R/W-1h   | R/W-0h  |
| 15       | 14       | 13       | 12       | 11        | 10       | 9        | 8       |
| RESERVED | RESERVED | OCP_DEG  |          | RESERVED  | OCP_LVL  | OCP_MODE |         |
| R/W-1h   | R/W-0h   | R/W-0h   |          | R/W-0h    | R/W-0h   | R/W-1h   |         |
| 7        | 6        | 5        | 4        | 3         | 2        | 1        | 0       |
| RESERVED | RESERVED | RESERVED | RESERVED | RESERVED  | RESERVED | CSA_GAIN |         |
| R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h   | R/W-0h    | R/W-0h   | R/W-0h   |         |

**Table 7-40. GD\_CONFIG1 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description  |
|-------|-----------|------|-------|--|
| 31    | PARITY    | R/W  | 0h    | Parity bit   |
| 30-29 | RESERVED  | R/W  | 0h    | Reserved   |
| 28    | RESERVED  | R/W  | 1h    | Reserved   |
| 27-26 | SLEW_RATE | R/W  | 0h    | Slew rate<br>0h = Not Applicable<br>1h = Not Applicable<br>2h = Slew rate is 125 V/μs<br>3h = Slew rate is 200 V/μs  |
| 25-24 | RESERVED  | R/W  | 0h    | Reserved   |
| 23    | RESERVED  | R/W  | 0h    | Reserved   |
| 22    | RESERVED  | R/W  | 0h    | Reserved   |
| 21    | RESERVED  | R/W  | 1h    | Reserved   |
| 20    | RESERVED  | R/W  | 0h    | Reserved   |
| 19    | OVP_SEL   | R/W  | 0h    | Overvoltage level<br>0h = VM overvoltage level is 34-V<br>1h = VM overvoltage level is 22-V  |
| 18    | OVP_EN    | R/W  | 0h    | Overvoltage enable<br>0h = Overvoltage protection is disabled<br>1h = Overvoltage protection is enabled  |
| 17    | RESERVED  | R/W  | 1h    | Reserved   |
| 16    | OTW_REP   | R/W  | 0h    | Overtemperature warning enable<br>0h = Over temperature reporting on nFAULT is disabled<br>1h = Over temperature reporting on nFAULT is enabled                            |
| 15    | RESERVED  | R/W  | 1h    | Reserved   |
| 14    | RESERVED  | R/W  | 0h    | Reserved   |
| 13-12 | OCP_DEG   | R/W  | 0h    | OCP Deglitch Time Settings<br>0h = OCP deglitch time is 0.2 μs<br>1h = OCP deglitch time is 0.6 μs<br>2h = OCP deglitch time is 1.1 μs<br>3h = OCP deglitch time is 1.6 μs |



**Table 7-40. GD\_CONFIG1 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description  |
|-----|----------|------|-------|--|
| 11  | RESERVED | R/W  | 0h    | Reserved   |
| 10  | OCP_LVL  | R/W  | 0h    | Overcurrent Level Setting<br>0h = OCP level is 16 A (Typical)<br>1h = OCP level is 24 A (Typical)  |
| 9-8 | OCP_MODE | R/W  | 1h    | OCP Fault Mode<br>0h = Overcurrent causes a latched fault<br>1h = Overcurrent causes an automatic retrying fault after 500ms<br>2h = Not Applicable<br>3h = Not Applicable               |
| 7   | RESERVED | R/W  | 0h    | Reserved   |
| 6   | RESERVED | R/W  | 0h    | Reserved   |
| 5   | RESERVED | R/W  | 0h    | Reserved   |
| 4   | RESERVED | R/W  | 0h    | Reserved   |
| 3   | RESERVED | R/W  | 0h    | Reserved   |
| 2   | RESERVED | R/W  | 0h    | Reserved   |
| 1-0 | CSA_GAIN | R/W  | 0h    | Current Sense Amplifier gain (used only if<br>DYNAMIC_CSA_GAIN_EN = 0b)<br>0h = CSA gain is 0.15 V/A<br>1h = CSA gain is 0.3 V/A<br>2h = CSA gain is 0.6 V/A<br>3h = CSA gain is 1.2 V/A |

### 7.7.3.6 GD\_CONFIG2 Register (Offset = AEh) [Reset = 0000000h]

GD\_CONFIG2 is shown in [Figure 7-77](#) and described in [Table 7-41](#).

Return to the [Summary Table](#).

Register to configure gated driver settings2

**Figure 7-77. GD\_CONFIG2 Register**

|          |          |          |          |             |    |          |             |
|----------|----------|----------|----------|-------------|----|----------|-------------|
| 31       | 30       | 29       | 28       | 27          | 26 | 25       | 24          |
| PARITY   | RESERVED | RESERVED |          |             |    | RESERVED | BUCK_PS_DIS |
| R/W-0h   | R/W-0h   | R/W-0h   |          |             |    | R/W-0h   | R/W1C-1h    |
| 23       | 22       | 21       | 20       | 19          | 18 | 17       | 16          |
| BUCK_CL  | BUCK_SEL |          | RESERVED | MIN_ON_TIME |    |          | RESERVED    |
| R/W-0h   | R/W-1h   |          | R/W-0h   | R/W-0h      |    |          | R/W-0h      |
| 15       | 14       | 13       | 12       | 11          | 10 | 9        | 8           |
| RESERVED |          |          |          |             |    |          |             |
| R/W-0h   |          |          |          |             |    |          |             |
| 7        | 6        | 5        | 4        | 3           | 2  | 1        | 0           |
| RESERVED |          |          |          |             |    |          |             |
| R/W-0h   |          |          |          |             |    |          |             |

**Table 7-41. GD\_CONFIG2 Register Field Descriptions**

| Bit   | Field       | Type  | Reset | Description  |
|-------|-------------|-------|-------|--|
| 31    | PARITY      | R/W   | 0h    | Parity bit   |
| 30    | RESERVED    | R/W   | 0h    | Reserved   |
| 29-26 | RESERVED    | R/W   | 0h    | Reserved   |
| 25    | RESERVED    | R/W   | 0h    | Reserved   |
| 24    | BUCK_PS_DIS | R/W1C | 1h    | Buck power sequencing disable<br>0h = Buck power sequencing is enabled<br>1h = Buck power sequencing is disabled   |
| 23    | BUCK_CL     | R/W   | 0h    | Buck current limit<br>0h = Buck regulator current limit is set to 600 mA<br>1h = Buck regulator current limit is set to 150 mA   |
| 22-21 | BUCK_SEL    | R/W   | 1h    | Buck voltage<br>0h = Buck voltage is 3.3 V<br>1h = Buck voltage is 5.0 V<br>2h = Buck voltage is 4.0 V<br>3h = Buck voltage is 5.7 V   |
| 20    | RESERVED    | R/W   | 0h    | Reserved   |
| 19-17 | MIN_ON_TIME | R/W   | 0h    | Minimum ON time for low side MOSFET<br>0h = 0 $\mu$ s<br>1h = Automatic based on Slew rate<br>2h = 0.5 $\mu$ s<br>3h = 0.75 $\mu$ s<br>4h = 1 $\mu$ s<br>5h = 1.25 $\mu$ s<br>6h = 1.5 $\mu$ s<br>7h = 2 $\mu$ s |
| 16-0  | RESERVED    | R/W   | 0h    | Reserved   |

### 7.7.4 Internal\_Algorithm\_Configuration Registers

Table 7-42 lists the memory-mapped registers for the Internal\_Algorithm\_Configuration registers. All register offset addresses not listed in Table 7-42 should be considered as reserved locations and the register contents should not be modified.

**Table 7-42. INTERNAL\_ALGORITHM\_CONFIGURATION Registers**

| Offset | Acronym    | Register Name                     | Section            |
|--------|------------|-----------------------------------|--------------------|
| A0h    | INT_ALGO_1 | Internal Algorithm Configuration1 | <a href="#">Go</a> |
| A2h    | INT_ALGO_2 | Internal Algorithm Configuration2 | <a href="#">Go</a> |

Complex bit access types are encoded to fit into small table cells. Table 7-43 shows the codes that are used for access types in this section.

**Table 7-43. Internal\_Algorithm\_Configuration  
Access Type Codes**

| Access Type            | Code | Description                            |
|------------------------|------|--|
| Read Type              |      |  |
| R                      | R    | Read                                   |
| Write Type             |      |  |
| W                      | W    | Write                                  |
| Reset or Default Value |      |  |
| -n                     |      | Value after reset or the default value |

### 7.7.4.1 INT\_ALGO\_1 Register (Offset = A0h) [Reset = 0000000h]

INT\_ALGO\_1 is shown in [Figure 7-78](#) and described in [Table 7-44](#).

Return to the [Summary Table](#).

Register to configure internal algorithm parameters1

**Figure 7-78. INT\_ALGO\_1 Register**

|                          |                                     |                          |                         |                       |                            |               |                       |
|--------------------------|-------------------------------------|--------------------------|-------------------------|-----------------------|----------------------------|---------------|-----------------------|
| 31                       | 30                                  | 29                       | 28                      | 27                    | 26                         | 25            | 24                    |
| RESERVED                 | ACTIVE_BRAKE_SPEED_DELTA_LIMIT_EXIT |                          | SPEED_PIN_GLITCH_FILTER |                       | FAST_ISD_EN                | ISD_STOP_TIME |                       |
| R/W-0h                   | R/W-0h                              |                          | R/W-0h                  |                       | R/W-0h                     | R/W-0h        |                       |
| 23                       | 22                                  | 21                       | 20                      | 19                    | 18                         | 17            | 16                    |
| ISD_RUN_TIME             |                                     | ISD_TIMEOUT              |                         | AUTO_HANDOFF_MIN_BEMF |                            |               | BRAKE_CURRENT_PERSIST |
| R/W-0h                   |                                     | R/W-0h                   |                         | R/W-0h                |                            |               | R/W-0h                |
| 15                       | 14                                  | 13                       | 12                      | 11                    | 10                         | 9             | 8                     |
| BRAKE_CURRENT_PERSIST    | MPET_IPD_CURRENT_LIMIT              |                          | MPET_IPD_FREQ           |                       | MPET_OPEN_LOOP_CURRENT_REF |               |                       |
| R/W-0h                   | R/W-0h                              |                          | R/W-0h                  |                       | R/W-0h                     |               |                       |
| 7                        | 6                                   | 5                        | 4                       | 3                     | 2                          | 1             | 0                     |
| MPET_OPEN_LOOP_SPEED_REF |                                     | MPET_OPEN_LOOP_SLEW_RATE |                         |                       | REV_DRV_OPEN_LOOP_DEC      |               |                       |
| R/W-0h                   |                                     | R/W-0h                   |                         |                       | R/W-0h                     |               |                       |

**Table 7-44. INT\_ALGO\_1 Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description  |
|-------|-------------------------------------|------|-------|--|
| 31    | RESERVED                            | R/W  | 0h    | Reserved   |
| 30-29 | ACTIVE_BRAKE_SPEED_DELTA_LIMIT_EXIT | R/W  | 0h    | Difference between final speed and present speed below which active braking will be stopped<br>0h = 2.5%<br>1h = 5%<br>2h = 7.5%<br>3h = 10% |
| 28-27 | SPEED_PIN_GLITCH_FILTER             | R/W  | 0h    | Glitch filter applied on speed pin input<br>0h = No Glitch Filter<br>1h = 0.2 μs<br>2h = 0.5 μs<br>3h = 1.0 μs                               |
| 26    | FAST_ISD_EN                         | R/W  | 0h    | Enable fast speed detection during ISD<br>0h = Disable Fast ISD<br>1h = Enable Fast ISD  |
| 25-24 | ISD_STOP_TIME                       | R/W  | 0h    | Persistence time for declaring motor has stopped<br>0h = 1 ms<br>1h = 5 ms<br>2h = 50 ms<br>3h = 100 ms                                      |
| 23-22 | ISD_RUN_TIME                        | R/W  | 0h    | Persistence time for declaring motor is running<br>0h = 1 ms<br>1h = 5 ms<br>2h = 50 ms<br>3h = 100 ms                                       |
| 21-20 | ISD_TIMEOUT                         | R/W  | 0h    | Timeout in case ISD is unable to reliably detect speed or direction<br>0h = 500ms<br>1h = 750 ms<br>2h = 1000 ms<br>3h = 2000 ms             |

**Table 7-44. INT\_ALGO\_1 Register Field Descriptions (continued)**

| Bit   | Field                      | Type | Reset | Description   |
|-------|----------------------------|------|-------|---|
| 19-17 | AUTO_HANDOFF_MIN_BEMF      | R/W  | 0h    | Minimum BEMF for handoff<br>0h = 0 mV<br>1h = 50 mV<br>2h = 100 mV<br>3h = 250 mV<br>4h = 500 mV<br>5h = 1000 mV<br>6h = 1250 mV<br>7h = 1500 mV  |
| 16-15 | BRAKE_CURRENT_PERSIST      | R/W  | 0h    | Persistence time for current below threshold during current based ISD brake<br>0h = 50 ms<br>1h = 100 ms<br>2h = 250 ms<br>3h = 500 ms  |
| 14-13 | MPET_IPD_CURRENT_LIMIT     | R/W  | 0h    | IPD current limit for MPET<br>0h = 0.1 A<br>1h = 0.5 A<br>2h = 1.0 A<br>3h = 2.0 A  |
| 12-11 | MPET_IPD_FREQ              | R/W  | 0h    | Number of times IPD is executed for MPET<br>0h = 1<br>1h = 2<br>2h = 4<br>3h = 8  |
| 10-8  | MPET_OPEN_LOOP_CURRENT_REF | R/W  | 0h    | Open loop current reference for MPET<br>0h = 1 A<br>1h = 2 A<br>2h = 3 A<br>3h = 4 A<br>4h = 5 A<br>5h = 6 A<br>6h = 7 A<br>7h = 8 A  |
| 7-6   | MPET_OPEN_LOOP_SPEED_REF   | R/W  | 0h    | Open loop speed reference for MPET (% of MAX_SPEED)<br>0h = 15%<br>1h = 25%<br>2h = 35%<br>3h = 50%   |
| 5-3   | MPET_OPEN_LOOP_SLEW_RATE   | R/W  | 0h    | Open loop acceleration for MPET<br>0h = 0.1 Hz/s<br>1h = 0.5 Hz/s<br>2h = 1 Hz/s<br>3h = 2 Hz/s<br>4h = 3 Hz/s<br>5h = 5 Hz/s<br>6h = 10 Hz/s<br>7h = 20 Hz/s                               |
| 2-0   | REV_DRV_OPEN_LOOP_DEC      | R/W  | 0h    | % of open loop acceleration to be applied during open loop deceleration in reverse drive<br>0h = 50%<br>1h = 60%<br>2h = 70%<br>3h = 80%<br>4h = 90%<br>5h = 100%<br>6h = 125%<br>7h = 150% |

### 7.7.4.2 INT\_ALGO\_2 Register (Offset = A2h) [Reset = 0000000h]

INT\_ALGO\_2 is shown in [Figure 7-79](#) and described in [Table 7-45](#).

Return to the [Summary Table](#).

Register to configure internal algorithm parameters2

**Figure 7-79. INT\_ALGO\_2 Register**

|             |    |                                    |    |    |                 |                              |                        |
|-------------|----|------------------------------------|----|----|-----------------|------------------------------|------------------------|
| 31          | 30 | 29                                 | 28 | 27 | 26              | 25                           | 24                     |
| RESERVED    |    | RESERVED                           |    |    |                 |                              |                        |
| R/W-0h      |    | R/W-0h                             |    |    |                 |                              |                        |
| 23          | 22 | 21                                 | 20 | 19 | 18              | 17                           | 16                     |
| RESERVED    |    |                                    |    |    |                 |                              |                        |
| R/W-0h      |    |                                    |    |    |                 |                              |                        |
| 15          | 14 | 13                                 | 12 | 11 | 10              | 9                            | 8                      |
| RESERVED    |    |                                    |    |    |                 | CL_SLOW_ACC                  |                        |
| R/W-0h      |    |                                    |    |    |                 | R/W-0h                       |                        |
| 7           | 6  | 5                                  | 4  | 3  | 2               | 1                            | 0                      |
| CL_SLOW_ACC |    | ACTIVE_BRAKE_BUS_CURRENT_SLEW_RATE |    |    | MPET_IPD_SELECT | MPET_KEY_AS_PARAMETER_SELECT | IPD_HIGH_RESOLUTION_EN |
| R/W-0h      |    | R/W-0h                             |    |    | R/W-0h          | R/W-0h                       | R/W-0h                 |

**Table 7-45. INT\_ALGO\_2 Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description   |
|-------|------------------------------------|------|-------|---|
| 31    | RESERVED                           | R/W  | 0h    | Reserved  |
| 30-10 | RESERVED                           | R/W  | 0h    | Reserved  |
| 9-6   | CL_SLOW_ACC                        | R/W  | 0h    | Close loop acceleration when estimator is not yet fully aligned just after transition to closed loop<br>0h = 0.1 Hz/s<br>1h = 1 Hz/s<br>2h = 2 Hz/s<br>3h = 3 Hz/s<br>4h = 5 Hz/s<br>5h = 10 Hz/s<br>6h = 20 Hz/s<br>7h = 30 Hz/s<br>8h = 40 Hz/s<br>9h = 50 Hz/s<br>Ah = 100 Hz/s<br>Bh = 200 Hz/s<br>Ch = 500 Hz/s<br>Dh = 750 Hz/s<br>Eh = 1000 Hz/s<br>Fh = 2000 Hz/s |
| 5-3   | ACTIVE_BRAKE_BUS_CURRENT_SLEW_RATE | R/W  | 0h    | Bus current slew rate during active braking<br>0h = 10 A/s<br>1h = 50 A/s<br>2h = 100 A/s<br>3h = 250 A/s<br>4h = 500 A/s<br>5h = 1000 A/s<br>6h = 5000 A/s<br>7h = No Limit  |

**Table 7-45. INT\_ALGO\_2 Register Field Descriptions (continued)**

| Bit | Field                         | Type | Reset | Description  |
|-----|-------------------------------|------|-------|--|
| 2   | MPET_IPD_SELECT               | R/W  | 0h    | Selection between MPET_IPD_CURRENT_LIMIT for IPD current limit, MPET_IPD_FREQ for IPD Repeat OR IPD_CURR_THR for IPD current limit, IPD_REPEAT for IPD Repeat<br>0h = Configured parameters for normal motor operation<br>1h = MPET specific parameters  |
| 1   | MPET_KE_MEAS_PARAMETER_SELECT | R/W  | 0h    | Selection between MPET_OPEN_LOOP_SLEW_RATE for slew rate, MPET_OPEN_LOOP_CURR_REF for current reference, MPET_OPEN_LOOP_SPEED_REF for speed reference OR OL_ACC_A1, OL_ACC_A2 for slew rate, open loop current reference for current reference and open to closed loop speed threshold for speed reference<br>0h = Configured parameters for normal motor operation<br>1h = MPET specific parameters |
| 0   | IPD_HIGH_RESOLUTION_EN        | R/W  | 0h    | IPD high resolution enable<br>0h = Disable<br>1h = Enable  |

## 7.8 RAM (Volatile) Register Map

### 7.8.1 Fault\_Status Registers

Table 7-46 lists the memory-mapped registers for the Fault\_Status registers. All register offset addresses not listed in Table 7-46 are considered as reserved locations and the register contents are not be modified.

**Table 7-46. FAULT\_STATUS Registers**

| Offset | Acronym                  | Register Name         | Section            |
|--------|--------------------------|-----------------------|--------------------|
| E0h    | GATE_DRIVER_FAULT_STATUS | Fault Status Register | <a href="#">Go</a> |
| E2h    | CONTROLLER_FAULT_STATUS  | Fault Status Register | <a href="#">Go</a> |

Complex bit access types are encoded to fit into small table cells. Table 7-47 shows the codes that are used for access types in this section.

**Table 7-47. Fault\_Status Access Type Codes**

| Access Type            | Code | Description                            |
|------------------------|------|--|
| Read Type              |      |  |
| R                      | R    | Read                                   |
| Reset or Default Value |      |  |
| -n                     |      | Value after reset or the default value |



### 7.8.1.1 GATE\_DRIVER\_FAULT\_STATUS Register (Offset = E0h) [Reset = 0000000h]

GATE\_DRIVER\_FAULT\_STATUS is shown in [Figure 7-80](#) and described in [Table 7-48](#).

Return to the [Summary Table](#).

Status of various gate driver faults

**Figure 7-80. GATE\_DRIVER\_FAULT\_STATUS Register**

|              |         |          |         |          |          |        |          |
|--------------|---------|----------|---------|----------|----------|--------|----------|
| 31           | 30      | 29       | 28      | 27       | 26       | 25     | 24       |
| DRIVER_FAULT | BK_FLT  | RESERVED | OCP     | RESERVED | OVP      | OT     | RESERVED |
| R-0h         | R-0h    | R-0h     | R-0h    | R-0h     | R-0h     | R-0h   | R-0h     |
| 23           | 22      | 21       | 20      | 19       | 18       | 17     | 16       |
| OTW          | OTS     | OCP_HC   | OCP_LC  | OCP_HB   | OCP_LB   | OCP_HA | OCP_LA   |
| R-0h         | R-0h    | R-0h     | R-0h    | R-0h     | R-0h     | R-0h   | R-0h     |
| 15           | 14      | 13       | 12      | 11       | 10       | 9      | 8        |
| RESERVED     | OTP_ERR | BUCK_OCP | BUCK_UV | VCP_UV   | RESERVED |        |          |
| R-0h         | R-0h    | R-0h     | R-0h    | R-0h     | R-0h     |        |          |
| 7            | 6       | 5        | 4       | 3        | 2        | 1      | 0        |
| RESERVED     |         |          |         |          |          |        |          |
| R-0h         |         |          |         |          |          |        |          |

**Table 7-48. GATE\_DRIVER\_FAULT\_STATUS Register Field Descriptions**

| Bit | Field        | Type | Reset | Description   |
|-----|--------------|------|-------|---|
| 31  | DRIVER_FAULT | R    | 0h    | Logic OR of FAULT status registers. Mirrors nFAULT pin.   |
| 30  | BK_FLT       | R    | 0h    | Buck Fault Bit<br>0h = No buck regulator fault condition is detected<br>1h = Buck regulator fault condition is detected   |
| 29  | RESERVED     | R    | 0h    | Reserved  |
| 28  | OCP          | R    | 0h    | Over Current Protection Status Bit<br>0h = No overcurrent condition is detected<br>1h = Overcurrent condition is detected   |
| 27  | RESERVED     | R    | 0h    | Reserved  |
| 26  | OVP          | R    | 0h    | Supply Overvoltage Protection Status Bit<br>0h = No overvoltage condition is detected on VM<br>1h = Overvoltage condition is detected on VM                         |
| 25  | OT           | R    | 0h    | Overtemperature Fault Status Bit<br>0h = No overtemperature warning / shutdown is detected<br>1h = Overtemperature warning / shutdown is detected                   |
| 24  | RESERVED     | R    | 0h    | Reserved  |
| 23  | OTW          | R    | 0h    | Overtemperature Warning Status Bit<br>0h = No overtemperature warning is detected<br>1h = Overtemperature warning is detected                                       |
| 22  | OTS          | R    | 0h    | Overtemperature Shutdown Status Bit<br>0h = No overtemperature shutdown is detected<br>1h = Overtemperature shutdown is detected                                    |
| 21  | OCP_HC       | R    | 0h    | Overcurrent Status on High-side switch of OUTC<br>0h = No overcurrent detected on high-side switch of OUTC<br>1h = Overcurrent detected on high-side switch of OUTC |
| 20  | OCP_LC       | R    | 0h    | Overcurrent Status on Low-side switch of OUTC<br>0h = No overcurrent detected on low-side switch of OUTC<br>1h = Overcurrent detected on low-side switch of OUTC    |

**Table 7-48. GATE\_DRIVER\_FAULT\_STATUS Register Field Descriptions (continued)**

| Bit  | Field    | Type | Reset | Description   |
|------|----------|------|-------|---|
| 19   | OCP_HB   | R    | 0h    | Overcurrent Status on High-side switch of OUTB<br>0h = No overcurrent detected on high-side switch of OUTB<br>1h = Overcurrent detected on high-side switch of OUTB |
| 18   | OCP_LB   | R    | 0h    | Overcurrent Status on Low-side switch of OUTB<br>0h = No overcurrent detected on low-side switch of OUTB<br>1h = Overcurrent detected on low-side switch of OUTB    |
| 17   | OCP_HA   | R    | 0h    | Overcurrent Status on High-side switch of OUTA<br>0h = No overcurrent detected on high-side switch of OUTA<br>1h = Overcurrent detected on high-side switch of OUTA |
| 16   | OCP_LA   | R    | 0h    | Overcurrent Status on Low-side switch of OUTA<br>0h = No overcurrent detected on low-side switch of OUTA<br>1h = Overcurrent detected on low-side switch of OUTA    |
| 15   | RESERVED | R    | 0h    | Reserved  |
| 14   | OTP_ERR  | R    | 0h    | OTP Error<br>0h = No OTP error is detected<br>1h = OTP Error is detected  |
| 13   | BUCK_OCP | R    | 0h    | Buck Regulator Overcurrent Status Bit<br>0h = No buck regulator overcurrent is detected<br>1h = Buck regulator overcurrent is detected                              |
| 12   | BUCK_UV  | R    | 0h    | Buck Regulator Undervoltage Status Bit<br>0h = No buck regulator undervoltage is detected<br>1h = Buck regulator undervoltage is detected                           |
| 11   | VCP_UV   | R    | 0h    | Charge Pump Undervoltage Status Bit<br>0h = No charge pump undervoltage is detected<br>1h = Charge pump undervoltage is detected                                    |
| 10-0 | RESERVED | R    | 0h    | Reserved  |

### 7.8.1.2 CONTROLLER\_FAULT\_STATUS Register (Offset = E2h) [Reset = 0000000h]

CONTROLLER\_FAULT\_STATUS is shown in [Figure 7-81](#) and described in [Table 7-49](#).

Return to the [Summary Table](#).

Status of various controller faults

**Figure 7-81. CONTROLLER\_FAULT\_STATUS Register**

|                       |                         |                |              |                |                          |                     |                    |
|-----------------------|-------------------------|----------------|--------------|----------------|--------------------------|---------------------|--------------------|
| 31                    | 30                      | 29             | 28           | 27             | 26                       | 25                  | 24                 |
| CONTROLLER_FAULT      | RESERVED                | IPD_FREQ_FAULT | IPD_T1_FAULT | IPD_T2_FAULT   | BUS_CURRENT_LIMIT_STATUS | MPET_IPD_FAULT      | MPET_BEMF_FAULT    |
| R-0h                  | R-0h                    | R-0h           | R-0h         | R-0h           | R-0h                     | R-0h                | R-0h               |
| 23                    | 22                      | 21             | 20           | 19             | 18                       | 17                  | 16                 |
| ABN_SPEED             | ABN_BEMF                | NO_MTR         | MTR_LCK      | LOCK_LIMIT     | HW_LOCK_LIMIT            | DCBUS_UNDER_VOLTAGE | DCBUS_OVER_VOLTAGE |
| R-0h                  | R-0h                    | R-0h           | R-0h         | R-0h           | R-0h                     | R-0h                | R-0h               |
| 15                    | 14                      | 13             | 12           | 11             | 10                       | 9                   | 8                  |
| SPEED_LOOP_SATURATION | CURRENT_LOOP_SATURATION | RESERVED       |              |                |                          |                     |                    |
| R-0h                  | R-0h                    | R-0h           |              |                |                          |                     |                    |
| 7                     | 6                       | 5              | 4            | 3              | 2                        | 1                   | 0                  |
| RESERVED              |                         |                |              | WATCHDOG_FAULT | RESERVED                 | RESERVED            | RESERVED           |
| R-0h                  |                         |                |              | R-0h           | R-0h                     | R-0h                | R-0h               |

**Table 7-49. CONTROLLER\_FAULT\_STATUS Register Field Descriptions**

| Bit | Field                    | Type | Reset | Description  |
|-----|--------------------------|------|-------|--|
| 31  | CONTROLLER_FAULT         | R    | 0h    | Logic OR of Controller FAULT status registers                |
| 30  | RESERVED                 | R    | 0h    | Reserved   |
| 29  | IPD_FREQ_FAULT           | R    | 0h    | Indicates IPD frequency fault                                |
| 28  | IPD_T1_FAULT             | R    | 0h    | Indicates IPD T1 fault                                       |
| 27  | IPD_T2_FAULT             | R    | 0h    | Indicates IPD T2 fault                                       |
| 26  | BUS_CURRENT_LIMIT_STATUS | R    | 0h    | Indicates status of Bus Current limit                        |
| 25  | MPET_IPD_FAULT           | R    | 0h    | Indicates error during resistance and inductance measurement |
| 24  | MPET_BEMF_FAULT          | R    | 0h    | Indicates error during BEMF constant measurement             |
| 23  | ABN_SPEED                | R    | 0h    | Indicates Abnormal speed motor lock condition                |
| 22  | ABN_BEMF                 | R    | 0h    | Indicates Abnormal BEMF motor lock condition                 |
| 21  | NO_MTR                   | R    | 0h    | Indicates No Motor fault                                     |
| 20  | MTR_LCK                  | R    | 0h    | Indicates when one of the motor lock is triggered            |
| 19  | LOCK_LIMIT               | R    | 0h    | Indicates Lock limit fault                                   |
| 18  | HW_LOCK_LIMIT            | R    | 0h    | Indicates Hardware Lock limit fault                          |
| 17  | DCBUS_UNDER_VOLTAGE      | R    | 0h    | Indicates DC bus undervoltage fault                          |
| 16  | DCBUS_OVER_VOLTAGE       | R    | 0h    | Indicates DC bus overvoltage fault                           |
| 15  | SPEED_LOOP_SATURATION    | R    | 0h    | Indicates speed loop saturation                              |
| 14  | CURRENT_LOOP_SATURATION  | R    | 0h    | Indicates current loop saturation                            |

**Table 7-49. CONTROLLER\_FAULT\_STATUS Register Field Descriptions (continued)**

| Bit  | Field          | Type | Reset | Description              |
|------|----------------|------|-------|--------------------------|
| 13-4 | RESERVED       | R    | 0h    | Reserved                 |
| 3    | WATCHDOG_FAULT | R    | 0h    | indicates Watchdog fault |
| 2    | RESERVED       | R    | 0h    | Reserved                 |
| 1    | RESERVED       | R    | 0h    | Reserved                 |
| 0    | RESERVED       | R    | 0h    | Reserved                 |

### 7.8.2 System\_Status Registers

Table 7-50 lists the memory-mapped registers for the System\_Status registers. All register offset addresses not listed in Table 7-50 should be considered as reserved locations and the register contents should not be modified.

**Table 7-50. SYSTEM\_STATUS Registers**

| Offset | Acronym          | Register Name          | Section |
|--------|------------------|------------------------|---------|
| E4h    | ALGO_STATUS      | System Status Register |         |
| E6h    | MTR_PARAMS       | System Status Register |         |
| E8h    | ALGO_STATUS_MPET | System Status Register |         |

Complex bit access types are encoded to fit into small table cells. Table 7-51 shows the codes that are used for access types in this section.

**Table 7-51. System\_Status Access Type Codes**

| Access Type            | Code | Description                            |
|------------------------|------|--|
| Read Type              |      |  |
| R                      | R    | Read                                   |
| Reset or Default Value |      |  |
| -n                     |      | Value after reset or the default value |

### 7.8.3 Device\_Control Registers

Table 7-52 lists the memory-mapped registers for the Device\_Control registers. All register offset addresses not listed in Table 7-52 should be considered as reserved locations and the register contents should not be modified.

**Table 7-52. DEVICE\_CONTROL Registers**

| Offset | Acronym    | Register Name           | Section            |
|--------|------------|-------------------------|--------------------|
| EAh    | ALGO_CTRL1 | Device Control Register | <a href="#">Go</a> |

Complex bit access types are encoded to fit into small table cells. Table 7-53 shows the codes that are used for access types in this section.

**Table 7-53. Device\_Control Access Type Codes**

| Access Type            | Code | Description                            |
|------------------------|------|--|
| Read Type              |      |  |
| R                      | R    | Read                                   |
| Write Type             |      |  |
| W                      | W    | Write                                  |
| Reset or Default Value |      |  |
| -n                     |      | Value after reset or the default value |

### 7.8.3.1 ALGO\_CTRL1 Register (Offset = EAh) [Reset = 0000000h]

ALGO\_CTRL1 is shown in [Figure 7-82](#) and described in [Table 7-54](#).

Return to the [Summary Table](#).

Control settings

**Figure 7-82. ALGO\_CTRL1 Register**

|                    |             |         |                     |                    |                 |          |    |
|--------------------|-------------|---------|---------------------|--------------------|-----------------|----------|----|
| 31                 | 30          | 29      | 28                  | 27                 | 26              | 25       | 24 |
| EEPROM_WRT         | EEPROM_READ | CLR_FLT | CLR_FLT_RETRY_COUNT | RESERVED           |                 |          |    |
| R/W-0h             | R/W-0h      | W-0h    | W-0h                | W-0h               |                 |          |    |
| 23                 | 22          | 21      | 20                  | 19                 | 18              | 17       | 16 |
| RESERVED           |             |         |                     | FORCED_ALIGN_ANGLE |                 |          |    |
| W-0h               |             |         |                     | W-0h               |                 |          |    |
| 15                 | 14          | 13      | 12                  | 11                 | 10              | 9        | 8  |
| FORCED_ALIGN_ANGLE |             |         |                     |                    | WATCHDOG_TICKLE | RESERVED |    |
| W-0h               |             |         |                     |                    | R/W-0h          | W-0h     |    |
| 7                  | 6           | 5       | 4                   | 3                  | 2               | 1        | 0  |
| RESERVED           |             |         |                     |                    |                 |          |    |
| W-0h               |             |         |                     |                    |                 |          |    |

**Table 7-54. ALGO\_CTRL1 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description  |
|-------|---------------------|------|-------|--|
| 31    | EEPROM_WRT          | R/W  | 0h    | Write the configuration to EEPROM  |
| 30    | EEPROM_READ         | R/W  | 0h    | Read the default configuration from EEPROM   |
| 29    | CLR_FLT             | W    | 0h    | Clears all faults  |
| 28    | CLR_FLT_RETRY_COUNT | W    | 0h    | Clears fault retry count   |
| 27-20 | RESERVED            | W    | 0h    | Reserved   |
| 19-11 | FORCED_ALIGN_ANGLE  | W    | 0h    | 9-bit value (in degrees) used during forced Align state ( FORCE_ALIGN_EN = 1) Angle applied = FORCED_ALIGN_ANGLE % 360deg                  |
| 10    | WATCHDOG_TICKLE     | R/W  | 0h    | RAM bit to tickle watchdog in I2C mode. This bit should be written 1 by external controller every EXT_WDT_CFG. The MCF will reset this bit |
| 9-0   | RESERVED            | W    | 0h    | Reserved   |

### 7.8.4 Algorithm\_Control Registers

[Table 7-55](#) lists the memory-mapped registers for the Algorithm\_Control registers. All register offset addresses not listed in [Table 7-55](#) should be considered as reserved locations and the register contents should not be modified.

**Table 7-55. ALGORITHM\_CONTROL Registers**

| Offset | Acronym     | Register Name              | Section            |
|--------|-------------|----------------------------|--------------------|
| ECh    | ALGO_DEBUG1 | Algorithm Control Register | <a href="#">Go</a> |
| EEh    | ALGO_DEBUG2 | Algorithm Control Register | <a href="#">Go</a> |
| F0h    | CURRENT_PI  | Current PI Controller used | <a href="#">Go</a> |
| F2h    | SPEED_PI    | Speed PI controller used   | <a href="#">Go</a> |
| F4h    | DAC_1       | DAC1 Control Register      | <a href="#">Go</a> |

**Table 7-55. ALGORITHM\_CONTROL Registers (continued)**

| Offset | Acronym | Register Name         | Section            |
|--------|---------|-----------------------|--------------------|
| F6h    | DAC_2   | DAC2 Control Register | <a href="#">Go</a> |

Complex bit access types are encoded to fit into small table cells. [Table 7-56](#) shows the codes that are used for access types in this section.

**Table 7-56. Algorithm\_Control Access Type Codes**

| Access Type            | Code | Description                            |
|------------------------|------|--|
| Read Type              |      |  |
| R                      | R    | Read                                   |
| Write Type             |      |  |
| W                      | W    | Write                                  |
| Reset or Default Value |      |  |
| -n                     |      | Value after reset or the default value |

### 7.8.4.1 ALGO\_DEBUG1 Register (Offset = ECh) [Reset = 0000000h]

ALGO\_DEBUG1 is shown in [Figure 7-83](#) and described in [Table 7-57](#).

Return to the [Summary Table](#).

Algorithm control register for debug

**Figure 7-83. ALGO\_DEBUG1 Register**

|                             |                |                           |              |              |                           |                             |    |
|-----------------------------|----------------|---------------------------|--------------|--------------|---------------------------|-----------------------------|----|
| 31                          | 30             | 29                        | 28           | 27           | 26                        | 25                          | 24 |
| OVERRIDE                    |                | DIGITAL_SPEED_CTRL        |              |              |                           |                             |    |
| W-0h                        |                | W-0h                      |              |              |                           |                             |    |
| 23                          | 22             | 21                        | 20           | 19           | 18                        | 17                          | 16 |
| DIGITAL_SPEED_CTRL          |                |                           |              |              |                           |                             |    |
| W-0h                        |                |                           |              |              |                           |                             |    |
| 15                          | 14             | 13                        | 12           | 11           | 10                        | 9                           | 8  |
| CLOSED_LOOP_DIS             | FORCE_ALIGN_EN | FORCE_SLOW_FIRST_CYCLE_EN | FORCE_IPD_EN | FORCE_ISD_EN | FORCE_ALIGN_ANGLE_SRC_SEL | FORCE_IQ_REF_SPEED_LOOP_DIS |    |
| W-0h                        | W-0h           | W-0h                      | W-0h         | W-0h         | W-0h                      | W-0h                        |    |
| 7                           | 6              | 5                         | 4            | 3            | 2                         | 1                           | 0  |
| FORCE_IQ_REF_SPEED_LOOP_DIS |                |                           |              |              |                           |                             |    |
| W-0h                        |                |                           |              |              |                           |                             |    |

**Table 7-57. ALGO\_DEBUG1 Register Field Descriptions**

| Bit   | Field                     | Type | Reset | Description  |
|-------|---------------------------|------|-------|--|
| 31    | OVERRIDE                  | W    | 0h    | Use to control the SPD_CTRL bits. If OVERRIDE = '1', speed command can be written by the user through serial interface.<br>0h = SPEED_CMD using Analog/PWM mode<br>1h = SPEED_CMD using DIGITAL_SPEED_CTRL   |
| 30-16 | DIGITAL_SPEED_CTRL        | W    | 0h    | Digital Speed Control If OVERRIDE = 0b1, then SPEED_CMD is control using DIGITAL_SPEED_CTRL  |
| 15    | CLOSED_LOOP_DIS           | W    | 0h    | Use to disable Closed loop<br>0h = Enable Closed Loop<br>1h = Disable Closed loop, motor commutation in open loop  |
| 14    | FORCE_ALIGN_EN            | W    | 0h    | Force Align State Enable<br>0h = Disable Force Align state, device comes out of align state if MTR_STARTUP is selected as ALIGN or DOUBLE ALIGN<br>1h = Enable Force Align state, device stays in align state if MTR_STARTUP is selected as ALIGN or DOUBLE ALIGN  |
| 13    | FORCE_SLOW_FIRST_CYCLE_EN | W    | 0h    | Force Slow First Cycle Enable<br>0h = Disable Force Slow First Cycle state, device comes out of slow first cycle state if MTR_STARTUP is selected as SLOW FIRST CYCLE<br>1h = Enable Force Slow First Cycle state, device stays in slow first cycle state if MTR_STARTUP is selected as SLOW FIRST CYCLE |
| 12    | FORCE_IPD_EN              | W    | 0h    | Force IPD Enable<br>0h = Disable Force IPD state, device comes out of IPD state if MTR_STARTUP is selected as IPD<br>1h = Enable Force IPD state, device stays in IPD state if MTR_STARTUP is selected as IPD  |
| 11    | FORCE_ISD_EN              | W    | 0h    | Force ISD enable<br>0h = Disable Force ISD state, device comes out of ISD state if ISD_EN is set<br>1h = Enable Force ISD state, device stays in ISD state if ISD_EN is set  |

**Table 7-57. ALGO\_DEBUG1 Register Field Descriptions (continued)**

| Bit | Field                       | Type | Reset | Description   |
|-----|-----------------------------|------|-------|---|
| 10  | FORCE_ALIGN_ANGLE_SRC_SEL   | W    | 0h    | Force Align Angle State Source Select<br>0h = Force Align Angle defined by ALIGN_ANGLE<br>1h = Force Align Angle defined by FORCED_ALIGN_ANGLE  |
| 9-0 | FORCE_IQ_REF_SPEED_LOOP_DIS | W    | 0h    | Sets IQ Ref (% of BASE_CURRENT) when speed loop is disabled If SPEED_LOOP_DIS = 0b1, then Iq_ref is control using IQ_REF_SPEED_LOOP_DIS<br>$iqRef = (FORCE\_IQ\_REF\_SPEED\_LOOP\_DIS / 500) * BASE\_CURRENT$ if $FORCE\_IQ\_REF\_SPEED\_LOOP\_DIS < 500$<br>$iqRef = (FORCE\_IQ\_REF\_SPEED\_LOOP\_DIS - 1024) / 500 * BASE\_CURRENT$ if $FORCE\_IQ\_REF\_SPEED\_LOOP\_DIS > 512$<br>Valid values are 0 to 500 and 512 to 1000 |



### 7.8.4.2 ALGO\_DEBUG2 Register (Offset = EEh) [Reset = 0000000h]

ALGO\_DEBUG2 is shown in [Figure 7-84](#) and described in [Table 7-58](#).

Return to the [Summary Table](#).

Algorithm control register for debug

**Figure 7-84. ALGO\_DEBUG2 Register**

|                           |                               |          |                           |                  |                           |           |                   |
|---------------------------|-------------------------------|----------|---------------------------|------------------|---------------------------|-----------|-------------------|
| 31                        | 30                            | 29       | 28                        | 27               | 26                        | 25        | 24                |
| RESERVED                  | FORCE_RECIRCULATE_STOP_SECTOR |          | FORCE_RECIRCULATE_STOP_EN | CURRENT_LOOP_DIS | FORCE_VD_CURRENT_LOOP_DIS |           |                   |
| W-0h                      | W-0h                          |          | W-0h                      | W-0h             | W-0h                      |           |                   |
| 23                        | 22                            | 21       | 20                        | 19               | 18                        | 17        | 16                |
| FORCE_VD_CURRENT_LOOP_DIS |                               |          |                           |                  |                           |           |                   |
| W-0h                      |                               |          |                           |                  |                           |           |                   |
| 15                        | 14                            | 13       | 12                        | 11               | 10                        | 9         | 8                 |
| FORCE_VQ_CURRENT_LOOP_DIS |                               |          |                           |                  |                           |           |                   |
| W-0h                      |                               |          |                           |                  |                           |           |                   |
| 7                         | 6                             | 5        | 4                         | 3                | 2                         | 1         | 0                 |
| FORCE_VQ_CURRENT_LOOP_DIS |                               | MPET_CMD | MPET_R                    | MPET_L           | MPET_KE                   | MPET_MECH | MPET_WRITE_SHADOW |
| W-0h                      |                               | W-0h     | W-0h                      | W-0h             | W-0h                      | W-0h      | W-0h              |

**Table 7-58. ALGO\_DEBUG2 Register Field Descriptions**

| Bit   | Field                         | Type | Reset | Description   |
|-------|-------------------------------|------|-------|---|
| 31    | RESERVED                      | W    | 0h    | Reserved  |
| 30-28 | FORCE_RECIRCULATE_STOP_SECTOR | W    | 0h    | use to do the recirculation at specific sector during force motor stop condition<br>0h = The last sector before stop condition<br>1h = Sector1<br>2h = Sector2<br>3h = Sector3<br>4h = Sector4<br>5h = Sector5<br>6h = Sector6<br>7h = The last sector before stop condition  |
| 27    | FORCE_RECIRCULATE_STOP_EN     | W    | 0h    | Force recirculate stop Enable<br>0h = Enable Force recirculate stop<br>1h = Disable Force recirculate stop  |
| 26    | CURRENT_LOOP_DIS              | W    | 0h    | Use to control the FORCE_VD_CURRENT_LOOP_DIS and FORCE_VQ_CURRENT_LOOP_DIS. If CURRENT_LOOP_DIS = '1', Current loop and speed loop is disabled<br>0h = Enable Current Loop<br>1h = Disable Current Loop   |
| 25-16 | FORCE_VD_CURRENT_LOOP_DIS     | W    | 0h    | Sets Vd when current loop speed loop are disabled If CURRENT_LOOP_DIS = 0b1, then Vd is control using FORCE_VD_CURRENT_LOOP_DIS<br>mdRef = (FORCE_VD_CURRENT_LOOP_DIS /500)<br>if FORCE_VD_CURRENT_LOOP_DIS < 500<br>(FORCE_VD_CURRENT_LOOP_DIS - 1024)/500 if FORCE_VD_CURRENT_LOOP_DIS > 512 Valid values: 0 to 500 and 512 to 1000 |

**Table 7-58. ALGO\_DEBUG2 Register Field Descriptions (continued)**

| Bit  | Field                     | Type | Reset | Description   |
|------|---------------------------|------|-------|---|
| 15-6 | FORCE_VQ_CURRENT_LOOP_DIS | W    | 0h    | Sets Vq when current loop speed loop are disabled If CURRENT_LOOP_DIS = 0b1, then Vq is control using FORCE_VQ_CURRENT_LOOP_DIS<br>$m_qRef = (FORCE\_VQ\_CURRENT\_LOOP\_DIS / 500)$<br>if $FORCE\_VQ\_CURRENT\_LOOP\_DIS < 500$<br>$(FORCE\_VQ\_CURRENT\_LOOP\_DIS - 1024) / 500$ if $FORCE\_VQ\_CURRENT\_LOOP\_DIS > 512$ Valid values: 0 to 500 and 512 to 1000 |
| 5    | MPET_CMD                  | W    | 0h    | Initiates motor parameter measurement routine when set to 1   |
| 4    | MPET_R                    | W    | 0h    | Enables motor resistance measurement during motor parameter measurement routine<br>0h = Disables Motor Resistance measurement during motor parameter measurement routine<br>1h = Enable Motor Resistance measurement during motor parameter measurement routine   |
| 3    | MPET_L                    | W    | 0h    | Enables motor inductance measurement during motor parameter measurement routine<br>0h = Disables Motor Inductance measurement during motor parameter measurement routine<br>1h = Enable Motor Inductance measurement during motor parameter measurement routine   |
| 2    | MPET_KE                   | W    | 0h    | Enables motor BEMF constant measurement during motor parameter measurement routine<br>0h = Disables Motor BEMF constant measurement during motor parameter measurement routine<br>1h = Enable Motor BEMF constant measurement during motor parameter measurement routine  |
| 1    | MPET_MECH                 | W    | 0h    | Enables motor mechanical parameter measurement during motor parameter measurement routine<br>0h = Disables Motor mechanical parameter measurement during motor parameter measurement routine<br>1h = Enable Motor mechanical parameter measurement during motor parameter measurement routine   |
| 0    | MPET_WRITE_SHADOW         | W    | 0h    | Write measured parameters to shadow register when set to 1  |

### 7.8.4.3 CURRENT\_PI Register (Offset = F0h) [Reset = 0000000h]

CURRENT\_PI is shown in [Figure 7-85](#) and described in [Table 7-59](#).

Return to the [Summary Table](#).

Current PI controller used

**Figure 7-85. CURRENT\_PI Register**

|                 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CURRENT_LOOP_KI |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CURRENT_LOOP_KP |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R-0h            |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**Table 7-59. CURRENT\_PI Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description   |
|-------|-----------------|------|-------|---|
| 31-16 | CURRENT_LOOP_KI | R    | 0h    | 10 bit for current loop ki Same Scaling as CURR_LOOP_KI |
| 15-0  | CURRENT_LOOP_KP | R    | 0h    | 10 bit for current loop kp Same Scaling as CURR_LOOP_KP |

#### 7.8.4.4 SPEED\_PI Register (Offset = F2h) [Reset = 0000000h]

SPEED\_PI is shown in [Figure 7-86](#) and described in [Table 7-60](#).

Return to the [Summary Table](#).

Speed PI controller used

**Figure 7-86. SPEED\_PI Register**

|               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |               |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPEED_LOOP_KI |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SPEED_LOOP_KP |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | R-0h          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**Table 7-60. SPEED\_PI Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description  |
|-------|---------------|------|-------|--|
| 31-16 | SPEED_LOOP_KI | R    | 0h    | 10 bit for Speed loop ki Same Scaling as SPD_LOOP_KI |
| 15-0  | SPEED_LOOP_KP | R    | 0h    | 10 bit for Speed loop kp Same Scaling as SPD_LOOP_KP |

### 7.8.4.5 DAC\_1 Register (Offset = F4h) [Reset = 0000000h]

DAC\_1 is shown in [Figure 7-87](#) and described in [Table 7-61](#).

Return to the [Summary Table](#).

DAC1 Control Register

**Figure 7-87. DAC\_1 Register**

|                  |    |    |                      |                  |    |    |                 |
|------------------|----|----|----------------------|------------------|----|----|-----------------|
| 31               | 30 | 29 | 28                   | 27               | 26 | 25 | 24              |
| RESERVED         |    |    |                      |                  |    |    |                 |
| R-0h             |    |    |                      |                  |    |    |                 |
| 23               | 22 | 21 | 20                   | 19               | 18 | 17 | 16              |
| RESERVED         |    |    | DACOUT1_ENUM_SCALING |                  |    |    | DACOUT1_SCALING |
| R-0h             |    |    | W-8h                 |                  |    |    | W-8h            |
| 15               | 14 | 13 | 12                   | 11               | 10 | 9  | 8               |
| DACOUT1_SCALING  |    |    | DACOUT1_UNIPOLAR     | DACOUT1_VAR_ADDR |    |    |                 |
| W-8h             |    |    | W-0h                 | R/W-0h           |    |    |                 |
| 7                | 6  | 5  | 4                    | 3                | 2  | 1  | 0               |
| DACOUT1_VAR_ADDR |    |    |                      |                  |    |    |                 |
| R/W-0h           |    |    |                      |                  |    |    |                 |

**Table 7-61. DAC\_1 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description   |
|-------|----------------------|------|-------|---|
| 31-21 | RESERVED             | R    | 0h    | Reserved  |
| 20-17 | DACOUT1_ENUM_SCALING | W    | 8h    | Multiplication Factor for DACOUT1 Algorithm Variable extracted from the address contained in DACOUT1_VAR_ADDR multiplied with $2^{\text{DACOUT1\_ENUM\_SCALING}}$ . DACOUT1_ENUM_SCALING comes into effect only if DACOUT1_SCALING is zero  |
| 16-13 | DACOUT1_SCALING      | W    | 8h    | Scaling factor for DACOUT1 Algorithm Variable extracted from the address contained in DACOUT1_VAR_ADDR scaled with $\text{DACOUT1\_SCALING} / 8$ . Actual voltage depends on DACOUT1_UNIPOLAR. If DACOUT1_UNIPOLAR = 1, $0V == 0pu$ of $\text{algorithmVariable} * \text{DACOUT1\_SCALING} / 8$ , $3V == 1pu$ of $\text{algorithmVariable} * \text{DACOUT1\_SCALING} / 8$ If DACOUT1_UNIPOLAR = 0, $0V == -1pu$ of $\text{algorithmVariable} * \text{DACOUT1\_SCALING} / 8$ , $3V == 1pu$ of $\text{algorithmVariable} * \text{DACOUT1\_SCALING} / 8$<br>0h = Treated as Enum with max value being 31<br>1h = 1 / 8<br>2h = 2 / 8<br>3h = 3 / 8<br>4h = 4 / 8<br>5h = 5 / 8<br>6h = 6 / 8<br>7h = 7 / 8<br>8h = 8 / 8<br>9h = 9 / 8<br>Ah = 10 / 8<br>Bh = 11 / 8<br>Ch = 12 / 8<br>Dh = 13 / 8<br>Eh = 14 / 8<br>Fh = 15 / 8 |

**Table 7-61. DAC\_1 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description  |
|------|------------------|------|-------|--|
| 12   | DACOUT1_UNIPOLAR | W    | 0h    | Configures output of DACOUT1 If DACOUT1_UNIPOLAR = 1, 0V == 0pu of algorithmVariable * DACOUT1_SCALING / 16, 3V == 1pu of algorithmVariable * DACOUT1_SCALING / 16 If DACOUT1_UNIPOLAR = 0, 0V == -1pu of algorithmVariable * DACOUT1_SCALING / 16, 3V == 1pu of algorithmVariable * DACOUT1_SCALING / 16<br>0h = Bipolar (Offset of 1.5 V)<br>1h = Unipolar (No Offset) |
| 11-0 | DACOUT1_VAR_ADDR | R/W  | 0h    | 12-bit address of variable to be monitored   |

### 7.8.4.6 DAC\_2 Register (Offset = F6h) [Reset = 80XX0000h]

DAC\_2 is shown in [Figure 7-88](#) and described in [Table 7-62](#).

Return to the [Summary Table](#).

DAC2 Control Register

**Figure 7-88. DAC\_2 Register**

|                  |                      |                  |        |    |                 |    |    |
|------------------|----------------------|------------------|--------|----|-----------------|----|----|
| 31               | 30                   | 29               | 28     | 27 | 26              | 25 | 24 |
| RESERVED         |                      |                  |        |    |                 |    |    |
| R-0h             |                      |                  |        |    |                 |    |    |
| 23               | 22                   | 21               | 20     | 19 | 18              | 17 | 16 |
| RESERVED         | DACOUT2_ENUM_SCALING |                  |        |    | DACOUT2_SCALING |    |    |
| R-0h             |                      | W-X              |        |    | W-8h            |    |    |
| 15               | 14                   | 13               | 12     | 11 | 10              | 9  | 8  |
| DACOUT2_SCALING  | DACOUT2_UNIPOLAR     | DACOUT2_VAR_ADDR |        |    |                 |    |    |
| W-8h             |                      | W-0h             | R/W-0h |    |                 |    |    |
| 7                | 6                    | 5                | 4      | 3  | 2               | 1  | 0  |
| DACOUT2_VAR_ADDR |                      |                  |        |    |                 |    |    |
| R/W-0h           |                      |                  |        |    |                 |    |    |

**Table 7-62. DAC\_2 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description   |
|-------|----------------------|------|-------|---|
| 31-23 | RESERVED             | R    | 0h    | Reserved  |
| 22-19 | DACOUT2_ENUM_SCALING | W    | X     | Multiplication Factor for DACOUT2 Algorithm Variable extracted from the address contained in DACOUT2_VAR_ADDR multiplied with $2^{\text{DACOUT2\_ENUM\_SCALING}}$ . DACOUT2_ENUM_SCALING comes into effect only if DACOUT2_SCALING is zero  |
| 18-15 | DACOUT2_SCALING      | W    | 8h    | Scaling factor for DACOUT2 Algorithm Variable extracted from the address contained in DACOUT2_VAR_ADDR scaled with DACOUT2_SCALING / 8. Actual voltage depends on DACOUT2_UNIPOLAR. If DACOUT2_UNIPOLAR = 1, 0V == 0pu of algorithmVariable * DACOUT2_SCALING / 8, 3V == 1pu of algorithmVariable * DACOUT2_SCALING / 8 If DACOUT2_UNIPOLAR = 0, 0V == -1pu of algorithmVariable * DACOUT2_SCALING / 8, 3V == 1pu of algorithmVariable * DACOUT2_SCALING / 8<br>0h = Treated s Enum with max value being 31<br>1h = 1 / 8<br>2h = 2 / 8<br>3h = 3 / 8<br>4h = 4 / 8<br>5h = 5 / 8<br>6h = 6 / 8<br>7h = 7 / 8<br>8h = 8 / 8<br>9h = 9 / 8<br>Ah = 10 / 8<br>Bh = 11 / 8<br>Ch = 12 / 8<br>Dh = 13 / 8<br>Eh = 14 / 8<br>Fh = 15 / 8 |

**Table 7-62. DAC\_2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description  |
|------|------------------|------|-------|--|
| 14   | DACOUT2_UNIPOLAR | W    | 0h    | Configures output of DACOUT2 If DACOUT2_UNIPOLAR = 1, 0V == 0pu of algorithmVariable * DACOUT2_SCALING / 16, 3V == 1pu of algorithmVariable * DACOUT2_SCALING / 16 If DACOUT2_UNIPOLAR = 0, 0V == -1pu of algorithmVariable * DACOUT2_SCALING / 16, 3V == 1pu of algorithmVariable * DACOUT2_SCALING / 16<br>0h = Bipolar (Offset of 1.5 V)<br>1h = Unipolar (No Offset) |
| 13-0 | DACOUT2_VAR_ADDR | R/W  | 0h    | 14-bit address of variable to be monitored   |

### 7.8.5 Algorithm\_Variables Registers

Table 7-63 lists the memory-mapped registers for the Algorithm\_Variables registers. All register offset addresses not listed in Table 7-63 should be considered as reserved locations and the register contents should not be modified.

**Table 7-63. ALGORITHM\_VARIABLES Registers**

| Offset | Acronym               | Register Name                        | Section            |
|--------|-----------------------|--------------------------------------|--------------------|
| 190h   | ALGORITHM_STATE       | Current Algorithm State Register     | <a href="#">Go</a> |
| 196h   | FG_SPEED_FDBK         | FG Speed Feedback Register           | <a href="#">Go</a> |
| 410h   | BUS_CURRENT           | Calculated DC Bus Current Register   | <a href="#">Go</a> |
| 440h   | PHASE_CURRENT_A       | Measured Current on Phase A Register | <a href="#">Go</a> |
| 442h   | PHASE_CURRENT_B       | Measured Current on Phase B Register | <a href="#">Go</a> |
| 444h   | PHASE_CURRENT_C       | Measured Current on Phase C Register | <a href="#">Go</a> |
| 468h   | CSA_GAIN_FEEDBACK     | CSA Gain Register                    | <a href="#">Go</a> |
| 472h   | VOLTAGE_GAIN_FEEDBACK | Voltage Gain Register                | <a href="#">Go</a> |
| 476h   | VM_VOLTAGE            | VM Voltage Register                  | <a href="#">Go</a> |
| 47Ah   | PHASE_VOLTAGE_VA      | Phase A Voltage Register             | <a href="#">Go</a> |
| 47Ch   | PHASE_VOLTAGE_VB      | Phase B Voltage Register             | <a href="#">Go</a> |
| 47Eh   | PHASE_VOLTAGE_VC      | Phase C Voltage Register             | <a href="#">Go</a> |
| 4B6h   | SIN_COMMUTATION_ANGLE | Sine of Commutation Angle            | <a href="#">Go</a> |
| 4B8h   | COS_COMMUTATION_ANGLE | Cosine of Commutation Angle          | <a href="#">Go</a> |
| 4D2h   | IALPHA                | IALPHA Current Register              | <a href="#">Go</a> |
| 4D4h   | IBETA                 | IBETA Current Register               | <a href="#">Go</a> |
| 4D6h   | VALPHA                | VALPHA Voltage Register              | <a href="#">Go</a> |
| 4D8h   | VBETA                 | VBETA Voltage Register               | <a href="#">Go</a> |
| 4E2h   | ID                    | Measured d-axis Current Register     | <a href="#">Go</a> |
| 4E4h   | IQ                    | Measured q-axis Current Register     | <a href="#">Go</a> |
| 4E6h   | VD                    | VD Voltage Register                  | <a href="#">Go</a> |
| 4E8h   | VQ                    | VQ Voltage Register                  | <a href="#">Go</a> |
| 524h   | IQ_REF_ROTOR_ALIGN    | Align Current Reference              | <a href="#">Go</a> |
| 53Ch   | SPEED_REF_OPEN_LOOP   | Open Loop Speed Register             | <a href="#">Go</a> |
| 54Ch   | IQ_REF_OPEN_LOOP      | Open Loop Current Reference          | <a href="#">Go</a> |
| 5D4h   | SPEED_REF_CLOSED_LOOP | Speed Reference Register             | <a href="#">Go</a> |
| 606h   | ID_REF_CLOSED_LOOP    | Reference for Current Loop Register  | <a href="#">Go</a> |
| 608h   | IQ_REF_CLOSED_LOOP    | Reference for Current Loop Register  | <a href="#">Go</a> |
| 682h   | ISD_STATE             | ISD State Register                   | <a href="#">Go</a> |
| 68Ch   | ISD_SPEED             | ISD Speed Register                   | <a href="#">Go</a> |
| 6C0h   | IPD_STATE             | IPD State Register                   | <a href="#">Go</a> |



**Table 7-63. ALGORITHM\_VARIABLES Registers (continued)**

| Offset | Acronym    | Register Name                     | Section            |
|--------|------------|-----------------------------------|--------------------|
| 704h   | IPD_ANGLE  | Calculated IPD Angle Register     | <a href="#">Go</a> |
| 74Ah   | ED         | Estimated BEMF EQ Register        | <a href="#">Go</a> |
| 74Ch   | EQ         | Estimated BEMF ED Register        | <a href="#">Go</a> |
| 75Ah   | SPEED_FDBK | Speed Feedback Register           | <a href="#">Go</a> |
| 75Eh   | THETA_EST  | Estimated rotor Position Register | <a href="#">Go</a> |

Complex bit access types are encoded to fit into small table cells. [Table 7-64](#) shows the codes that are used for access types in this section.

**Table 7-64. Algorithm\_Variables Access Type Codes**

| Access Type            | Code | Description                            |
|------------------------|------|--|
| Read Type              |      |  |
| R                      | R    | Read                                   |
| Reset or Default Value |      |  |
| -n                     |      | Value after reset or the default value |

### 7.8.5.1 ALGORITHM\_STATE Register (Offset = 190h) [Reset = 0000h]

ALGORITHM\_STATE is shown in [Figure 7-89](#) and described in [Table 7-65](#).

Return to the [Summary Table](#).

Current Algorithm State Register

**Figure 7-89. ALGORITHM\_STATE Register**

|                 |    |    |    |    |    |   |   |
|-----------------|----|----|----|----|----|---|---|
| 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ALGORITHM_STATE |    |    |    |    |    |   |   |
| R-0h            |    |    |    |    |    |   |   |
| 7               | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| ALGORITHM_STATE |    |    |    |    |    |   |   |
| R-0h            |    |    |    |    |    |   |   |

**Table 7-65. ALGORITHM\_STATE Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description  |
|------|-----------------|------|-------|--|
| 15-0 | ALGORITHM_STATE | R    | 0h    | 16-bit value indicating current state of device<br>0h = MOTOR_IDLE<br>1h = MOTOR_ISD<br>2h = MOTOR_TRISTATE<br>3h = MOTOR_BRAKE_ON_START<br>4h = MOTOR_IPD<br>5h = MOTOR_SLOW_FIRST_CYCLE<br>6h = MOTOR_ALIGN<br>7h = MOTOR_OPEN_LOOP<br>8h = MOTOR_CLOSED_LOOP_UNALIGNED<br>9h = MOTOR_CLOSED_LOOP_ALIGNED<br>Ah = MOTOR_CLOSED_LOOP_ACTIVE_BRAKING<br>Bh = MOTOR_SOFT_STOP<br>Ch = MOTOR_RECIRCULATE_STOP<br>Dh = MOTOR_BRAKE_ON_STOP<br>Eh = MOTOR_FAULT<br>Fh = MOTOR_MPET_MOTOR_STOP_CHECK<br>10h = MOTOR_MPET_MOTOR_STOP_WAIT<br>11h = MOTOR_MPET_MOTOR_BRAKE<br>12h = MOTOR_MPET_ALGORITHM_PARAMETERS_INIT<br>13h = MOTOR_MPET_RL_MEASURE<br>14h = MOTOR_MPET_KE_MEASURE<br>15h = MOTOR_MPET_STALL_CURRENT_MEASURE<br>16h = MOTOR_MPET_TORQUE_MODE<br>17h = MOTOR_MPET_DONE<br>18h = MOTOR_MPET_FAULT |

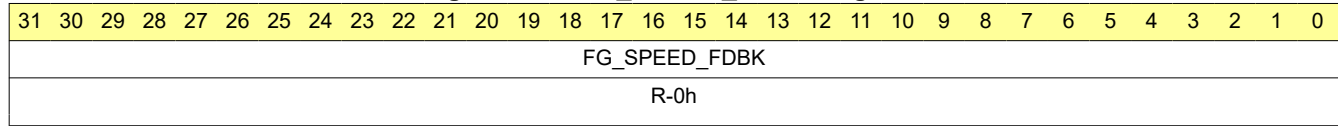
**7.8.5.2 FG\_SPEED\_FDBK Register (Offset = 196h) [Reset = 0000000h]**

FG\_SPEED\_FDBK is shown in [Figure 7-90](#) and described in [Table 7-66](#).

Return to the [Summary Table](#).

Speed Feedback from FG

**Figure 7-90. FG\_SPEED\_FDBK Register**



**Table 7-66. FG\_SPEED\_FDBK Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description  |
|------|---------------|------|-------|--|
| 31-0 | FG_SPEED_FDBK | R    | 0h    | 32-bit unsigned value indicating absolute estimated rotor speed $estimatedSpeed = (FG\_SPEED\_FDBK / 2^{27}) * MAXIMUM\_SPEED\_HZ$ |

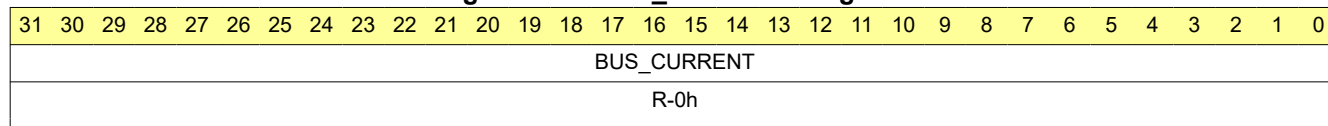
### 7.8.5.3 BUS\_CURRENT Register (Offset = 410h) [Reset = 00000000h]

BUS\_CURRENT is shown in [Figure 7-91](#) and described in [Table 7-67](#).

Return to the [Summary Table](#).

Calculated Supply Current Register

**Figure 7-91. BUS\_CURRENT Register**



**Table 7-67. BUS\_CURRENT Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description  |
|------|-------------|------|-------|--|
| 31-0 | BUS_CURRENT | R    | 0h    | 32-bit signed value indicating bus current. Negative value is represented in two's complement $iBus = (BUS\_CURRENT / 2^{27}) * Base\_Current/8$ |

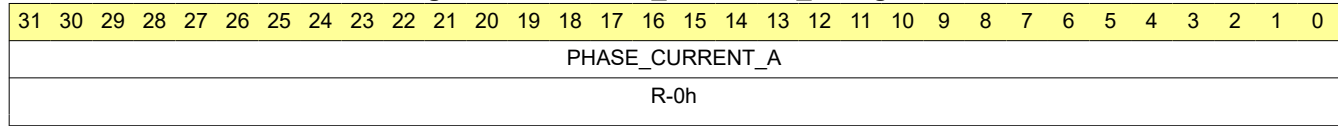
**7.8.5.4 PHASE\_CURRENT\_A Register (Offset = 440h) [Reset = 0000000h]**

PHASE\_CURRENT\_A is shown in [Figure 7-92](#) and described in [Table 7-68](#).

Return to the [Summary Table](#).

Measured current on Phase A Register

**Figure 7-92. PHASE\_CURRENT\_A Register**



**Table 7-68. PHASE\_CURRENT\_A Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description  |
|------|-----------------|------|-------|--|
| 31-0 | PHASE_CURRENT_A | R    | 0h    | 32-bit signed value indicating measured current on Phase A. Negative value is represented in two's complement $i_A = (\text{PHASE\_CURRENT\_A} / 2^{27}) * \text{Base\_Current}/8$ |

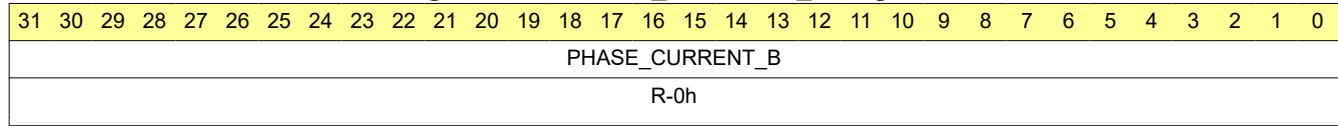
### 7.8.5.5 PHASE\_CURRENT\_B Register (Offset = 442h) [Reset = 0000000h]

PHASE\_CURRENT\_B is shown in [Figure 7-93](#) and described in [Table 7-69](#).

Return to the [Summary Table](#).

Measured current on Phase B Register

**Figure 7-93. PHASE\_CURRENT\_B Register**



**Table 7-69. PHASE\_CURRENT\_B Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description   |
|------|-----------------|------|-------|---|
| 31-0 | PHASE_CURRENT_B | R    | 0h    | 32-bit signed value indicating measured current on Phase B. Negative value is represented in two's complement $iB = (PHASE\_CURRENT\_B / 2^{27}) * Base\_Current/8$ |

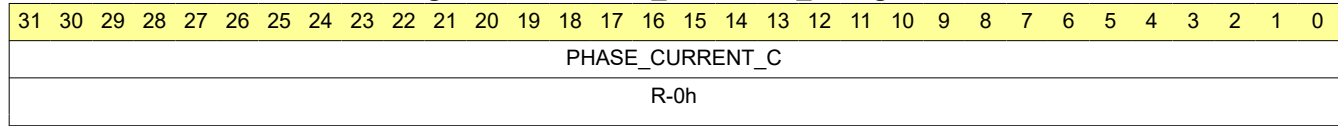
**7.8.5.6 PHASE\_CURRENT\_C Register (Offset = 444h) [Reset = 0000000h]**

PHASE\_CURRENT\_C is shown in [Figure 7-94](#) and described in [Table 7-70](#).

Return to the [Summary Table](#).

Measured current on Phase C Register

**Figure 7-94. PHASE\_CURRENT\_C Register**



**Table 7-70. PHASE\_CURRENT\_C Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description  |
|------|-----------------|------|-------|--|
| 31-0 | PHASE_CURRENT_C | R    | 0h    | 32-bit signed value indicating measured current on Phase C. Negative value is represented in two's complement $i_C = (\text{PHASE\_CURRENT\_C} / 2^{27}) * \text{Base\_Current}/8$ |

### 7.8.5.7 CSA\_GAIN\_FEEDBACK Register (Offset = 468h) [Reset = 0000h]

CSA\_GAIN\_FEEDBACK is shown in [Figure 7-95](#) and described in [Table 7-71](#).

Return to the [Summary Table](#).

VM Voltage Register

**Figure 7-95. CSA\_GAIN\_FEEDBACK Register**

|                   |    |    |    |    |    |   |   |
|-------------------|----|----|----|----|----|---|---|
| 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CSA_GAIN_FEEDBACK |    |    |    |    |    |   |   |
| R-0h              |    |    |    |    |    |   |   |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CSA_GAIN_FEEDBACK |    |    |    |    |    |   |   |
| R-0h              |    |    |    |    |    |   |   |

**Table 7-71. CSA\_GAIN\_FEEDBACK Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description  |
|------|-------------------|------|-------|--|
| 15-0 | CSA_GAIN_FEEDBACK | R    | 0h    | 16-bit value indicating current sense gain<br>0h = MAX_CSA_GAIN * 8<br>1h = MAX_CSA_GAIN * 4<br>2h = MAX_CSA_GAIN * 2<br>3h = MAX_CSA_GAIN * 1 |



### 7.8.5.8 VOLTAGE\_GAIN\_FEEDBACK Register (Offset = 472h) [Reset = 0000h]

VOLTAGE\_GAIN\_FEEDBACK is shown in [Figure 7-96](#) and described in [Table 7-72](#).

Return to the [Summary Table](#).

Voltage Gain Register

**Figure 7-96. VOLTAGE\_GAIN\_FEEDBACK Register**

|                       |    |    |    |    |    |   |   |
|-----------------------|----|----|----|----|----|---|---|
| 15                    | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VOLTAGE_GAIN_FEEDBACK |    |    |    |    |    |   |   |
| R-0h                  |    |    |    |    |    |   |   |
| 7                     | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| VOLTAGE_GAIN_FEEDBACK |    |    |    |    |    |   |   |
| R-0h                  |    |    |    |    |    |   |   |

**Table 7-72. VOLTAGE\_GAIN\_FEEDBACK Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description  |
|------|-----------------------|------|-------|--|
| 15-0 | VOLTAGE_GAIN_FEEDBACK | R    | 0h    | 16-bit value indicating voltage gain<br>0h = 60V<br>1h = 30V<br>2h = 15V |

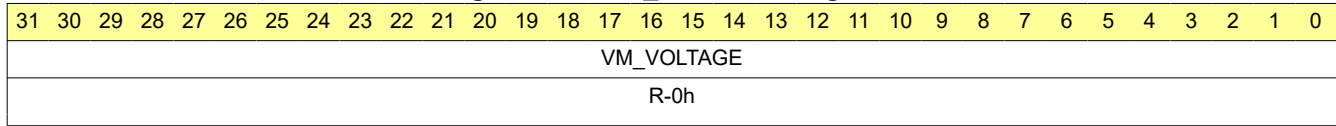
**7.8.5.9 VM\_VOLTAGE Register (Offset = 476h) [Reset = 0000000h]**

VM\_VOLTAGE is shown in [Figure 7-97](#) and described in [Table 7-73](#).

Return to the [Summary Table](#).

Supply voltage register

**Figure 7-97. VM\_VOLTAGE Register**



**Table 7-73. VM\_VOLTAGE Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description   |
|------|------------|------|-------|---|
| 31-0 | VM_VOLTAGE | R    | 0h    | 32-bit value indicating dc bus voltage DC Bus Voltage = VM_VOLTAGE * 60 / 2 <sup>27</sup> |

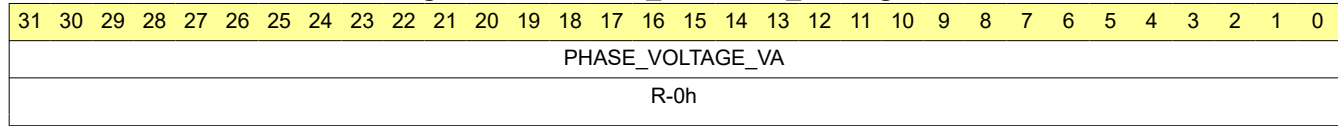
**7.8.5.10 PHASE\_VOLTAGE\_VA Register (Offset = 47Ah) [Reset = 0000000h]**

PHASE\_VOLTAGE\_VA is shown in [Figure 7-98](#) and described in [Table 7-74](#).

Return to the [Summary Table](#).

Phase A Voltage Register

**Figure 7-98. PHASE\_VOLTAGE\_VA Register**



**Table 7-74. PHASE\_VOLTAGE\_VA Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description   |
|------|------------------|------|-------|---|
| 31-0 | PHASE_VOLTAGE_VA | R    | 0h    | 32-bit value indicating Phase Voltage Va during ISD Phase A voltage<br>= PHASE_VOLTAGE_VA * 60 / (sqrt(3) * 2 <sup>27</sup> ) |

### 7.8.5.11 PHASE\_VOLTAGE\_VB Register (Offset = 47Ch) [Reset = 0000000h]

PHASE\_VOLTAGE\_VB is shown in [Figure 7-99](#) and described in [Table 7-75](#).

Return to the [Summary Table](#).

Phase B Voltage Register

**Figure 7-99. PHASE\_VOLTAGE\_VB Register**

|                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PHASE_VOLTAGE_VB |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**Table 7-75. PHASE\_VOLTAGE\_VB Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description  |
|------|------------------|------|-------|--|
| 31-0 | PHASE_VOLTAGE_VB | R    | 0h    | 32-bit value indicating Phase Voltage Vb during ISD Phase B voltage = PHASE_VOLTAGE_VB * 60 / (sqrt(3) * 2 <sup>27</sup> ) |

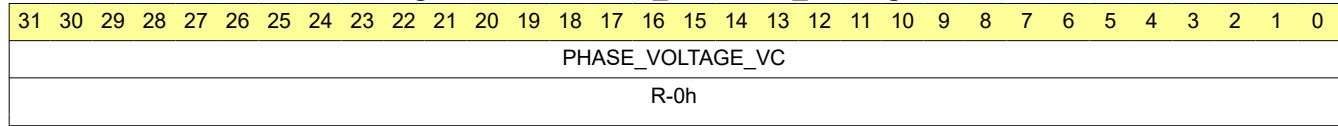
**7.8.5.12 PHASE\_VOLTAGE\_VC Register (Offset = 47Eh) [Reset = 0000000h]**

PHASE\_VOLTAGE\_VC is shown in [Figure 7-100](#) and described in [Table 7-76](#).

Return to the [Summary Table](#).

Phase C Voltage Register

**Figure 7-100. PHASE\_VOLTAGE\_VC Register**



**Table 7-76. PHASE\_VOLTAGE\_VC Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description   |
|------|------------------|------|-------|---|
| 31-0 | PHASE_VOLTAGE_VC | R    | 0h    | 32-bit value indicating Phase Voltage Vc during ISD Phase C voltage = $PHASE\_VOLTAGE\_VC * 60 / (\sqrt{3}) * 2^{27}$ |

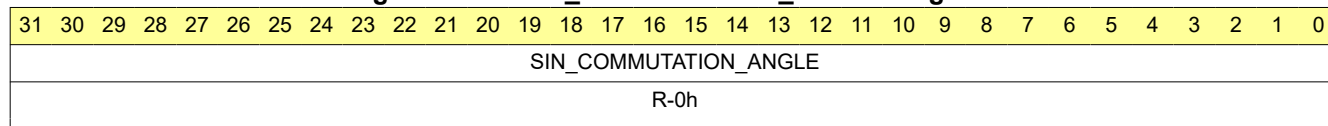
### 7.8.5.13 SIN\_COMMUTATION\_ANGLE Register (Offset = 4B6h) [Reset = 0000000h]

SIN\_COMMUTATION\_ANGLE is shown in [Figure 7-101](#) and described in [Table 7-77](#).

Return to the [Summary Table](#).

Sine of Commutation Angle

**Figure 7-101. SIN\_COMMUTATION\_ANGLE Register**



**Table 7-77. SIN\_COMMUTATION\_ANGLE Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description  |
|------|-----------------------|------|-------|--|
| 31-0 | SIN_COMMUTATION_ANGLE | R    | 0h    | 32-bit signed value indicating sine of commutation Angle. Negative value is represented in two's complement $\text{sinCommutationAngle} = (\text{SIN\_COMMUTATION\_ANGLE} / 2^{27})$ |

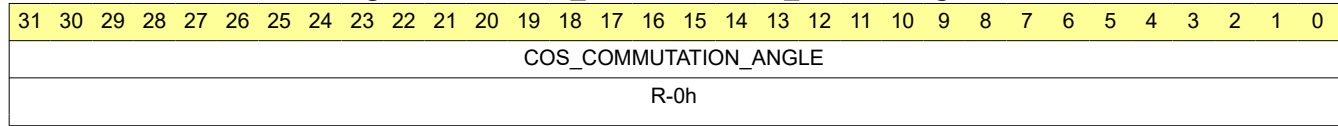
**7.8.5.14 COS\_COMMUTATION\_ANGLE Register (Offset = 4B8h) [Reset = 0000000h]**

COS\_COMMUTATION\_ANGLE is shown in [Figure 7-102](#) and described in [Table 7-78](#).

Return to the [Summary Table](#).

Cosine of Commutation Angle

**Figure 7-102. COS\_COMMUTATION\_ANGLE Register**



**Table 7-78. COS\_COMMUTATION\_ANGLE Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description  |
|------|-----------------------|------|-------|--|
| 31-0 | COS_COMMUTATION_ANGLE | R    | 0h    | 32-bit signed value indicating cosine of commutation Angle. Negative value is represented in two's complement $\text{cosCommutationAngle} = (\text{COS\_COMMUTATION\_ANGLE} / 2^{27})$ |

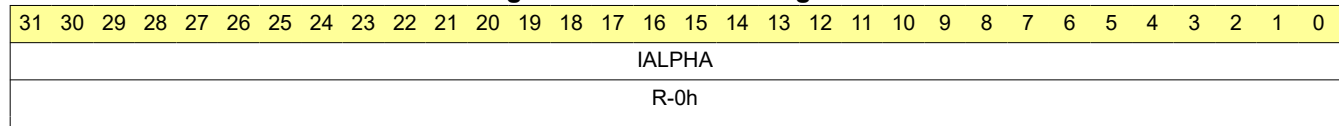
### 7.8.5.15 IALPHA Register (Offset = 4D2h) [Reset = 0000000h]

IALPHA is shown in [Figure 7-103](#) and described in [Table 7-79](#).

Return to the [Summary Table](#).

IALPHA Current Register

**Figure 7-103. IALPHA Register**



**Table 7-79. IALPHA Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description  |
|------|--------|------|-------|--|
| 31-0 | IALPHA | R    | 0h    | 32-bit signed value indicating calculated IALPHA. Negative value is represented in two's complement $iAlpha = (IALPHA / 2^{27}) * Base\_Current/8$ |



**7.8.5.16 IBETA Register (Offset = 4D4h) [Reset = 0000000h]**

IBETA is shown in [Figure 7-104](#) and described in [Table 7-80](#).

Return to the [Summary Table](#).

IBETA Current Register

**Figure 7-104. IBETA Register**

|       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IBETA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**Table 7-80. IBETA Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---|
| 31-0 | IBETA | R    | 0h    | 32-bit signed value indicating calculated IBETA. Negative value is represented in two's complement $iBeta = (IBETA / 2^{27}) * Base\_Current/8$ |

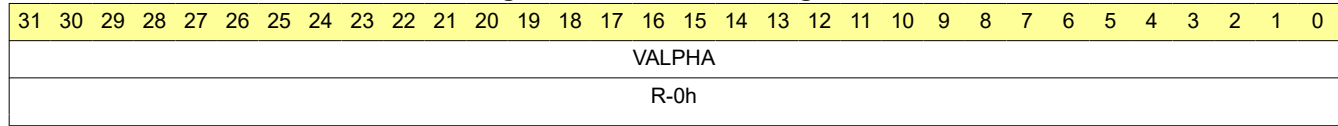
**7.8.5.17 VALPHA Register (Offset = 4D6h) [Reset = 0000000h]**

VALPHA is shown in [Figure 7-105](#) and described in [Table 7-81](#).

Return to the [Summary Table](#).

VALPHA Voltage Register

**Figure 7-105. VALPHA Register**



**Table 7-81. VALPHA Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description  |
|------|--------|------|-------|--|
| 31-0 | VALPHA | R    | 0h    | 32-bit signed value indicating calculated VALPHA. Negative value is represented in two's complement $vAlpha = (VALPHA / 2^{27}) * 60 / \sqrt{3}$ |

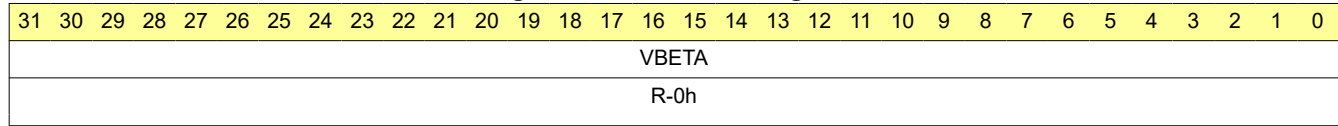
**7.8.5.18 VBETA Register (Offset = 4D8h) [Reset = 0000000h]**

VBETA is shown in [Figure 7-106](#) and described in [Table 7-82](#).

Return to the [Summary Table](#).

VBETA Voltage Register

**Figure 7-106. VBETA Register**



**Table 7-82. VBETA Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---|
| 31-0 | VBETA | R    | 0h    | 32-bit signed value indicating calculated VBETA. Negative value is represented in two's complement $vBeta = (VBETA / 2^{27}) * 60 / \text{sqrt}(3)$ |

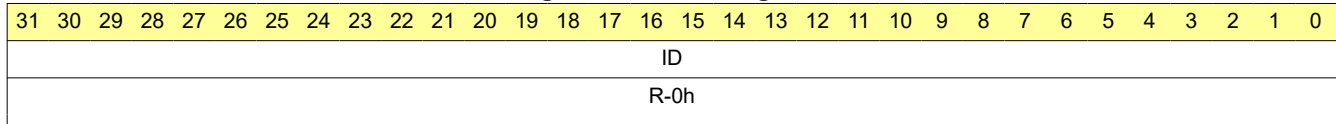
### 7.8.5.19 ID Register (Offset = 4E2h) [Reset = 0000000h]

ID is shown in [Figure 7-107](#) and described in [Table 7-83](#).

Return to the [Summary Table](#).

Measured d-axis Current Register

**Figure 7-107. ID Register**



**Table 7-83. ID Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---|
| 31-0 | ID    | R    | 0h    | 32-bit signed value indicating estimated Id. Negative value is represented in two's complement $id = (ID / 2^{27}) * Base\_Current/8$ |

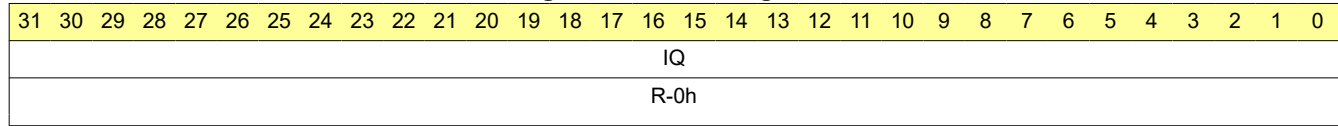
**7.8.5.20 IQ Register (Offset = 4E4h) [Reset = 0000000h]**

IQ is shown in [Figure 7-108](#) and described in [Table 7-84](#).

Return to the [Summary Table](#).

Measured q-axis Current Register

**Figure 7-108. IQ Register**



**Table 7-84. IQ Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---|
| 31-0 | IQ    | R    | 0h    | 32-bit signed value indicating estimated Iq. Negative value is represented in two's complement $iq = (IQ / 2^{27}) * Base\_Current/8$ |

**7.8.5.21 VD Register (Offset = 4E6h) [Reset = 0000000h]**

VD is shown in [Figure 7-109](#) and described in [Table 7-85](#).

Return to the [Summary Table](#).

VD Voltage Register

**Figure 7-109. VD Register**

|      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VD   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**Table 7-85. VD Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---|
| 31-0 | VD    | R    | 0h    | 32-bit signed value indicating applied Vd. Negative value is represented in two's complement $vd = (VD / 2^{27}) * 60 / \text{sqrt}(3)$ |

### 7.8.5.22 VQ Register (Offset = 4E8h) [Reset = 0000000h]

VQ is shown in [Figure 7-110](#) and described in [Table 7-86](#).

Return to the [Summary Table](#).

VQ Voltage Register

**Figure 7-110. VQ Register**

|      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VQ   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**Table 7-86. VQ Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---|
| 31-0 | VQ    | R    | 0h    | 32-bit signed value indicating applied Vq. Negative value is represented in two's complement $vq = (VQ / 2^{27}) * 60 / \text{sqrt}(3)$ |

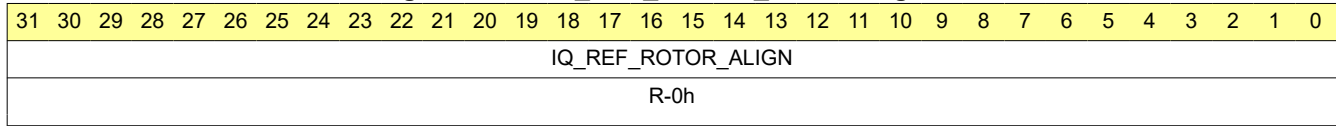
**7.8.5.23 IQ\_REF\_ROTATOR\_ALIGN Register (Offset = 524h) [Reset = 0000000h]**

IQ\_REF\_ROTATOR\_ALIGN is shown in [Figure 7-111](#) and described in [Table 7-87](#).

Return to the [Summary Table](#).

Align Current Reference

**Figure 7-111. IQ\_REF\_ROTATOR\_ALIGN Register**



**Table 7-87. IQ\_REF\_ROTATOR\_ALIGN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description  |
|------|----------------------|------|-------|--|
| 31-0 | IQ_REF_ROTATOR_ALIGN | R    | 0h    | 32-bit signed value indicating Align Current Reference. Negative value is represented in two's complement $iqRefRotorAlign = (IQ\_REF\_ROTATOR\_ALIGN / 2^{27}) * Base\_Current/8$ |



### 7.8.5.24 SPEED\_REF\_OPEN\_LOOP Register (Offset = 53Ch) [Reset = 0000000h]

SPEED\_REF\_OPEN\_LOOP is shown in [Figure 7-112](#) and described in [Table 7-88](#).

Return to the [Summary Table](#).

Speed at which motor transitions to close loop

**Figure 7-112. SPEED\_REF\_OPEN\_LOOP Register**

|                     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPEED_REF_OPEN_LOOP |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**Table 7-88. SPEED\_REF\_OPEN\_LOOP Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description   |
|------|---------------------|------|-------|---|
| 31-0 | SPEED_REF_OPEN_LOOP | R    | 0h    | 32-bit signed value indicating Open Loop Speed. The value is positive for OUTA-OUTB-OUTC and Negative and represented in two's complement for OUTA-OUTC-OUTB<br>$\text{openLoopSpeedRef} = (\text{SPEED\_REF\_OPEN\_LOOP} / 2^{27}) * \text{MAX\_SPEED (Hz)}$ |

### 7.8.5.25 IQ\_REF\_OPEN\_LOOP Register (Offset = 54Ch) [Reset = 0000000h]

IQ\_REF\_OPEN\_LOOP is shown in [Figure 7-113](#) and described in [Table 7-89](#).

Return to the [Summary Table](#).

Open Loop Current Reference

**Figure 7-113. IQ\_REF\_OPEN\_LOOP Register**

|                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IQ_REF_OPEN_LOOP |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**Table 7-89. IQ\_REF\_OPEN\_LOOP Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description  |
|------|------------------|------|-------|--|
| 31-0 | IQ_REF_OPEN_LOOP | R    | 0h    | 32-bit signed value indicating Open Loop Current Reference. Negative value is represented in two's complement $iqRefOpenLoop = (IQ\_REF\_OPEN\_LOOP / 2^{27}) * Base\_Current/8$ |

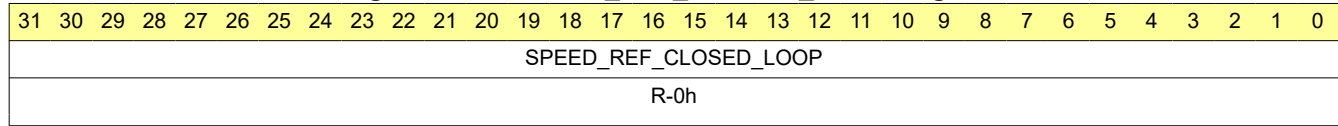
**7.8.5.26 SPEED\_REF\_CLOSED\_LOOP Register (Offset = 5D4h) [Reset = 0000000h]**

SPEED\_REF\_CLOSED\_LOOP is shown in [Figure 7-114](#) and described in [Table 7-90](#).

Return to the [Summary Table](#).

Speed Reference Register

**Figure 7-114. SPEED\_REF\_CLOSED\_LOOP Register**



**Table 7-90. SPEED\_REF\_CLOSED\_LOOP Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description  |
|------|-----------------------|------|-------|--|
| 31-0 | SPEED_REF_CLOSED_LOOP | R    | 0h    | 32-bit signed value indicating reference for speed loop. The value is positive for OUTA-OUTB-OUTC and Negative and represented in two's complement for OUTA-OUTC-OUTB Speed Reference in closed loop (Hz) = (SPEED_REF_CLOSED_LOOP/ 2 <sup>27</sup> ) * MAX_SPEED (Hz) |

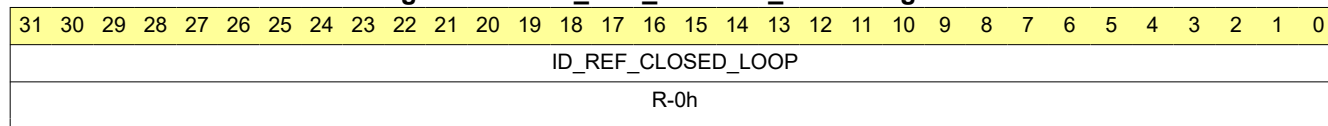
### 7.8.5.27 ID\_REF\_CLOSED\_LOOP Register (Offset = 606h) [Reset = 0000000h]

ID\_REF\_CLOSED\_LOOP is shown in [Figure 7-115](#) and described in [Table 7-91](#).

Return to the [Summary Table](#).

Reference for Current Loop Register

**Figure 7-115. ID\_REF\_CLOSED\_LOOP Register**



**Table 7-91. ID\_REF\_CLOSED\_LOOP Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description   |
|------|--------------------|------|-------|---|
| 31-0 | ID_REF_CLOSED_LOOP | R    | 0h    | 32-bit signed value indicating Id_ref for flux loop. Negative value is represented in two's complement $idRefClosedLoop = (ID\_REF\_CLOSED\_LOOP / 2^{27}) * Base\_Current/8$ |

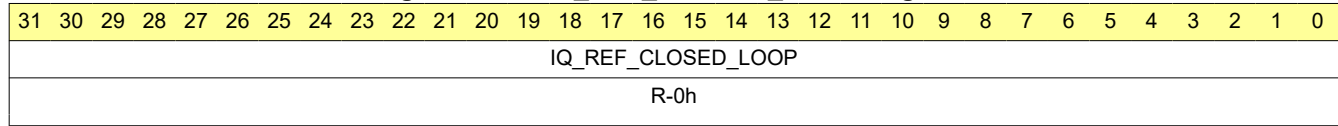
**7.8.5.28 IQ\_REF\_CLOSED\_LOOP Register (Offset = 608h) [Reset = 0000000h]**

IQ\_REF\_CLOSED\_LOOP is shown in [Figure 7-116](#) and described in [Table 7-92](#).

Return to the [Summary Table](#).

Reference for Current Loop Register

**Figure 7-116. IQ\_REF\_CLOSED\_LOOP Register**



**Table 7-92. IQ\_REF\_CLOSED\_LOOP Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description   |
|------|--------------------|------|-------|---|
| 31-0 | IQ_REF_CLOSED_LOOP | R    | 0h    | 32-bit signed value indicating Iq_ref for torque loop. Negative value is represented in two's complement $iqRefClosedLoop = (IQ\_REF\_CLOSED\_LOOP / 2^{27}) * Base\_Current/8$ |

**7.8.5.29 ISD\_STATE Register (Offset = 682h) [Reset = 0000h]**

ISD\_STATE is shown in [Figure 7-117](#) and described in [Table 7-93](#).

Return to the [Summary Table](#).

ISD state Register

**Figure 7-117. ISD\_STATE Register**

|           |    |    |    |    |    |   |   |
|-----------|----|----|----|----|----|---|---|
| 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISD_STATE |    |    |    |    |    |   |   |
| R-0h      |    |    |    |    |    |   |   |
| 7         | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| ISD_STATE |    |    |    |    |    |   |   |
| R-0h      |    |    |    |    |    |   |   |

**Table 7-93. ISD\_STATE Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description   |
|------|-----------|------|-------|---|
| 15-0 | ISD_STATE | R    | 0h    | 16-bit value indicating current ISD state<br>0h = ISD_INIT<br>1h = ISD_MOTOR_STOP_CHECK<br>2h = ISD_ESTIM_INIT<br>3h = ISD_RUN_MOTOR_CHECK<br>4h = ISD_MOTOR_DIRECTION_CHECK<br>5h = ISD_COMPLETE<br>6h = ISD_FAULT |

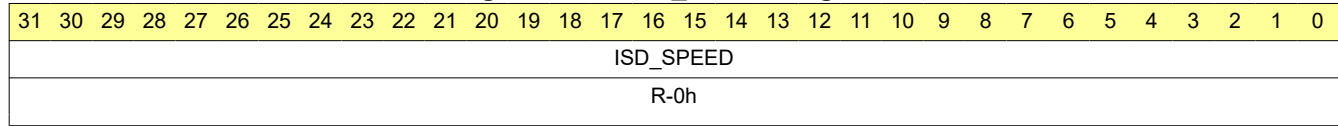
**7.8.5.30 ISD\_SPEED Register (Offset = 68Ch) [Reset = 0000000h]**

ISD\_SPEED is shown in [Figure 7-118](#) and described in [Table 7-94](#).

Return to the [Summary Table](#).

ISD Speed Register

**Figure 7-118. ISD\_SPEED Register**



**Table 7-94. ISD\_SPEED Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description  |
|------|-----------|------|-------|--|
| 31-0 | ISD_SPEED | R    | 0h    | 32-bit value indicating calculated absolute speed during ISD state<br>$isdSpeed = (ISD\_SPEED / 2^{27}) * max\_Speed - In\ Hz$ |

### 7.8.5.31 IPD\_STATE Register (Offset = 6C0h) [Reset = 0000h]

IPD\_STATE is shown in [Figure 7-119](#) and described in [Table 7-95](#).

Return to the [Summary Table](#).

IPD state Register

**Figure 7-119. IPD\_STATE Register**

|           |    |    |    |    |    |   |   |
|-----------|----|----|----|----|----|---|---|
| 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| IPD_STATE |    |    |    |    |    |   |   |
| R-0h      |    |    |    |    |    |   |   |
| 7         | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| IPD_STATE |    |    |    |    |    |   |   |
| R-0h      |    |    |    |    |    |   |   |

**Table 7-95. IPD\_STATE Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description  |
|------|-----------|------|-------|--|
| 15-0 | IPD_STATE | R    | 0h    | 16-bit value indicating current IPD state<br>0h = IPD_INIT<br>1h = IPD_VECTOR_CONFIG<br>2h = IPD_RUN<br>3h = IPD_SLOW_RISE_CLOCK<br>4h = IPD_SLOW_FALL_CLOCK<br>5h = IPD_WAIT_CURRENT_DECAY<br>6h = IPD_GET_TIMES<br>7h = IPD_SET_NEXT_VECTOR<br>8h = IPD_CALC_SECTOR_RISE<br>9h = IPD_CALC_ROTOR_POSITION<br>Ah = IPD_CALC_ANGLE<br>Bh = IPD_COMPLETE<br>Ch = IPD_FAULT |



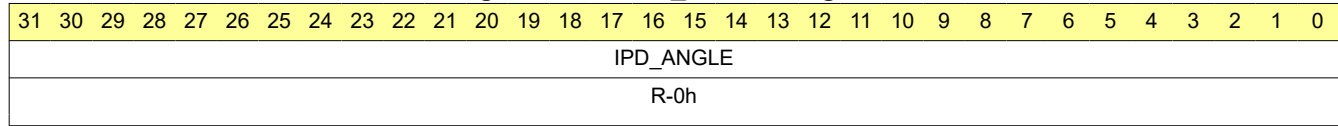
**7.8.5.32 IPD\_ANGLE Register (Offset = 704h) [Reset = 0000000h]**

IPD\_ANGLE is shown in [Figure 7-120](#) and described in [Table 7-96](#).

Return to the [Summary Table](#).

Calculated IPD Angle Register

**Figure 7-120. IPD\_ANGLE Register**



**Table 7-96. IPD\_ANGLE Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description   |
|------|-----------|------|-------|---|
| 31-0 | IPD_ANGLE | R    | 0h    | 32-bit signed value indicating measured IPD angle $ipdAngle = (IPD\_ANGLE / 2^{27}) * 360$ (Degree) |

### 7.8.5.33 ED Register (Offset = 74Ah) [Reset = 0000000h]

ED is shown in [Figure 7-121](#) and described in [Table 7-97](#).

Return to the [Summary Table](#).

Estimated BEMF EQ Register

**Figure 7-121. ED Register**

|      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ED   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**Table 7-97. ED Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---|
| 31-0 | ED    | R    | 0h    | 32-bit signed value indicating estimated ED. Negative value is represented in two's complement $Ed = (ED / 2^{27}) * 60 / \text{sqrt}(3)$ |

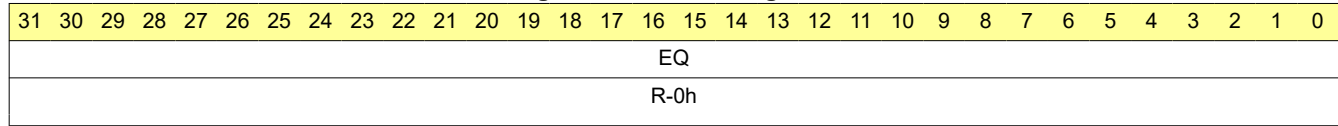
**7.8.5.34 EQ Register (Offset = 74Ch) [Reset = 0000000h]**

EQ is shown in [Figure 7-122](#) and described in [Table 7-98](#).

Return to the [Summary Table](#).

Estimated BEMF ED Register

**Figure 7-122. EQ Register**



**Table 7-98. EQ Register Field Descriptions**

| Bit  | Field | Type | Reset | Description  |
|------|-------|------|-------|--|
| 31-0 | EQ    | R    | 0h    | 32-bit signed value indicating estimated EQ. Negative value is represented in two's complement $E_q = (EQ / 2^{27}) * 60 / \text{sqrt}(3)$ |

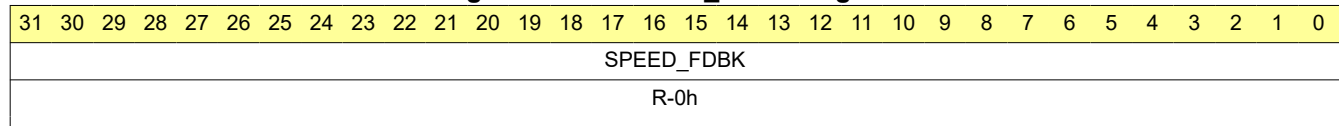
### 7.8.5.35 SPEED\_FDBK Register (Offset = 75Ah) [Reset = 0000000h]

SPEED\_FDBK is shown in [Figure 7-123](#) and described in [Table 7-99](#).

Return to the [Summary Table](#).

Speed Feedback Register

**Figure 7-123. SPEED\_FDBK Register**



**Table 7-99. SPEED\_FDBK Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description  |
|------|------------|------|-------|--|
| 31-0 | SPEED_FDBK | R    | 0h    | 32-bit signed value indicating estimated rotor speed. The value is positive for OUTA-OUTB-OUTC and Negative and represented in two's complement for OUTA-OUTC-OUTB estimatedSpeed = (SPEED_FDBK / 2 <sup>27</sup> )*MAXIMUM_SPEED_HZ |

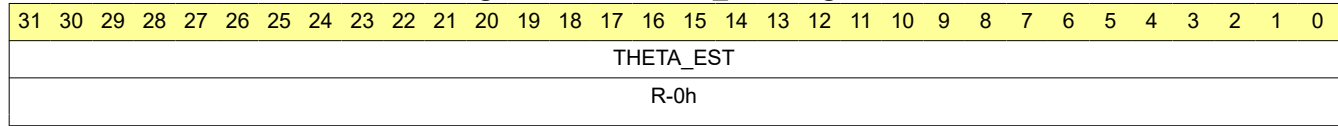
**7.8.5.36 THETA\_EST Register (Offset = 75Eh) [Reset = 0000000h]**

THETA\_EST is shown in [Figure 7-124](#) and described in [Table 7-100](#).

Return to the [Summary Table](#).

Estimated rotor Position Register

**Figure 7-124. THETA\_EST Register**



**Table 7-100. THETA\_EST Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description   |
|------|-----------|------|-------|---|
| 31-0 | THETA_EST | R    | 0h    | 32-bit signed value indicating estimated rotor angle. Negative value is represented in two's complement $estimatedAngle = (THETA\_EST / 2^{27}) * 360$ (Degree) |

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The MCF8316C-Q1 device is used in sensorless 3-phase BLDC motor control. The driver provides a high performance, high-reliability, flexible solution for appliances, fans, pumps, residential and living fans, seat cooling fans, automotive fans and blowers. The following section shows a common application of the MCF8316C-Q1 device.

### 8.2 Typical Applications

Figure 8-1 shows the typical schematic of MCF8316C-Q1.

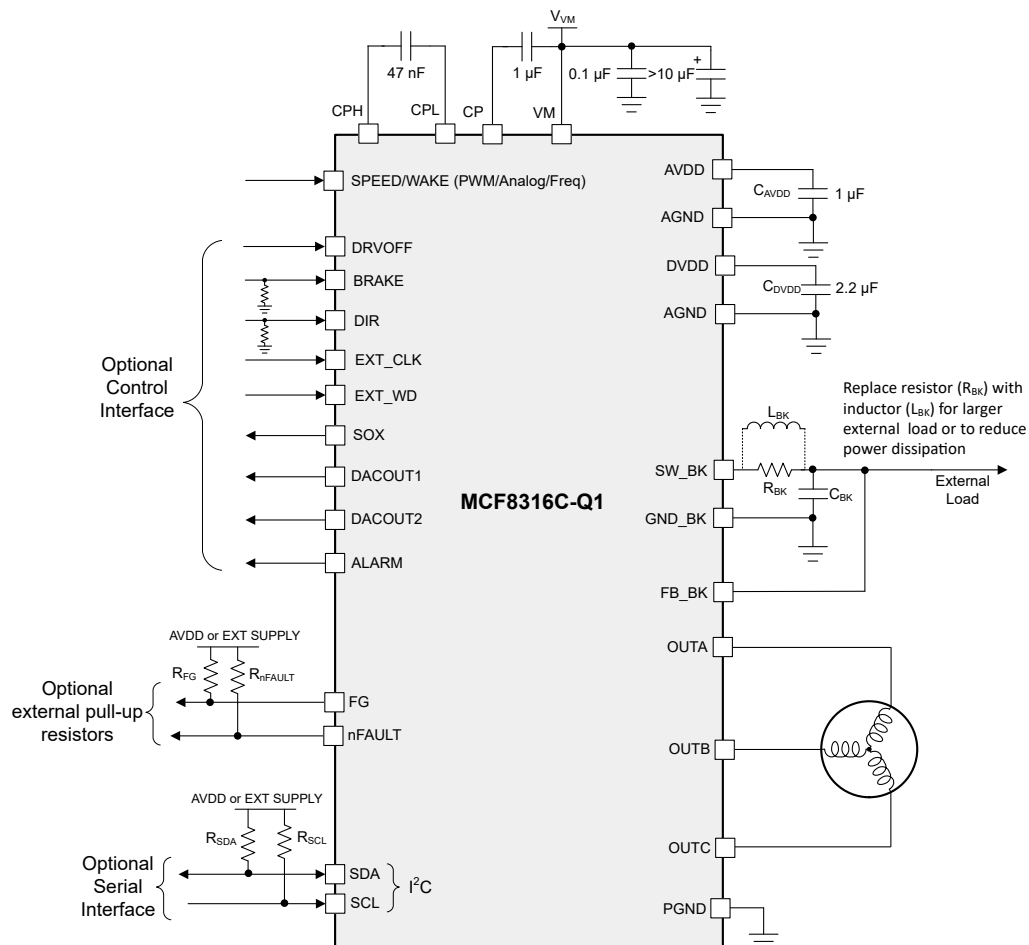


Figure 8-1. Example Application Schematic

Table 8-1 lists the recommended values of the external components for MCF8316C-Q1.

**Table 8-1. MCF8316C-Q1 External Components**

| COMPONENTS          | PIN 1               | PIN 2  | RECOMMENDED   |
|---------------------|---------------------|--------|---|
| C <sub>VM1</sub>    | VM                  | PGND   | X5R or X7R, 0.1-μF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device  |
| C <sub>VM2</sub>    | VM                  | PGND   | ≥ 10-μF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device   |
| C <sub>CP</sub>     | CP                  | VM     | X5R or X7R, 16-V, 1-μF capacitor  |
| C <sub>FLY</sub>    | CPH                 | CPL    | X5R or X7R, 47-nF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin  |
| C <sub>AVDD</sub>   | AVDD                | AGND   | X5R or X7R, 1-μF, ≥ 6.3-V. In order for AVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.7-μF to 1.3-μF at 3.3-V across operating temperature.   |
| C <sub>DVDD</sub>   | DVDD                | DGND   | X5R or X7R, 2.2-μF, ≥ 6.3-V. In order for DVDD to accurately regulate output voltage, capacitor should have effective capacitance between 1.1-μF to 2.5-μF at 1.5-V across operating temperature. |
| C <sub>BK</sub>     | FB_BK               | GND_BK | X5R or X7R, buck-output rated capacitor   |
| L <sub>BK</sub>     | SW_BK               | FB_BK  | Buck-output inductor  |
| R <sub>FG</sub>     | 1.8 to 5-V Supply   | FG     | 5.1-kΩ, Pull-up resistor  |
| R <sub>nFAULT</sub> | 1.8 to 5-V Supply   | nFAULT | 5.1-kΩ, Pull-up resistor  |
| R <sub>SDA</sub>    | 1.8 to 3.3-V Supply | SDA    | 5.1-kΩ, Pull-up resistor  |
| R <sub>SCL</sub>    | 1.8 to 3.3-V Supply | SCL    | 5.1-kΩ, Pull-up resistor  |

Recommended application range for MCF8316C-Q1 is shown in [Table 8-2](#).

**Table 8-2. Recommended Application Range**

| Parameter   | Min   | Max  | Unit  |
|---|-------|------|-------|
| Motor voltage   | 4.5   | 35   | V     |
| Back-EMF constant (see <a href="#">Section 7.3.12.3</a> ) | 0.6   | 2000 | mV/Hz |
| Motor resistance (see <a href="#">Section 7.3.12.1</a> )  | 0.006 | 20   | Ω     |
| Motor inductance (see <a href="#">Section 7.3.12.2</a> )  | 0.006 | 20   | mH    |
| Motor electrical speed                                    | -     | 1500 | Hz    |
| Peak motor phase current                                  | -     | 8    | A     |

Default EEPROM configuration for MCF8316C-Q1 is listed in [Table 8-3](#). Default values are chosen for reliable motor start-up and closed loop operation. Refer to [MCF8316C-Q1 tuning guide](#) which provides step by step procedure to tune a 3-phase BLDC motor in closed loop, conform to use-case and explore features in the device.

**Table 8-3. Recommended Default Values**

| Address Name     | Address    | Recommended Value |
|------------------|------------|-------------------|
| ISD_CONFIG       | 0x00000080 | 0x64738CA0        |
| REV_DRIVE_CONFIG | 0x00000082 | 0x28200000        |
| MOTOR_STARTUP1   | 0x00000084 | 0x0B6807D0        |
| MOTOR_STARTUP2   | 0x00000086 | 0x23066004        |
| CLOSED_LOOP1     | 0x00000088 | 0x113181B8        |
| CLOSED_LOOP2     | 0x0000008A | 0x0BAD0000        |
| CLOSED_LOOP3     | 0x0000008C | 0x00000000        |
| CLOSED_LOOP4     | 0x0000008E | 0x000004B0        |
| SPEED_PROFILES1  | 0x00000094 | 0x00000000        |

**Table 8-3. Recommended Default Values (continued)**

| Address Name    | Address    | Recommended Value |
|-----------------|------------|-------------------|
| SPEED_PROFILES2 | 0x00000096 | 0x00000000        |
| SPEED_PROFILES3 | 0x00000098 | 0x00000006        |
| SPEED_PROFILES4 | 0x0000009A | 0x000D0000        |
| SPEED_PROFILES5 | 0x0000009C | 0x00000000        |
| SPEED_PROFILES6 | 0x0000009E | 0x00000000        |
| FAULT_CONFIG1   | 0x00000090 | 0x3EDA30A6        |
| FAULT_CONFIG2   | 0x00000092 | 0x71522088        |
| PIN_CONFIG      | 0x000000A4 | 0x00000309        |
| DEVICE_CONFIG1  | 0x000000A6 | 0x00100001        |
| DEVICE_CONFIG2  | 0x000000A8 | 0x03E8C000        |
| PERI_CONFIG1    | 0x000000AA | 0x41C45C00        |
| GD_CONFIG1      | 0x000000AC | 0x1C461900        |
| GD_CONFIG2      | 0x000000AE | 0x01840000        |
| INT_ALGO_1      | 0x000000A0 | 0x0D48C175        |
| INT_ALGO_2      | 0x000000A2 | 0x000001A7        |

Once the device EEPROM is programmed with the desired configuration, device can be operated stand-alone and I<sup>2</sup>C serial interface is not required anymore. Speed can be commanded using SPEED pin.

Below are the two essential parameters that are required to spin the motor in closed loop.

1. Maximum motor speed.
2. Current limit for torque PI loop.

## 8.2.1 Application Curves

### 8.2.1.1 Motor startup

Figure 8-2 shows the FG waveform and the phase current waveform at different motor operations.



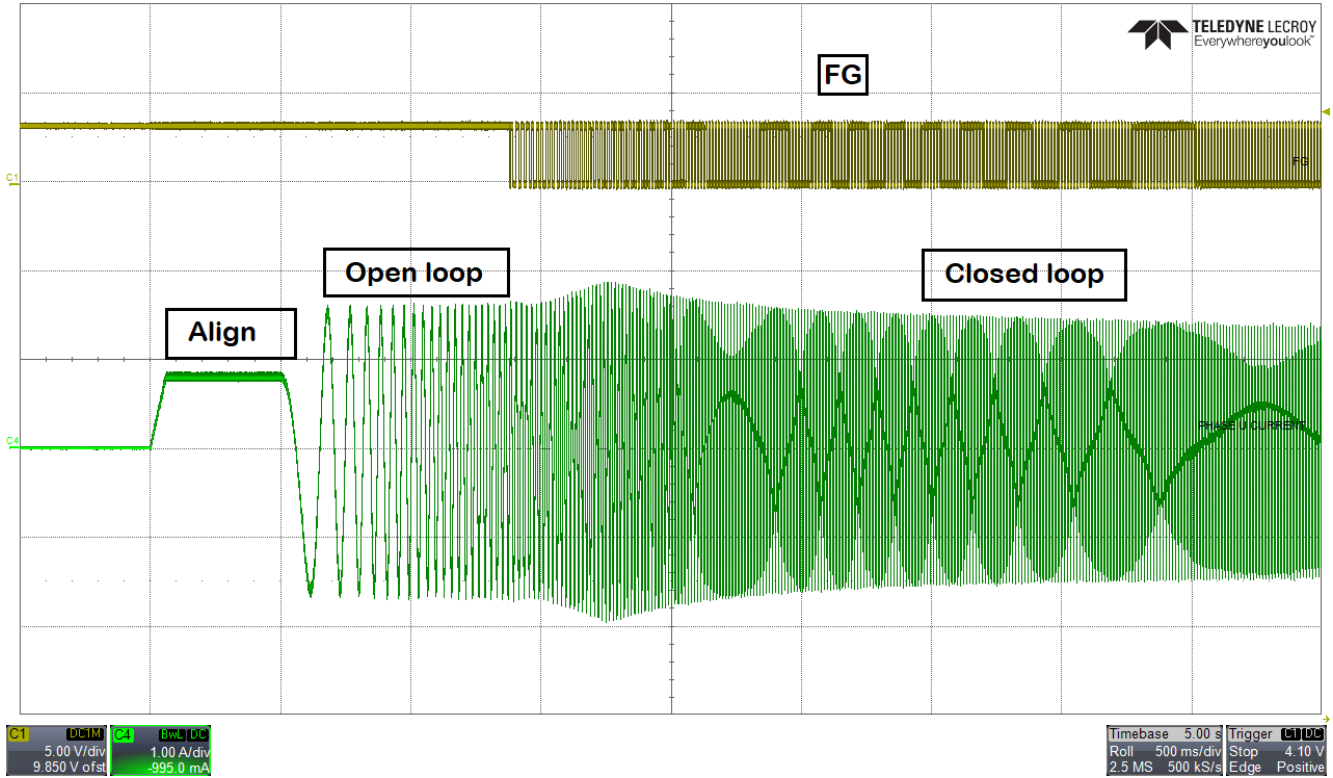


Figure 8-2. Motor Startup - FG and Phase current

### 8.2.1.2 MPET

Figure 8-3 shows the phase current waveform during motor parameter measurement. Figure 8-4 shows the IPD current waveform during R, L and  $K_e$  measurement. Bottom half of Figure 8-4 shows the IPD current waveform during R and L measurement. R is measured during the rising of phase current and L is measured during the falling of phase current. After R and L measurement, motor spins in open loop. Once the speed reaches MPET open loop speed reference [MPET\_OPEN\_LOOP\_SPEED\_REF], motor is coasted. BEMF voltage of all three phases are measured and  $K_e$  is calculated.

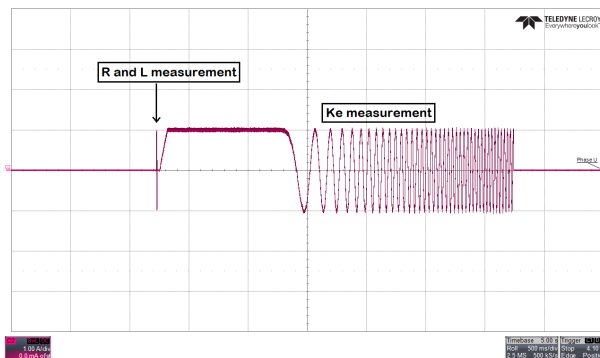


Figure 8-3. MPET - Phase current

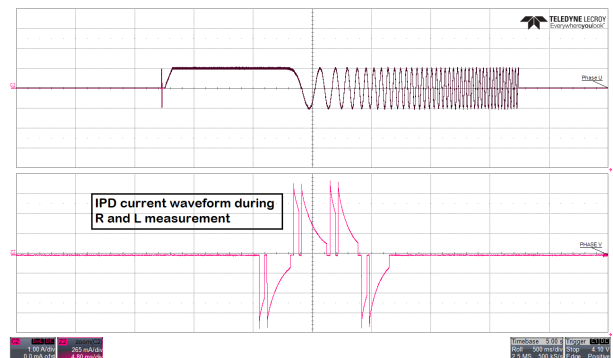
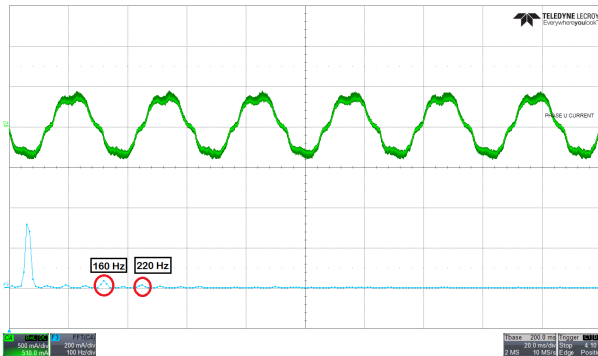


Figure 8-4. IPD current waveform during R and L measurement

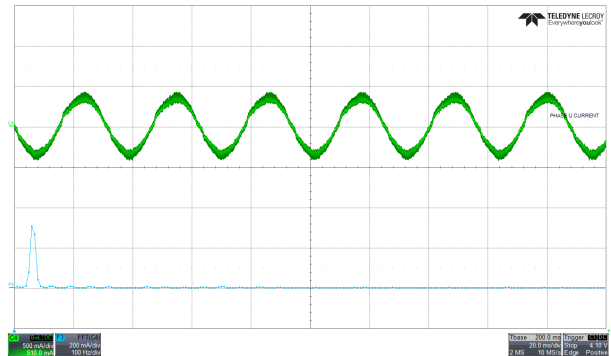
### 8.2.1.3 Dead time compensation

Figure 8-5 shows the phase current waveform when dead time compensation is disabled. Fundamental frequency of phase current is 40 Hz. Fast Fourier transform (FFT) of phase current plot shows harmonics at

160 Hz and 220 Hz. [Figure 8-6](#) shows the phase current waveform when dead time compensation is enabled. Phase current looks more sinusoidal and the FFT of phase current plot does not have any harmonics.



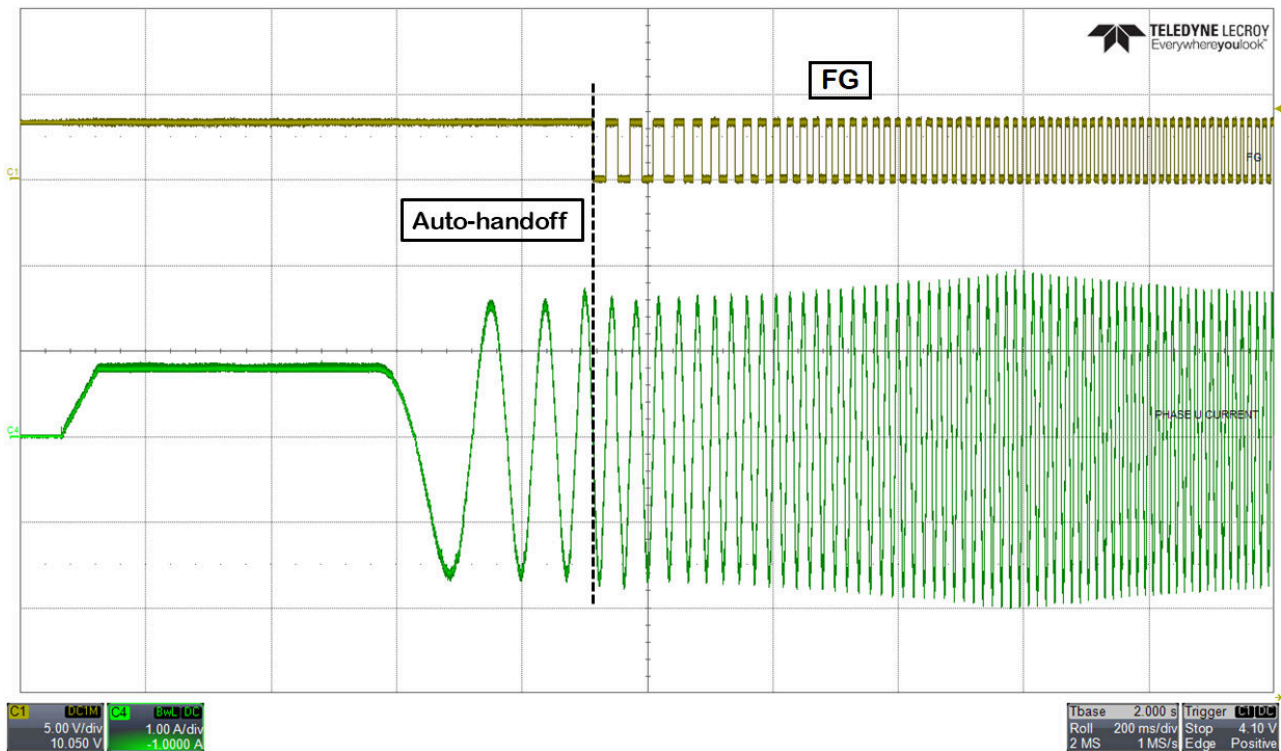
**Figure 8-5. Phase current and FFT - Dead time compensation disabled**



**Figure 8-6. Phase current and FFT - Dead time compensation enabled**

#### 8.2.1.4 Auto handoff

[Figure 8-7](#) shows the auto handoff feature in MCF8316C-Q1 where the motor transitions seamlessly from open loop to closed loop.

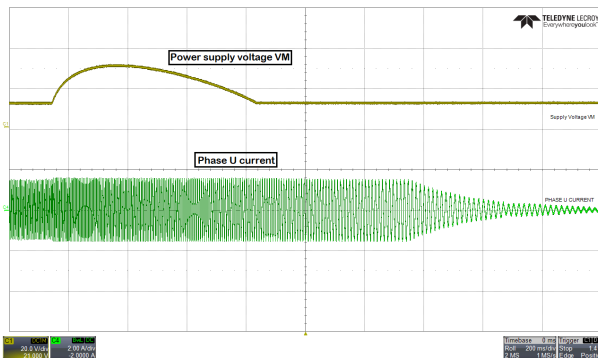


**Figure 8-7. Auto-handoff**

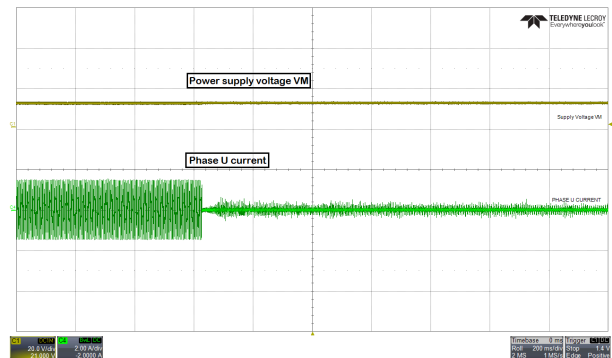
#### 8.2.1.5 Anti voltage surge (AVS)

When motor speed decelerates at a very high deceleration rate, mechanical energy from the motor returns to the power supply which could result in pumping up the supply voltage, VM. [Figure 8-8](#) shows overshoot in power supply voltage when AVS is disabled. Motor decelerates from 100% duty cycle to 10% duty cycle at

a deceleration rate of 70,000 Hz/sec. [Figure 8-9](#) shows no overshoot in power supply voltage when AVS is enabled.



**Figure 8-8. Power supply voltage and phase current waveform when AVS is disabled**



**Figure 8-9. Power supply voltage and phase current waveform when AVS is enabled**

### 8.2.1.6 Real time variable tracking using DACOUT

MCF8316C-Q1 has two 12-bit DAC which outputs analog voltage equivalent of digital variables on DACOUT1 and DACOUT2 pins with resolution of 12 bits and max voltage of 3V. Signals available on DACOUT pins can be used for tuning speed controller or other driver configuration or bus current monitoring. Check algorithm variable registers in datasheet for list of all algorithm variables.

The addresses for variables for DACOUT1 and DACOUT2 are configured using register bits DACOUT1\_VAR\_ADDR and DACOUT2\_VAR\_ADDR. This is useful in applications which require tracking algorithm variables in real time without having any delay from the communication bus. Pin 37 and 38 should be configured as DACOUT1 and DACOUT2.

For example, if the user wants to read phase A current from pin 37, configure pin 37 as DACOUT1 and program the phase A current register address (0x0000440) in Hex in [DACOUT1\_VAR\_ADDR]. If the user wants to read estimated rotor angle from pin 38, configure pin 38 as DACOUT2 and program the estimated rotor angle register address (0x0000736) in Hex in [DACOUT2\_VAR\_ADDR].

[Figure 8-10](#) shows the outputs of DACOUT1 and DACOUT2. DACOUT1 is configured to read phase A current and DACOUT2 is configured to read estimated rotor angle.

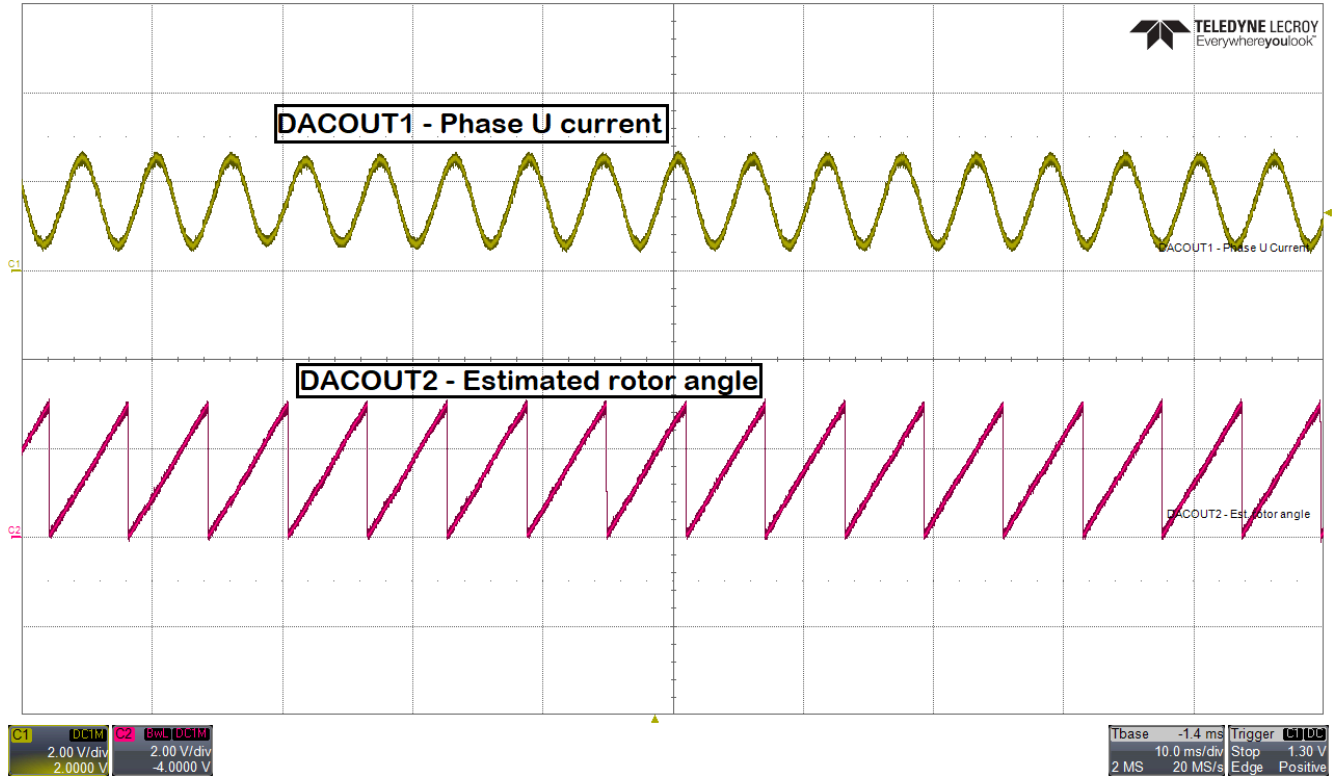


Figure 8-10. DACOUT1 and DACOUT2

## 9 Power Supply Recommendations

### 9.1 Bulk Capacitance

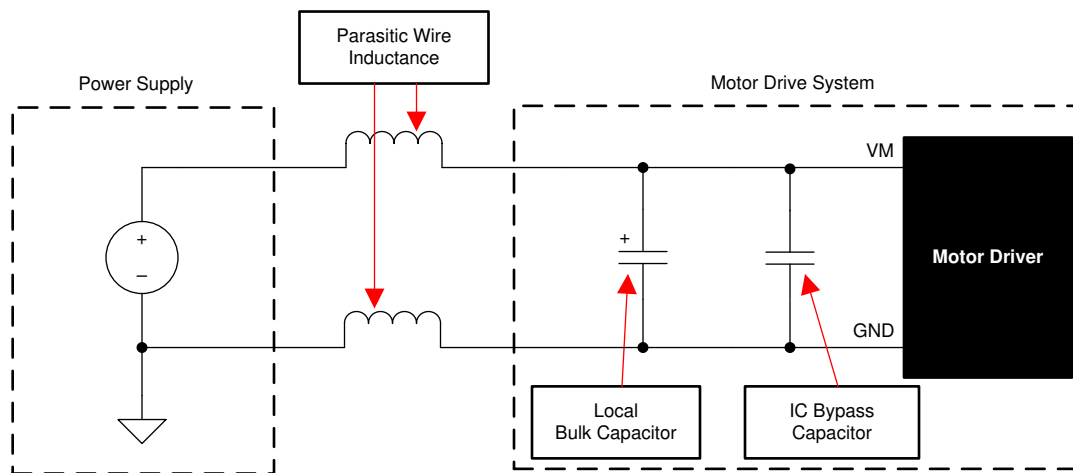
Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in VM voltage. When adequate bulk capacitance is used, the VM voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate bulk capacitor.



**Figure 9-1. Example Setup of Motor Drive System With External Power Supply**

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

## 10 Layout

### 10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize parasitic inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

To reduce noise coupling and EMI interference from large transient currents into small-current signal paths, grounding should be partitioned between PGND and AGND. TI recommends connecting all non-power stage circuitry (including the thermal pad) to AGND to reduce parasitic effects and improve power dissipation from the device. Optionally, GND\_BK can be split. Ensure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the  $I^2 \times R_{DS(on)}$  heat that is generated in the device.

To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

Separate the SW\_BK and FB\_BK traces with ground separation to reduce buck switching from coupling as noise into the buck outer feedback loop. Widen the FB\_BK trace as much as possible to allow for faster load switching.

[Figure 10-1](#) shows a layout example for the MCF8316C-Q1. Also, for layout example, refer to [MCF8316C-Q1 EVM](#).

## 10.2 Layout Example

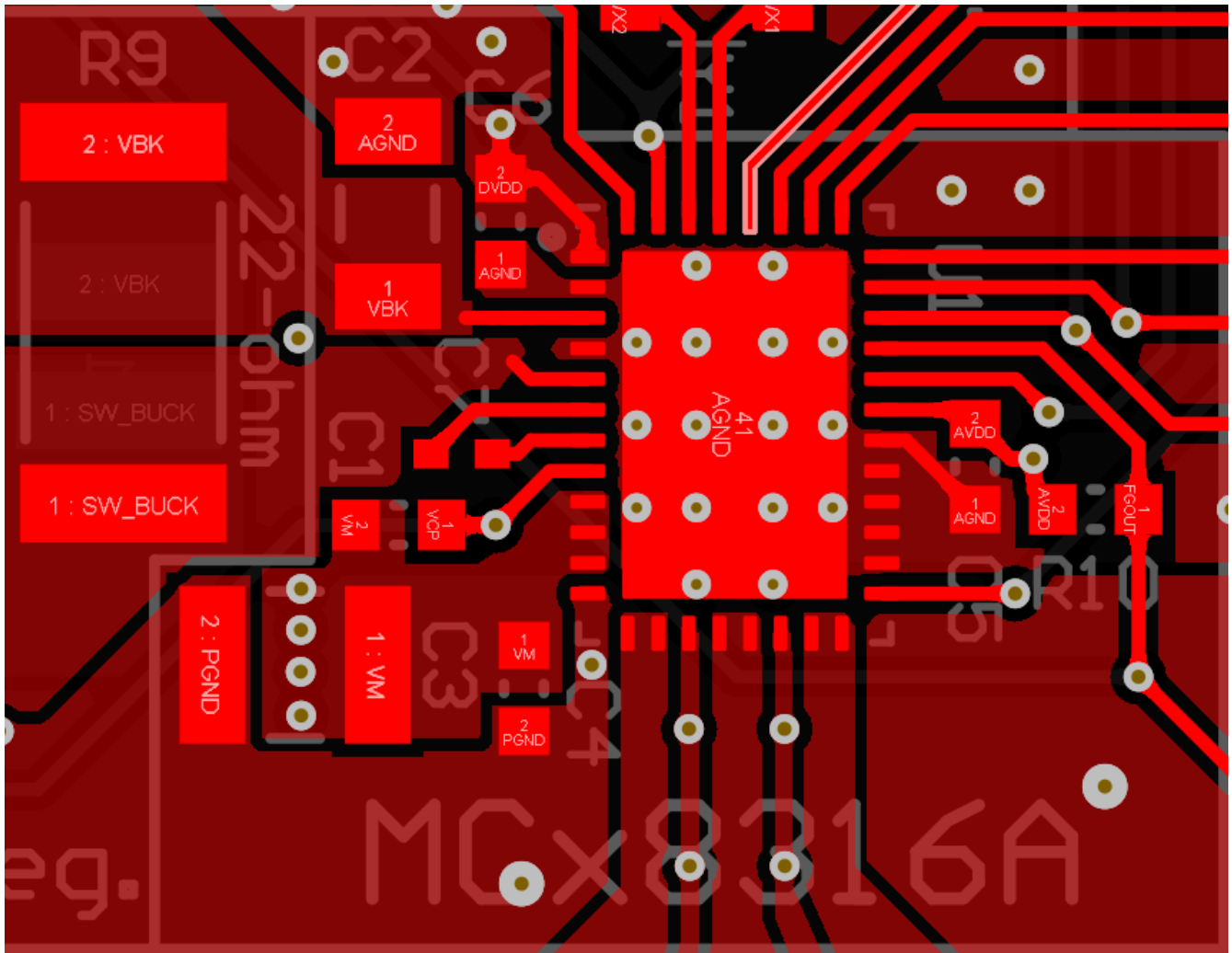


Figure 10-1. Recommended Layout Example

## 10.3 Thermal Considerations

The MCF8316C-Q1 has thermal shutdown (TSD) as previously described. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

### 10.3.1 Power Dissipation

The power dissipated in the output FET resistance ( $R_{DS(on)}$ ) dominates power dissipation in MCF8316C-Q1.

At start-up and fault conditions, the FET current is much higher than normal operating FET current; remember to take these peak currents and their duration into consideration.

The total device power dissipation is the power dissipated in each of the three half-bridges added together along with standby power, LDO and buck regulator losses.

The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking.

Note that  $R_{DS(on)}$  increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when sizing the heatsink.

A summary of equations for calculating each loss is shown below in [Table 10-1](#).

**Table 10-1. Power Losses for MCF8316C-Q1**

| Loss type      | MCF8316C-Q1   |
|----------------|---|
| Standby power  | $P_{standby} = V_M \times I_{VM\_TA}$   |
| LDO            | $P_{LDO} = (V_M - V_{AVDD}) \times I_{AVDD}$ , if BUCK_PS_DIS = 1b<br>$P_{LDO} = (V_{BK} - V_{AVDD}) \times I_{AVDD}$ , if BUCK_PS_DIS = 0b |
| FET conduction | $P_{CON} = 3 \times (I_{RMS(FOC)})^2 \times R_{ds,on(TA)}$  |
| FET switching  | $P_{SW} = 3 \times I_{PK(FOC)} \times V_{PK(FOC)} \times t_{rise/fall} \times f_{PWM}$  |
| Diode          | $P_{diode} = 3 \times I_{PK(FOC)} \times V_{diode} \times t_{dead} \times f_{PWM}$  |
| Buck           | $P_{BK} = 0.11 \times V_{BK} \times I_{BK}$ ( $\eta_{BK} = 90\%$ )  |



## 11 Device and Documentation Support

### 11.1 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 11.2 Trademarks

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### 11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

**PACKAGING INFORMATION**

| Orderable Device  | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| MCF8316C1VQRGFRQ1 | ACTIVE        | VQFN         | RGF             | 40   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | MF16C1V                 | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MCF8316C1VQRGFRQ1 | VQFN         | RGF             | 40   | 3000 | 330.0              | 16.4               | 5.25    | 7.25    | 1.45    | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MCF8316C1VQRGFRQ1 | VQFN         | RGF             | 40   | 3000 | 367.0       | 367.0      | 35.0        |

## GENERIC PACKAGE VIEW

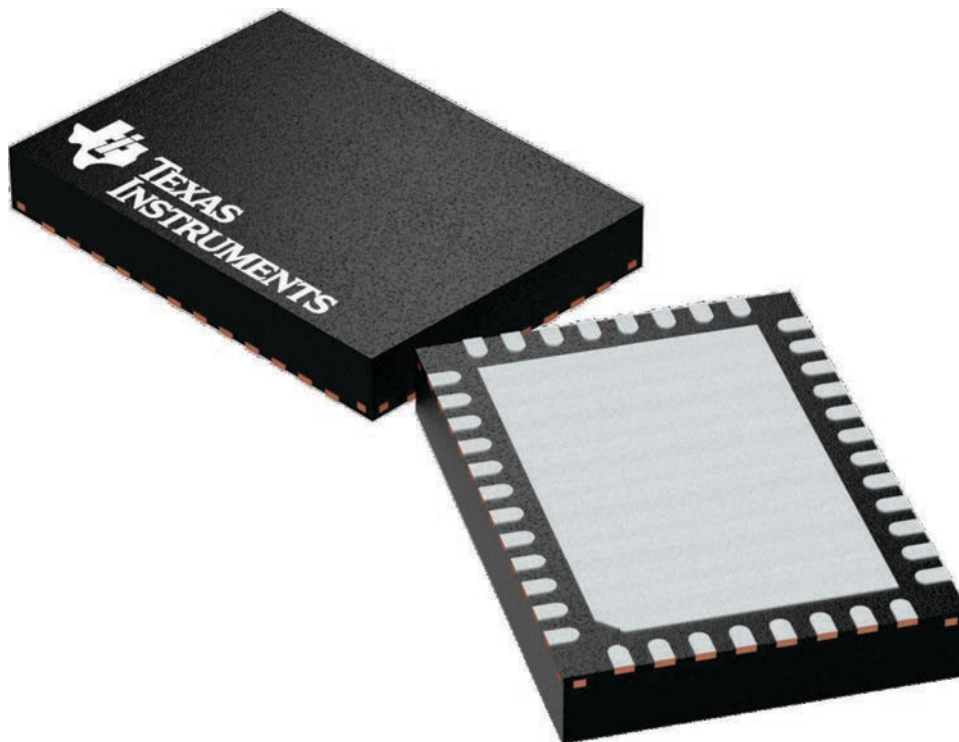
**RGF 40**

**VQFN - 1 mm max height**

5 x 7, 0.5 mm pitch

PLASTIC QUAD FLAT PACK- NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225115/A

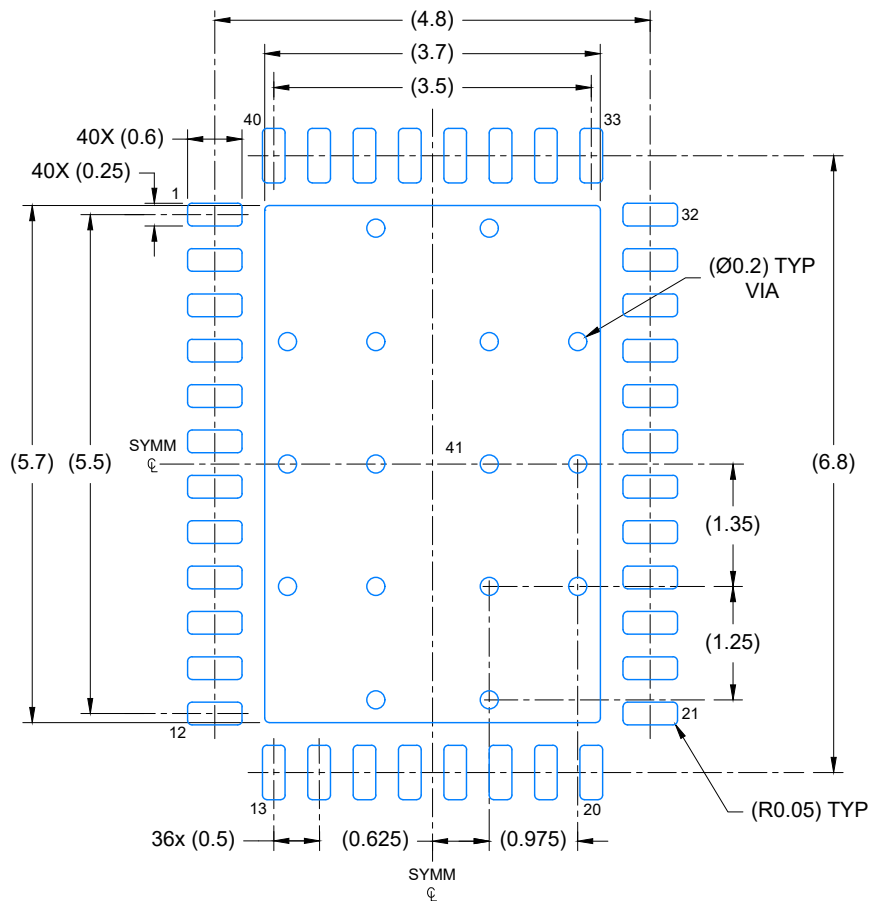


# EXAMPLE BOARD LAYOUT

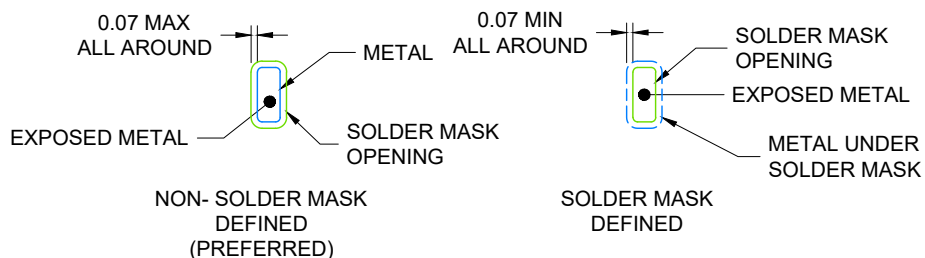
RGF0040E

VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 12X



SOLDER MASK DETAILS

4224999/B 06/2021

NOTES: (continued)

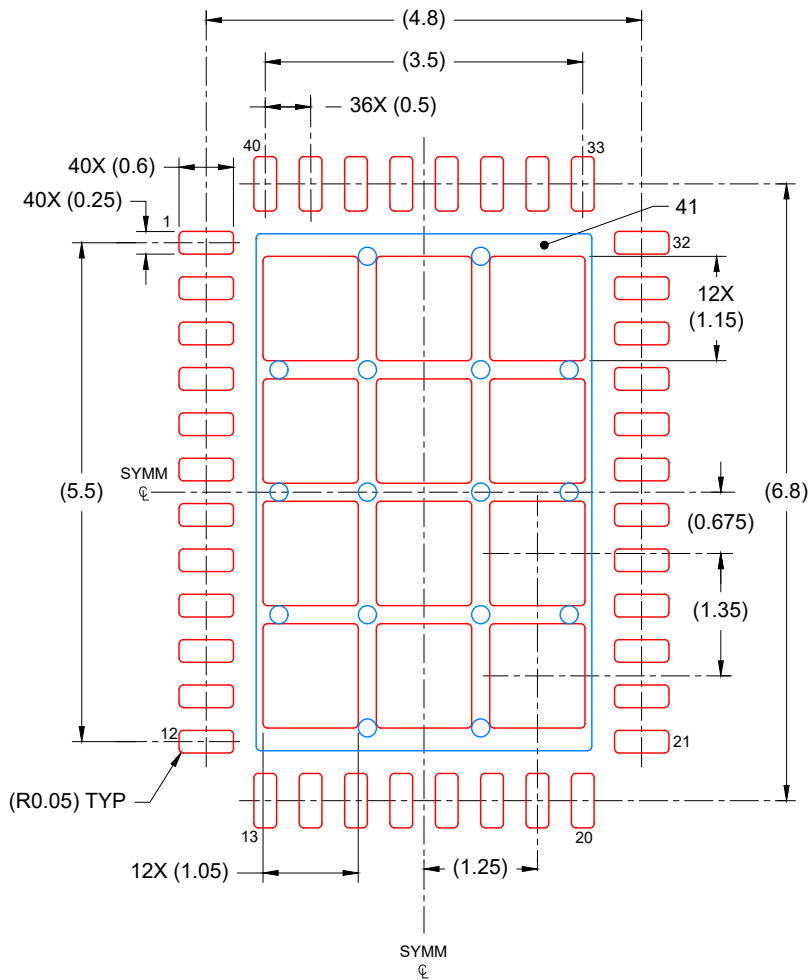
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGF0040E

VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
69% PRINTED COVERAGE BY AREA  
SCALE: 12X

4224999/B 06/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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