FEATURES

- Low Supply Voltage Range: 1.8 V to 3.6 V (A/D) Conversion (MSP430G2210 Only)
- Ultra-Low Power Consumption
  - Active Mode: 220 µA at 1 MHz, 2.2 V
  - Standby Mode: 0.5 µA
  - Off Mode (RAM Retention): 0.1 µA
- 10-Bit 200-ksps Analog-to-Digital (A/D) Converter With Internal Reference, Sample- and-Hold, and Autoscan (MSP430G2230 Only)
- Five Power-Saving Modes
- Universal Serial Interface (USI) Supports SPI and I2C (MSP430G2230 Only)
- Ultra-Fast Wake-Up From Standby Mode in Less Than 1 µs
- Brownout Detector
- Five Power-Saving Modes
- Basic Clock Module Configurations
  - Internal Frequencies up to 16 MHz With
    Four Calibrated Frequencies to ±1%
  - Internal Very-Low-Power Low-Frequency Oscillator
- 16-Bit Timer_A With Two Capture/Compare Registers
- Available in 8-Pin Plastic Packages (D)
- On-Chip Comparator for Analog Signal Compare Function or Slope Analog-to-Digital
- Family Members:
  - MSP430G22x0
  - 2KB + 256B Flash Memory
  - 128B RAM
- For Complete Module Descriptions, See the MSP430x2xx Family User's Guide (SLAU144)

DESCRIPTION

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

The MSP430G22x0 series is an ultra-low-power mixed signal microcontroller with a built-in 16-bit timer and four I/O pins. In addition, the MSP430G2230 has a built-in communication capability using synchronous protocols (SPI or I2C) and a 10-bit A/D converter. The MSP430G2210 has a versatile analog comparator.

Table 1. Available Options(1)

<table>
<thead>
<tr>
<th>TA</th>
<th>PACKAGED DEVICES(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40°C to 85°C</td>
<td>MSP430G2230ID</td>
</tr>
<tr>
<td></td>
<td>MSP430G2210ID</td>
</tr>
</tbody>
</table>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging
Device Pinout and Functional Block Diagram, MSP430G2210

See Application Information for detailed I/O information.

Figure 1. Device Pinout, MSP430G2210

Figure 2. Functional Block Diagram, MSP430G2210
Device Pinout and Functional Block Diagram, MSP430G2230

See Application Information for detailed I/O information.

**Figure 3. Device Pinout, MSP430G2230**

**Figure 4. Functional Block Diagram, MSP430G2230**
Table 2. Terminal Functions, MSP430G2210

<table>
<thead>
<tr>
<th>TERMINAL</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1.2/ TA0.1/ CA2</td>
<td>2</td>
<td>I/O</td>
<td>General-purpose digital I/O pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Timer_A, capture: CCI1A input, compare Out1 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Comparator_A+, CA2 input</td>
</tr>
<tr>
<td>P1.5/ TA0.0/ CA5</td>
<td>3</td>
<td>I/O</td>
<td>General-purpose digital I/O pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Timer_A, compare Out0 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Comparator_A+, CA5 input</td>
</tr>
<tr>
<td>P1.6/ TA0.1/ CA6</td>
<td>4</td>
<td>I/O</td>
<td>General-purpose digital I/O pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Timer_A, compare: Out1 output</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Comparator_A+, CA6 input</td>
</tr>
<tr>
<td>P1.7/ CAOUT/ CA7</td>
<td>5</td>
<td>I/O</td>
<td>General-purpose digital I/O pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Comparator_A+, output</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Comparator_A+, CA7 input</td>
</tr>
<tr>
<td>RST/ NMI/ SBWTDO</td>
<td>6</td>
<td>I</td>
<td>Reset input</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Nonmaskable interrupt input</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Spy-Bi-Wire test data input/output during programming and test</td>
</tr>
<tr>
<td>TEST/ SBWTCK</td>
<td>7</td>
<td>I</td>
<td>Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Spy-Bi-Wire test clock input during programming and test</td>
</tr>
<tr>
<td>DVCC</td>
<td>1</td>
<td></td>
<td>Digital supply voltage</td>
</tr>
<tr>
<td>DVSS</td>
<td>8</td>
<td></td>
<td>Digital ground reference</td>
</tr>
</tbody>
</table>

(1) The GPIOs P1.0, P1.1, P1.3, P1.4, P2.6, and P2.7 are implemented but not available on the device pinout. To avoid floating inputs, these digital I/Os should be properly configured. The pullup or pulldown resistors of the unbounded P1.x GPIOs should be enabled, and the VLO should be selected as the ACLK source (see the MSP430x2xx Family User’s Guide (SLAU144)).
### Table 3. Terminal Functions, MSP430G2230\(^{(1)}\)

<table>
<thead>
<tr>
<th>TERMINAL</th>
<th>NO. D</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
</table>
| P1.2/TA0.1/A2 | 2 | I/O | General-purpose digital I/O pin  
Timer_A, capture: CCI1A input, compare Out1 output  
ADC10 analog input A2 |
| P1.5/TA0.0/A5/SCLK | 3 | I/O | General-purpose digital I/O pin  
Timer_A, compare Out0 output  
ADC10 analog input A5  
USI: clock input in I2C mode; clock input/output in SPI mode |
| P1.6/TA0.1/A6/SDO/SCL | 4 | I/O | General-purpose digital I/O pin  
Timer_A, capture: CCI1B input, compare: Out1 output  
ADC10 analog input A6  
USI: Data output in SPI mode  
USI: I2C clock in I2C mode |
| P1.7/A7/SDI/SDA | 5 | I/O | General-purpose digital I/O pin  
ADC10 analog input A7  
USI: Data input in SPI mode  
USI: Data input in I2C mode |
| RST/NMI/SBWTDIO | 6 | I | Reset input  
Nonmaskable interrupt input  
Spy-Bi-Wire test data input/output during programming and test |
| TEST/SBWTCX | 7 | I | Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST.  
Spy-Bi-Wire test clock input during programming and test |
| DVCC | 1 | | Digital supply voltage |
| DVSS | 8 | | Digital ground reference |

\(^{(1)}\) The GPIOs P1.0, P1.1, P1.3, P1.4, P2.6, and P2.7 are implemented but not available on the device pinout. To avoid floating inputs, these digital I/Os should be properly configured. The pullup or pulldown resistors of the unbounded P1.x GPIOs should be enabled, and the VLO should be selected as the ACLK source (see the MSP430x2xx Family User’s Guide (SLAU144)).
SHORT-FORM DESCRIPTION

CPU
The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

Instruction Set
The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 4 shows examples of the three types of instruction formats; Table 5 shows the address modes.

Table 4. Instruction Word Formats

<table>
<thead>
<tr>
<th>INSTRUCTION FORMAT</th>
<th>EXAMPLE</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual operands, source-destination</td>
<td>ADD R4,R5</td>
<td>R4 + R5 --&gt; R5</td>
</tr>
<tr>
<td>Single operands, destination only</td>
<td>CALL R8</td>
<td>PC --&gt; (TOS), R8 --&gt; PC</td>
</tr>
<tr>
<td>Relative jump, un/conditional</td>
<td>JNE</td>
<td>Jump-on-equal bit = 0</td>
</tr>
</tbody>
</table>

Table 5. Address Mode Descriptions

<table>
<thead>
<tr>
<th>ADDRESS MODE</th>
<th>S(1)</th>
<th>D(1)</th>
<th>SYNTAX</th>
<th>EXAMPLE</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register</td>
<td>✓</td>
<td>✓</td>
<td>MOV Rs,Rd</td>
<td>MOV R10,R11</td>
<td>R10 --&gt; R11</td>
</tr>
<tr>
<td>Indexed</td>
<td>✓</td>
<td>✓</td>
<td>MOV X(Rn),Y(Rm)</td>
<td>MOV 2(R5),6(R6)</td>
<td>M(2+R5) --&gt; M(6+R6)</td>
</tr>
<tr>
<td>Symbolic (PC relative)</td>
<td>✓</td>
<td>✓</td>
<td>MOV EDE,TONI</td>
<td></td>
<td>M(EDE) --&gt; M(TONI)</td>
</tr>
<tr>
<td>Absolute</td>
<td>✓</td>
<td>✓</td>
<td>MOV &amp;MEM,&amp;TCMDAT</td>
<td></td>
<td>M(MEM) --&gt; M(TCDAT)</td>
</tr>
<tr>
<td>Indirect</td>
<td>✓</td>
<td></td>
<td>MOV @Rn,Y(Rm)</td>
<td>MOV @R10,Tab(R6)</td>
<td>M(R10) --&gt; M(Tab+R6)</td>
</tr>
<tr>
<td>Indirect autoincrement</td>
<td>✓</td>
<td></td>
<td>MOV @Rn++,Rm</td>
<td></td>
<td>M(R10) --&gt; R11</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>R10 + 2 --&gt; R10</td>
</tr>
<tr>
<td>Immediate</td>
<td>✓</td>
<td></td>
<td>MOV #X,TONI</td>
<td>MOV #45,TONI</td>
<td>#45 --&gt; M(TONI)</td>
</tr>
</tbody>
</table>

(1) S = source, D = destination
Operating Modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- **Active mode (AM)**
  - All clocks are active

- **Low-power mode 0 (LPM0)**
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled

- **Low-power mode 1 (LPM1)**
  - CPU is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
  - DCO’s dc-generator is disabled if DCO not used in active mode

- **Low-power mode 2 (LPM2)**
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO’s dc-generator remains enabled
  - ACLK remains active

- **Low-power mode 3 (LPM3)**
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO’s dc-generator is disabled
  - ACLK remains active

- **Low-power mode 4 (LPM4)**
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DCO’s dc-generator is disabled
  - Crystal oscillator is stopped
Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range of 0x0FFFF to 0xFFC0. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0xFFFFE) contains 0xFFFF (for example, flash is not programmed) the CPU goes into LPM4 immediately after power-up.

Table 6. Interrupt Sources

<table>
<thead>
<tr>
<th>SYSTEM INTERRUPT</th>
<th>WORD ADDRESS</th>
<th>PRIORITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-up</td>
<td>0xFFFE</td>
<td>31, highest</td>
</tr>
<tr>
<td>External reset</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Watchdog Timer+</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flash key violation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PC out-of-range</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NMI</td>
<td>0xFFFFC</td>
<td>30</td>
</tr>
<tr>
<td>Oscillator fault</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flash memory access violation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Comparator_A+</td>
<td>0xFFF6</td>
<td>27</td>
</tr>
<tr>
<td>(MSP430G2210 Only)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Watchdog Timer+</td>
<td>0xFFF4</td>
<td>26</td>
</tr>
<tr>
<td>Timer_A2</td>
<td>0xFFF2</td>
<td>25</td>
</tr>
<tr>
<td>Timer_A2</td>
<td>0xFFF0</td>
<td>24</td>
</tr>
<tr>
<td>ADC10 (MSP430G2230 Only)</td>
<td></td>
<td>21</td>
</tr>
<tr>
<td>USI (MSP430G2230 Only)</td>
<td></td>
<td>20</td>
</tr>
<tr>
<td>I/O Port P1(four flags)</td>
<td>0xFFF4</td>
<td>18</td>
</tr>
<tr>
<td>See (6)</td>
<td>0xFFDE to 0xFFC0</td>
<td>15 to 0, lowest</td>
</tr>
</tbody>
</table>

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) All eight interrupt flags P1IFG.0 to P1IFG.7 are implemented while four are connected to pins.
(6) The interrupt vectors at addresses 0xFFDE to 0xFFC0 are not used in this device and can be used for regular program code if necessary.
Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend
- **rw:** Bit can be read and written.
- **rw-0,1:** Bit can be read and written. It is reset or set by PUC.
- **rw-(0,1):** Bit can be read and written. It is reset or set by POR.

| SFR bit is not present in device. |

### Table 7. Interrupt Enable Register 1 and 2

<table>
<thead>
<tr>
<th>Address</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td></td>
<td></td>
<td>ACCVIE</td>
<td>NMIIE</td>
<td>OFIE</td>
<td>WDTIE</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>rw-0</td>
<td>rw-0</td>
<td>rw-0</td>
<td>rw-0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**WDTIE** Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.

**OFIE** Oscillator fault interrupt enable. Set to 0.

**NMIIE** (Non)maskable interrupt enable

**ACCVIE** Flash access violation interrupt enable

### Table 8. Interrupt Flag Register 1 and 2

<table>
<thead>
<tr>
<th>Address</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>02h</td>
<td></td>
<td></td>
<td>NMIIFG</td>
<td>RSTIFG</td>
<td>PORIFG</td>
<td>OFIFG</td>
<td>WDTIFG</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>rw-0</td>
<td>rw-(0)</td>
<td>rw-(1)</td>
<td>rw-1</td>
<td>rw-(0)</td>
<td></td>
</tr>
</tbody>
</table>

**WDTIFG** Set on watchdog timer overflow (in watchdog mode) or security key violation.

Reset on V<sub>CC</sub> power-on or a reset condition at the RST/NMI pin in reset mode.

**OFIFG** Flag set on oscillator fault. The XIN/XOUT pins are not available as device terminals.

**PORIFG** Power-On Reset interrupt flag. Set on V<sub>CC</sub> power-up.

**RSTIFG** External reset interrupt flag. Set on a reset condition at RST/NMI pin in reset mode. Reset on V<sub>CC</sub> power-up.

**NMIIFG** Set by RST/NMI pin

### Table 9. Interrupt Flags Register 1 and 2

<table>
<thead>
<tr>
<th>Address</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>03h</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Memory Organization

<table>
<thead>
<tr>
<th>Table 9. Memory Organization</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Memory</strong></td>
</tr>
<tr>
<td>Main: interrupt vector</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Main: code memory</td>
</tr>
<tr>
<td><strong>Information memory</strong></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td><strong>RAM</strong></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td><strong>Peripherals</strong></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

Flash Memory

The flash memory can be programmed by the Spy-Bi-Wire or JTAG port, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called information memory.
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.
Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the MSP430x2xx Family User's Guide (SLAU144).

Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator and an internal digitally-controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF (VLOCLK) oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

NOTE

The LFXT1 oscillator is not available. LFXT1Sx bits of the BCSCTL3 register should be configured to use VLOCLK (see the MSP430x2xx Family User's Guide (SLAU144)).

Table 10. DCO Calibration Data (Provided From Factory in Flash Information Memory Segment A)

<table>
<thead>
<tr>
<th>DCO FREQUENCY</th>
<th>CALIBRATION REGISTER</th>
<th>SIZE</th>
<th>ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 MHz</td>
<td>CALBC1_1MHZ</td>
<td>byte</td>
<td>010FFh</td>
</tr>
<tr>
<td></td>
<td>CALDCO_1MHZ</td>
<td>byte</td>
<td>010FEh</td>
</tr>
<tr>
<td>8 MHz</td>
<td>CALBC1_8MHZ</td>
<td>byte</td>
<td>010FDh</td>
</tr>
<tr>
<td></td>
<td>CALDCO_8MHZ</td>
<td>byte</td>
<td>010FCh</td>
</tr>
<tr>
<td>12 MHz</td>
<td>CALBC1_12MHZ</td>
<td>byte</td>
<td>010FBh</td>
</tr>
<tr>
<td></td>
<td>CALDCO_12MHZ</td>
<td>byte</td>
<td>010FAh</td>
</tr>
<tr>
<td>16 MHz</td>
<td>CALBC1_16MHZ</td>
<td>byte</td>
<td>010F9h</td>
</tr>
<tr>
<td></td>
<td>CALDCO_16MHZ</td>
<td>byte</td>
<td>010F8h</td>
</tr>
</tbody>
</table>

Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

Digital I/O

There are four pins of one 8-bit I/O port implemented—port P1:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all the four bits of port P1.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.
Watchdog Timer (WDT+)

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Timer_A2

Timer_A2 is a 16-bit timer/counter with two capture/compare registers. Timer_A2 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

<table>
<thead>
<tr>
<th>INPUT PIN NUMBER</th>
<th>DEVICE INPUT SIGNAL</th>
<th>MODULE INPUT NAME</th>
<th>MODULE BLOCK</th>
<th>MODULE OUTPUT SIGNAL</th>
<th>OUTPUT PIN NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>TACLK</td>
<td>TACLK</td>
<td>Timer</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ACLK</td>
<td>ACLK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SMCLK</td>
<td>SMCLK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TACLK</td>
<td>INCLK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>TACLK (internal)</td>
<td>CCI0A</td>
<td>CCR0</td>
<td>TA0</td>
<td>3 - P1.5</td>
</tr>
<tr>
<td>-</td>
<td>VSS</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>VCC</td>
<td>VCC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 - P1.2</td>
<td>CAOUT</td>
<td>CCI1A</td>
<td>CCR1</td>
<td>TA1</td>
<td>2 - P1.2</td>
</tr>
<tr>
<td></td>
<td>VSS</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VCC</td>
<td>VCC</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>INPUT PIN NUMBER</th>
<th>DEVICE INPUT SIGNAL</th>
<th>MODULE INPUT NAME</th>
<th>MODULE BLOCK</th>
<th>MODULE OUTPUT SIGNAL</th>
<th>OUTPUT PIN NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>TACLK</td>
<td>TACLK</td>
<td>Timer</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ACLK</td>
<td>ACLK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SMCLK</td>
<td>SMCLK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>TACLK</td>
<td>INCLK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>TACLK (internal)</td>
<td>CCI0A</td>
<td>CCR0</td>
<td>TA0</td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>VSS</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>VCC</td>
<td>VCC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 - P1.2</td>
<td>TA1</td>
<td>CCI1A</td>
<td>CCR1</td>
<td>TA1</td>
<td>2 - P1.2</td>
</tr>
<tr>
<td>4 - P1.6</td>
<td>TA1</td>
<td>CCI1B</td>
<td></td>
<td></td>
<td>4 - P1.6</td>
</tr>
<tr>
<td></td>
<td>VSS</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VCC</td>
<td>VCC</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
USI (MSP430G2230 Only)
The universal serial interface (USI) module is used for serial data communication and provides the basic hardware for synchronous communication protocols like SPI and I2C.

ADC10 (MSP430G2230 Only)
The ADC10 module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and data transfer controller (DTC) for automatic conversion result handling, allowing ADC samples to be converted and stored without any CPU intervention.

Comparator_A+ (MSP430G2210 Only)
The primary function of the comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals

Peripheral File Map

### Table 13. Peripherals With Word Access

<table>
<thead>
<tr>
<th>ADC10 (MSP430G2230 Only)</th>
<th>ADC control 0</th>
<th>ADC control 1</th>
<th>ADC control memory</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ADC10CTL0</td>
<td>ADC10CTL1</td>
<td>ADC10MEM</td>
</tr>
<tr>
<td>Timer_A</td>
<td>Capture/compare register</td>
<td>TACCR1</td>
<td>0174h</td>
</tr>
<tr>
<td></td>
<td>Capture/compare register</td>
<td>TACCR0</td>
<td>0172h</td>
</tr>
<tr>
<td></td>
<td>Timer_A register</td>
<td>TAR</td>
<td>0170h</td>
</tr>
<tr>
<td></td>
<td>Capture/compare control</td>
<td>TACCTL1</td>
<td>0164h</td>
</tr>
<tr>
<td></td>
<td>Capture/compare control</td>
<td>TACCTL0</td>
<td>0162h</td>
</tr>
<tr>
<td></td>
<td>Timer_A control</td>
<td>TACL</td>
<td>0160h</td>
</tr>
<tr>
<td></td>
<td>Timer_A interrupt register</td>
<td>TAIL</td>
<td>012Eh</td>
</tr>
<tr>
<td>Flash Memory</td>
<td>Flash control 3</td>
<td>FCTL3</td>
<td>012Ch</td>
</tr>
<tr>
<td></td>
<td>Flash control 2</td>
<td>FCTL2</td>
<td>012Ah</td>
</tr>
<tr>
<td></td>
<td>Flash control 1</td>
<td>FCTL1</td>
<td>012Bh</td>
</tr>
<tr>
<td>Watchdog Timer+</td>
<td>Watchdog/timer control</td>
<td>WDTCTL</td>
<td>0120h</td>
</tr>
</tbody>
</table>

### Table 14. Peripherals With Byte Access

<table>
<thead>
<tr>
<th>ADC10 (MSP430G2230 Only)</th>
<th>Analog Enable</th>
<th>ADC10AE</th>
</tr>
</thead>
<tbody>
<tr>
<td>USI (MSP430G2230 Only)</td>
<td>USI control 0</td>
<td>USICL0</td>
</tr>
<tr>
<td></td>
<td>USI control 1</td>
<td>USICL1</td>
</tr>
<tr>
<td></td>
<td>USI clock control</td>
<td>USICKCTL</td>
</tr>
<tr>
<td></td>
<td>USI bit counter</td>
<td>USICNT</td>
</tr>
<tr>
<td></td>
<td>USI shift register</td>
<td>USISR</td>
</tr>
<tr>
<td>Comparator_A+ (MSP430G2210 Only)</td>
<td>Comparator_A+ port disable</td>
<td>CAPD</td>
</tr>
<tr>
<td></td>
<td>Comparator_A+ control 2</td>
<td>CACTL2</td>
</tr>
<tr>
<td></td>
<td>Comparator_A+ control 1</td>
<td>CACTL1</td>
</tr>
<tr>
<td>Basic Clock System+</td>
<td>Basic clock system control 3</td>
<td>BCSCCL3</td>
</tr>
<tr>
<td></td>
<td>Basic clock system control 2</td>
<td>BCSCCL2</td>
</tr>
<tr>
<td></td>
<td>Basic clock system control 1</td>
<td>BCSCCL1</td>
</tr>
<tr>
<td></td>
<td>DCO clock frequency control</td>
<td>DCOCCTL</td>
</tr>
<tr>
<td>Port P1</td>
<td>Port P1 resistor enable</td>
<td>P1REN</td>
</tr>
<tr>
<td></td>
<td>Port P1 selection</td>
<td>P1SEL</td>
</tr>
<tr>
<td></td>
<td>Port P1 interrupt enable</td>
<td>P1IE</td>
</tr>
<tr>
<td></td>
<td>Port P1 interrupt edge select</td>
<td>P1IES</td>
</tr>
<tr>
<td></td>
<td>Port P1 interrupt flag</td>
<td>P1IFG</td>
</tr>
<tr>
<td></td>
<td>Port P1 direction</td>
<td>P1DIR</td>
</tr>
<tr>
<td></td>
<td>Port P1 output</td>
<td>P1OUT</td>
</tr>
<tr>
<td></td>
<td>Port P1 input</td>
<td>P1IN</td>
</tr>
<tr>
<td>Special Function</td>
<td>SFR interrupt flag 2</td>
<td>IFG2</td>
</tr>
<tr>
<td></td>
<td>SFR interrupt flag 1</td>
<td>IFG1</td>
</tr>
<tr>
<td></td>
<td>SFR interrupt enable 2</td>
<td>IE2</td>
</tr>
<tr>
<td></td>
<td>SFR interrupt enable 1</td>
<td>IE1</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings

| Voltage applied at V\text{CC} to V\text{SS} | -0.3 V to 4.1 V |
| Voltage applied to any pin | -0.3 V to V\text{CC} + 0.3 V |
| Diode current at any device terminal | ±2 mA |
| T_{\text{stg}} Storage temperature | Unprogrammed device -55°C to 150°C |
| | Programmed device -40°C to 150°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages referenced to V\text{SS}. The JTAG fuse-blow voltage, V_F\text{B}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.

(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

Typical values are specified at V\text{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

<table>
<thead>
<tr>
<th>V\text{CC}</th>
<th>Supply voltage</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>During program execution</td>
<td>1.8</td>
<td>3.6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>During flash program or erase</td>
<td>2.2</td>
<td>3.6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| V\text{SS} | Supply voltage | 0 | V |

| T_A | Operating free-air temperature | -40 | 85 | °C |

<table>
<thead>
<tr>
<th>f_{\text{SYSTEM}}</th>
<th>Processor frequency (maximum MCLK frequency)</th>
<th>6</th>
<th>MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{\text{CC}} = 1.8 V, Duty cycle = 50% ± 10%</td>
<td>dc</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{\text{CC}} = 2.7 V, Duty cycle = 50% ± 10%</td>
<td>dc</td>
<td>12</td>
<td>MHz</td>
</tr>
<tr>
<td>V_{\text{CC}} ≥ 3.3 V, Duty cycle = 50% ± 10%</td>
<td>dc</td>
<td>16</td>
<td>MHz</td>
</tr>
</tbody>
</table>

(1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.

(2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.

Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{\text{CC}} of 2.2 V.

Figure 5. Safe Operating Area
Electrical Characteristics

Active Mode Supply Current Into $V_{CC}$ Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$T_A$</th>
<th>$V_{CC}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{AM,1MHz}$</td>
<td>Active mode (AM) current (1 MHz)</td>
<td>$f_{DCO} = f_{MCLK} = f_{SMCLK} = 1$ MHz, $f_{ACLK} = 0$ Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0</td>
<td>2.2 V</td>
<td>220</td>
<td></td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3 V</td>
<td>300</td>
<td>370</td>
<td></td>
<td>$\mu$A</td>
</tr>
</tbody>
</table>

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.

Typical Characteristics – Active Mode Supply Current (Into $V_{CC}$)

**ACTIVE MODE CURRENT vs $V_{CC}$**

$T_A = 25^°C$

$V_{CC}$ – Supply Voltage – V

<table>
<thead>
<tr>
<th>Active Mode Current – mA</th>
<th>$f_{DCO}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0</td>
<td>$f_{DCO} = 1$ MHz</td>
</tr>
<tr>
<td>1.0</td>
<td>$f_{DCO} = 8$ MHz</td>
</tr>
<tr>
<td>2.0</td>
<td>$f_{DCO} = 12$ MHz</td>
</tr>
<tr>
<td>3.0</td>
<td>$f_{DCO} = 16$ MHz</td>
</tr>
</tbody>
</table>

**ACTIVE MODE CURRENT vs DCO FREQUENCY**

$T_A = 25^°C$

$V_{CC}$ = 3 V

$T_A = 85^°C$

$V_{CC}$ = 2.2 V

Figure 6.

Figure 7.
## Low-Power Mode Supply Currents (Into V\(_{CC}\)) Excluding External Current

Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>(T_A)</th>
<th>(V_{CC})</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{LPM0,1MHz})</td>
<td>Low-power mode 0 (LPM0) current(^{(3)})</td>
<td></td>
<td>25°C</td>
<td>2.2 V</td>
<td>65</td>
<td></td>
<td>(\mu)A</td>
</tr>
<tr>
<td></td>
<td>(f_{MCLK} = 0) MHz, (f_{SMCLK} = f_{DCO} = 1) MHz, (f_{ACLK} = 32,768) MHz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{LPM2})</td>
<td>Low-power mode 2 (LPM2) current(^{(3)})</td>
<td></td>
<td>25°C</td>
<td>2.2 V</td>
<td>22</td>
<td>29</td>
<td>(\mu)A</td>
</tr>
<tr>
<td></td>
<td>(f_{MCLK} = f_{SMCLK} = 0) MHz, (f_{DCO} = 1) MHz, (f_{ACLK} = 32,768) MHz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{LPM3,VLO})</td>
<td>Low-power mode 3 (LPM3) current(^{(3)})</td>
<td></td>
<td>25°C</td>
<td>2.2 V</td>
<td>0.5</td>
<td>0.7</td>
<td>(\mu)A</td>
</tr>
<tr>
<td></td>
<td>(f_{DCO} = f_{MCLK} = f_{SMCLK} = 0) MHz, (f_{ACLK}) from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{LPM4})</td>
<td>Low-power mode 4 (LPM4) current(^{(3)})</td>
<td></td>
<td>25°C</td>
<td>2.2 V</td>
<td>0.1</td>
<td>0.5</td>
<td>(\mu)A</td>
</tr>
<tr>
<td></td>
<td>(f_{DCO} = f_{MCLK} = f_{SMCLK} = 0) MHz, (f_{ACLK} = 0) Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) All inputs are tied to 0 V or to \(V_{CC}\). Outputs do not source or sink any current.

\(^{(2)}\) Current for brownout and WDT clocked by SMCLK included.

\(^{(3)}\) Current for brownout and WDT clocked by ACLK included.

\(^{(4)}\) Current for brownout included.
Schmitt-Trigger Inputs (Port P1)
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( V_{CC} )</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IT^+} ) Positive-going input threshold voltage</td>
<td>3 V</td>
<td>0.45 ( V_{CC} )</td>
<td>0.75 ( V_{CC} )</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IT^-} ) Negative-going input threshold voltage</td>
<td>3 V</td>
<td>0.25 ( V_{CC} )</td>
<td>0.55 ( V_{CC} )</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{hys} ) Input voltage hysteresis ((V_{IT^+} - V_{IT^-}))</td>
<td>3 V</td>
<td>0.75</td>
<td>1.65</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{Pull} ) Pullup/pulldown resistor</td>
<td>20 - 35 kΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_I ) Input capacitance</td>
<td></td>
<td>( V_{IN} = V_{SS} ) or ( V_{CC} )</td>
<td>5</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Leakage Current (Port P1)
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( V_{CC} )</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{\text{hlg}(P\times y)} ) High-impedance leakage current</td>
<td>/3 V</td>
<td>±50 nA</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) The leakage current is measured with \( V_{SS} \) or \( V_{CC} \) applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

Outputs (Port P1)
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( V_{CC} )</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OH} ) High-level output voltage</td>
<td>3 V</td>
<td>( V_{CC} - 0.6 )</td>
<td>( V_{CC} )</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OL} ) Low-level output voltage</td>
<td>3 V</td>
<td>( V_{SS} )</td>
<td>( V_{SS} + 0.6 )</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) The maximum total current, \( I_{\text{OH}max} \) and \( I_{\text{OL}max} \), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

Output Frequency (Port P1)
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( V_{CC} )</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{Px,y} ) Port output frequency (with load)</td>
<td>( C_L = 20 \ pF, \ R_L = 1 \ k\Omega )</td>
<td>3 V</td>
<td>12</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_{\text{Port CLK}} ) Clock output frequency</td>
<td>( C_L = 20 \ pF )</td>
<td>3 V</td>
<td>16</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) A resistive divider with two 0.5-kΩ resistors between \( V_{CC} \) and \( V_{SS} \) is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% \( V_{CC} \) at the specified toggle frequency.
Typical Characteristics – Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

Figure 8.

Figure 9.

Figure 10.

Figure 11.
POR and BOR\(^{(1)}\)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>(V_{\text{CC}})</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{CC(start)}})</td>
<td>See Figure 12</td>
<td>(dV_{\text{CC}}/dt \leq 3) V/s</td>
<td>(0.7 \times V_{(B_IT-)})</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{(B_IT-)})</td>
<td>See Figure 12 through Figure 14</td>
<td>(dV_{\text{CC}}/dt \leq 3) V/s</td>
<td>1.35</td>
<td>1 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{\text{hys(B_IT-)}})</td>
<td>See Figure 12</td>
<td>(dV_{\text{CC}}/dt \leq 3) V/s</td>
<td>140</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_d(BOR))</td>
<td>See Figure 12</td>
<td></td>
<td>2000</td>
<td>(\mu)s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{(\text{reset})})</td>
<td>Pulse duration needed at RST/NMI pin to accept reset internally</td>
<td>3 V</td>
<td>2</td>
<td>(\mu)s</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) The current consumption of the brownout module is already included in the \(I_{\text{CC}}\) current consumption data. The voltage level \(V_{(B\_IT-)} + V_{\text{hys(B\_IT-)}}\) is \(\leq 1.8\) V.

(2) During power up, the CPU begins code execution following a period of \(t_d(BOR)\) after \(V_{\text{CC}} = V_{(B\_IT-)} + V_{\text{hys(B\_IT-)}}\). The default DCO settings must not be changed until \(V_{\text{CC}} \geq V_{\text{CC(min)}}\), where \(V_{\text{CC(min)}}\) is the minimum supply voltage for the desired operating frequency.
Typical Characteristics – POR and BOR

Figure 13. V_{CC\text{drop}} Level With a Square Voltage Drop to Generate a POR or BOR Signal

Figure 14. V_{CC\text{drop}} Level With a Triangle Voltage Drop to Generate a POR or BOR Signal
Main DCO Characteristics

- All ranges selected by \( RSEL_x \) overlap with \( RSEL_x + 1 \): \( RSEL_x = 0 \) overlaps \( RSEL_x = 1 \), ... \( RSEL_x = 14 \) overlaps \( RSEL_x = 15 \).
- DCO control bits \( DCO_x \) have a step size as defined by parameter \( S_{DCO} \).
- Modulation control bits \( MOD_x \) select how often \( f_{DCO}(RSEL,DCO+1) \) is used within the period of 32 DCOCLK cycles. The frequency \( f_{DCO}(RSEL,DCO) \) is used for the remaining cycles. The frequency is an average equal to:

\[
    f_{\text{average}} = \frac{32 \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)}}
\]

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( V_{CC} )</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} )</td>
<td>Supply voltage</td>
<td>( RSEL_x &lt; 14 )</td>
<td>1.8</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( RSEL_x = 14 )</td>
<td>2.2</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( RSEL_x = 15 )</td>
<td>3.0</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( f_{DCO(0,0)} )</td>
<td>DCO frequency (0, 0)</td>
<td>( RSEL_x = 0, DCO_x = 0, MOD_x = 0 )</td>
<td>3 V</td>
<td>0.06</td>
<td>0.14</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{DCO(0,3)} )</td>
<td>DCO frequency (0, 3)</td>
<td>( RSEL_x = 0, DCO_x = 3, MOD_x = 0 )</td>
<td>3 V</td>
<td>0.12</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( f_{DCO(1,3)} )</td>
<td>DCO frequency (1, 3)</td>
<td>( RSEL_x = 1, DCO_x = 3, MOD_x = 0 )</td>
<td>3 V</td>
<td>0.15</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( f_{DCO(2,3)} )</td>
<td>DCO frequency (2, 3)</td>
<td>( RSEL_x = 2, DCO_x = 3, MOD_x = 0 )</td>
<td>3 V</td>
<td>0.21</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( f_{DCO(3,3)} )</td>
<td>DCO frequency (3, 3)</td>
<td>( RSEL_x = 3, DCO_x = 3, MOD_x = 0 )</td>
<td>3 V</td>
<td>0.30</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( f_{DCO(4,3)} )</td>
<td>DCO frequency (4, 3)</td>
<td>( RSEL_x = 4, DCO_x = 3, MOD_x = 0 )</td>
<td>3 V</td>
<td>0.41</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( f_{DCO(5,3)} )</td>
<td>DCO frequency (5, 3)</td>
<td>( RSEL_x = 5, DCO_x = 3, MOD_x = 0 )</td>
<td>3 V</td>
<td>0.58</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( f_{DCO(6,3)} )</td>
<td>DCO frequency (6, 3)</td>
<td>( RSEL_x = 6, DCO_x = 3, MOD_x = 0 )</td>
<td>3 V</td>
<td>0.80</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( f_{DCO(7,3)} )</td>
<td>DCO frequency (7, 3)</td>
<td>( RSEL_x = 7, DCO_x = 3, MOD_x = 0 )</td>
<td>3 V</td>
<td>0.80</td>
<td>1.50</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{DCO(8,3)} )</td>
<td>DCO frequency (8, 3)</td>
<td>( RSEL_x = 8, DCO_x = 3, MOD_x = 0 )</td>
<td>3 V</td>
<td>1.6</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( f_{DCO(9,3)} )</td>
<td>DCO frequency (9, 3)</td>
<td>( RSEL_x = 9, DCO_x = 3, MOD_x = 0 )</td>
<td>3 V</td>
<td>2.3</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( f_{DCO(10,3)} )</td>
<td>DCO frequency (10, 3)</td>
<td>( RSEL_x = 10, DCO_x = 3, MOD_x = 0 )</td>
<td>3 V</td>
<td>3.4</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( f_{DCO(11,3)} )</td>
<td>DCO frequency (11, 3)</td>
<td>( RSEL_x = 11, DCO_x = 3, MOD_x = 0 )</td>
<td>3 V</td>
<td>4.25</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( f_{DCO(12,3)} )</td>
<td>DCO frequency (12, 3)</td>
<td>( RSEL_x = 12, DCO_x = 3, MOD_x = 0 )</td>
<td>3 V</td>
<td>4.3</td>
<td>7.30</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{DCO(13,3)} )</td>
<td>DCO frequency (13, 3)</td>
<td>( RSEL_x = 13, DCO_x = 3, MOD_x = 0 )</td>
<td>3 V</td>
<td>7.8</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( f_{DCO(14,3)} )</td>
<td>DCO frequency (14, 3)</td>
<td>( RSEL_x = 14, DCO_x = 3, MOD_x = 0 )</td>
<td>3 V</td>
<td>8.6</td>
<td>13.9</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{DCO(15,3)} )</td>
<td>DCO frequency (15, 3)</td>
<td>( RSEL_x = 15, DCO_x = 3, MOD_x = 0 )</td>
<td>3 V</td>
<td>15.25</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( f_{DCO(15,7)} )</td>
<td>DCO frequency (15, 7)</td>
<td>( RSEL_x = 15, DCO_x = 7, MOD_x = 0 )</td>
<td>3 V</td>
<td>21</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( S_{RSEL} )</td>
<td>Frequency step between range RSEL and RSEL+1</td>
<td>( S_{RSEL} = \frac{f_{DCO}(RSEL+1,DCO)}{f_{DCO}(RSEL,DCO)} )</td>
<td>3 V</td>
<td>1.35</td>
<td>ratio</td>
<td></td>
</tr>
<tr>
<td>( S_{DCO} )</td>
<td>Frequency step between tap DCO and DCO+1</td>
<td>( S_{DCO} = \frac{f_{DCO}(RSEL,DCO+1)}{f_{DCO}(RSEL,DCO)} )</td>
<td>3 V</td>
<td>1.08</td>
<td>ratio</td>
<td></td>
</tr>
<tr>
<td>Duty cycle</td>
<td></td>
<td></td>
<td>3 V</td>
<td>50</td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>
### Calibrated DCO Frequencies - Tolerance Over Temperature 0°C to 85°C

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( T_A )</th>
<th>( V_{CC} )</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-MHz tolerance over temperature</td>
<td>BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V</td>
<td>0°C to 85°C</td>
<td>3 V</td>
<td>-3</td>
<td>±0.5</td>
<td>3</td>
<td>%</td>
</tr>
<tr>
<td>8-MHz tolerance over temperature</td>
<td>BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V</td>
<td>0°C to 85°C</td>
<td>3 V</td>
<td>-3</td>
<td>±1.0</td>
<td>3</td>
<td>%</td>
</tr>
<tr>
<td>12-MHz tolerance over temperature</td>
<td>BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V</td>
<td>0°C to 85°C</td>
<td>3 V</td>
<td>-3</td>
<td>±1.0</td>
<td>3</td>
<td>%</td>
</tr>
<tr>
<td>16-MHz tolerance over temperature</td>
<td>BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V</td>
<td>0°C to 85°C</td>
<td>3 V</td>
<td>-3</td>
<td>±2.0</td>
<td>3</td>
<td>%</td>
</tr>
</tbody>
</table>

### Calibrated DCO Frequencies - Tolerance Over Supply Voltage \( V_{CC} \)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( T_A )</th>
<th>( V_{CC} )</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-MHz tolerance over ( V_{CC} )</td>
<td>BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V</td>
<td>25°C</td>
<td>1.8 V to 3.6 V</td>
<td>-3</td>
<td>±2</td>
<td>+3</td>
<td>%</td>
</tr>
<tr>
<td>8-MHz tolerance over ( V_{CC} )</td>
<td>BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V</td>
<td>25°C</td>
<td>1.8 V to 3.6 V</td>
<td>-3</td>
<td>±2</td>
<td>+3</td>
<td>%</td>
</tr>
<tr>
<td>12-MHz tolerance over ( V_{CC} )</td>
<td>BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V</td>
<td>25°C</td>
<td>2.2 V to 3.6 V</td>
<td>-3</td>
<td>±2</td>
<td>+3</td>
<td>%</td>
</tr>
<tr>
<td>16-MHz tolerance over ( V_{CC} )</td>
<td>BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V</td>
<td>25°C</td>
<td>3 V to 3.6 V</td>
<td>-6</td>
<td>±2</td>
<td>+3</td>
<td>%</td>
</tr>
</tbody>
</table>

### Calibrated DCO Frequencies - Overall Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( T_A )</th>
<th>( V_{CC} )</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-MHz tolerance overall</td>
<td>BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V</td>
<td>I: -40°C to 85°C</td>
<td>1.8 V to 3.6 V</td>
<td>-5</td>
<td>±2</td>
<td>+5</td>
<td>%</td>
</tr>
<tr>
<td>8-MHz tolerance overall</td>
<td>BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V</td>
<td>I: -40°C to 85°C</td>
<td>1.8 V to 3.6 V</td>
<td>-5</td>
<td>±2</td>
<td>+5</td>
<td>%</td>
</tr>
<tr>
<td>12-MHz tolerance overall</td>
<td>BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V</td>
<td>I: -40°C to 85°C</td>
<td>2.2 V to 3.6 V</td>
<td>-5</td>
<td>±2</td>
<td>+5</td>
<td>%</td>
</tr>
<tr>
<td>16-MHz tolerance overall</td>
<td>BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V</td>
<td>I: -40°C to 85°C</td>
<td>3 V to 3.6 V</td>
<td>-6</td>
<td>±3</td>
<td>+6</td>
<td>%</td>
</tr>
</tbody>
</table>
Wake-Up From Lower-Power Modes (LPM3, LPM4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>V&lt;sub&gt;CC&lt;/sub&gt;</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>t&lt;sub&gt;DCO,LPM3/4&lt;/sub&gt;</td>
<td>BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz</td>
<td>2.2 V, 3 V</td>
<td>2</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz</td>
<td></td>
<td>1.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz</td>
<td>3 V</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;CPU,LPM3/4&lt;/sub&gt;</td>
<td>CPU wake-up time from LPM3 or LPM4&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<sup>(1)</sup> The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).

<sup>(2)</sup> Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics – DCO Clock Wake-Up Time From LPM3/4

![DCO Wake-Up Time From LPM3 vs DCO Frequency](image-url)
Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>V_{CC}</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>f_{VLO}</td>
<td>VLO frequency</td>
<td>-40°C to 85°C</td>
<td>3 V</td>
<td>4</td>
<td>12</td>
<td>20 kHz</td>
</tr>
<tr>
<td>df_{VLO}/dT</td>
<td>VLO frequency temperature drift $^{(1)}$</td>
<td>-40°C to 85°C</td>
<td>3 V</td>
<td>0.5</td>
<td>%/°C</td>
<td></td>
</tr>
<tr>
<td>df_{VLO}/dV_{CC}</td>
<td>VLO frequency supply voltage drift $^{(2)}$</td>
<td>25°C</td>
<td>1.8 V to 3.6 V</td>
<td>4 %/V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$^{(1)}$ Calculated using the box method: \((\text{MAX}(-40 \text{ to } 85°C) - \text{MIN}(-40 \text{ to } 85°C)) / \text{MIN}(-40 \text{ to } 85°C) / (85°C - (-40°C))\)

$^{(2)}$ Calculated using the box method: \((\text{MAX}(1.8 \text{ to } 3.6 V) - \text{MIN}(1.8 \text{ to } 3.6 V)) / \text{MIN}(1.8 \text{ to } 3.6 V) / (3.6 \text{ V} - 1.8 \text{ V})\)

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>V_{CC}</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
</table>
| f_{TA}             | Timer_A clock frequency  | Internal: SMCLK  
External: TACLK, INCLK  
Duty cycle = 50% ± 10%  |        |     |     |     | MHz |
| t_{TA,cap}         | Timer_A capture timing   | TAx    | 3 V | 20  |     | ns   |

USI, Universal Serial Interface (MSP430G2230 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>V_{CC}</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>f_{USI}</td>
<td>USI clock frequency</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>V_{OL,2C}</td>
<td>Low-level output voltage on SDA and SCL</td>
<td></td>
<td>3 V</td>
<td>V_{SS}</td>
<td>V_{SS} + 0.4</td>
<td>V</td>
</tr>
</tbody>
</table>

Typical Characteristics, USI Low-Level Output Voltage on SDA and SCL (MSP430G2230 Only)

Figure 16.

Figure 17.
Comparator_A+ (MSP430G2210 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{(DD)}^{(1)}$</td>
<td>CAON = 1, CARSEL = 0, CAREF = 0</td>
<td>3 V</td>
<td>45</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{(Refladder/}$</td>
<td>CAON = 1, CARSEL = 0, CAREF = 1/2/3,</td>
<td>3 V</td>
<td>45</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>RefDiode)</td>
<td>No load at CA0 and CA1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{(IC)}$</td>
<td>Common–mode input voltage</td>
<td>CAON = 1</td>
<td>3 V</td>
<td>0</td>
<td>$V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{(Ref025)}$</td>
<td>(Voltage at 0.25 $V_{CC}$ node) / $V_{CC}$</td>
<td>PCA0 = 1, CARSEL = 1, CAREF = 1, No load at CA0 and CA1</td>
<td>3 V</td>
<td>0.24</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{(Ref050)}$</td>
<td>(Voltage at 0.5 $V_{CC}$ node) / $V_{CC}$</td>
<td>PCA0 = 1, CARSEL = 1, CAREF = 2, No load at CA0 and CA1</td>
<td>3 V</td>
<td>0.48</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{(RefVT)}$</td>
<td>See Figure 18 and Figure 19</td>
<td>PCA0 = 1, CARSEL = 1, CAREF = 3, No load at CA0 and CA1, $T_A = 85^\circ$C</td>
<td>3 V</td>
<td>490</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$V_{(offset)}$</td>
<td>Offset voltage$^{(2)}$</td>
<td>CAON = 1</td>
<td>3 V</td>
<td>±10</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$V_{hys}$</td>
<td>Input hysteresis</td>
<td>CAON = 1</td>
<td>3 V</td>
<td>0.7</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$I_{(response)}$</td>
<td>Response time</td>
<td>$T_A = 25^\circ$, Overdrive 10 mV, Without filter: CAF = 0</td>
<td>3 V</td>
<td>120</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>(low-to-high and high-to-low)</td>
<td>$T_A = 25^\circ$, Overdrive 10 mV, With filter: CAF = 1</td>
<td>3 V</td>
<td>1.5</td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

(1) The leakage current for the Comparator_A+ terminals is identical to $I_{kg(P_{x,y})}$ specification.
(2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.
Typical Characteristics – Comparator_A+ (MSP430G2210 Only)

Figure 18. $V_{\text{RefVT}}$ vs Temperature, $V_{\text{CC}} = 3$ V

Figure 19. $V_{\text{RefVT}}$ vs Temperature, $V_{\text{CC}} = 2.2$ V

Figure 20. Short Resistance vs $\frac{V_{\text{IN}}}{V_{\text{CC}}}$
10-Bit ADC, Power Supply and Input Range Conditions (MSP430G2230 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$T_A$</th>
<th>$V_{CC}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{SS}$</td>
<td>$V_{SS} = 0 \text{ V}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{Ax}$</td>
<td>All Ax terminals, Analog inputs selected in ADC10AE register</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{ADC10}$</td>
<td>$I_{ADC10CLK} = 5.0 \text{ MHz},\ ADC10ON = 1, REFON = 0,\ ADC10SHT0 = 1,\ ADC10SHT1 = 0,\ ADC10DIV = 0$</td>
<td>25°C</td>
<td>3 V</td>
<td>0.6</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{REF+}$</td>
<td>$I_{ADC10CLK} = 5.0 \text{ MHz},\ ADC10ON = 0, REF2_5V = 0,\ REFON = 1,\ REFOUT = 0$</td>
<td>25°C</td>
<td>3 V</td>
<td>0.25</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{REFB,0}$</td>
<td>$I_{ADC10CLK} = 5.0 \text{ MHz},\ ADC10ON = 0, REF2_5V = 1,\ REFON = 1,\ REFOUT = 0$</td>
<td>25°C</td>
<td>3 V</td>
<td>1.1</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{REFB,1}$</td>
<td>$I_{ADC10CLK} = 5.0 \text{ MHz},\ ADC10ON = 0, REF2_5V = 0,\ REFOUT = 1,\ ADC10SR = 1$</td>
<td>25°C</td>
<td>3 V</td>
<td>0.5</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$C_i$</td>
<td>Only one terminal $Ax$ can be selected at one time</td>
<td>25°C</td>
<td>3 V</td>
<td></td>
<td>27</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$R_i$</td>
<td>$0 \text{ V} \leq V_{Ax} \leq V_{CC}$</td>
<td>25°C</td>
<td>3 V</td>
<td></td>
<td>1000</td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>

(1) The leakage current is defined in the leakage current table with $P_{x,y/Ax}$ parameter.
(2) The analog input voltage range must be within the selected reference voltage range $V_{RL}$ to $V_{RL}$ for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter $I_{ADC10}$. 
(4) The internal reference current is supplied by terminal $V_{CC}$. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.
## 10-Bit ADC, Built-In Voltage Reference (MSP430G2230 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>V&lt;sub&gt;CC&lt;/sub&gt;</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;CC,REF+&lt;/sub&gt;</td>
<td>Positive built-in reference analog supply voltage range</td>
<td></td>
<td></td>
<td>2.2</td>
<td>2.9</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.2</td>
<td>2.9</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;REF+&lt;/sub&gt;</td>
<td>Positive built-in reference voltage</td>
<td></td>
<td>3 V</td>
<td>1.41</td>
<td>1.5</td>
<td>1.59</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.35</td>
<td>2.5</td>
<td>2.65</td>
<td>V</td>
</tr>
<tr>
<td>I&lt;sub&gt;LD,VREF+&lt;/sub&gt;</td>
<td>Maximum VREF+ load current</td>
<td></td>
<td>3 V</td>
<td>±1 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±1 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VREF+ load regulation</td>
<td></td>
<td>3 V</td>
<td>±2 LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±2 LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;REF+&lt;/sub&gt; load regulation response time</td>
<td></td>
<td>3 V</td>
<td>400 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>400 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C&lt;sub&gt;VREF+&lt;/sub&gt;</td>
<td>Maximum capacitance at pin VREF+</td>
<td></td>
<td>3 V</td>
<td>100 pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>100 pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>T&lt;sub&gt;REF+&lt;/sub&gt;</td>
<td>Temperature coefficient&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td></td>
<td>3 V</td>
<td>±100 ppm/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±100 ppm/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;REFON&lt;/sub&gt;</td>
<td>Setting time of internal reference voltage to 99.9% VREF</td>
<td></td>
<td>3.6 V</td>
<td>30 µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>30 µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;REFBURST&lt;/sub&gt;</td>
<td>Setting time of reference buffer to 99.9% VREF</td>
<td></td>
<td>3 V</td>
<td>2 µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2 µs</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<sup>(1)</sup> Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))
10-Bit ADC, External Reference (MSP430G2230 Only)\(^{(1)}\)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>(V_{CC})</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{REF+})</td>
<td>Positive external reference input voltage range (^{(2)})</td>
<td>(V_{REF+} &gt; V_{REF-})</td>
<td>1.4</td>
<td>(V_{CC})</td>
<td>1.4</td>
<td>(V)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(SREF1 = 1, SREF0 = 0)</td>
<td></td>
<td></td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>(V_{REF-})</td>
<td>Negative external reference input voltage range (^{(4)})</td>
<td>(V_{REF-} \leq V_{REF+} \leq V_{CC} - 0.15\ V, SREF1 = 1, SREF0 = 0)</td>
<td>1.4</td>
<td>(V_{CC})</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>(\Delta V_{REF})</td>
<td>Differential external reference input voltage range, (\Delta V_{REF} = V_{REF+} - V_{REF-})</td>
<td>(V_{REF+} &gt; V_{REF-}) (^{(5)})</td>
<td>1.4</td>
<td>(V_{CC})</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>(I_{V{REF+}})</td>
<td>Static input current into (V_{REF+})</td>
<td>(0 \leq V_{REF+} \leq V_{CC} - 0.15\ V, SREF1 = 1, SREF0 = 0)</td>
<td>3</td>
<td>(V)</td>
<td>±1</td>
<td>(\mu\A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(0 \leq V_{REF+} \leq 3\ V, SREF1 = 1, SREF0 = 0)</td>
<td></td>
<td></td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>(I_{V{REF-}})</td>
<td>Static input current into (V_{REF-})</td>
<td>(0 \leq V_{REF-} \leq V_{CC})</td>
<td>3</td>
<td>(V)</td>
<td>±1</td>
<td>(\mu\A)</td>
</tr>
</tbody>
</table>

\(^{(1)}\) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, \(C_{I}\), is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.

\(^{(2)}\) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.

\(^{(3)}\) Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current \(I_{REFB}\). The current consumption can be limited to the sample and conversion period with \(REBURST = 1\).

\(^{(4)}\) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.

\(^{(5)}\) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

10-Bit ADC, Timing Parameters (MSP430G2230 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>(V_{CC})</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(f_{ADC10CLK})</td>
<td>ADC10 input clock frequency</td>
<td>For specified performance of ADC10 linearity parameters</td>
<td>3</td>
<td>(V)</td>
<td>0.45</td>
<td>6.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ADC10SR = 0</td>
<td></td>
<td></td>
<td>0.45</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ADC10SR = 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(f_{ADC10OSC})</td>
<td>ADC10 built-in oscillator frequency</td>
<td>ADC10DIVx = 0, ADC10SSELx = 0, (f_{ADC10CLK} = f_{ADC10OSC})</td>
<td>3</td>
<td>(V)</td>
<td>3.7</td>
<td>6.3</td>
</tr>
<tr>
<td>(t_{CONVERT})</td>
<td>Conversion time</td>
<td>ADC10 built-in oscillator, ADC10SSELx = 0, (f_{ADC10CLK} = f_{ADC10OSC}) (\Delta V_{REF} = V_{REF+} - V_{REF-}) (^{(5)})</td>
<td>3</td>
<td>(V)</td>
<td>2.06</td>
<td>3.51</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(f_{ADC10CLK}) from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0</td>
<td></td>
<td></td>
<td>(13 \times 1/ADC10DIV) (\div 1/f_{ADC10CLK})</td>
<td></td>
</tr>
<tr>
<td>(t_{ADC10ON})</td>
<td>Turn-on settling time of the ADC (^{(1)})</td>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td>(ns)</td>
</tr>
</tbody>
</table>

\(^{(1)}\) The condition is that the error in a conversion started after \(t_{ADC10ON}\) is less than ±0.5 LSB. The reference and input signal are already settled.

10-Bit ADC, Linearity Parameters (MSP430G2230 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>(V_{CC})</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(E_{I})</td>
<td>Integral linearity error</td>
<td>3</td>
<td>(V)</td>
<td>±1</td>
<td></td>
<td>(LSB)</td>
</tr>
<tr>
<td>(E_{D})</td>
<td>Differential linearity error</td>
<td>3</td>
<td>(V)</td>
<td>±1</td>
<td></td>
<td>(LSB)</td>
</tr>
<tr>
<td>(E_{O})</td>
<td>Offset error</td>
<td>Source impedance (R_{S} &lt; 100\ \Omega)</td>
<td>3</td>
<td>(V)</td>
<td>±1</td>
<td></td>
</tr>
<tr>
<td>(E_{G})</td>
<td>Gain error</td>
<td>3</td>
<td>(V)</td>
<td>±1.1</td>
<td>±2</td>
<td></td>
</tr>
<tr>
<td>(E_{T})</td>
<td>Total unadjusted error</td>
<td>3</td>
<td>(V)</td>
<td>±2</td>
<td>±5</td>
<td></td>
</tr>
</tbody>
</table>
10-Bit ADC, Temperature Sensor and Built-In $V_{\text{MID}}$ (MSP430G2230 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{\text{CC}}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{\text{SENSOR}}$</td>
<td>Temperature sensor supply current $^{(1)}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$T_{\text{CSENSOR}}$</td>
<td>REFON = 0, INCHx = 0Ah, $T_A = 25^\circ\text{C}$</td>
<td>3 V</td>
<td>60</td>
<td></td>
<td></td>
<td>mV/°C</td>
</tr>
<tr>
<td>$I_{\text{Sensor(sample)}}$</td>
<td>ADC10ON = 1, INCHx = 0Ah $^{(2)}$</td>
<td>3 V</td>
<td>3.55</td>
<td></td>
<td></td>
<td>mV/°C</td>
</tr>
<tr>
<td>$I_{\text{VMID}}$</td>
<td>Sample time required if channel 10 is selected $^{(3)}$</td>
<td>3 V</td>
<td>30</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$V_{\text{MID}}$</td>
<td>ADC10ON = 1, INCHx = 0Bh</td>
<td>3 V</td>
<td>1.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{MID(sample)}}$</td>
<td>ADC10ON = 1, INCHx = 0Bh, $V_{\text{MID}} \approx 0.5 \times V_{\text{CC}}$</td>
<td>3 V</td>
<td>1220</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

$^{(1)}$ The sensor current $I_{\text{SENSOR}}$ is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, $I_{\text{SENSOR}}$ is included in $I_{\text{REF+}}$. When REFON = 0, $I_{\text{SENSOR}}$ applies during conversion of the temperature sensor input (INCH = 0Ah).

$^{(2)}$ The following formula can be used to calculate the temperature sensor output voltage:

$$V_{\text{Sensor,typ}} = T_{\text{CSENSOR}} (273 + T [\degree\text{C}]) + V_{\text{Offset,sensor}} [\text{mV}]$$

$^{(3)}$ The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $I_{\text{SENSOR(on)}}$.

$^{(4)}$ No additional current is needed. The $V_{\text{MID}}$ is used during sampling.

$^{(5)}$ The on-time $t_{\text{VMID(on)}}$ is included in the sampling time $I_{\text{VMID(sample)}}$; no additional on time is needed.
## Flash Memory

Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>Vcc</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC(PGM/ERASE)}$</td>
<td>Program and erase supply voltage</td>
<td>2.2</td>
<td>3.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$f_{FTG}$</td>
<td>Flash timing generator frequency</td>
<td>257</td>
<td>476</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{PGM}$</td>
<td>Supply current from $V_{CC}$ during program</td>
<td>2.2 V, 3.6 V</td>
<td>1</td>
<td>5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{ERASE}$</td>
<td>Supply current from $V_{CC}$ during erase</td>
<td>2.2 V, 3.6 V</td>
<td>1</td>
<td>7</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$t_{CPT}$</td>
<td>Cumulative program time&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>2.2 V, 3.6 V</td>
<td>10</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{CMErase}$</td>
<td>Cumulative mass erase time</td>
<td>2.2 V, 3.6 V</td>
<td>20</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{Retention}$</td>
<td>Data retention duration</td>
<td>$T_J = 25^\circ C$</td>
<td>10&lt;sup&gt;4&lt;/sup&gt;</td>
<td>10&lt;sup&gt;5&lt;/sup&gt;</td>
<td>cycles</td>
<td></td>
</tr>
<tr>
<td>$t_{Word}$</td>
<td>Word or byte program time</td>
<td>(2)</td>
<td>30</td>
<td>$f_{FTG}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{Block, 0}$</td>
<td>Block program time for first byte or word</td>
<td>(2)</td>
<td>25</td>
<td>$f_{FTG}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{Block, 1-63}$</td>
<td>Block program time for each additional byte or word</td>
<td>(2)</td>
<td>18</td>
<td>$f_{FTG}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{Block, End}$</td>
<td>Block program end-sequence wait time</td>
<td>(2)</td>
<td>6</td>
<td>$f_{FTG}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{Mass Erase}$</td>
<td>Mass erase time</td>
<td>(2)</td>
<td>10593</td>
<td>$f_{FTG}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{Seg Erase}$</td>
<td>Segment erase time</td>
<td>(2)</td>
<td>4819</td>
<td>$f_{FTG}$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<sup>(1)</sup> The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.

<sup>(2)</sup> These values are hardwired into the Flash Controller's state machine ($f_{FTG} = 1/f_{FTG}$).

## RAM

Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(RAMh)}$</td>
<td>RAM retention supply voltage&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>CPU halted</td>
<td>1.6</td>
<td>V</td>
</tr>
</tbody>
</table>

<sup>(1)</sup> This parameter defines the minimum supply voltage $V_{CC}$ when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

## Spy-Bi-Wire Interface

Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{SBW}$</td>
<td>Spy-Bi-Wire input frequency</td>
<td>2.2 V, 3 V</td>
<td>0</td>
<td>20</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{SBW,Low}$</td>
<td>Spy-Bi-Wire low clock pulse duration</td>
<td>2.2 V, 3 V</td>
<td>0.025</td>
<td>15</td>
<td>µs</td>
</tr>
<tr>
<td>$f_{SBW,En}$</td>
<td>Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge&lt;sup&gt;(1)&lt;/sup&gt;)</td>
<td>2.2 V, 3 V</td>
<td>1</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$f_{SBW,Ret}$</td>
<td>Spy-Bi-Wire return to normal operation time</td>
<td>2.2 V, 3 V</td>
<td>15</td>
<td>100</td>
<td>µs</td>
</tr>
<tr>
<td>$R_{Internal}$</td>
<td>Internal pulldown resistance on TEST</td>
<td>2.2 V, 3 V</td>
<td>25</td>
<td>60</td>
<td>90</td>
</tr>
</tbody>
</table>

<sup>(1)</sup> Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.

## JTAG Fuse<sup>(1)</sup>

Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC,(FB)}$</td>
<td>Supply voltage during fuse-blow condition</td>
<td>$T_A = 25^\circ C$</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{FB}$</td>
<td>Voltage level on TEST for fuse blow</td>
<td>6</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>$I_{FB}$</td>
<td>Supply current into TEST during fuse blow</td>
<td>100</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$t_{FB}$</td>
<td>Time to blow fuse</td>
<td>1</td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

<sup>(1)</sup> After the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.
APPLICATION INFORMATION

Port (P1.2 and P1.5) Pin Schematics - MSP430G2210

Figure 21.

Table 15. Port P1 (P1.2 to P1.5) Pin Functions - MSP430G2210

<table>
<thead>
<tr>
<th>PIN NAME (P1.x)</th>
<th>x</th>
<th>FUNCTION</th>
<th>CONTROL BITS AND SIGNALS(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1.2/TA0.1/CA2</td>
<td>2</td>
<td>P1.x (I/O)</td>
<td>P1DIR.x</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I: 0; O: 1</td>
<td>1</td>
</tr>
<tr>
<td>P1.5/TA0.0/CA5</td>
<td>5</td>
<td>P1.x (I/O)</td>
<td>P1DIR.x</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I: 0; O: 1</td>
<td>1</td>
</tr>
</tbody>
</table>

(1) X = don’t care
Port P1 (P1.6 and 1.7) Pin Schematic - MSP430G2210

Figure 22.
Figure 23.

Table 16. Port P1 (P1.6 and P1.7) Pin Functions - MSP430G2210

<table>
<thead>
<tr>
<th>PIN NAME (P1.x)</th>
<th>x</th>
<th>FUNCTION</th>
<th>CONTROL BITS AND SIGNALS(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1.6/TA0.1/CA6</td>
<td>6</td>
<td>P1.x (I/O)</td>
<td>P1DIR.x P1SEL.x CAPD.y</td>
</tr>
<tr>
<td>P1.7/CA7/CAOUT</td>
<td>7</td>
<td>P1.x (I/O)</td>
<td>X X 1 (y = 7)</td>
</tr>
</tbody>
</table>

(1) X = don't care
Port P1 (P1.2 ) Pin Schematics - MSP430G2230

Figure 24.

Table 17. Port P1 (P1.2) Pin Functions - MSP430G2230

<table>
<thead>
<tr>
<th>PIN NAME (P1.x)</th>
<th>x</th>
<th>FUNCTION</th>
<th>CONTROL BITS AND SIGNALS(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>P1DIR.x</td>
</tr>
<tr>
<td>P1.2/TA0.1/</td>
<td>2</td>
<td>P1.x (I/O)</td>
<td>I: 0</td>
</tr>
<tr>
<td>A2</td>
<td></td>
<td>TA0.1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TA0.CCI1A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A2</td>
<td>X</td>
</tr>
</tbody>
</table>

(1) X = don’t care
Table 18. Port P1 (P1.5) Pin Functions - MSP430G2230

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>x</th>
<th>FUNCTION</th>
<th>CONTROL BITS AND SIGNALS(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1.5/</td>
<td>5</td>
<td>P1.x (I/O)</td>
<td>P1DIR.x  P1SEL.x  USIP.x  ADC10AE.x  INCHx</td>
</tr>
<tr>
<td>TA0.0/</td>
<td></td>
<td>TA0.0</td>
<td>1  1  0  0  0 X</td>
</tr>
<tr>
<td>SCLK/</td>
<td></td>
<td>SCLK</td>
<td>X  X  1  X  X</td>
</tr>
<tr>
<td>A5</td>
<td></td>
<td>A5</td>
<td>X  X  X  1 (y = 5)  5</td>
</tr>
</tbody>
</table>

(1) X = don’t care
Port P1 (P1.6 and 1.7) Pin Schematic - MSP430G2230

USI in I2C mode: Output driver drives low level only.

Figure 26.
### Table 19. Port P1 (P1.6 and P1.7) Pin Functions - MSP430G2230

<table>
<thead>
<tr>
<th>PIN NAME (P1.x)</th>
<th>x</th>
<th>FUNCTION</th>
<th>CONTROL BITS AND SIGNALS(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>P1DIR.x</td>
</tr>
<tr>
<td>P1.6/TA0.1</td>
<td>6</td>
<td>P1.x (I/O)</td>
<td>I: 0; O: 1</td>
</tr>
<tr>
<td>SDO/SCL/A6</td>
<td>6</td>
<td>TA0.CC11A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>TA0.1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>SPI Mode</td>
<td>from USI</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>I2C Mode</td>
<td>from USI</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>A6</td>
<td>X</td>
</tr>
<tr>
<td>P1.7/SDI/SDA/A7</td>
<td>7</td>
<td>P1.x (I/O)</td>
<td>I: 0; O: 1</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>SDI</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>SDA</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>A7</td>
<td>X</td>
</tr>
</tbody>
</table>

(1) X = don’t care

### Figure 27.
## REVISION HISTORY

<table>
<thead>
<tr>
<th>Literature Number</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLAS753</td>
<td>Production Data release</td>
</tr>
</tbody>
</table>
| SLAS753A          | Changed Table 11.  
                    | Added Table 12. |
| SLAS753B          | Corrected “Basic Clock Module Configurations” list in Features.  
                    | Added note to TCREF, in 10-Bit ADC, Built-In Voltage Reference (MSP430G2230 Only). |
| SLAS753C          | Added Flash Memory. |
| SLAS753D          | Table 15, Removed ADC10AE.x column and removed A2 and A5 rows (no ADC on this device).  
                    | Table 18, Added USIP,x column.  
                    | Table 19, Added “(INCH,y = 1)” to ADC10AE.x column header. |
| SLAS753E          | Recommended Operating Conditions, Added test conditions for typical values.  
                    | POR and BOR, Added note (2). |
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSP430G2210ID</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>G2210</td>
<td>Samples</td>
</tr>
<tr>
<td>MSP430G2210IDR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>G2210</td>
<td>Samples</td>
</tr>
<tr>
<td>MSP430G2230ID</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>G2230</td>
<td>Samples</td>
</tr>
<tr>
<td>MSP430G2230IDR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>G2230</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF MSP430G2230:**


NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications
TAPE AND REEL INFORMATION

REEL DIMENSIONS

- Reel Diameter
- Reel Width (W1)

TAPE DIMENSIONS

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- Pocket Quadrants
- Sprocket Holes
- User Direction of Feed

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSP430G2210IDR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>MSP430G2230IDR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSP430G2210IDR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
</tr>
<tr>
<td>MSP430G2230IDR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
**TUBE**

![Diagram of TUBE dimensions]

- **T** - Tube height
- **W** - Tube width
- **L** - Tube length
- **B** - Alignment groove width

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Name</th>
<th>Package Type</th>
<th>Pins</th>
<th>SPQ</th>
<th>L (mm)</th>
<th>W (mm)</th>
<th>T (µm)</th>
<th>B (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSP430G2210ID</td>
<td>D</td>
<td>SOIC</td>
<td>8</td>
<td>75</td>
<td>506.6</td>
<td>8</td>
<td>3940</td>
<td>4.32</td>
</tr>
<tr>
<td>MSP430G2230ID</td>
<td>D</td>
<td>SOIC</td>
<td>8</td>
<td>75</td>
<td>506.6</td>
<td>8</td>
<td>3940</td>
<td>4.32</td>
</tr>
</tbody>
</table>
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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