Low Power, Precision
FET-INPUT OPERATIONAL AMPLIFIERS

FEATURES
- LOW QUIESCENT CURRENT: 530μA/amp
- LOW OFFSET VOLTAGE: 1mV max
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH CMRR: 90dB min
- FET INPUT: I_b = 20pA max
- EXCELLENT BANDWIDTH: 1MHz
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- SINGLE, DUAL, AND QUAD VERSIONS

DESCRIPTION
The OPA130 series of FET-input op amps combine precision dc performance with low quiescent current. Single, dual, and quad versions have identical specifications for maximum design flexibility. They are ideal for general-purpose, portable, and battery operated applications, especially with high source impedance.

OPA130 op amps are easy to use and free from phase inversion and overload problems often found in common FET-input op amps. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over its wide input voltage range. OPA130 series op amps are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Single and dual versions are available in DIP-8 and SO-8 surface-mount packages. Quad is available in DIP-14 and SO-14 surface-mount packages. All are specified for −40°C to +85°C operation.
ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Specification</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, V+ to V-</td>
<td>36V</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>(V-) –0.7V to (V+)+0.7V</td>
</tr>
<tr>
<td>Output Short-Circuit (2)</td>
<td>Continuous</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>–40°C to +125°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>–40°C to +125°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>150°C</td>
</tr>
</tbody>
</table>

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Short-circuit to ground, one amplifier per package.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.
ELECTRICAL CHARACTERISTICS

At \( T_A = +25^\circ\text{C}, \ V_S = \pm 15\text{V}, \) and \( R_L = 10k\Omega, \) unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>OPA130PA, UA</th>
<th>OPA2130PA, UA</th>
<th>OPA4130PA, UA</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
</tr>
</tbody>
</table>

**OFFSET VOLTAGE**
- Input Offset Voltage: \( \pm 0.2 \text{mV} \)
- Channel Separation (dual and quad): \( 0.3 \text{µV} \)

**INPUT BIAS CURRENT**
- Input Bias Current: \( \pm 5 \text{µA} \)
- Input Offset Current: \( \pm 2 \text{µA} \)

**NOISE**
- Input Voltage Noise: \( 30 \text{nV/√Hz} \)
- Current Noise Density, \( f = 1\text{kHz} \): \( 4 \text{fA/√Hz} \)

**INPUT VOLTAGE RANGE**
- Common-Mode Voltage Range, Positive: \( -13 \text{V} \) to \( +13\text{V} \)
- Common-Mode Rejection: \( 90 \text{dB} \)

**INPUT IMPEDANCE**
- Differential: \( 10^{13} \| 1 \text{Ω} \) || \( 10 \text{pF} \)
- Common-Mode: \( 10^{13} \| 3 \text{Ω} \) || \( 3 \text{pF} \)

**OPEN-LOOP GAIN**
- Open-loop Voltage Gain (V\(_O\)):
  - \( V_O = -13.8\text{V} \) to \( +13\text{V} \)
  - \( R_L = 2k\Omega, \ V_O = -13\text{V} \) to \( +12\text{V} \)

**FREQUENCY RESPONSE**
- Gain-Bandwidth Product:
  - 1 \text{MHz} \)
- Slew Rate:
  - 2 V/\(µ\text{s} \)
- Settling Time: 0.1%:
  - 5.5 \(µ\text{s} \)
- Overload Recovery Time:
  - 7 \(µ\text{s} \)
- Total Harmonic Distortion + Noise:
  - 0.0003 %

**OUTPUT**
- Voltage Output, Positive:
  - \( R_L = 2k\Omega \)
  - \( (V+) = -2 \text{V} \)
  - \( (V+) = -1.5 \text{V} \)
- Negative:
  - \( (V-) = +1 \text{V} \)
  - \( (V-) = +1.2 \text{V} \)
- Positive:
  - \( (V+) = +2.5 \text{V} \)
  - \( (V+) = +1.5 \text{V} \)
- Negative:
  - \( (V-) = -18 \text{mA} \)
  - \( (V-) = +18 \text{mA} \)

**POWER SUPPLY**
- Specified Operating Voltage:
  - \( ±15 \text{V} \)
- Operating Voltage Range:
  - \( ±18 \text{V} \)
- Quiescent Current (per amplifier):
  - \( ±530 \text{µA} \)
  - \( ±650 \text{µA} \)

**TEMPERATURE RANGE**
- Operating Range:
  - \( -40 \) to \( +85 \text{°C} \)
- Storage:
  - \( -40 \) to \( +125 \text{°C} \)

**NOTES:** (1) Ensured by wafer test. (2) High-speed test at \( T_J = 25^\circ\text{C} \).
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ \text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 10\text{k}\Omega$, unless otherwise noted.

- **Input Voltage and Current Noise Spectral Density vs Frequency**
- **Channel Separation vs Frequency**
- **Input Bias and Input Offset Current vs Temperature**
- **Input Bias Current vs Input Common-Mode Voltage**
- **Open-Loop Gain/Phase vs Frequency**
- **Power Supply and Common-Mode Rejection vs Frequency**
TYPICAL CHARACTERISTICS (Cont.)

At \( T_A = +25^\circ \text{C} \), \( V_S = \pm 15 \text{V} \), and \( R_L = 10\text{k}\Omega \), unless otherwise noted.

[Graphs and charts showing typical characteristics such as maximum output voltage vs frequency, offset voltage production distribution, total harmonic distortion + noise vs frequency, and quiescent current and short-circuit current vs temperature.]

**OFFSET VOLTAGE PRODUCTION DISTRIBUTION**

**OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION**

**TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY**

**MAXIMUM OUTPUT VOLTAGE vs FREQUENCY**
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ C$, $V_S = \pm 15V$, and $R_L = 10k\Omega$, unless otherwise noted.

**SMALL-SIGNAL STEP RESPONSE**

$G = 1, C_L = 100pF$

500ns/div

$G = 1, C_L = 1000pF$

5µs/div

**LARGE-SIGNAL STEP RESPONSE**

$G = 1, C_L = 100pF$

5µs/div

**SMALL-SIGNAL OVERSHoot**

vs LOAD CAPACITANCE

<table>
<thead>
<tr>
<th>Load Capacitance (F)</th>
<th>10pF</th>
<th>100pF</th>
<th>1nF</th>
<th>10nF</th>
<th>100nF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overshoot (%)</td>
<td>80%</td>
<td>70%</td>
<td>60%</td>
<td>50%</td>
<td>40%</td>
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</table>

**OUTPUT VOLTAGE SWING vs OUTPUT CURRENT**

<table>
<thead>
<tr>
<th>Output Current (mA)</th>
<th>±5</th>
<th>±10</th>
<th>±15</th>
<th>±20</th>
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<tbody>
<tr>
<td>Output Voltage Swing (V)</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
</tr>
</tbody>
</table>

**SETTLING TIME vs GAIN**

Gain (V/V) | ±1 | ±10 | ±100 |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Settling Time (µs)</td>
<td>100</td>
<td>10</td>
<td>1</td>
</tr>
</tbody>
</table>

**SMALL-SIGNAL OVERSHOOT**

vs LOAD CAPACITANCE

<table>
<thead>
<tr>
<th>Load Capacitance (F)</th>
<th>±5</th>
<th>±10</th>
<th>±100</th>
</tr>
</thead>
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<tr>
<td>Overshoot (%)</td>
<td>80%</td>
<td>70%</td>
<td>60%</td>
</tr>
</tbody>
</table>
APPLICATIONS INFORMATION

OPA130 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10nF ceramic capacitors or larger.

OPA130 op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. OPA130 series op amps are free from this undesirable behavior. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

OPERATING VOLTAGE

OPA130 series op amps operate with power supplies from $\pm 2.25V$ to $\pm 18V$ with excellent performance. Although specifications are production tested with $\pm 15V$ supplies, most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical performance curves.

OFFSET VOLTAGE TRIM

Offset voltage of OPA130 series amplifiers is laser trimmed and usually requires no user adjustment. The OPA130 (single op amp version) provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset that is not produced by the amplifier will change the offset voltage drift behavior of the op amp.

![FIGURE 1. OPA130 Offset Voltage Trim Circuit.](image-url)
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA130UA</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>OPA130UA</td>
<td></td>
</tr>
<tr>
<td>OPA130UA/2K5</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>OPA130UA</td>
<td></td>
</tr>
<tr>
<td>OPA130UA/2K5E4</td>
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<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>OPA130UA</td>
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<td>OPA130UAE4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>OPA130UA</td>
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<tr>
<td>OPA2130UA</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>OPA2130UA</td>
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</tr>
<tr>
<td>OPA2130UA/2K5</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>OPA2130UA</td>
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<tr>
<td>OPA2130UAE4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>OPA2130UA</td>
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<tr>
<td>OPA4130UA</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU-DCC</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>OPA4130UA</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA4130UA/2K5</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU-DCC</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>OPA4130UA</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp. -** The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) **Eco Plan:**

- **Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- **NIPDAU:** No internal packages used.

(5) **Lead/Ball Finish:**

- **NIPDAU:** No internal packages used.

- **DCC:** Dry-Cured Curing.

(6) **Samples:**

- **Samples:** Available for review.
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a “~” will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<tbody>
<tr>
<td>OPA130UA/2K5</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
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<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
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<td>Q1</td>
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<td>D</td>
<td>8</td>
<td>2500</td>
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<td>12.4</td>
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<td>12.0</td>
<td>Q1</td>
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TAPE AND REEL BOX DIMENSIONS

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<tr>
<th>Device</th>
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<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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<tbody>
<tr>
<td>OPA130UA/2K5</td>
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<td>367.0</td>
<td>367.0</td>
<td>38.0</td>
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</tbody>
</table>

*All dimensions are nominal
NOTES:  
A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.  
⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.  
E. Reference JEDEC MS-012 variation AB.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.

4. This dimension does not include interlead flash.

5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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