OPAx210 2.2-nV/√Hz Precision, Low-Power, 36-V Operational Amplifiers

1 Features
- Precision super beta input performance:
  - Low offset voltage: 5 µV (typical)
  - Ultra-low drift: 0.1 µV/°C (typical)
  - Low input bias current: 0.3 nA (typical)
- Ultra-low noise:
  - Low 0.1-Hz to 10-Hz noise: 90 nV
  - Low voltage noise: 2.2 nV/√Hz at 1 kHz
- High CMRR: 132 dB (minimum)
- Gain bandwidth product: 18 MHz
- Slew rate: 6.4 V/µs
- Low quiescent current: 2.5 mA/channel (maximum)
- Wide supply range: ±2.25 V to ±18 V
- No phase reversal
- Rail-to-rail output
- Industry-standard packages

2 Applications
- Ultrasound scanner
- Multiparameter patient monitor
- Merchant network and server PSU
- Semiconductor test
- Spectrum analyzer
- Lab and field instrumentation
- Data acquisition (DAQ)
- Professional microphone and wireless systems

3 Description
The OPA210 and OPA2210 (OPAx210) are the next generation of OPAx209 operational amplifier (op amp). The OPAx210 precision op amps are built on TI’s precision, super-beta, complementary bipolar semiconductor process, which offers ultra-low flicker noise, low offset voltage, and low offset voltage temperature drift.

The OPAx210 achieve very low voltage noise density (2.2 nV/√Hz) while consuming only 2.5 mA (maximum) per amplifier. These devices also offer rail-to-rail output swing, which helps maximize dynamic range.

In precision data-acquisition applications, the OPAx210 provide fast settling time to 16-bit accuracy, even for 10-V output swings. Excellent ac performance, combined with only 35 µV (maximum) of offset and 0.6 µV/°C (maximum) drift over temperature, makes the OPAx210 an excellent choice for high-speed, high-precision applications.

The OPAx210 are specified over a wide dual power-supply range of ±2.25 V to ±18 V, or single-supply operation from 4.5 V to 36 V, are specified from –40°C to +125°C.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA210</td>
<td>SOIC (8)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
<tr>
<td></td>
<td>SOT-23 (5) (Preview)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
<tr>
<td></td>
<td>VSSOP (8) (Preview)</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
<tr>
<td>OPA2210</td>
<td>SOIC (8)</td>
<td>4.90 mm × 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>VSSOP (8)</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
<tr>
<td></td>
<td>WSON (8)</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the package option addendum at the end of the data sheet.
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# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## Changes from Revision F (January 2021) to Revision G (April 2021)

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed OPA210 D (SOIC-8) package from advanced information (preview) to production data (active) ........................................ 1</td>
</tr>
<tr>
<td>• Added OPA210 DBV (SOT-23-5) package as advanced information (preview) .......................................................... 1</td>
</tr>
</tbody>
</table>

## Changes fromRevision E (November 2020) to Revision F (January 2021)

<table>
<thead>
<tr>
<th>Page</th>
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</thead>
<tbody>
<tr>
<td>• Added OPA210 device with D and DGK packages as advanced information (preview) ........................................ 1</td>
</tr>
</tbody>
</table>

## Changes from Revision D (January 2020) to Revision E (November 2020)

<table>
<thead>
<tr>
<th>Page</th>
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</thead>
<tbody>
<tr>
<td>• Changed OPA2210 DRG package from advanced information (preview) to production data (active) ........................................ 1</td>
</tr>
</tbody>
</table>

## Changes from Revision C (September 2019) to Revision D (January 2020)

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Added OPA2210 DRG package to data sheet as advanced information (preview) ........................................ 1</td>
</tr>
</tbody>
</table>

## Changes from Revision B (March 2019) to Revision C (September 2019)

<table>
<thead>
<tr>
<th>Page</th>
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<tbody>
<tr>
<td>• Changed super-ß to super beta for easier searching .......................................................... 1</td>
</tr>
<tr>
<td>• Added SOIC package ................................................ 1</td>
</tr>
</tbody>
</table>

## Changes from Revision A (December 2018) to Revision B (February 2019)

<table>
<thead>
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<th>Page</th>
</tr>
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<tbody>
<tr>
<td>• Changed &quot;OPAx145&quot; to &quot;OPA2210&quot; ........................................ 19</td>
</tr>
<tr>
<td>• Fixed link to TIDA-01427 .................................................. 21</td>
</tr>
</tbody>
</table>

## Changes from Revision * (September 2018) to Revision A (December 2018)

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• First release of production-data data sheet .......................................................... 1</td>
</tr>
</tbody>
</table>
5 Pin Configuration and Functions

![Pin Configuration Diagram](Not to scale)

Figure 5-1. OPA210: D (8-Pin SOIC) and DGK (8-Pin VSSOP, Preview) Packages, Top View

Table 5-1. Pin Functions: OPA210

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>NO.</td>
<td></td>
</tr>
<tr>
<td>–IN</td>
<td>2</td>
<td>Inverting input</td>
</tr>
<tr>
<td>+IN</td>
<td>3</td>
<td>Noninverting input</td>
</tr>
<tr>
<td>NC</td>
<td>1, 5, 8</td>
<td>No internal connection</td>
</tr>
<tr>
<td>OUT</td>
<td>6</td>
<td>Output</td>
</tr>
<tr>
<td>V–</td>
<td>4</td>
<td>Negative (lowest) power supply</td>
</tr>
<tr>
<td>V+</td>
<td>7</td>
<td>Positive (highest) power supply</td>
</tr>
</tbody>
</table>

![Pin Configuration Diagram](Not to scale)

Figure 5-2. OPA210: DBV (5-Pin SOT-23, Preview) Package, Top View

Table 5-2. Pin Functions: OPA2210

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>NO.</td>
<td></td>
</tr>
<tr>
<td>–IN A</td>
<td>2</td>
<td>Inverting input, channel A</td>
</tr>
<tr>
<td>+IN A</td>
<td>3</td>
<td>Noninverting input, channel A</td>
</tr>
<tr>
<td>–IN B</td>
<td>6</td>
<td>Inverting input, channel B</td>
</tr>
<tr>
<td>+IN B</td>
<td>5</td>
<td>Noninverting input, channel B</td>
</tr>
<tr>
<td>OUT A</td>
<td>1</td>
<td>Output, channel A</td>
</tr>
<tr>
<td>OUT B</td>
<td>7</td>
<td>Output, channel B</td>
</tr>
<tr>
<td>V–</td>
<td>4</td>
<td>Negative (lowest) power supply</td>
</tr>
<tr>
<td>V+</td>
<td>8</td>
<td>Positive (highest) power supply</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply voltage, (V_S = (V^+) - (V^-))</td>
<td>40</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Signal input pins(^{(2)})</td>
<td>((V^-) – 0.5)</td>
<td>((V^+) + 0.5)</td>
<td></td>
</tr>
<tr>
<td>Signal input pins</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signal input pins(^{(2)})</td>
<td>–10</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Output short circuit(^{(3)})</td>
<td>Continuous</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction, (T_J)</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, (T_{stg})</td>
<td>–65</td>
<td>150</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) For input voltages beyond the power-supply rails, voltage or current must be limited.

\(^{(3)}\) Short circuit to ground, one amplifier per package.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{(ESD)})</th>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±4000</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>±1500</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specified voltage, (V_S)</td>
<td>±2.25</td>
<td>±18</td>
<td>V</td>
</tr>
<tr>
<td>Specified temperature</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Operating temperature, (T_A)</td>
<td>–55</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>
### 6.4 Thermal Information: OPA210

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>OPA210 D (SOIC)</th>
<th>OPA210 DGK (VSSOP)</th>
<th>OPA210 DBV (SOT-23)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JA}$</td>
<td>131.2</td>
<td>171.3</td>
<td>180.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JC\text{top}}$</td>
<td>71.6</td>
<td>64.7</td>
<td>67.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JB}$</td>
<td>74.6</td>
<td>92.4</td>
<td>102.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$</td>
<td>22.4</td>
<td>10.4</td>
<td>10.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JB}$</td>
<td>73.8</td>
<td>90.9</td>
<td>100.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JC\text{bottom}}$</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

### 6.5 Thermal Information: OPA2210

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>OPA2210 D (SOIC)</th>
<th>OPA2210 DGK (VSSOP)</th>
<th>OPA2210 DRG (SON)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JA}$</td>
<td>126.1</td>
<td>132.7</td>
<td>52.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JC\text{top}}$</td>
<td>65.7</td>
<td>38.5</td>
<td>51.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JB}$</td>
<td>69.5</td>
<td>52.1</td>
<td>24.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$</td>
<td>17.4</td>
<td>2.4</td>
<td>1.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JB}$</td>
<td>68.9</td>
<td>52.8</td>
<td>24.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JC\text{bottom}}$</td>
<td>n/a</td>
<td>n/a</td>
<td>9.0</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
6.6 Electrical Characteristics

at \(V_S = \pm 15\) V, \(T_A = 25\)°C, \(R_L = 10\) kΩ connected to midsupply, and \(V_{CM} = V_{OUT} = \text{midsupply}\) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFFSET VOLTAGE</td>
<td>(V_{OS})</td>
<td>(V_S = \pm 15) V, (V_{CM} = 0) V</td>
<td>(\pm 5)</td>
<td>(\pm 35)</td>
<td>µV</td>
</tr>
<tr>
<td></td>
<td>(dV_{OS}/dT)</td>
<td>(T_A = -40)°C to 125°C</td>
<td>(\pm 0.1)</td>
<td>(\pm 0.5)</td>
<td>µV/°C</td>
</tr>
<tr>
<td></td>
<td>(V_{OS}) - matching</td>
<td></td>
<td>(\pm 2)</td>
<td>(\pm 2)</td>
<td>nA</td>
</tr>
<tr>
<td>PSRR vs power supply</td>
<td></td>
<td>(V_S = \pm 2.25) V to ±18 V</td>
<td>(T_A = 25)°C</td>
<td>(0.05)</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td>Channel separation</td>
<td>DC</td>
<td></td>
<td>(\pm 0.1)</td>
<td>µV/V</td>
</tr>
</tbody>
</table>

INPUT BIAS OPERATION

| \(I_B\) | \(V_{CM} = 0\) V | \(T_A = 25\)°C | \(T_A = -40\)°C to 85°C | \(T_A = -40\)°C to 125°C | \(\pm 4\) | nA |
| \(I_{OS}\) | \(V_{CM} = 0\) V | \(T_A = 25\)°C | \(T_A = -40\)°C to 85°C | \(T_A = -40\)°C to 125°C | \(\pm 1\) | µA |

NOISE

| \(e_{n-p-p}\) | f = 0.1 Hz to 10 Hz | 0.09 | µVpp |
| \(e_n\) | f = 10 Hz | 2.5 | nV/√Hz |
| | f = 100 Hz | 2.25 | nV/√Hz |
| | f = 1 kHz | 2.2 | nV/√Hz |
| \(I_n\) | f = 1 kHz | 400 | fA/√Hz |

INPUT VOLTAGE RANGE

| \(V_{CM}\) | Common-mode voltage range | \((V-) + 1.5\) | \((V+) - 1.5\) | V |
| CMRR | Common-mode rejection ratio | \((V-) + 1.5\) V < \(V_{CM} < (V+) - 1.5\) V | 132 | 140 |
| | \((V-) + 1.5\) V < \(V_{CM} < (V+) - 1.5\) V, \(T_A = -40\)°C to 125°C | 120 | 130 |

INPUT IMPEDANCE

| Differential | 400 || 9 | kΩ || pF |
| Common-mode | \(10^9\) || 0.5 | Ω || pF |

OPEN-LOOP GAIN

| \(A_{OL}\) | Open-loop voltage gain | \(T_A = 25\)°C | \(T_A = -40\)°C to 125°C | 126 | 132 |
| | \(V-) + 0.2\) V < \(V_O < (V+) - 0.2\) V, \(R_L = 10\) kΩ | 120 | 130 |
| | \(V-) + 0.6\) V < \(V_O < (V+) - 0.6\) V, \(R_L = 600\) Ω | 114 | 120 |
| | \(T_A = -40\)°C to 85°C | 110 |

FREQUENCY RESPONSE

| GBW | Gain bandwidth product | 18 | MHz |
| SR | Slew rate | 6.4 | V/µs |
| | Phase margin (Φm) | \(R_L = 10\) kΩ, \(C_L = 25\) pF | 80 | degrees |
| | \(I_s\) | \(G = -1\), 10-V step, \(C_L = 100\) pF | \(0.0015\)%, \(G = -1\), 10-V step, \(C_L = 100\) pF | 2.1 | µs |
| | | 0.0015% (16-bit), \(G = -1\), 10-V step, \(C_L = 100\) pF | | 2.6 | µs |
| | Overload recovery time | \(G = -10\) | | 0.5 | µs |
| | Total harmonic distortion + noise (THD+N) | \(G = +1\), \(f = 1\) kHz, \(V_O = 20\) Vpp, \(600\) Ω | | 0.000025 | % |
6.6 Electrical Characteristics (continued)

at $V_S = \pm 15$ V, $T_A = 25^\circ$C, $R_L = 10 \, \text{k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output</td>
<td>Voltage output swing</td>
<td>$R_L = 10 , \text{k}\Omega, A_{DL} &gt; 130 , \text{dB}$</td>
<td>$(V–) + 0.2$</td>
<td>$(V+) – 0.2$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 600 , \Omega, A_{CL} &gt; 114 , \text{dB}$</td>
<td>$(V–) + 0.6$</td>
<td>$(V+) – 0.6$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 10 , \text{k}\Omega, A_{DL} &gt; 120 , \text{dB}, T_A = –40^\circ$ to $125^\circ$C</td>
<td>$(V–) + 0.2$</td>
<td>$(V+) – 0.2$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{SC}$</td>
<td>Short-circuit current</td>
<td>$V_S = \pm 18$ V</td>
<td>±65</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$C_{LOAD}$</td>
<td>Capacitive load drive (stable operation)</td>
<td></td>
<td>See Section 6.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Z_O$</td>
<td>Open-loop output impedance</td>
<td></td>
<td>See Section 6.7</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**POWER SUPPLY**

| $I_Q$ | Quiescent current (per amplifier) | $I_Q = 0$ A | $T_A = 25^\circ$C | 2.2 | 2.5 | mA |
|       |                                |               | $T_A = –40^\circ$ to $125^\circ$C | 3.25 | |

(1) Temperature range limited by thermal performance of the package.
6.7 Typical Characteristics

at $T_A = 25^\circ C$, $V_S = \pm 15 \, V$, $R_L = 10 \, k\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = $ midsupply (unless otherwise noted)
6.7 Typical Characteristics (continued)

at $T_A = 25^\circ C$, $V_S = \pm 15$ V, $R_L = 10$ k$\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} =$ midsupply (unless otherwise noted)

$\begin{array}{l}
\text{Total Harmonic Distortion} + \text{Noise (dB)} \\
\text{G } 1 \\
\text{G } 1 \\
\end{array}$

$f = 1$ kHz $\quad R_L = 600$ $\Omega$

$\begin{array}{l}
\text{Input Common-mode Voltage (V)} \\
\text{Input-referred Offset Voltage (PV)} \\
\text{V}_{cm} = -13.5$ V $\quad V_{cm} = 13.5$ V
\end{array}$

$\begin{array}{l}
\text{Supply Voltage (V)} \\
\text{Input-Referred Offset Voltage (PV)} \\
0 \quad 4 \quad 8 \quad 12 \quad 16 \quad 20 \quad 24 \quad 28 \quad 32 \quad 36
\end{array}$

$\begin{array}{l}
\text{Frequency (Hz)} \\
\text{Power-Supply Rejection Ratio (dB)} \\
0 \quad 20 \quad 40 \quad 60 \quad 80 \quad 100 \quad 120 \quad 140 \quad 160
\end{array}$

$\begin{array}{l}
\text{Temperature (qC)} \\
\text{Power Supply Rejection Ratio (PV/V)} \\
-50 \quad -25 \quad 0 \quad 25 \quad 50 \quad 75 \quad 100 \quad 125
\end{array}$

$\begin{array}{l}
\text{Figure 6-7. THD+N vs Output Amplitude} \\
\text{Figure 6-8. Input Offset Voltage vs Temperature} \\
\text{Figure 6-9. Offset Voltage vs Common-Mode Voltage} \\
\text{Figure 6-10. Offset Voltage vs Supply Voltage} \\
\text{Figure 6-11. PSSR vs Frequency} \\
\text{Figure 6-12. PSRR vs Temperature}
\end{array}$
6.7 Typical Characteristics (continued)

at $T_A = 25^\circ C$, $V_S = \pm 15\, \text{V}$, $R_L = 10\, \text{k\Omega}$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)
6.7 Typical Characteristics (continued)

at $T_A = 25^\circ C$, $V_S = \pm 15$ V, $R_L = 10$ k$\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} =$ midsupply (unless otherwise noted)
6.7 Typical Characteristics (continued)

at $T_A = 25^\circ C$, $V_S = \pm 15\ V$, $R_L = 10\ k\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = $ midsupply (unless otherwise noted)

---

**Figure 6-25. Quiescent Current vs Supply Voltage**

**Figure 6-26. Quiescent Current vs Temperature**

**Figure 6-27. Output Voltage vs Output Current (Sourcing)**

**Figure 6-28. Output Voltage vs Output Current (Sinking)**

**Figure 6-29. Short-Circuit Current vs Temperature**

**Figure 6-30. No Phase Reversal**
6.7 Typical Characteristics (continued)

at $T_A = 25^\circ C$, $V_S = \pm 15 \, V$, $R_L = 10 \, k\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)

---

**Figure 6-31. Positive Overload Recovery**

![Diagram](image1.png)

$G = -10$

**Figure 6-32. Negative Overload Recovery**

![Diagram](image2.png)

$G = -10$

---

**Figure 6-33. Small-Signal Step Response**

![Diagram](image3.png)

$G = +1$, 10-mV step, $C_L = 100 \, \text{pF}$, $R_L = 600 \, \Omega$

**Figure 6-34. Small-Signal Step Response**

![Diagram](image4.png)

$G = -1$, 10-mV step, $C_L = 100 \, \text{pF}$, $R_L = 600 \, \Omega$

---

**Figure 6-35. Large-Signal Step Response**

![Diagram](image5.png)

$G = +1$, 10-V step, $C_L = 100 \, \text{pF}$, $R_L = 600 \, \Omega$

**Figure 6-36. Large-Signal Step Response**

![Diagram](image6.png)

$G = -1$, 10-V step, $C_L = 100 \, \text{pF}$, $R_L = 600 \, \Omega$
6.7 Typical Characteristics (continued)

at \( T_A = 25^\circ C, V_S = \pm 15 \text{ V}, R_L = 10 \text{ k}\Omega \) connected to midsupply, and \( V_{CM} = V_{OUT} = \text{midsupply} \) (unless otherwise noted)

---

![Figure 6-37. Small-Signal Overshoot vs Capacitive Load](image1)

![Figure 6-38. Settling Time](image2)

![Figure 6-39. EMIRR vs Frequency](image3)

---

\[ P_{RF} = -10 \text{ dBm} \]
7 Detailed Description

7.1 Overview

The OPAx210 are the next generation of the OPAx209 operational amplifiers. The OPAx210 offer improved input offset voltage, offset voltage temperature drift, input bias current, and lower 1/f noise corner frequency. In addition, these devices offer excellent overall performance with high CMRR, PSRR, and $A_{OL}$. The OPAx210 precision operational amplifiers are unity-gain stable, and free from unexpected output and phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate. Section 7.2 shows a simplified schematic of the OPAx210. The die uses a SiGe bipolar process and contains 180 transistors.

7.2 Functional Block Diagram

![Functional Block Diagram](image)

7.3 Feature Description

7.3.1 Operating Voltage

The OPAx210 op amps can be used with single or dual supplies within an operating range of $V_S = 4.5$ V (±2.25 V) up to 36 V (±18 V).

**CAUTION**
Supply voltages greater than 40 V total can permanently damage the device.

In addition, key parameters are specified over the temperature range of $T_A = -40°C$ to +125°C. Parameters that vary significantly with operating voltage or temperature are shown in Section 6.7.

7.3.2 Input Protection

The input pins of the OPAx210 are protected from excessive differential voltage with back-to-back diodes, as shown in Figure 7-1. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or $G = 1$ circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in Figure 6-35 and Figure 6-36 in Section 6.7. If the input signal is fast enough to create this forward-bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPAx210. See Section 7.3.3 for further information on noise performance.
Figure 7-1 shows an example configuration that implements a current-limiting feedback resistor.

![Figure 7-1. Pulsed Operation](image)

7.3.3 Noise Performance

Figure 7-2 shows the total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore, no additional noise contributions). Two different op amps are shown with the total circuit noise calculated. The OPAx210 have very low voltage noise, making these devices a great choice for low source impedances (less than 2 kΩ). As a comparable, precision FET-input op amp (very low current noise), the OPA827 has somewhat higher voltage noise, but lower current noise. The device provides excellent noise performance at moderate to high source impedance (10 kΩ and up). For source impedance lower than 300 Ω, the OPA211 may provide lower noise.

The equation in Figure 7-2 shows the calculation of the total circuit noise, with these parameters:
- $e_n =$ voltage noise,
- $i_n =$ current noise,
- $R_S =$ source impedance,
- $k =$ Boltzmann’s constant = $1.38 \times 10^{-23}$ J/K, and
- $T =$ temperature in kelvins

For more details on calculating noise, see Section 8.1.1.

![Figure 7-2. Noise Performance of the OPAx210 and OPA827 in Unity-Gain Buffer Configuration](image)

7.3.4 Phase-Reversal Protection

The OPAx210 have internal phase-reversal protection. Many FET- and bipolar-input op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPAx210 prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see Figure 6-30).
7.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. See Figure 7-3 for an illustration of the ESD circuits contained in the OPAx210 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is greater than the normal operating voltage of the OPAx210 but less than the device breakdown voltage level. After this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as the one Figure 7-3 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 7-3 depicts a specific example where the input voltage, \( V_{\text{IN}} \), exceeds the positive supply voltage, \( +V_{\text{S}} \), by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If \( +V_{\text{S}} \) can sink the current, one of the upper input steering diodes conducts and directs current to \( +V_{\text{S}} \). Excessively high current levels can flow with increasingly higher \( V_{\text{IN}} \). As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, \( V_{\text{IN}} \) may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while power supplies \( +V_{\text{S}}, -V_{\text{S}} \), or both are at 0 V.

Again, the answer depends on the supply characteristic while at 0 V, or at a level less than the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source through the current steering diodes. This state is not a normal bias condition; the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external transient voltage suppressor (TVS) diodes may be added to the supply pins as shown in Figure 7-3. The breakdown voltage must be selected so that the diode does not turn on during normal operation. However, the breakdown voltage must be low enough so that the TVS diode conducts if the supply pin begins to rise to greater than the safe operating supply voltage level.
7.4 Device Functional Modes

The OPAx210 are operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power-supply voltage for the OPAx210 is 36 V (±18 V).

(1) $V_{IN} = +V_S + 500 \text{ mV}$.
(2) TVS: $+V_{S(max)} > V_{TVSBR (Min)} > +V_S$.
(3) Suggested value approximately 1 kΩ.

Figure 7-3. Equivalent Internal ESD Circuitry and Relation to a Typical Circuit Application
8 Application and Implementation

8.1 Application Information

The OPAx210 are unity-gain stable, precision operational amplifiers with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.1.1 Basic Noise Calculations

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 7-2. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 8-1 illustrates both noninverting (A) and inverting (B) op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPAx210 means that the device current noise contribution can be neglected.

Generally, the feedback resistor values are chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

(A) Noise in Noninverting Gain Configuration

Figure 8-1: Noise Calculation in Gain Configurations

(B) Noise in Inverting Gain Configuration

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Where $e_N$ is the voltage noise of the amplifier. For the OPAx210 op amp, $e_N = 2.2 \text{nV}/\sqrt{\text{Hz}}$ at 1 kHz.

Where $i_N$ is the current noise of the amplifier. For the OPAx210 op amp, $i_N = 400 \text{fA}/\sqrt{\text{Hz}}$ at 1 kHz.

NOTE: For additional resources on noise calculations visit the TI Precision Labs Series.
8.2 Typical Application

8.2.1 Design Requirements

Low-pass filters are commonly used in signal processing applications to reduce noise and prevent aliasing. The OPAx210 are designed to construct high-speed, high-precision active filters. Figure 8-2 shows a second-order, low-pass filter commonly encountered in signal-processing applications.

Use the following parameters for this design example:
- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the pass band

8.2.2 Detailed Design Procedure

The infinite-gain, multiple-feedback circuit for a low-pass network function is shown in Figure 8-2. Use Equation 1 to calculate the voltage transfer function.

\[
\frac{Output(s)}{Input(s)} = \frac{-1/R_4 R_3 C_2 C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3 R_4 C_2 C_5}
\]  

(1)

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by Equation 2:

\[
Gain = \frac{R_4}{R_1}
\]

\[
f_c = \frac{1}{2\pi} \sqrt{\frac{1}{R_3 R_4 C_2 C_5}}
\]  

(2)

8.2.3 Application Curve

Figure 8-3. OPAx210 Second-Order, 25-kHz, Chebyshev, Low-Pass Filter
8.3 System Example

8.3.1 Time Gain Control System for Ultrasound Applications

During an ultrasound send-receive cycle, the magnitude of reflected signal depends on the depth of penetration. The ultrasound signal incident on the receiver decreases in amplitude as a function of the time elapsed since transmission. The time gain control (TGC) system helps achieve the best possible signal-to-noise ratio (SNR), even with the decreasing signal amplitude. When the image is displayed, similar materials have similar brightness, regardless of depth. Linear-in-db gain, which means the decibel gain is a linear function of the control voltage \( V_{CNTL} \), is used to generate this image.

There are multiple approaches for a TGC control circuit that are based on the type of DAC. Figure 8-4 shows a high-level block diagram for the topology using a current-output multiplying DAC (MDAC) to generate the drive for \( V_{CNTL} \). The op amp used for current-to-voltage (I-to-V) conversion must have low-voltage noise, as well as low-current noise density. The current density helps reduce the overall noise performance because of the DAC output configuration. The DAC output can go up to ±10 V; therefore, the op amp must have bipolar operation. The OPAx210 is used here because of the low-voltage noise density of 2.2 nV/√Hz, low-current noise density of 500 fA/√Hz, rail-to-rail output, and the ability to accept a wide supply range of ±2.25 V to ±18 V and provide rail-to-rail output. The low offset voltage and offset drift of the OPAx210 facilitate excellent dc accuracy for the circuit.

The OPAx210 is used to filter and buffer the 10-V reference voltage generated by the REF5010. The REF5010 serves as the reference voltage for the DAC8802, which generates a current output on \( I_{OUT} \) corresponding to the digital input code. The \( I_{OUT} \) pin of the DAC8802 is connected to the virtual ground (negative terminal) of the OPAx210; the feedback resistor \( R_{FB} \) is internal to the DAC8802) is connected to the output of the OPAx210, and results in a current-to-voltage conversion. The output of the OPAx210 has a range of −10 V to 0 V, which is fed to the THS4130 configured as a Sallen-Key filter. Finally, the 10-V range is attenuated down to a 1.5-V range, with a common-mode voltage of 0.75 V using a resistive attenuator. See the 2.3-nV/√Hz, Differential, Time Gain Control DAC Reference Design for Ultrasound for an in-depth analysis of Figure 8-4.
Figure 8-4. Block Diagram for Time Gain Control System for Ultrasound
9 Power Supply Recommendations

The OPAx210 are specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in Section 6.7.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including the following guidelines:

- Noise from the amplifier can propagate into other analog circuits through the power pins of the amplifiers. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than running in parallel with the noisy trace.
- Place the external components as close as possible to the device.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, clean the PCB following board assembly.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

Figure 10-1. OPA2210 Layout Example
11 Device and Documentation Support
11.1 Device Support
11.1.1 Development Support

11.1.1.1 TINA-TI™ Simulation Software (Free Download)
TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ simulation software is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note
These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI software folder.

11.1.1.2 DIP Adapter EVM
The DIP Adapter EVM tool provides an easy, low-cost way to prototype small, surface-mount integrated circuits (ICs). The EVM includes footprint options for the following TI packages:

- D or U (SOIC-8)
- PW (TSSOP-8)
- DGK (VSSOP-8)
- DBV (SOT23-6, SOT23-5 and SOT23-3)
- DCK (SC70-6 and SC70-5)
- DRL (SOT563-6)

The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

11.1.1.3 Universal Operational Amplifier EVM
The Universal Op Amp evaluation module (EVM) is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The EVM board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. The PDIP, SOIC, VSSOP, TSSOP, and SOT-23 packages are all supported.

Note
These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

11.1.1.4 TI Precision Designs
TI Precision Designs are analog solutions created by TI's precision analog applications experts. These designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.1.1.5 WEBENCH® Filter Designer
The WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, the WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.
11.2 Documentation Support

11.2.1 Related Documentation

The following documents are relevant to using the OPAx210 and recommended for reference. All are available for download at www.ti.com (unless otherwise noted):

- Texas Instruments, OPA827 Low-Noise, High-Precision, JFET-Input Operational Amplifier data sheet
- Texas Instruments, OPA2x11 1.1-nV/√Hz Noise, Low-Power, Precision Operational Amplifier data sheet
- Texas Instruments, OPA210, OPA2210, OPA4210 EMI Immunity Performance technical brief
- Texas Instruments, OPAx209 2.2-nV/√Hz, Low-Power, 36-V Operational Amplifier data sheet
- Texas Instruments, Microcontroller PWM to 12-Bit Analog Out design guide
- Texas Instruments, Capacitive Load Drive Solution Using an Isolation Resistor design guide
- Texas Instruments, Noise Measurement Post Amp design guide

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Subscribe to updates to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## Packaging Information

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<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>O2210</td>
<td>Samples</td>
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<td>DRG</td>
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<td>-40 to 125</td>
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<td>-40 to 125</td>
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</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <= 1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.**: The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
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<td>12.0</td>
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</tbody>
</table>

*All dimensions are nominal.*

#### PACKAGE MATERIALS INFORMATION

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**TAPE AND REEL INFORMATION**

**TAPE DIMENSIONS**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**REEL DIMENSIONS**

- **Reel Diameter**
- **Reel Width (W1)**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- **Q1\_Q2**
- **Q3\_Q4**

---

*All dimensions are nominal.*
<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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*All dimensions are nominal*
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-157 variation AA, except interlead flash.
NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No-Lead) package configuration.
⚠ The package thermal pad must be soldered to the board for thermal and mechanical performance.
See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO-229 package registration pending.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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