

OPA2205 25- μ V, 0.3- μ V/ $^{\circ}$ C, Low-Power, Super Beta, Bipolar, e-trim™ Op Amp

1 Features

- e-trim operational amplifier performance
 - Low offset voltage: 25 μ V (max)
 - Low offset voltage drift: \pm 0.3 μ V/ $^{\circ}$ C (max)
- Super beta inputs
 - Input bias current: 0.75 nA (max)
 - Input current noise: 200 fA/ $\sqrt{\text{Hz}}$
- Low noise
 - 0.1 to 10-Hz: 0.15 μ V_{PP}
 - Voltage noise: 7.2 nV/ $\sqrt{\text{Hz}}$
- A_{OL}, CMRR, and PSRR: > 120 dB (full temperature range)
- Gain bandwidth product: 3.6 MHz
- Low quiescent current: 250 μ A (max)
- Slew rate: 4 V/ μ s
- Overload power limiter
- Rail-to-rail output
- EMI/RFI filtered inputs
- Wide supply: 4.5 V to 36 V
- Temperature range: -40° C to $+125^{\circ}$ C

2 Applications

- [Flow transmitter](#)
- [String inverter](#)
- [Data acquisition \(DAQ\)](#)
- [Source measurement unit \(SMU\)](#)
- [Lab and field instrumentation](#)
- [Battery test](#)
- [Analog input module](#)

3 Description

The OPA2205 is the next generation, precision, bipolar, e-trim™ operational amplifier featuring super beta inputs, and is an upgrade to the industry-standard OPA2277. Through the combination of a bipolar amplifier core and a digital trim, the OPA2205 achieves very low offset (\pm 25 μ V, max), offset drift (\pm 0.3 μ V/ $^{\circ}$ C, max) and noise (7.2 nV/ $\sqrt{\text{Hz}}$, typ).

The high dc and ac performance of the amplifier, along with a 3.6-MHz bandwidth and low-power consumption (250 μ A, max), make the OPA2205 an excellent choice for systems that require high precision and low power consumption, such as high-density data-acquisition systems (DAQ), source measurement units (SMU), and string inverters. The integrated EMI/RFI filter reduces system errors by eliminating unwanted RF-injected signals from neighboring circuits and other electronic systems.

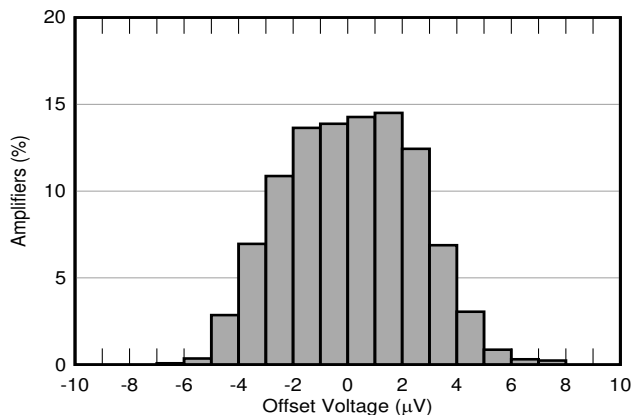
The OPA2205 amplifier is available in a standard-pinout, VSSOP package, and operates across the extended industrial ambient temperature range of -40° C to $+125^{\circ}$ C.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA2205	VSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

OPA2205 Offset Voltage



OPA2205 Offset Voltage Drift

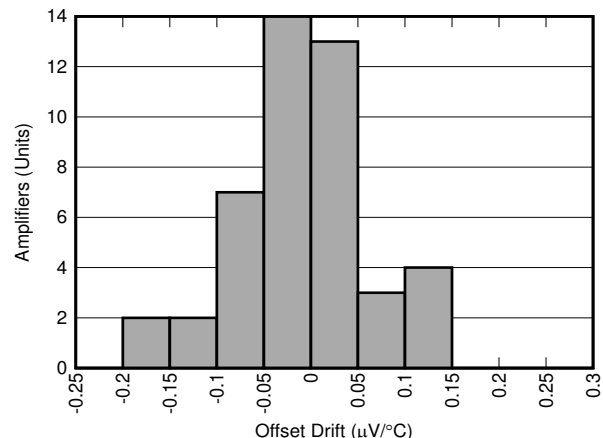


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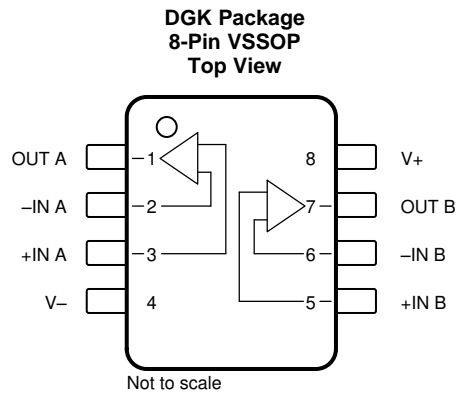
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4 Revision History

DATE	REVISION	NOTES
April 2020	*	Initial release.

ADVANCE INFORMATION

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
-IN A	2	I	Inverting input, channel A
+IN B	5	I	Noninverting input, channel B
-IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V-	4	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _S	Supply voltage, V _S = (V+) – (V–)	Single supply	40	V
		Dual supply	±20	
	Signal input pin voltage	Common-mode	(V–) – 0.5 (V+) + 0.5	V
		Differential	±0.5	
	Signal input pin current		±10	mA
	Output short-circuit ⁽²⁾	Continuous		
T _A	Operating temperature	–40	150	°C
T _J	Junction temperature		150	°C
T _{STG}	Storage temperature	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _S	Supply voltage, V _S = (V+) – (V–)	4.5		36	V
		±2.25		±18	
T _A	Operating temperature	–40		125	°C

6.4 Thermal Information: OPA2205

THERMAL METRIC ⁽¹⁾		OPA2205	UNIT
		DGK (VSSOP)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	164.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	57.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	85.8	°C/W
ψ _{JT}	Junction-to-top characterization parameter	6.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	84.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Electrical Characteristics: $V_S = \pm 5\text{ V}$

at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OFFSET VOLTAGE							
V_{OS}	Input offset voltage			± 5	± 25	μV	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 12	± 55		
dV_{OS}/dT	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 0.1	± 0.3	$\mu\text{V}/^\circ\text{C}$	
PSRR	Input offset voltage versus power supply	$V_S = \pm 2.25\text{ V}$ to $\pm 18\text{ V}$		± 0.05	± 0.5	$\mu\text{V}/\text{V}$	
		$V_S = \pm 2.25\text{ V}$ to $\pm 18\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$					± 1
INPUT BIAS CURRENT							
I_B	Input bias current			± 0.2	± 0.75	nA	
		$T_A = 0^\circ\text{C}$ to 85°C					± 1
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$					± 1.2
I_{OS}	Input offset current			± 0.1	± 0.4	nA	
		$T_A = 0^\circ\text{C}$ to 85°C					± 0.8
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$					± 0.9
NOISE							
$e_{n,p-p}$	Input voltage noise	$f = 0.1\text{ Hz}$ to 10 Hz		0.15		μV_{PP}	
e_n	Input voltage noise density	$f = 10\text{ Hz}$		7.4		$\text{nV}/\sqrt{\text{Hz}}$	
		$f = 100\text{ Hz}$		7.2			
		$f = 1\text{ kHz}$		7.2			
i_n	Input current noise	$f = 1\text{ kHz}$		200		$\text{fA}/\sqrt{\text{Hz}}$	
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage		$(V-) + 1$		$(V+) - 1.4$	V	
CMRR	Common-mode rejection ratio	$(V-) + 1\text{ V} < V_{CM} < (V+) - 1.4\text{ V}$	126	140		dB	
		$(V-) + 1\text{ V} < V_{CM} < (V+) - 1.4\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	120	140			
INPUT IMPEDANCE							
Z_{ID}	Differential			$3 \parallel 4$		$\text{M}\Omega \parallel \text{pF}$	
Z_{ICM}	Common-mode			$100 \parallel 4$		$\text{G}\Omega \parallel \text{pF}$	
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	$(V-) + 200\text{ mV} < V_O < (V+) - 200\text{ mV}$, $R_L = 10\text{ k}\Omega$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	126	132	dB	
				120			
		$(V-) + 200\text{ mV} < V_O < (V+) - 200\text{ mV}$, $R_L = 2\text{ k}\Omega$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	125	130		
				120			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product			3.6		MHz	
SR	Slew rate	4-V step, $G = -1$		4		$\text{V}/\mu\text{s}$	
	Phase margin	$R_L = 10\text{ k}\Omega$, $C_L = 25\text{ pF}$		55		degrees	
t_S	Settling time	To 0.1%, 4-V step, $G = -1$, $C_L = 30\text{ pF}$		1.9		μs	
		To 0.0015% (16-bit), 4-V step, $G = -1$, $C_L = 30\text{ pF}$			3.1		
	Overload recovery time	$G = -10$		2.2		μs	
THD+N	Total harmonic distortion + noise	$V_O = 5\text{ V}_{PP}$, $G = +1$, $f = 1\text{ kHz}$, $R_L = 2\text{ k}\Omega$		0.0004		%	
OUTPUT							
	Voltage output swing from rail	$T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$, $A_{OL} > 126\text{ dB}$	$(V-) + 0.2$		$(V+) + 0.2$	V	
		$T_A = 25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$, $A_{OL} > 125\text{ dB}$	$(V-) + 0.2$		$(V+) + 0.2$		
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$	$(V-) + 0.2$		$(V+) + 0.2$		
I_{SC}	Short-circuit current			± 25		mA	
C_{LOAD}	Capacitive load drive			See Typical Characteristics			
R_O	Open-loop output impedance			See Typical Characteristics			
POWER SUPPLY							
I_Q	Quiescent current per amplifier	$I_O = 0\text{ mA}$		220	250	μA	
		$I_O = 0\text{ mA}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$					335

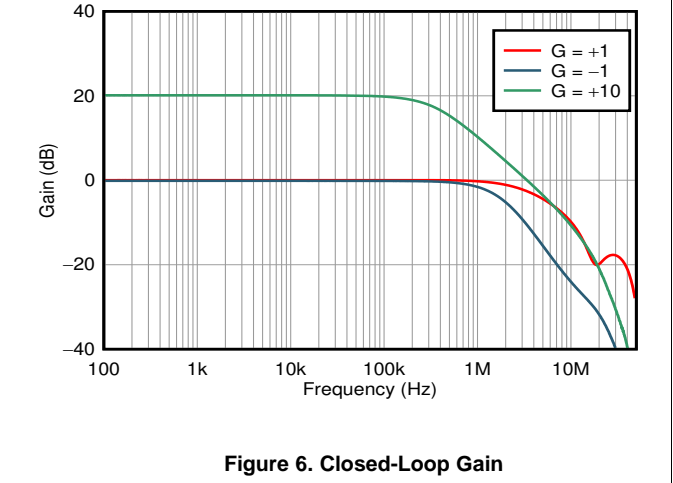
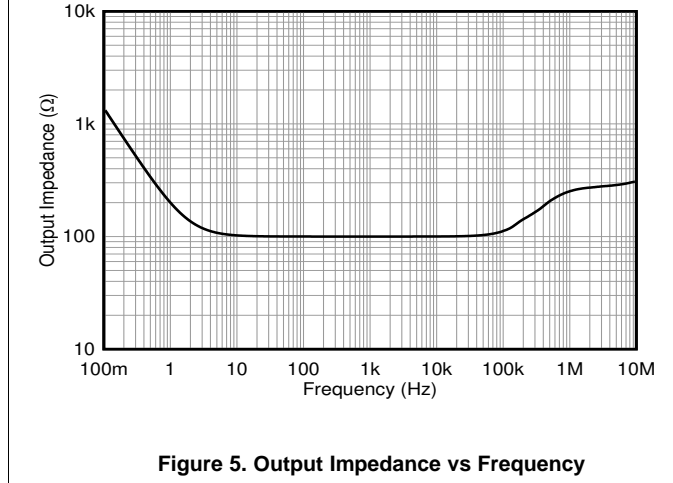
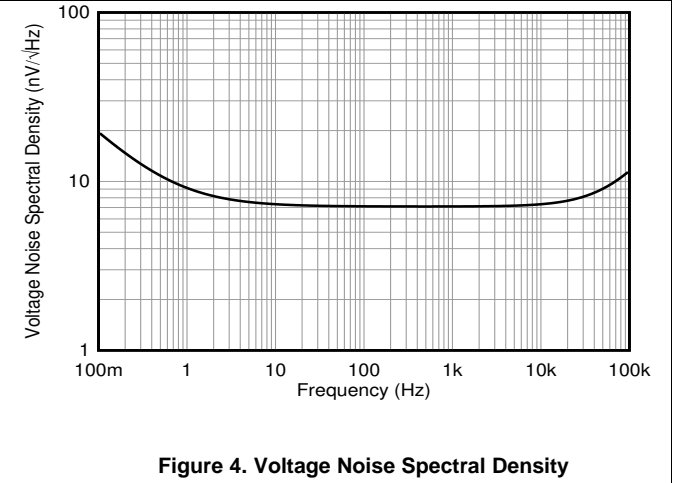
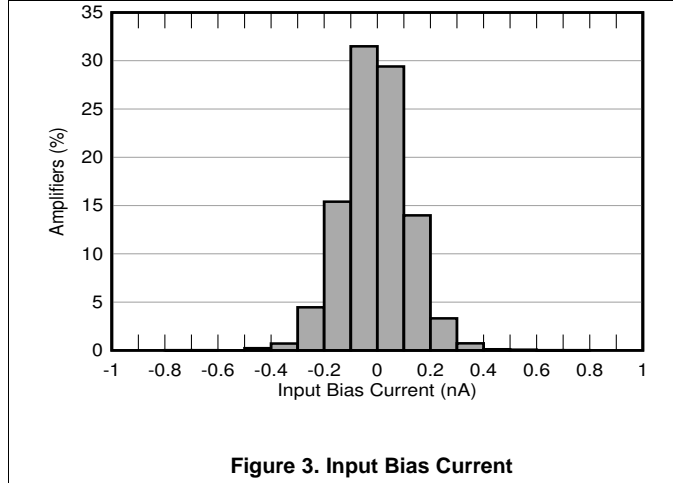
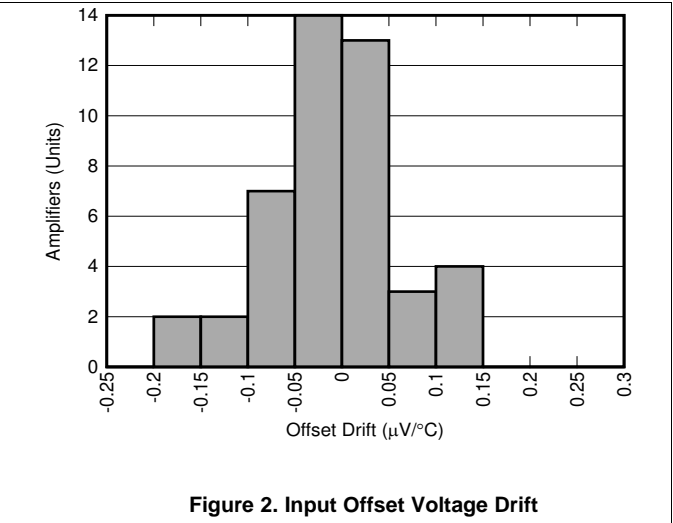
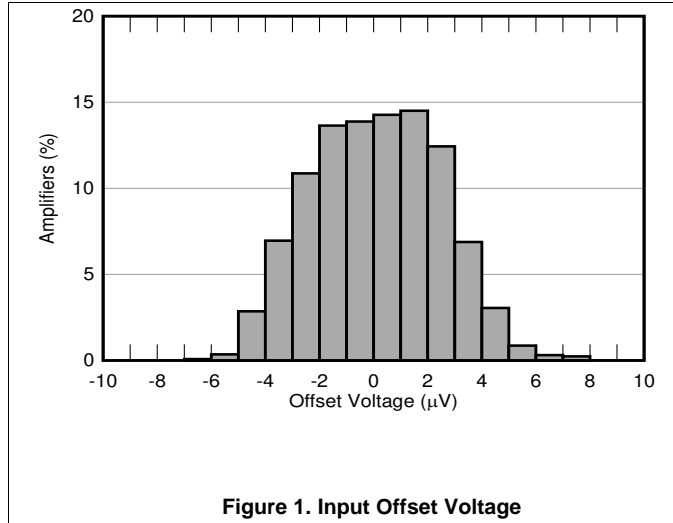
6.6 Electrical Characteristics: $V_S = \pm 15\text{ V}$

at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			± 5	± 25	μV
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 12	± 55	
dV_{OS}/dT	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 0.1	± 0.3	$\mu\text{V}/^\circ\text{C}$
PSRR	Input offset voltage versus power supply	$V_S = \pm 2.25\text{ V}$ to $\pm 18\text{ V}$		± 0.05	± 0.5	$\mu\text{V}/\text{V}$
		$V_S = \pm 2.25\text{ V}$ to $\pm 18\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			± 1	
INPUT BIAS CURRENT						
I_B	Input bias current			± 0.2	± 0.75	nA
		$T_A = 0^\circ\text{C}$ to 85°C			± 1	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			± 1.2	
I_{OS}	Input offset current			± 0.1	± 0.4	nA
		$T_A = 0^\circ\text{C}$ to 85°C			± 0.8	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			± 0.9	
NOISE						
$e_{n,p-p}$	Input voltage noise	$f = 0.1\text{ Hz}$ to 10 Hz		0.15		μV_{PP}
e_n	Input voltage noise density	$f = 10\text{ Hz}$		7.4		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 100\text{ Hz}$		7.2		
		$f = 1\text{ kHz}$		7.2		
i_n	Input current noise	$f = 1\text{ kHz}$		200		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage		$(V-) + 1$		$(V+) - 1.4$	V
CMRR	Common-mode rejection ratio	$(V-) + 1\text{ V} < V_{CM} < (V+) - 1.4\text{ V}$	126	140		dB
		$(V-) + 1\text{ V} < V_{CM} < (V+) - 1.4\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	120	140		
INPUT IMPEDANCE						
Z_{ID}	Differential			$3 \parallel 4$		$\text{M}\Omega \parallel \text{pF}$
Z_{ICM}	Common-mode			$100 \parallel 4$		$\text{G}\Omega \parallel \text{pF}$
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$(V-) + 200\text{ mV} < V_O < (V+) - 200\text{ mV}$, $R_L = 10\text{ k}\Omega$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	126	132	dB
				120		
		$(V-) + 350\text{ mV} < V_O < (V+) - 350\text{ mV}$, $R_L = 2\text{ k}\Omega$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	125	130	
				120		
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	$C_L = 30\text{ pF}$		3.6		MHz
SR	Slew rate	10-V step, $G = -1$		4		$\text{V}/\mu\text{s}$
	Phase margin	$R_L = 10\text{ k}\Omega$, $C_L = 25\text{ pF}$		58		degrees
t_S	Settling time	To 0.1%, 10-V step, $G = -1$, $C_L = 30\text{ pF}$		2.9		μs
		To 0.0015% (16-bit), 10-V step, $G = -1$, $C_L = 30\text{ pF}$		4.1		
	Overload recovery time	$G = -10$		2.2		μs
THD+N	Total harmonic distortion + noise	$V_O = 5\text{ V}_{PP}$, $G = +1$, $f = 1\text{ kHz}$, $R_L = 2\text{ k}\Omega$		0.0004		%
OUTPUT						
	Voltage output swing from rail	$T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$, $A_{OL} > 126\text{ dB}$	$(V-) + 0.2$		$(V+) + 0.2$	V
		$T_A = 25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$, $A_{OL} > 125\text{ dB}$	$(V-) + 0.35$		$(V+) + 0.35$	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$	$(V-) + 0.2$		$(V+) + 0.2$	
I_{SC}	Short-circuit current			± 25		mA
C_{LOAD}	Capacitive load drive			See Typical Characteristics		
R_O	Open-loop output impedance			See Typical Characteristics		
POWER SUPPLY						
I_Q	Quiescent current per amplifier	$I_O = 0\text{ mA}$		220	250	μA
		$I_O = 0\text{ mA}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			335	

6.7 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)



ADVANCE INFORMATION

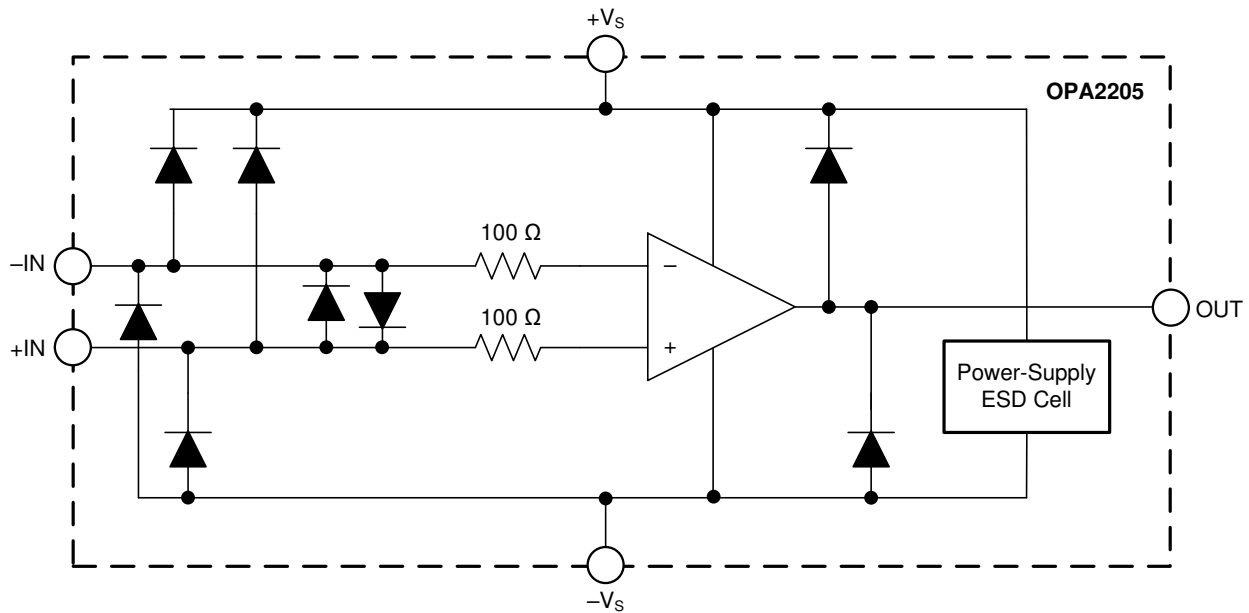
7 Detailed Description

7.1 Overview

The OPA2205 is the first 36-V bipolar, e-trim operational amplifier that uses a package-level offset trim to minimize the offset voltage and offset voltage drift introduced during the manufacturing process. This trim is performed after the device has been assembled to remove any offset errors introduced throughout the manufacturing process, and trim communication is disabled afterward. The device also features super beta inputs that decrease the input bias current and input current noise.

The [Functional Block Diagram](#) section shows the simplified diagram of the OPA2205.

7.2 Functional Block Diagram



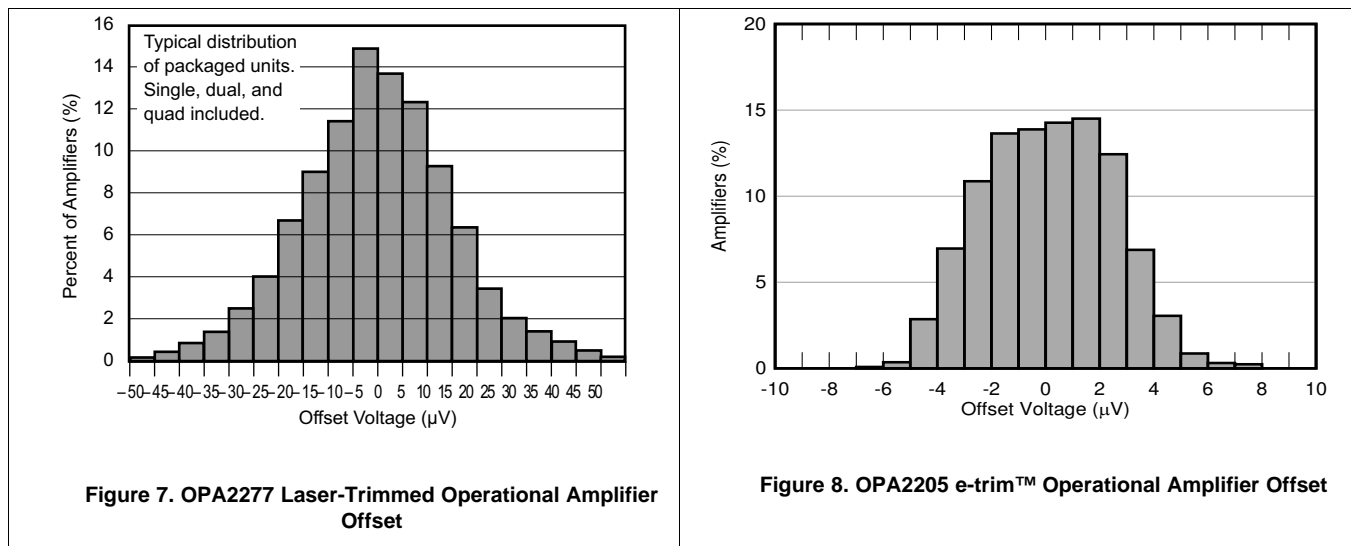
ADVANCE INFORMATION

7.3 Feature Description

7.3.1 Input Offset Digital Trimming

The OPA2205 is the industry's first e-trim operational amplifier built on a bipolar process. The input offset voltage of an amplifier is determined by the inherent mismatch between the inputs of the device. The offset can be minimized using laser-trimming performed during the manufacturing process while the device is still in the bare silicon form. However, when the silicon is packaged, the package process introduces additional offset. New digital trimming processes are used to trim the offset after the packaging process is complete to minimize both the inherent and package-induced offsets. The process takes place at the end of the manufacturing process when the final performance of the device is being tested. After trimming, communication is disabled to make sure the amplifier operates properly in the final system.

A comparison between production offset values for a laser-trimmed amplifier and the OPA2205 digital trim can be seen in [Figure 7](#) and [Figure 8](#).



The OPA2205 digital trim architecture is also used in a two-temperature trim to minimize the input offset voltage drift over temperature. The performance of the offset drift can be seen in [Figure 9](#).

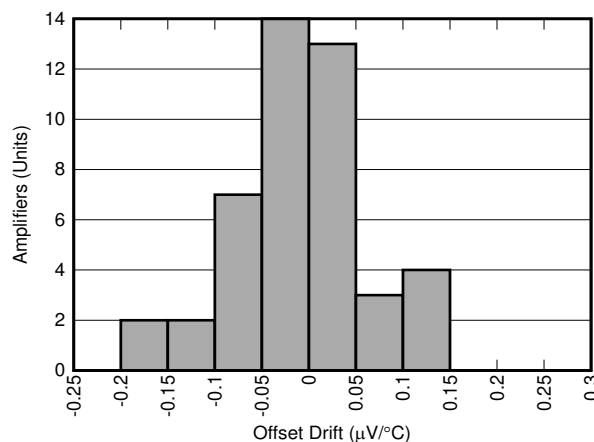
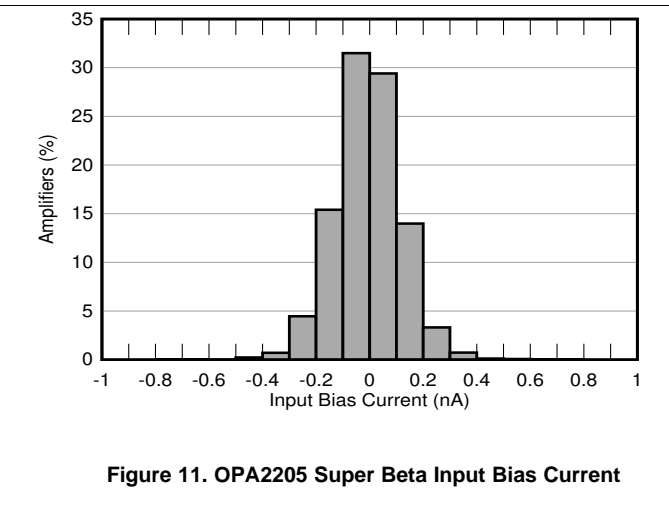
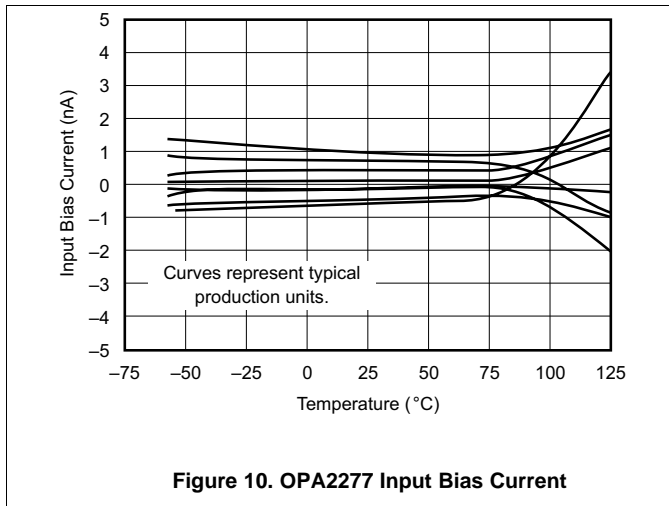


Figure 9. OPA2205 e-trim™ Operational Amplifier Drift

Feature Description (continued)

7.3.2 Lower Input Bias With Super Beta Inputs

The OPA2205 has a super beta input transistor architecture. In a transistor, the beta value is the ratio between the current flowing into the base and the current flowing from the collector to the emitter. A super-beta transistor is one where the beta value has been increased from several hundred to thousands. In a bipolar amplifier, the input bias current is the current flowing into the base of the input transistor pair, as well as a small leakage current that flows through the ESD diodes. A super beta input reduces the input bias current of the amplifier. In addition, the super beta inputs lower the input current noise that is directly related to the input bias current of the device. A comparison between the input bias current of a standard bipolar amplifier and the OPA2205 super beta input bias currents can be seen in [Figure 10](#) and [Figure 11](#).



7.3.3 Overload Power Limiter

In many bipolar-based amplifiers, the output stage of the amplifier can draw significant (several milliamperes) of quiescent current if the output voltage becomes clipped (meaning the output voltage becomes limited by the negative or positive supply voltage). This condition can cause the system to enter a high-power consumption state, and potentially cause oscillations between the power supply and signal chain. The OPA2205 has an advanced output stage design that eliminates this problem. When the output voltage reaches the either supply (V+ or V-), there is virtually no additional current consumption from the nominal quiescent current. This feature helps eliminate any potential system problems when the signal chain is disrupted by a large external transient voltage.

7.3.4 EMI Rejection

The OPA2205 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved through circuit design techniques that improve the system performance. Additional information can be found in the [EMI Rejection Ratio of Operation Amplifiers application report](#).

7.4 Device Functional Modes

The OPA2205 has a single functional mode and is operational with any supply between 4.5 V (± 2.25 V) and 36 V (± 18 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA2205 is a unity-gain stable operational amplifier with very low offset voltage, offset voltage drift, voltage noise, current noise and power consumption. These features make this device a great choice for a variety of space-constrained and power-constrained systems.

8.2 Typical Application

A common application for the OPA2205 is an input buffer for the signal chain of a data acquisition (DAQ) or field instrumentation system. This amplifier is selected because of the low offset and drift, which maintain system accuracy across a variety of operating conditions. The low power consumption of the OPA2205 enables the device to be used in battery-operated or high-density applications, where thermal dissipation is difficult. The low 1/f (flicker) noise and broadband noise allow for higher-accuracy signal chains, such as those using a 24-bit delta-sigma analog-to-digital converter (ADC). If a higher sampling rate is needed, the OPA2205 can be paired with a fully differential amplifier, such as the THP210, to drive the ADC inputs.

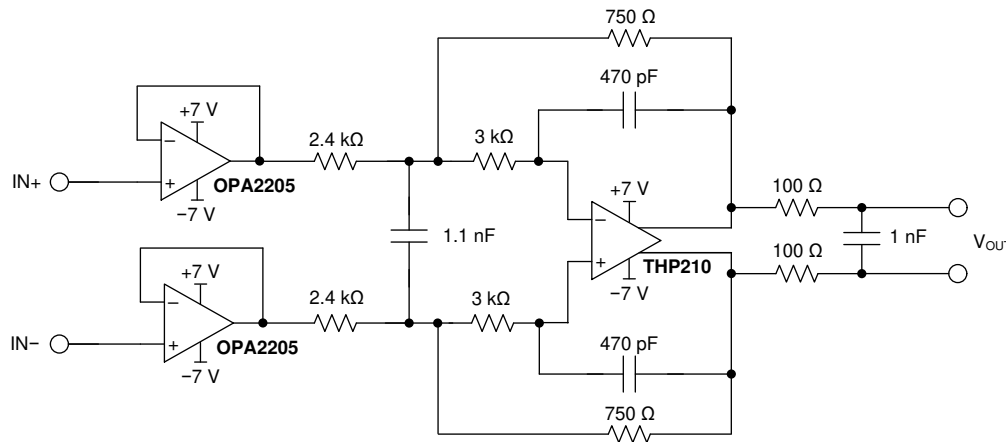


Figure 12. OPA2205 Configured as a DAQ Input Buffer

Typical Application (continued)

8.2.1 Design Requirements

The design requirements for this application are:

- Input range: ± 10 V
- Input frequency: 10 kHz
- Output voltage: ± 3.3 V
- Quiescent current: < 1.5 mA

8.2.2 Detailed Design Procedure

In this application, the input signal ranges from -10 V to $+10$ V and a frequency up to 10 kHz. Because of possible portable-use cases for this data acquisition system (DAQ), low power consumption is required to minimize battery drain and thermal dissipation requirements.

To maintain high system accuracy the OPA2205 is selected as input buffers. This device was selected due to its high DC precision (5 μ V offset and 0.1 μ V/ $^{\circ}$ C offset drift), low flicker noise (0.15 μ Vpp) and low quiescent current (220 μ A). The buffers are followed by a high-precision, fully differential amplifier such as the THP210 which is capable of accurately driving a 24-bit, fully differential analog-to-digital converter such as the ADS127L01.

8.2.3 Application Curves

The gain plot for this system can be seen in [Figure 13](#). This plot shows proper attenuation of the ± 10 -V signal to the target ± 3.3 -V output, and adequate bandwidth to support the input frequency range.

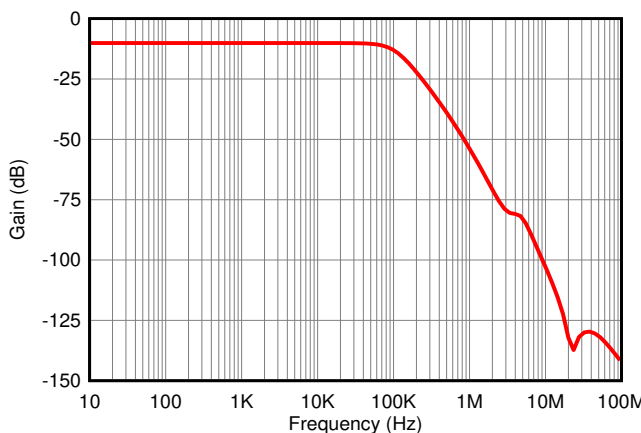


Figure 13. Gain Plot of DAQ Front End

9 Power Supply Recommendations

The OPA2205 operates with a power supply between 4.5 V to 36 V (± 2.25 V to ± 18 V). Parameters that can exhibit significant variance with regard to operating voltage are presented in the [Typical Characteristics](#).

Place 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout Guidelines](#) section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications. Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as through the individual op amp. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in [Figure 14](#), keep RF and RG close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. After any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

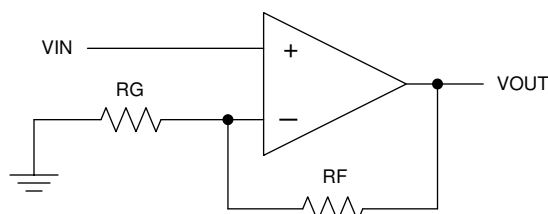


Figure 14. Schematic Representation

Layout Example (continued)

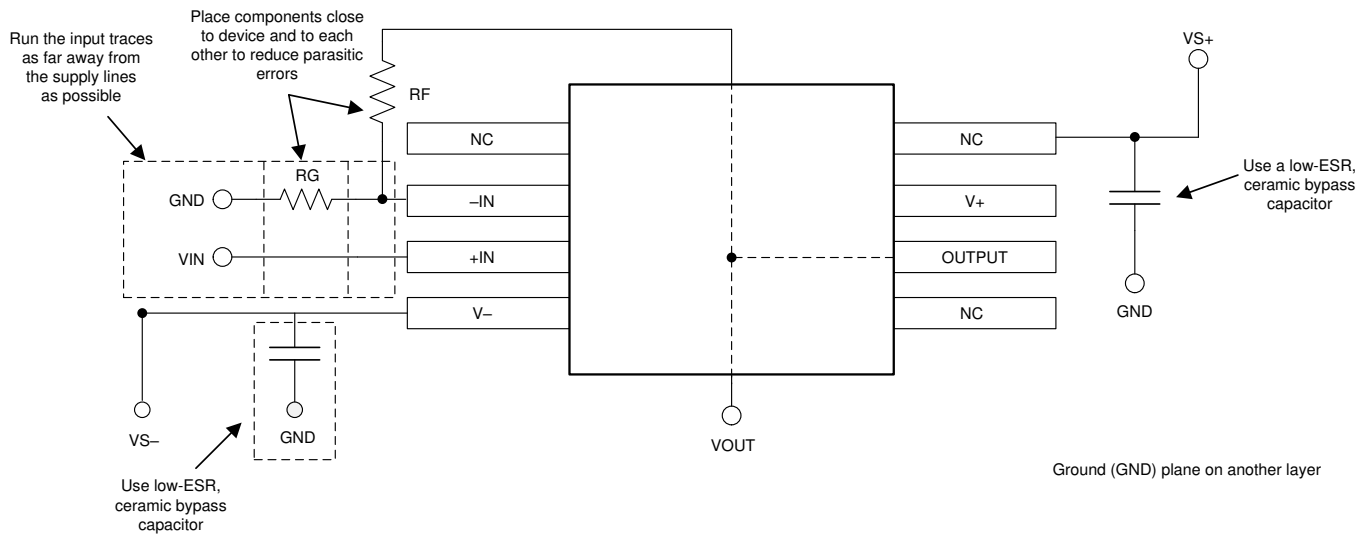


Figure 15. Operational Amplifier Board Layout for Noninverting Configuration

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.3 Trademarks

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11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2205DGKR	PREVIEW	VSSOP	DGK	8	2500	RoHS (In work & Non-Green)	Call TI	Call TI	-40 to 125		
XOPA2205DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS (In work & Non-Green)	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

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