OPA2206 ±40-V, Input-Overvoltage Protected, 25-µV, 0.3-µV/°C, Low-Power, Super Beta, e-trim™ Op Amp

1 Features

- Integrated input overvoltage protection up to ±40 V beyond supplies
- e-trim operational amplifier performance
  - Low offset voltage: 25 µV (max)
  - Low offset voltage drift: ±0.3 µV/°C (max)
- Super beta inputs
  - Input bias current: 0.75 nA (max)
  - Input current noise: 200 fA/√Hz
- Low noise
  - 0.1-Hz to 10-Hz: 0.15 μV_{PP}
  - Voltage noise: 8 nV/√Hz
- A_{OL}, CMRR, and PSRR: > 120 dB (full temperature range)
- Gain bandwidth product: 3.6 MHz
- Low quiescent current: 250 µA (max)
- Slew rate: 4 V/µs
- Overload power limiter
- Rail-to-rail output
- EMI/RFI filtered inputs
- Wide supply: 4.5 V to 36 V
- Temperature range: –40°C to +125°C

2 Applications

- Analog input module
- Mixed module (AI,AO,DI,DO)
- Lab and field Instrumentation
- Source measurement unit (SMU)
- Digital multimeter (DMM)
- Train control and management
- String inverter
- Data acquisition (DAQ)

3 Description

The OPA2206 is the next-generation precision bipolar, e-trim operational amplifier featuring super beta inputs and integrated input overvoltage protection. Through the combination of a bipolar amplifier core and a digital trim, the OPA2206 achieves very low offset (±25 µV, max), offset drift (±0.3 µV/°C, max) and noise (8 nV/√Hz, typ). The input overvoltage protection activates when the input signal exceeds the supply range of the amplifier, and can protect against voltages up to 40 V beyond either supply without degrading system performance during normal operation.

The high dc and ac performance of the amplifier, in combination with a 3.6-MHz bandwidth and low power consumption (250 µA, max), make the OPA2206 an excellent choice for systems requiring high precision and low power consumption, such as high-density analog input modules in programmable logic controllers, instrumentation systems, and source measurement units. The integrated EMI/RFI filter reduces system errors by eliminating unwanted RF-injected signals from neighboring circuits and other electronic systems.

The OPA2206 amplifier is available in standard-pinout, VSSOP package, and operates across the industrial ambient temperature range of –40°C to +125°C.

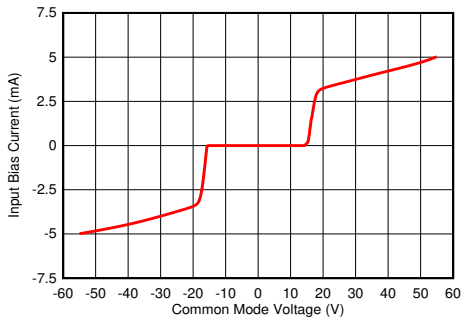
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA2206	VSSOP (8)	3.00 mm × 3.00 mm

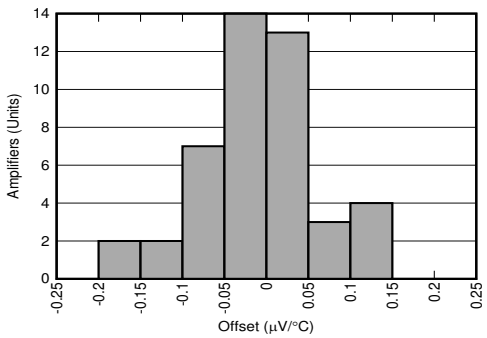
(1) For all available packages, see the package option addendum at the end of the data sheet.

ADVANCE INFORMATION

OPA2206 Input Overvoltage Protection



OPA2206 Input Offset Drift



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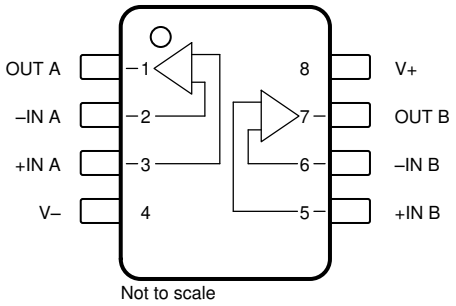
4 Revision History

DATE	REVISION	NOTES
April 2020	*	Initial release.

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
–IN A	2	I	Inverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, Vs = (V+) – (V–)	Single supply		40	V
		Dual supply		±20	
	Signal input pin voltage		(V–) – 40	(V+) + 40	V
	Output short-circuit(2)		Continuous		
T_A	Operating temperature		–40	150	°C
T_J	Junction temperature			150	°C
T_{STG}	Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	4.5		36	V
		±2.25		±18	
T_A	Operating temperature	–40		125	°C

6.4 Thermal Information: OPA2206

THERMAL METRIC(1)		OPA2206 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	164.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	84.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

ADVANCE INFORMATION

6.5 Electrical Characteristics: V_S = ±5 V

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±5	±25	µV
		T_A = –40°C to +125°C			±12	±55	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±0.1	±0.3	µV/°C
PSRR	Input offset voltage versus power supply	V_S = ±2.25 V to ±18 V			±0.05	±0.5	µV/V
		V_S = ±2.25 V to ±18 V, T_A = –40°C to +125°C				±1	
INPUT BIAS CURRENT							
I_B	Input bias current				±0.2	±0.75	nA
		T_A = 0°C to 85°C				±1	
		T_A = –40°C to +125°C				±1.2	
I_{OS}	Input offset current				±0.1	±0.4	nA
		T_A = 0°C to 85°C				±0.8	
		T_A = –40°C to +125°C				±0.9	
NOISE							
$e_{n\ p\text{-}p}$	Input voltage noise	f = 0.1 Hz to 10 Hz			0.15		μV_{PP}
e_n	Input voltage noise density	f = 10 Hz			8.4		$nV/\sqrt{Hz}$
		f = 100 Hz			8		
		f = 1 kHz			8		
i_n	Input current noise	f = 1 kHz			200		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage			(V–) + 1		(V+) – 1.4	V
CMRR	Common-mode rejection ratio	(V–) + 1 V < V_{CM} < (V+) – 1.4 V		126	140		dB
		(V–) + 1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to +125°C		120	140		
INPUT OVERVOLTAGE RANGE							
	Input overvoltage protection	T_A = –40℃ to +125℃		(V–) – 40		(V+) + 40	V
	Input current in overvoltage protected mode	V_{CM} = ±45 V			5		mA
INPUT IMPEDANCE							
Z_{ID}	Differential				3 || 4		MΩ || pF
Z_{ICM}	Common-mode				100 || 4		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 200 mV < V_O < (V+) – 200 mV, R_L = 10 kΩ		126	132		dB
			T_A = –40°C to +125°C	120			
		(V–) + 200 mV < V_O < (V+) – 200 mV, R_L = 2 kΩ		125	130		
			T_A = –40°C to +125°C	120			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				3.6		MHz
SR	Slew rate	4-V step, G = –1			4		V/µs
	Phase margin	R_L = 10 kΩ, C_L = 25 pF			55		degrees
t_S	Settling time	To 0.1%, 4-V step , G = –1, C_L = 30 pF			1.9		µs
		To 0.0015% (16-bit), 4-V step , G = –1, C_L = 30 pF			3.1		
	Overload recovery time	G = –10			2.2		µs
THD+N	Total harmonic distortion + noise	V_O = 5 V_{PP}, G = +1, f = 1 kHz, R_L = 2 kΩ			0.0004		%

ADVANCE INFORMATION

Electrical Characteristics: V_S = ±5 V (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	T_A = 25°C, R_L = 10 kΩ, A_{OL} > 126 dB	(V–) + 0.2		(V+) + 0.2	V
		T_A = 25°C, R_L = 2 kΩ, A_{OL} > 125 dB	(V–) + 0.2		(V+) + 0.2	
		T_A = –40°C to +125°C, R_L = 10 kΩ	(V–) + 0.2		(V+) + 0.2	
I_{SC}	Short-circuit current			±25		mA
C_{LOAD}	Capacitive load drive		See Typical Characteristics			
R_O	Open-loop output impedance		See Typical Characteristics			
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 mA		220	250	µA
		I_O = 0 mA, T_A = –40°C to +125°C			335	

ADVANCE INFORMATION

6.6 Electrical Characteristics: V_S = ±15 V

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±5	±25	µV
		T_A = –40°C to +125°C			±12	±55	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±0.1	±0.3	µV/°C
PSRR	Input offset voltage versus power supply	V_S = ±2.25 V to ±18 V			±0.05	±0.5	µV/V
		V_S = ±2.25 V to ±18 V, T_A = –40°C to +125°C				±1	
INPUT BIAS CURRENT							
I_B	Input bias current				±0.2	±0.75	nA
		T_A = 0°C to 85°C				±1	
		T_A = –40°C to +125°C				±1.2	
I_{OS}	Input offset current				±0.1	±0.4	nA
		T_A = 0°C to 85°C				±0.8	
		T_A = –40°C to +125°C				±0.9	
NOISE							
$e_{n\ p\text{-}p}$	Input voltage noise	f = 0.1 Hz to 10 Hz			0.15		μV_{PP}
e_n	Input voltage noise density	f = 10 Hz			8.4		$nV/\sqrt{Hz}$
		f = 100 Hz			8		
		f = 1 kHz			8		
i_n	Input current noise	f = 1 kHz			200		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage			(V–) + 1		(V+) – 1.4	V
CMRR	Common-mode rejection ratio	(V–) + 1 V < V_{CM} < (V+) – 1.4 V		126	140		dB
		(V–) + 1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to +125°C		120	140		
INPUT OVERVOLTAGE RANGE							
	Input overvoltage protection	T_A = –40°C to +125°C		(V–) – 40		(V+) + 40	V
	Input current in overvoltage protected mode	V_{CM} = (V+) + 40 V, V_{CM} = (V–) – 40 V			5		mA
INPUT IMPEDANCE							
Z_{ID}	Differential				3 || 4		MΩ || pF
Z_{ICM}	Common-mode				100 || 4		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 200 mV < V_O < (V+) – 200 mV, R_L = 10 kΩ		126	132		dB
			T_A = –40°C to +125°C	120			
		(V–) + 350 mV < V_O < (V+) – 350 mV, R_L = 2 kΩ		125	130		
			T_A = –40°C to +125°C	120			
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C_L = 30 pF			3.6		MHz
SR	Slew rate	10-V step, G = –1			4		V/µs
	Phase margin	R_L = 10 kΩ, C_L = 25 pF			58		degrees
t_S	Settling time	To 0.1%, 10-V step , G = –1, C_L = 30 pF			2.9		µs
		To 0.0015% (16-bit), 10-V step , G = –1, C_L = 30 pF			4.1		
	Overload recovery time	G = –10			2.2		µs
THD+N	Total harmonic distortion + noise	V_O = 5 V_{PP}, G = +1, f = 1 kHz, R_L = 2 kΩ			0.0004		%

ADVANCE INFORMATION

Electrical Characteristics: V_S = ±15 V (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	T_A = 25°C, R_L = 10 kΩ, A_{OL} > 126 dB	(V–) + 0.2		(V+) + 0.2	V
		T_A = 25°C, R_L = 2 kΩ, A_{OL} > 125 dB	(V–) + 0.35		(V+) + 0.35	
		T_A = –40°C to +125°C, R_L = 10 kΩ	(V–) + 0.2		(V+) + 0.2	
I_{SC}	Short-circuit current			±25		mA
C_{LOAD}	Capacitive load drive		See Typical Characteristics			
R_O	Open-loop output impedance		See Typical Characteristics			
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 mA		220	250	µA
		I_O = 0 mA, T_A = –40°C to +125°C			335	

ADVANCE INFORMATION

6.7 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

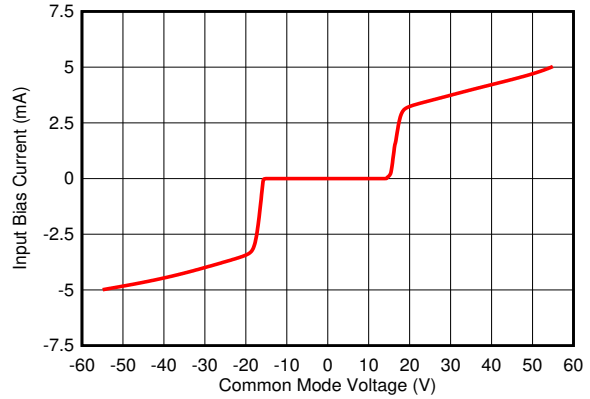


Figure 1. Input Overvoltage Protection Input Current

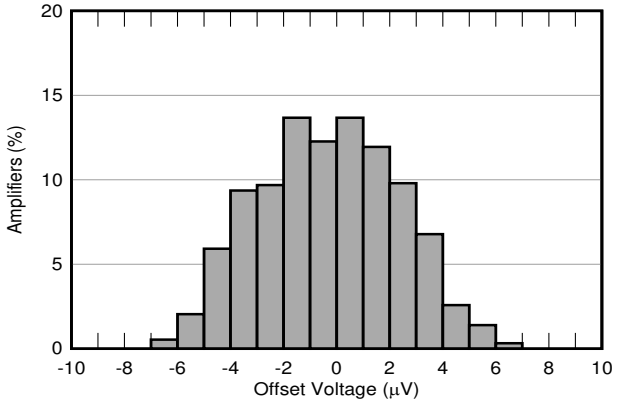


Figure 2. Input Offset Voltage

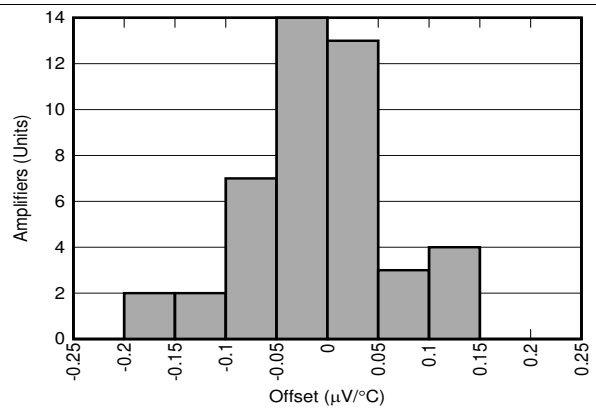


Figure 3. Input Offset Voltage Drift

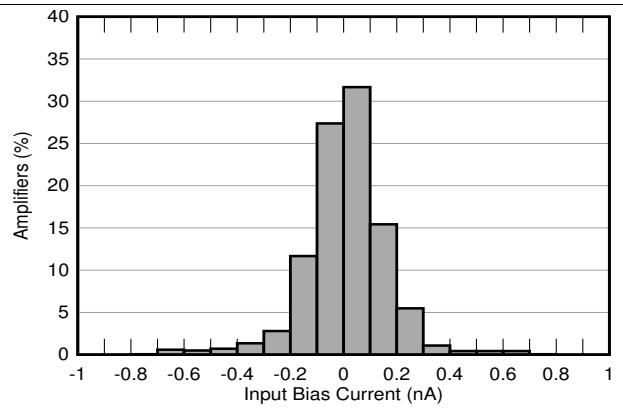


Figure 4. Input Bias Current

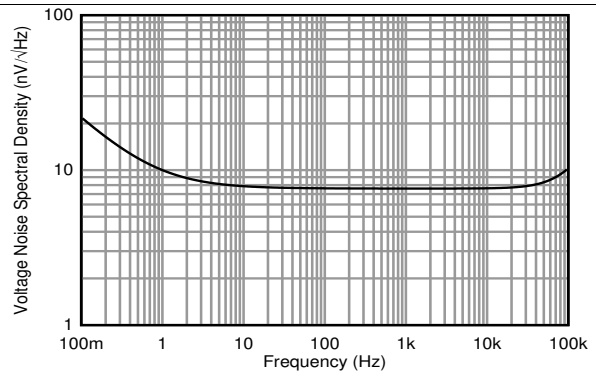


Figure 5. Voltage Noise Spectral Density

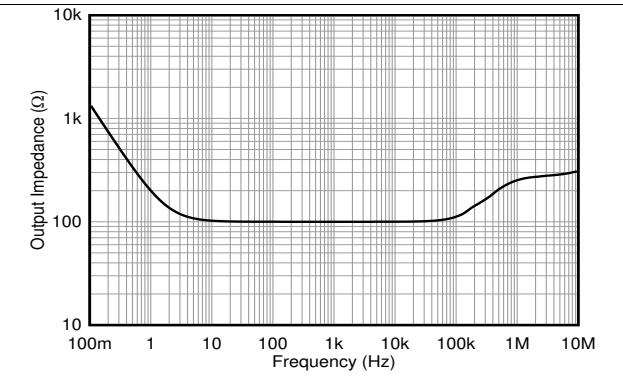


Figure 6. Output Impedance vs Frequency

ADVANCE INFORMATION

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

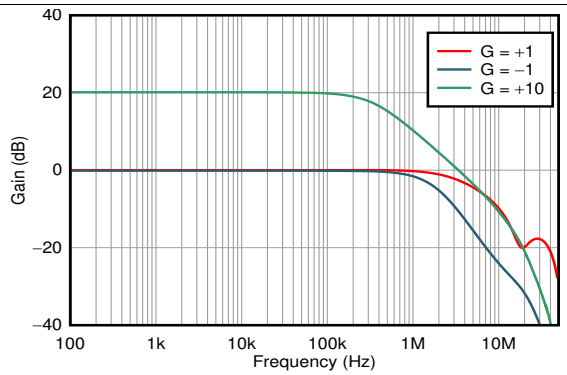


Figure 7. Closed Loop Gain

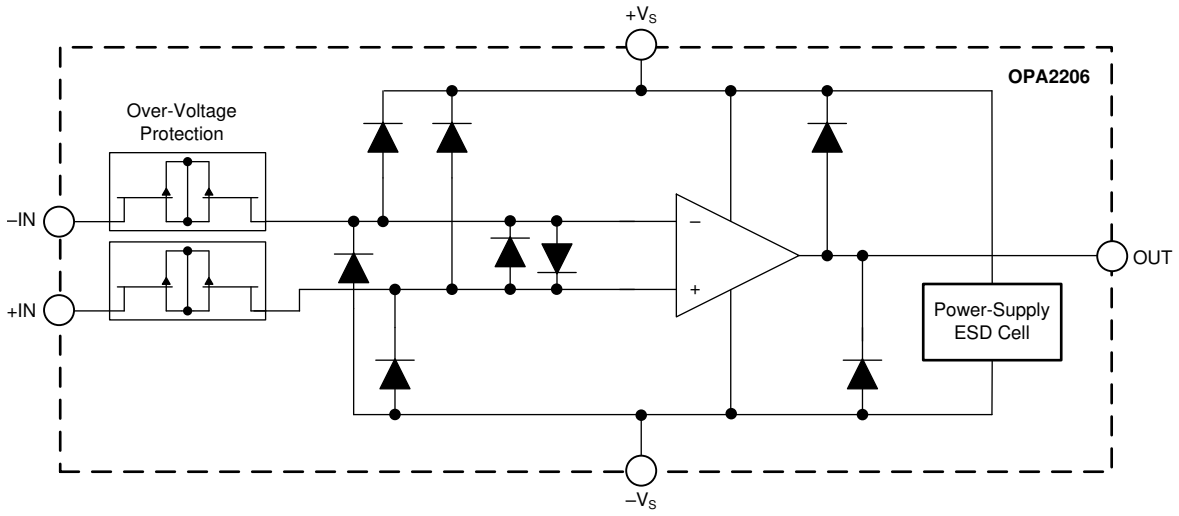
ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The OPA2206 is the first 36-V, bipolar, e-trim operational amplifier. This device uses a package-level offset trim to minimize the offset voltage and offset voltage drift introduced during the manufacturing process. This trim is performed after the device is assembled to remove any offset errors introduced throughout the manufacturing process, and trim communication is disabled afterward. The device features super beta inputs that decrease the input bias current and input current noise. The device also features input overvoltage protection that protects the device for input voltages up to ±40 V beyond either supply rail.

7.2 Functional Block Diagram



ADVANCE INFORMATION

7.3 Feature Description

7.3.1 Input Overvoltage Protection

The inputs of the OPA2206 are individually protected for voltages up to ±40 V beyond either supply. For example, a common-mode voltage anywhere between –55 V and +55 V does not cause damage when powered from ±15-V supplies. Internal circuitry on each input provides low series impedance under normal signal conditions thus maintaining high performance under normal operating conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 4.8 mA.

During an input overvoltage condition, current flows through the input protection diodes into the power supplies, as shown in Figure 8. If the power supplies are unable to sink current, then Zener diode clamps (ZD1 and ZD2) must be placed on the power supplies to provide a current pathway to ground. During an overvoltage condition, the input bias current of the inputs increase as shown in Figure 9.

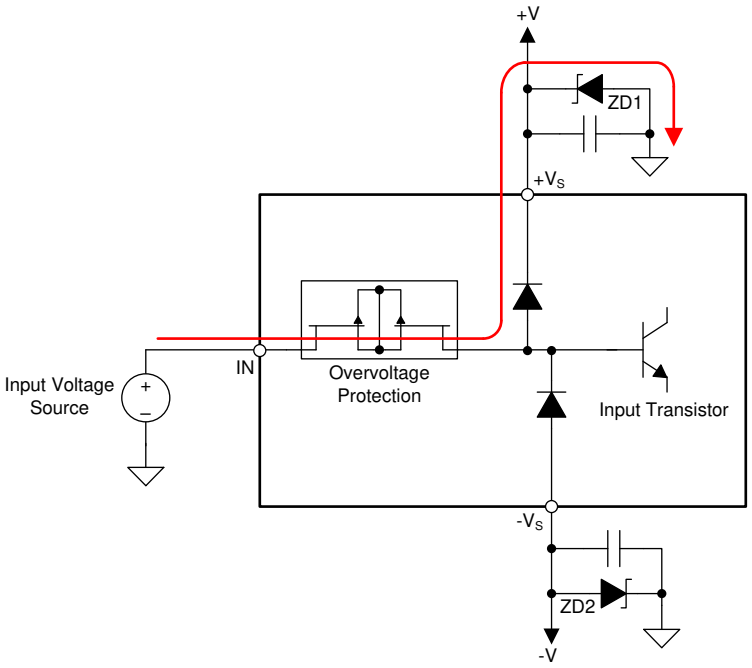


Figure 8. OPA2206 Input Overvoltage Current Path

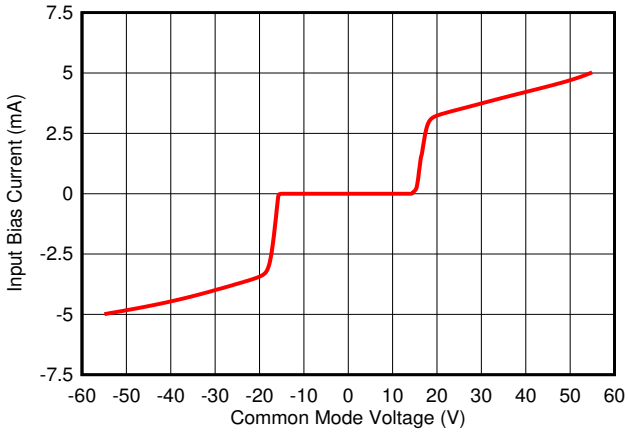


Figure 9. OPA2206 Input Current vs Input Voltage (V_S = ±15 V)

Feature Description (continued)

7.3.2 Input Offset Digital Trimming

The OPA2206 is the industry's first e-trim operational amplifier built on a bipolar process. The input offset voltage of an amplifier is determined by the inherent mismatch between the inputs of the device. The offset can be minimized using laser-trimming performed during the manufacturing process while the device is still in the bare silicon form. However, when the silicon is packaged, the package process introduces additional offset. New digital trimming processes are used to trim the offset after the packaging process is complete to minimize both the inherent and package-induced offsets. The process takes place at the end of the manufacturing process when the final performance of the device is being tested. After trimming, the communication is disabled to make sure the amplifier operates properly in the final system.

A comparison between production offset values for a laser-trimmed amplifier and the OPA2206 digital trim can be seen in Figure 10 and Figure 11.

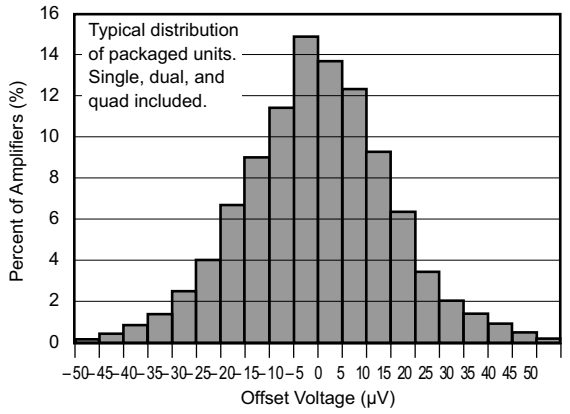


Figure 10. OPA2277 Laser-Trimmed Operational Amplifier Offset

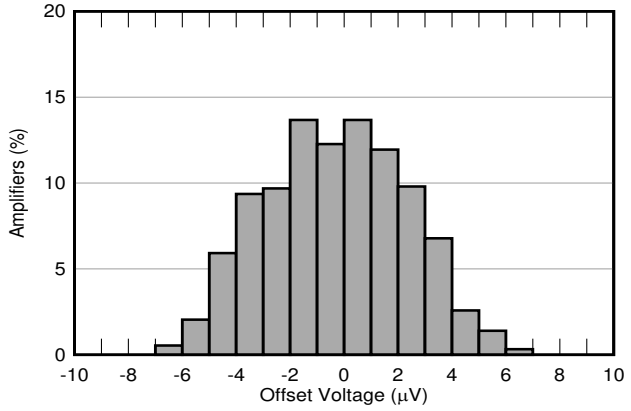


Figure 11. OPA2206 e-trim™ Operational Amplifier Offset

The OPA2206 digital trim architecture is also used in a two-temperature trim to minimize the input offset voltage drift over temperature. The final performance of the offset drift can be seen in Figure 12.

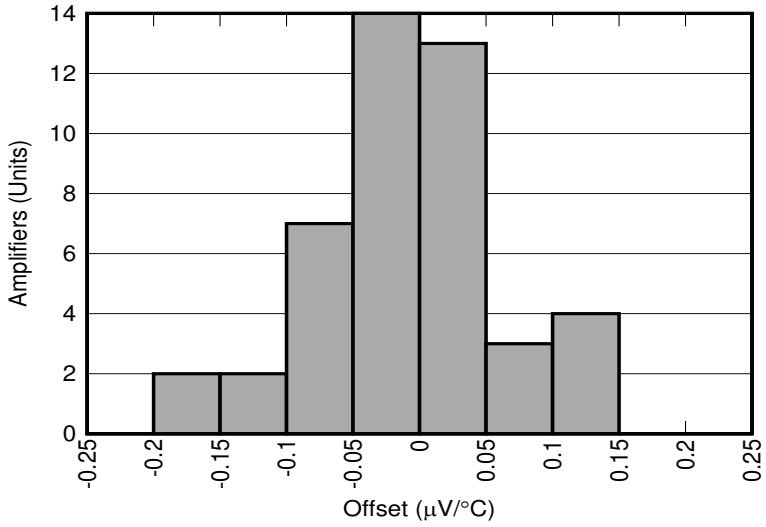


Figure 12. OPA2206 e-trim™ Operational Amplifier Drift

ADVANCE INFORMATION

Feature Description (continued)

7.3.3 Lower Input Bias With Super Beta Inputs

The OPA2206 has a super beta input transistor architecture. In a transistor, the beta value is the ratio between the current flowing into the base and the current flowing from the collector to the emitter. A super beta transistor is one where the beta value has been increased from several hundred to thousands. In a bipolar amplifier, the input bias current is the current flowing into the base of the input transistor pair, as well as a small leakage current that flows through the ESD diodes. A super beta input reduces the input bias current of the amplifier. In addition, the super beta inputs lower the input current noise that is directly related to the input bias current of the device. A comparison between the input bias current of a standard bipolar amplifier and the OPA2206 super beta input bias currents can be seen in Figure 13 and Figure 14.

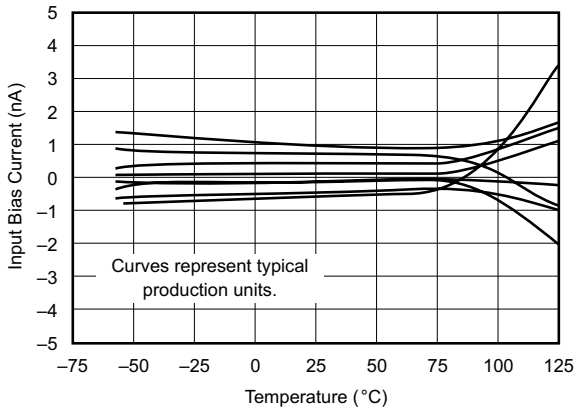


Figure 13. OPA2277 Input Bias Current

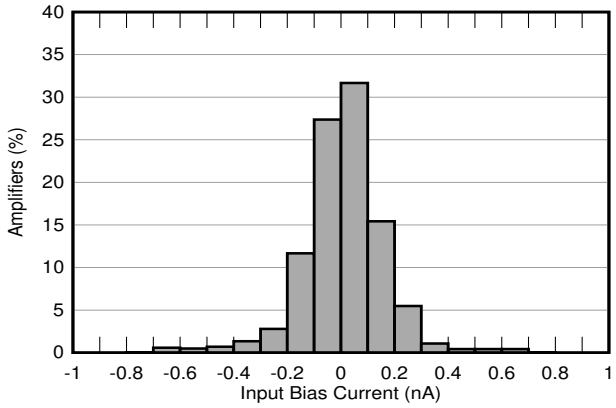


Figure 14. OPA2206 Super Beta Input Bias Current

7.3.4 Overload Power Limiter

In many bipolar-based amplifiers, the output stage of the amplifier can draw significant (several milliamperes) of quiescent current if the output voltage becomes clipped (meaning the output voltage becomes limited by the negative or positive supply voltage). This condition can cause the system to enter a high-power consumption state, and potentially cause oscillations between the power supply and signal chain. The OPA2206 has an advanced output stage design that eliminates this problem. When the output voltage reaches the either supply (V+ or V–), there is virtually no additional current consumption from the nominal quiescent current. This feature helps eliminate any potential system problems when the signal chain is disrupted by a large external transient voltage.

7.3.5 EMI Rejection

The OPA2206 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources, such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved through circuit design techniques that improve the system performance. Additional information can be found in the *EMI Rejection Ratio of Operation Amplifiers* application report.

7.4 Device Functional Modes

The OPA2206 has two functional modes. The device enters normal operation with any supply between 4.5 V (±2.25 V) and 36 V (±18 V), and an input voltage that meets the input common-mode voltage range shown in the *Specifications* section.

If the input voltage exceeds the device specifications, the device will enter an overvoltage protection mode. In this mode the input overvoltage protection sub-circuit will limit the voltage and current seen by the amplifier core by adding additional impedance between the input pins and the amplifier core. Additional current that is generated from the voltage drop across this input impedance is routed through the ESD structure of the OPA2206, as shown in Figure 8.

ADVANCE INFORMATION

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA2206 is a unity-gain stable operational amplifier with very low offset voltage, offset voltage drift, voltage noise, current noise, and power consumption. The built-in overvoltage protection allows the device to protect against signals outside of the expected range, a reverse connection, or in cases where the inputs are shorted to a system supply. These features make this device a great choice for a variety of space-constrained and power-constrained systems.

8.2 Typical Application

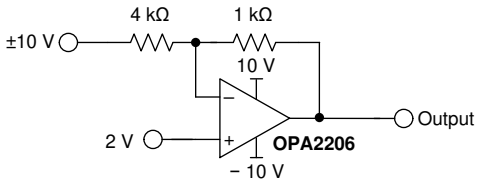


Figure 15. OPA2206 Configured as a Voltage Attenuator

8.2.1 Design Requirements

The design requirements for this system are:

- Input range: ±10 V
- Input frequency: up to 20 kHz
- Output voltage: 0 V to 5 V
- Input protection: up to ±50 V

8.2.2 Detailed Design Procedure

In this application, the input signal to the signal chain is ±20 V with a frequency up to 20 kHz. The output of the amplifier is configured as an attenuator with a bias voltage so that the output range is 0 V to 5 V, which is a common input range for single-ended ADCs.

The OPA2206 is selected for this application because of the high dc precision (5 µV offset and 0.1 µV/°C offset drift) and low power consumption (250 µA quiescent current) that minimizes thermal dissipation requirements. The integrated overvoltage protection (OVP) of the OPA2206 protects against fault voltages up to ±40 V beyond either supply rail, which in this design with ±10-V rails offers protection up to ±50 V. Because of the internal OVP topology, the device provides better dc and ac accuracy under normal operating conditions compared to passive external protection. Connect a zener diode between each supply to ground to provide a return path for the current that is generated during a fault condition.

8.2.3 Application Curves

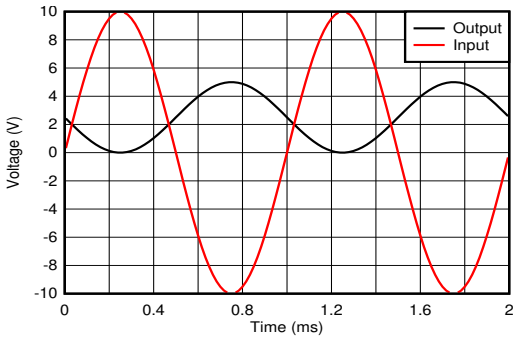


Figure 16. Attenuator Input and Output Voltage

ADVANCE INFORMATION

9 Power Supply Recommendations

The OPA2206 operates with a supply between 4.5 V (±2.25 V) and 36 V (±18 V). Parameters that can exhibit significant variance with regard to operating voltages are presented in the *Typical Characteristics* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications. Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as through the individual op amp. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Make sure to physically separate digital and analog grounds and pay attention to the flow of the ground current. Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better, as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 17, keep RF and RG close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. After any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

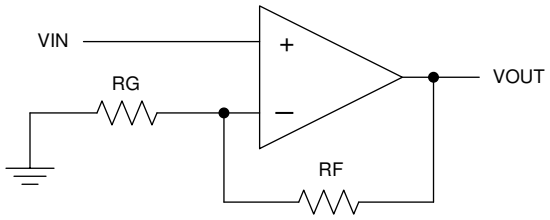


Figure 17. Schematic Representation

ADVANCE INFORMATION

Layout Example (continued)

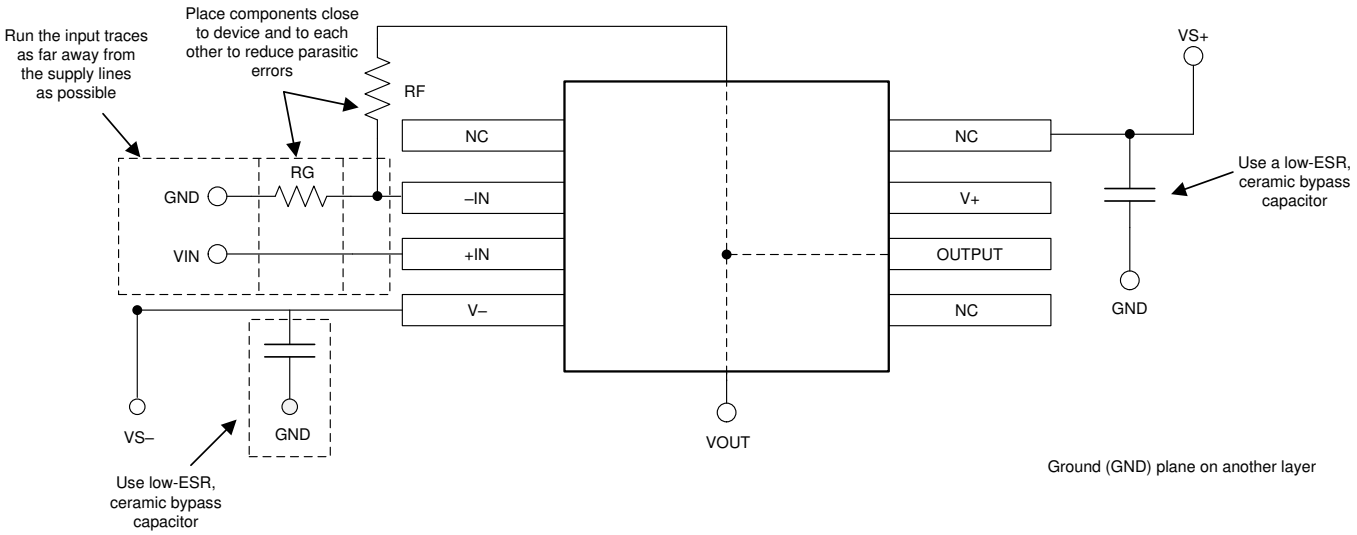


Figure 18. Operational Amplifier Board Layout for Noninverting Configuration

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2206DGKR	PREVIEW	VSSOP	DGK	8	2500	RoHS (In work) & Non-Green	Call TI	Call TI	-40 to 125		
XOPA2206DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS (In work) & Non-Green	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

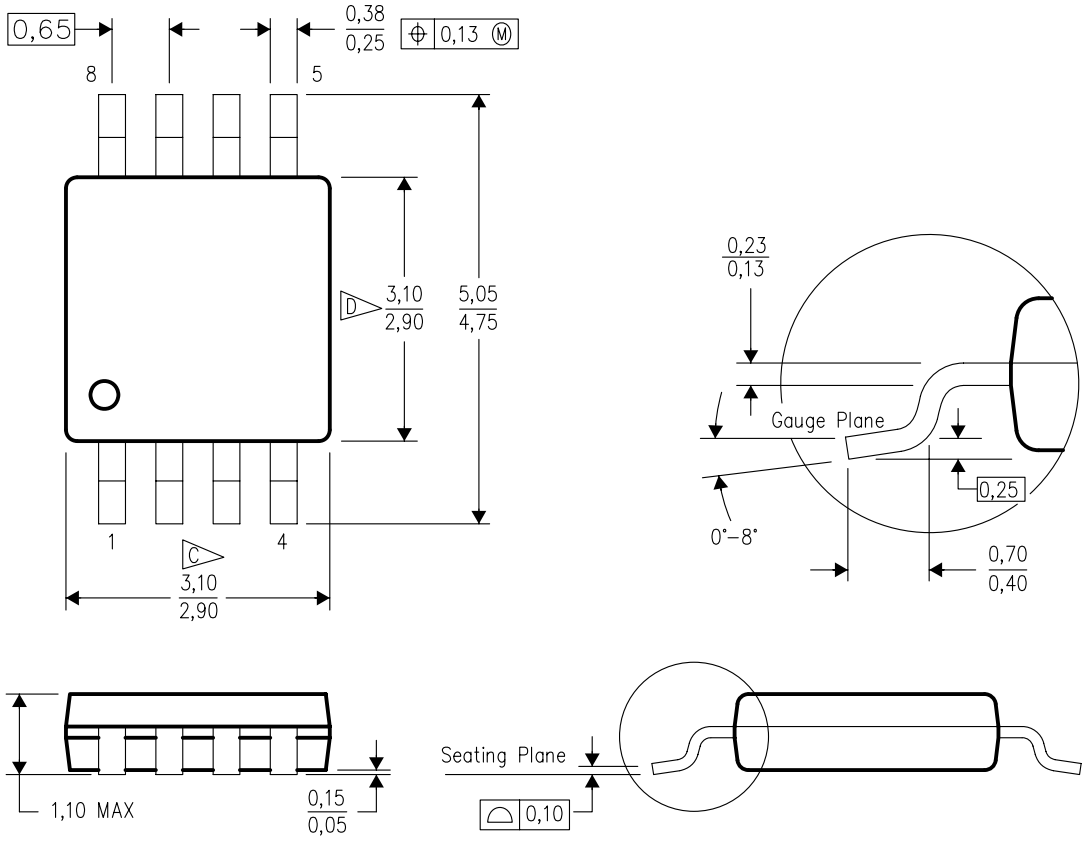
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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