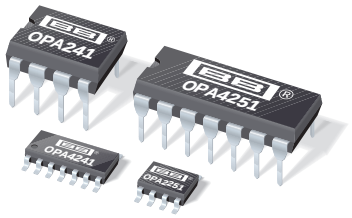
BURR-BROWN®



OPA241
OPA2241
OPA4241

OPA251
OPA2251
OPA4251

Single-Supply, *Micro*POWER OPERATIONAL AMPLIFIERS

OPA241 Family optimized for +5V supply.

OPA251 Family optimized for ±15V supply.

FEATURES

- ***Micro*POWER: I_Q = 25µA**
- **SINGLE-SUPPLY OPERATION**
- **RAIL-TO-RAIL OUTPUT (within 50mV)**
- **WIDE SUPPLY RANGE**
  Single Supply: +2.7V to +36V
  Dual Supply: ±1.35V to ±18V
- **LOW OFFSET VOLTAGE: ±250µV max**
- **HIGH COMMON-MODE REJECTION: 124dB**
- **HIGH OPEN-LOOP GAIN: 128dB**
- **SINGLE, DUAL, AND QUAD**

APPLICATIONS

- **BATTERY OPERATED INSTRUMENTS**
- **PORTABLE DEVICES**
- **MEDICAL INSTRUMENTS**
- **TEST EQUIPMENT**

DESCRIPTION

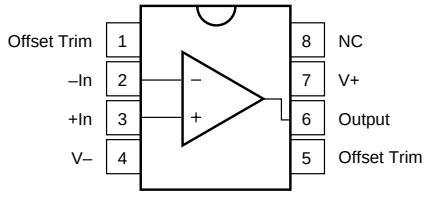
The OPA241 series and OPA251 series are specifically designed for battery powered, portable applications. In addition to very low power consumption (25µA), these amplifiers feature low offset voltage, rail-to-rail output swing, high common-mode rejection, and high open-loop gain.

The OPA241 series is optimized for operation at low power supply voltage while the OPA251 series is optimized for high power supplies. Both can operate from either single (+2.7V to +36V) or dual supplies (±1.35V to ±18V). The input common-mode voltage range extends 200mV below the negative supply—ideal for single-supply applications.

They are unity-gain stable and can drive large capacitive loads. Special design considerations assure that these products are easy to use. High performance is maintained as the amplifiers swing to their specified limits. Because the initial offset voltage (±250µV max) is so low, user adjustment is usually not required. However, external trim pins are provided for special applications (single versions only).

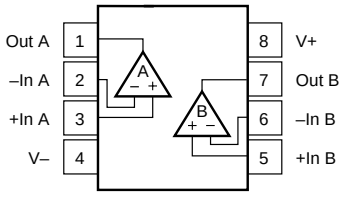
The OPA241 and OPA251 (single versions) are available in standard 8-pin DIP and SO-8 surface-mount packages. The OPA2241 and OPA2251 (dual versions) come in 8-pin DIP and SO-8 surface-mount packages. The OPA4241 and OPA4251 (quad versions) are available in 14-pin DIP and SO-14 surface-mount packages. All are fully specified from –40°C to +85°C and operate from –55°C to +125°C.

OPA241, OPA251



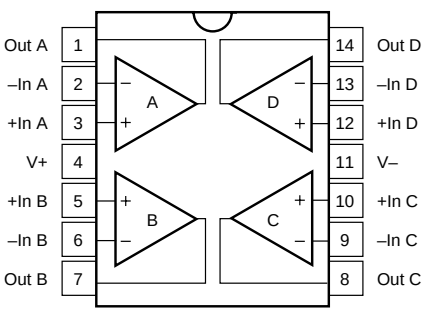
8-Pin DIP, SO-8

OPA2241, OPA2251



8-Pin DIP, SO-8

OPA4241, OPA4251



14-Pin DIP, SO-14

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1406B
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SBOS075

SPECIFICATIONS: V_S = 2.7V to 5V

At T_A = +25°C, R_L = 100kΩ connected to V_S/2, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = –40°C to +85°C.

PARAMETER		CONDITION	OPA241UA, PA OPA2241UA, PA OPA4241UA, PA MIN	TYP(1)	MAX	OPA251UA, PA OPA2251UA, PA OPA4251UA, PA MIN	TYP(1)	MAX	UNITS
OFFSET VOLTAGE									
Input Offset Voltage	V_{OS}			±50	±250		±100		µV
T_A = –40°C to +85°C				**±100**	**±400**		**±130**		µV
vs Temperature	dV_{OS}/dT	**T_A = –40°C to +85°C**		**±0.4**			**±0.6**		µV/°C
vs Power Supply	PSRR	V_S = 2.7V to 36V		3	30		*	*	µV/V
T_A = –40°C to +85°C		V_S = 2.7V to 36V			**30**			*	µV/V
Channel Separation (dual, quad)				0.3			*		µV/V
INPUT BIAS CURRENT									
Input Bias Current(2)	I_B			–4	–20		*		nA
T_A = –40°C to +85°C					**–25**				nA
Input Offset Current	I_{OS}			±0.1	±2		*		nA
T_A = –40°C to +85°C					**±2**				nA
NOISE									
Input Voltage Noise, f = 0.1Hz to 10Hz				1			*		µVp-p
Input Voltage Noise Density, f = 1kHz	e_n			45			*		nV/√Hz
Current Noise Density, f = 1kHz	i_n			40			*		fA/√Hz
INPUT VOLTAGE RANGE									
Common-Mode Voltage Range	V_{CM}		–0.2		(V+) –0.8				V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –0.2V to (V+) –0.8V	80	106			*		dB
T_A = –40°C to +85°C		V_{CM} = 0V to (V+) –0.8V	**80**						dB
INPUT IMPEDANCE									
Differential				10^7 || 2			*		Ω || pF
Common-Mode				10^9 || 4			*		Ω || pF
OPEN-LOOP GAIN									
Open-Loop Voltage Gain	A_{OL}	R_L = 100kΩ, V_O = (V–)+100mV to (V+)–100mV	100	120			*		dB
T_A = –40°C to +85°C		R_L = 100kΩ, V_O = (V–)+100mV to (V+)–100mV	**100**						dB
		R_L = 10kΩ, V_O = (V–)+200mV to (V+)–200mV	100	120			*		dB
T_A = –40°C to +85°C		R_L = 10kΩ, V_O = (V–)+200mV to (V+)–200mV	**100**						dB
FREQUENCY RESPONSE									
Gain-Bandwidth Product	GBW			35			*		kHz
Slew Rate	SR	V_S = 5V, G = 1		0.01			*		V/µs
Overload Recovery Time		V_{IN} • G = V_S		60			*		µs
OUTPUT									
Voltage Output Swing from Rail(3)	V_O	R_L = 100kΩ to V_S/2, A_{OL} ≥ 70dB		50			*		mV
		R_L = 100kΩ to V_S/2, A_{OL} ≥ 100dB		75	100		*		mV
T_A = –40°C to +85°C		R_L = 100kΩ to V_S/2, A_{OL} ≥ 100dB			**100**				mV
		R_L = 10kΩ to V_S/2, A_{OL} ≥ 100dB		100	200		*		mV
T_A = –40°C to +85°C		R_L = 10kΩ to V_S/2, A_{OL} ≥ 100dB			**200**				mV
Short-Circuit Current	I_{SC}								
Single Versions				–24/+4			*		mA
Dual, Quad Versions				–30/+4			*		mA
Capacitive Load Drive	C_{LOAD}	See Typical Curve					*		
POWER SUPPLY									
Specified Voltage Range	V_S			+2.7 to +5			*		V
Operating Voltage Range		**T_A = –40°C to +85°C**	**+2.7**		**+36**	*		*	V
Quiescent Current (per amplifier)	I_Q	I_O = 0		±25	±30		*		µA
T_A = –40°C to +85°C		I_O = 0			**±36**				µA
TEMPERATURE RANGE									
Specified Range			–40		+85	*		*	°C
Operating Range			–55		+125	*		*	°C
Storage Range			–55		+125	*		*	°C
Thermal Resistance	θ_{JA}								
8-Pin DIP				100			*		°C/W
SO-8 Surface Mount				150			*		°C/W
14-Pin DIP				80			*		°C/W
SO-14 Surface Mount				100			*		°C/W

* Specifications the same as OPA241UA, PA.

NOTES: (1) V_S = +5V. (2) The negative sign indicates input bias current flows out of the input terminals. (3) Output voltage swings are measured between the output and power supply rails.

SPECIFICATIONS: $V_S = \pm 15V$

At T_A = +25°C, R_L = 100kΩ connected to ground, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = –40°C to +85°C.

PARAMETER		CONDITION	OPA241UA, PA OPA2241UA, PA OPA4241UA, PA MIN	TYP	MAX	OPA251UA, PA OPA2251UA, PA OPA4251UA, PA MIN	TYP	MAX	UNITS
OFFSET VOLTAGE									
Input Offset Voltage	V_{OS}			±100			±50	±250	µV
T_A = –40°C to +85°C				**±150**			**±100**	**±300**	µV
vs Temperature	dV_{OS}/dT	**T_A = –40°C to +85°C**		**±0.6**			**±0.5**		µV/°C
vs Power Supply	PSRR	V_S = ±1.35V to ±18V		*	*		3	30	µV/V
T_A = –40°C to +85°C		V_S = ±1.35V to ±18V			*			**30**	µV/V
Channel Separation (dual, quad)				*			0.3		µV/V
INPUT BIAS CURRENT									
Input Bias Current[1]	I_B			*			–4	–20	nA
T_A = –40°C to +85°C								**–25**	nA
Input Offset Current	I_{OS}			*			±0.1	±2	nA
T_A = –40°C to +85°C								**±2**	nA
NOISE									
Input Voltage Noise, f = 0.1Hz to 10Hz				*			1		µVp-p
Input Voltage Noise Density, f = 1kHz	e_n			*			45		$nV/\sqrt{Hz}$
Current Noise Density, f = 1kHz	i_n			*			40		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE									
Common-Mode Voltage Range	V_{CM}					(V–) –0.2		(V+) –0.8	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –15.2V to 14.2V		*		100	124		dB
T_A = –40°C to +85°C		V_{CM} = –15V to 14.2V				**100**			dB
INPUT IMPEDANCE									
Differential				*			10^7 || 2		Ω || pF
Common-Mode				*			10^9 || 4		Ω || pF
OPEN-LOOP GAIN									
Open-Loop Voltage Gain	A_{OL}	R_L = 100kΩ, V_O = –14.75V to +14.75V		*		100	128		dB
T_A = –40°C to +85°C		R_L = 100kΩ, V_O = –14.75V to +14.75V				**100**			dB
		R_L = 20kΩ, V_O = –14.7V to +14.7V		*		100	128		dB
T_A = –40°C to +85°C		R_L = 20kΩ, V_O = –14.7V to +14.7V				**100**			dB
FREQUENCY RESPONSE									
Gain-Bandwidth Product	GBW			*			35		kHz
Slew Rate	SR	G = 1		*			0.01		V/µs
Overload Recovery Time		V_{IN} • G = V_S		*			60		µs
OUTPUT									
Voltage Output Swing from Rail[2]	V_O	R_L = 100kΩ, A_{OL} ≥ 70dB		*			50		mV
		R_L = 100kΩ, A_{OL} ≥ 100dB		*			75	250	mV
T_A = –40°C to +85°C		R_L = 100kΩ, A_{OL} ≥ 100dB						**250**	mV
		R_L = 20kΩ, A_{OL} ≥ 100dB		*			100	300	mV
T_A = –40°C to +85°C		R_L = 20kΩ, A_{OL} ≥ 100dB						**300**	mV
Short-Circuit Current	I_{SC}								
Single Versions				*			–21/+4		mA
Dual Versions				*			–50/+4		mA
Capacitive Load Drive	C_{LOAD}			*			See Typical Curve		
POWER SUPPLY									
Specified Voltage Range	V_S			*			±15		V
Operating Voltage Range		**T_A = –40°C to +85°C**	*		*	**±1.35**		**±18**	V
Quiescent Current (per amplifier)	I_Q	I_O = 0		*			±27	±38	µA
T_A = –40°C to +85°C		I_O = 0						**±45**	µA
TEMPERATURE RANGE									
Specified Range			*		*	–40		+85	°C
Operating Range			*		*	–55		+125	°C
Storage Range			*		*	–55		+125	°C
Thermal Resistance	θ_{JA}								
8-Pin DIP				*			100		°C/W
SO-8 Surface Mount				*			150		°C/W
14-Pin DIP				*			80		°C/W
SO-14 Surface Mount				*			100		°C/W

* Specifications the same as OPA251UA, PA.

NOTES: (1) The negative sign indicates input bias current flows out of the input terminals. (2) Output voltage swings are measured between the output and power supply rails.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	36V
Input Voltage[2]	(V–) –0.5V to (V+) +0.5V
Output Short Circuit to Ground[3]	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more that 0.5V beyond the supply rails should be current-limited to 5mA or less. (3) One amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	SPECIFIED VOLTAGE	OPERATING VOLTAGE RANGE	PACKAGE	PACKAGE DRAWING NUMBER[1]	SPECIFICATION TEMPERATURE RANGE
OPA241 SERIES					
Single					
OPA241PA	2.7V to 5V	2.7V to 36V	8-Pin DIP	006	–40°C to +85°C
OPA241UA	2.7V to 5V	2.7V to 36V	SO-8 Surface Mount	182	–40°C to +85°C
Dual					
OPA2241PA	2.7V to 5V	2.7V to 36V	8-Pin DIP	006	–40°C to +85°C
OPA2241UA	2.7V to 5V	2.7V to 36V	SO-8 Surface Mount	182	–40°C to +85°C
Quad					
OPA4241PA	2.7V to 5V	2.7V to 36V	14-Pin DIP	010	–40°C to +85°C
OPA4241UA	2.7V to 5V	2.7V to 36V	SO-14 Surface Mount	235	–40°C to +85°C
OPA251 SERIES					
Single					
OPA251PA	±15V	2.7V to 36V	8-Pin DIP	006	–40°C to +85°C
OPA251UA	±15V	2.7V to 36V	SO-8 Surface Mount	182	–40°C to +85°C
Dual					
OPA2251PA	±15V	2.7V to 36V	8-Pin DIP	006	–40°C to +85°C
OPA2251UA	±15V	2.7V to 36V	SO-8 Surface Mount	182	–40°C to +85°C
Quad					
OPA4251PA	±15V	2.7V to 36V	14-Pin DIP	010	–40°C to +85°C
OPA4251UA	±15V	2.7V to 36V	SO-14 Surface Mount	235	–40°C to +85°C

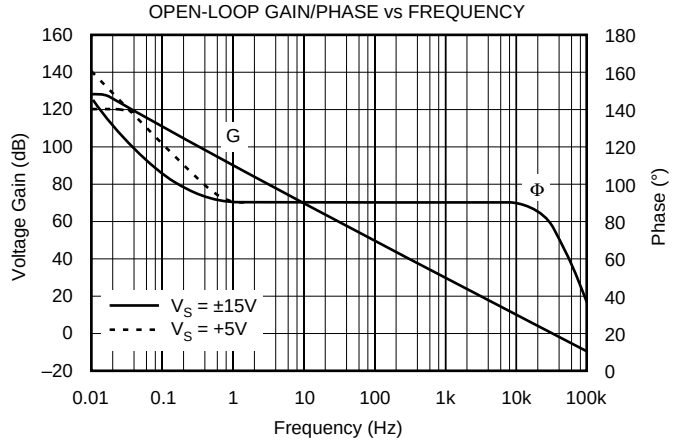
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

TYPICAL PERFORMANCE CURVES

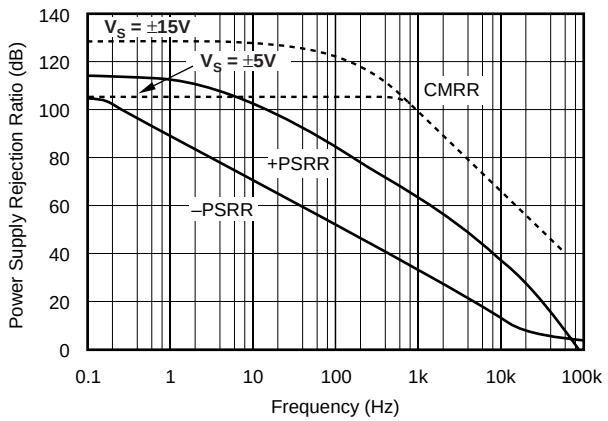
At T_A = +25°C, and R_L = 100kΩ connected to V_S/2 (ground for V_S = ±15V), unless otherwise noted.

Curves apply to OPA241 and OPA251 unless specified.

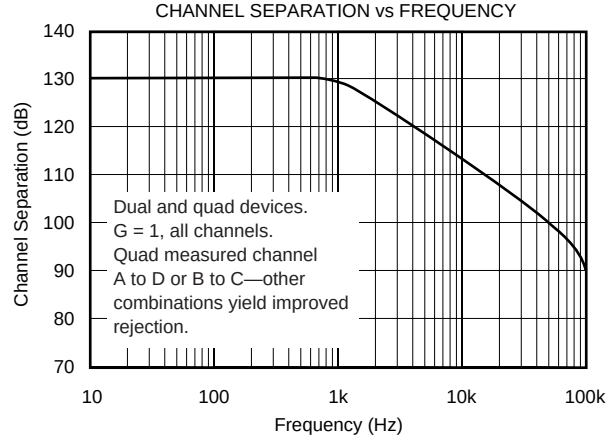
OPEN-LOOP GAIN/PHASE vs FREQUENCY



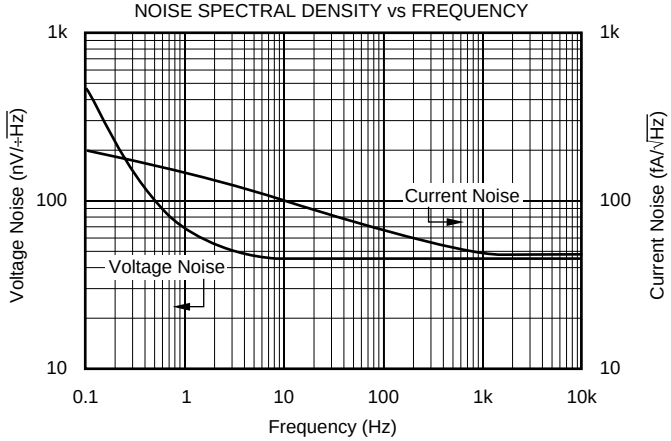
POWER SUPPLY and COMMON-MODE REJECTION RATIO vs FREQUENCY



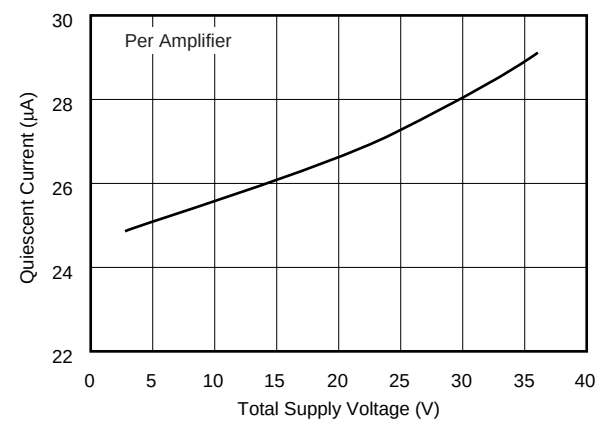
CHANNEL SEPARATION vs FREQUENCY



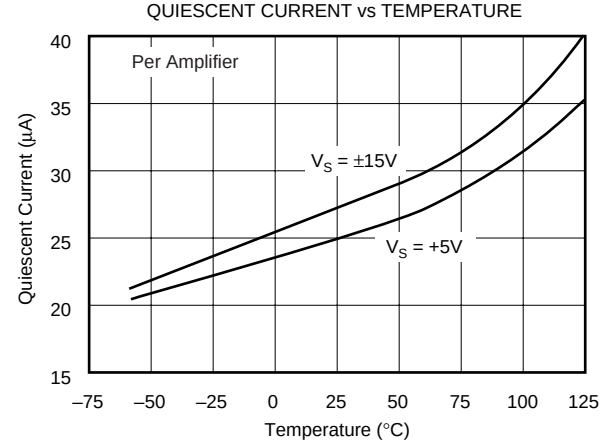
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



QUIESCENT CURRENT vs SUPPLY VOLTAGE



QUIESCENT CURRENT vs TEMPERATURE

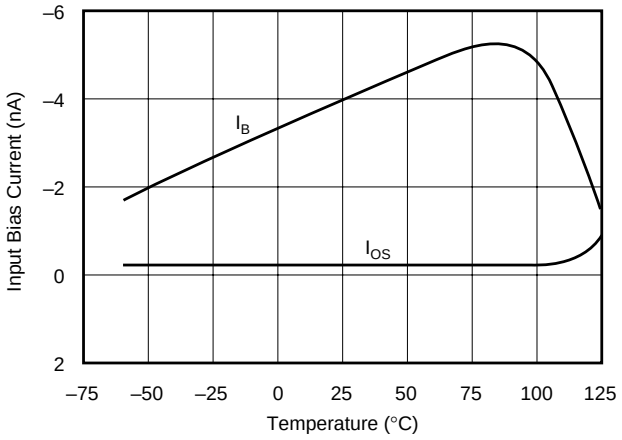


TYPICAL PERFORMANCE CURVES (CONT)

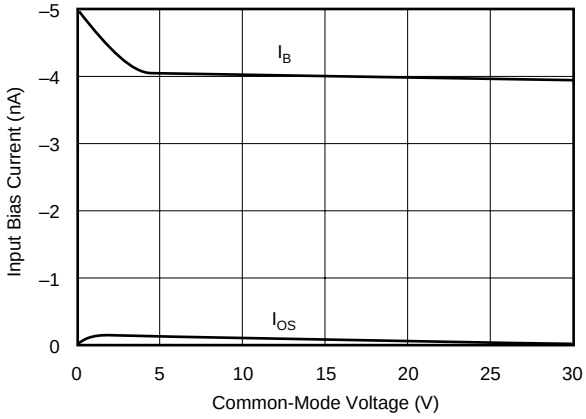
At T_A = +25°C, and R_L = 100kΩ connected to V_S/2 (ground for V_S = ±15V), unless otherwise noted.

Curves apply to OPA241 and OPA251 unless specified.

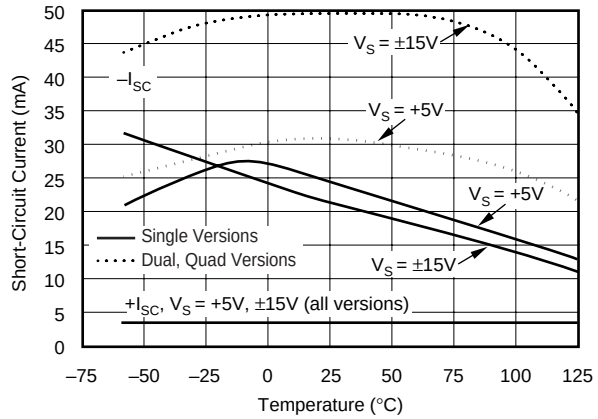
INPUT BIAS CURRENT vs TEMPERATURE



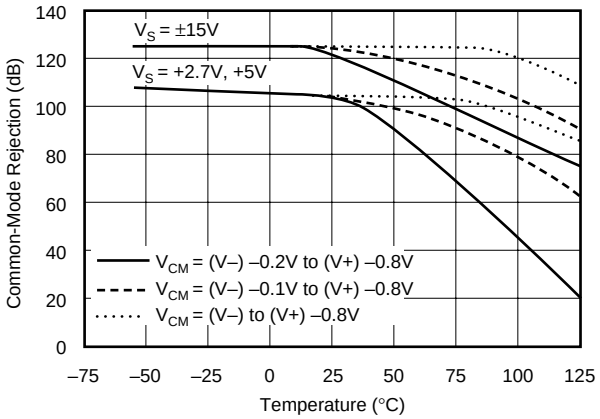
INPUT BIAS CURRENT
vs INPUT COMMON-MODE VOLTAGE



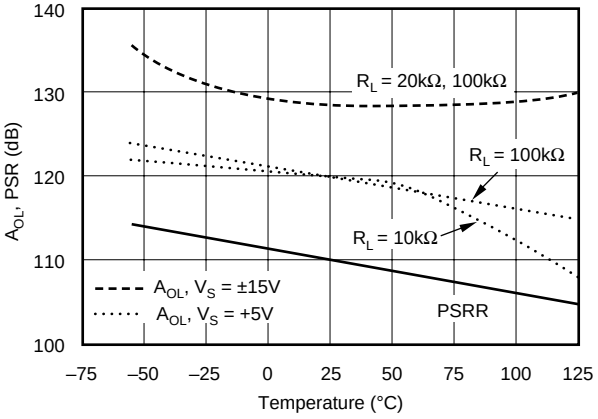
SHORT-CIRCUIT CURRENT vs TEMPERATURE



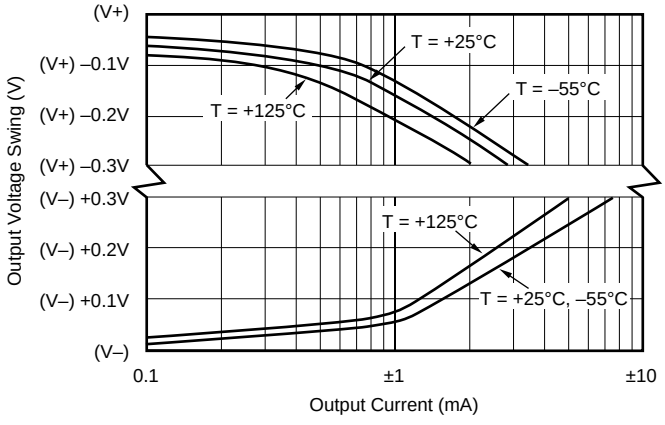
COMMON-MODE REJECTION vs TEMPERATURE



OPEN-LOOP GAIN AND POWER
SUPPLY REJECTION vs TEMPERATURE



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

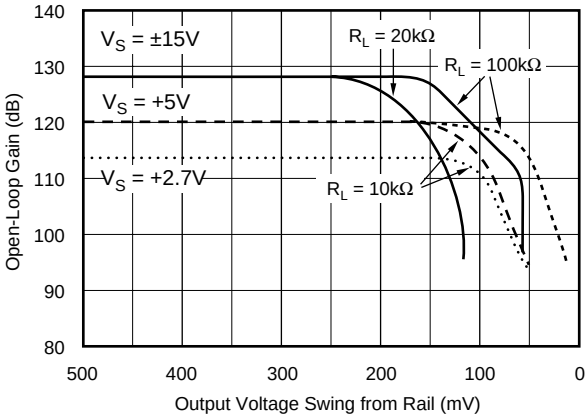


TYPICAL PERFORMANCE CURVES (CONT)

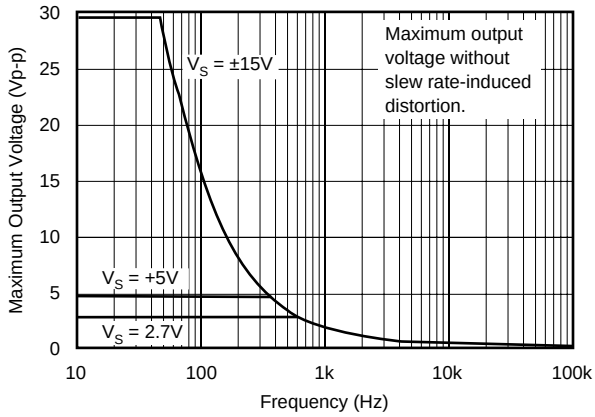
At T_A = +25°C, and R_L = 100kΩ connected to V_S/2 (ground for V_S = ±15V), unless otherwise noted.

Curves apply to OPA241 and OPA251 unless specified.

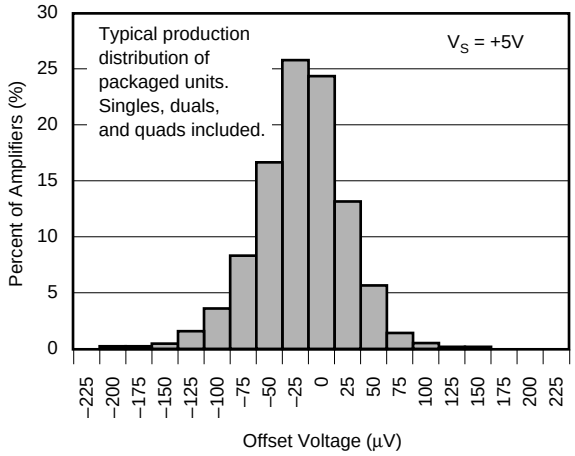
OPEN-LOOP GAIN vs OUTPUT VOLTAGE SWING



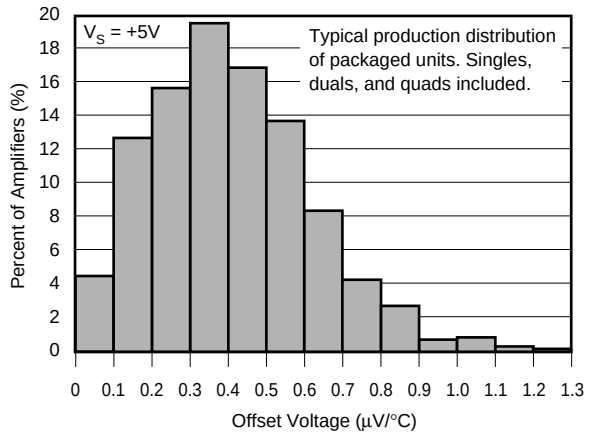
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



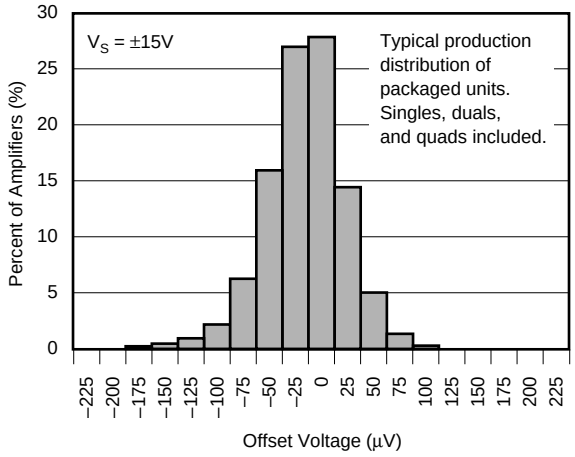
OPA241 SERIES OFFSET VOLTAGE PRODUCTION DISTRIBUTION



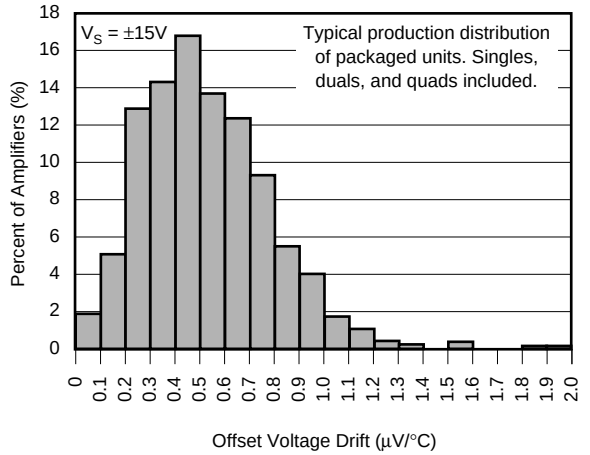
OPA241 SERIES OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



OPA251 SERIES OFFSET VOLTAGE PRODUCTION DISTRIBUTION



OPA251 SERIES OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

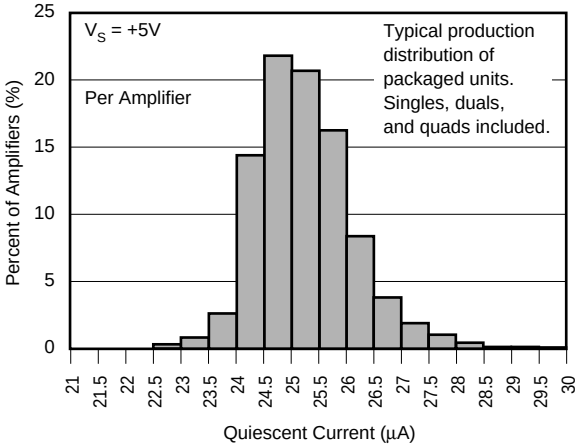


TYPICAL PERFORMANCE CURVES (CONT)

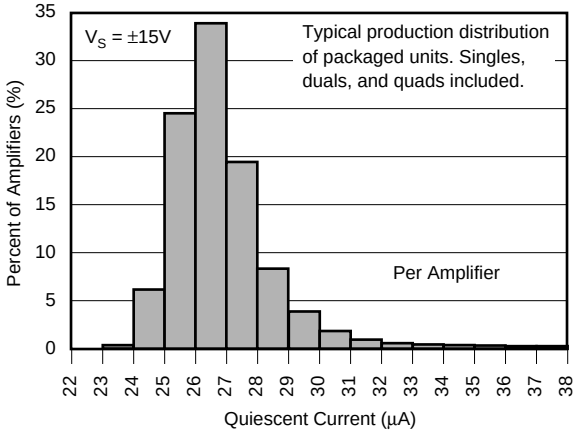
At T_A = +25°C, and R_L = 100kΩ connected to V_S/2 (ground for V_S ±15V), unless otherwise noted.

Curves apply to OPA241 and OPA251 unless specified.

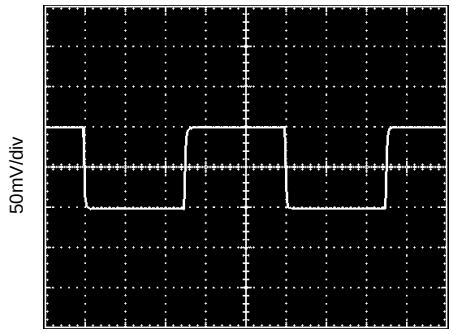
QUIESCENT CURRENT
PRODUCT DISTRIBUTION



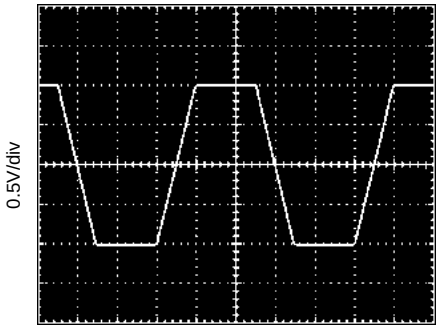
QUIESCENT CURRENT
PRODUCTION DISTRIBUTION



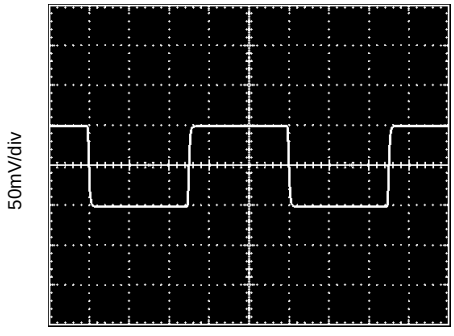
OPA241
SMALL-SIGNAL STEP RESPONSE
V_S = +5V, G = +1, R_L = 100kΩ, C_L = 100pF



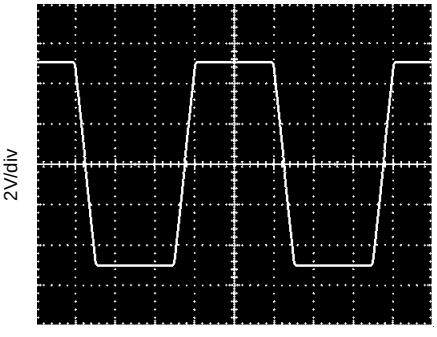
OPA241
LARGE-SIGNAL STEP RESPONSE
V_S = +5V, G + 1, R_L = 100kΩ, C_L = 100pF



OPA251
SMALL-SIGNAL STEP RESPONSE
V_S = ±15V, G = +1, R_L = 100kΩ, C_L = 500pF



OPA251
LARGE-SIGNAL STEP RESPONSE
V_S = ±15V, G = +1, R_L = 100kΩ, C_L = 500pF



APPLICATIONS INFORMATION

The OPA241 and OPA251 series are unity-gain stable and suitable for a wide range of general purpose applications. Power supply pins should be bypassed with 0.01µF ceramic capacitors.

OPERATING VOLTAGE

The OPA241 series is laser-trimmed for low offset voltage and drift at low supply voltage (V_S = +5V). The OPA251 series is trimmed for ±15V operation. Both products operate over the full voltage range (+2.7V to +36V or ±1.35V to ±18V) with some compromises in offset voltage and drift performance. However, all other parameters have similar performance. Key parameters are guaranteed over the specified temperature range, –40°C to +85°C. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage or temperature are shown in typical performance curves.

OFFSET VOLTAGE TRIM

As mentioned previously, offset voltage of the OPA241 series is laser-trimmed at +5V. The OPA251 series is trimmed at ±15V. Because the initial offset is so low, user adjustment is usually not required. However, the OPA241 and OPA251 (single op amp versions) provide offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset could degrade the offset drift behavior of the op amp. While it is not possible to predict the exact change in drift, the effect is usually small.

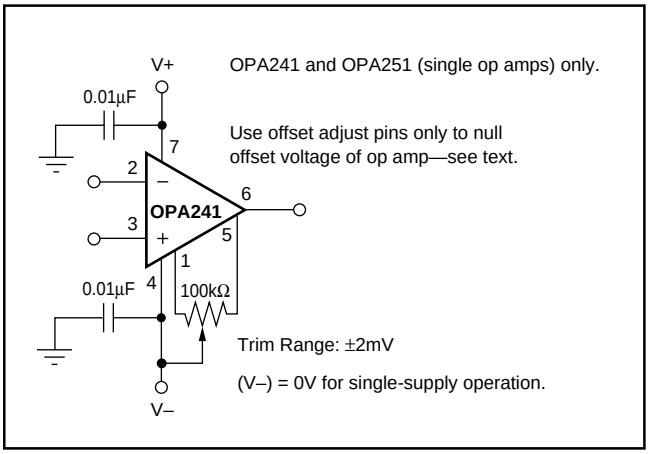


FIGURE 1. OPA241 and OPA251 Offset Voltage Trim Circuit.

CAPACITIVE LOAD AND STABILITY

The OPA241 series and OPA251 series can drive a wide range of capacitive loads. However, all op amps under certain conditions may be unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability.

Figures 2 and 3 show the regions where the OPA241 series and OPA251 series have the potential for instability. As shown, the unity gain configuration with low supplies is the most susceptible to the effects of capacitive load. With V_S = +5V, G = +1, and I_{OUT} = 0, operation remains stable with load capacitance up to approximately 200pF. Increasing supply voltage, output current, and/or gain significantly improves capacitive load drive. For example, increasing the supplies to ±15V and gain to 10 allows approximately 2700pF to be driven.

One method of improving capacitive load drive in the unity gain configuration is to insert a resistor inside the feedback loop as shown in Figure 4. This reduces ringing with large capacitive loads while maintaining dc accuracy. For example, with V_S = ±1.35V and R_S = 5kΩ, the OPA241 series and OPA251 series perform well with capacitive loads in excess of 1000pF. Without the series resistor, capacitive load drive is typically 200pF for these conditions. However, this method will result in a slight reduction of output voltage swing.

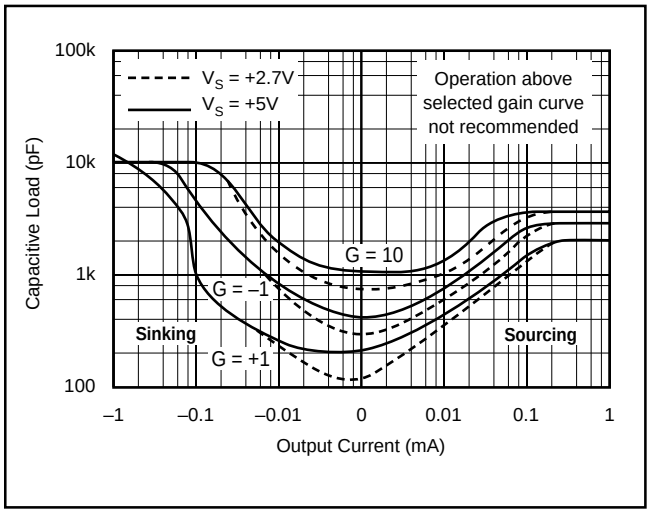


FIGURE 2. Stability—Capacitive Load versus Output Current for Low Supply Voltage.

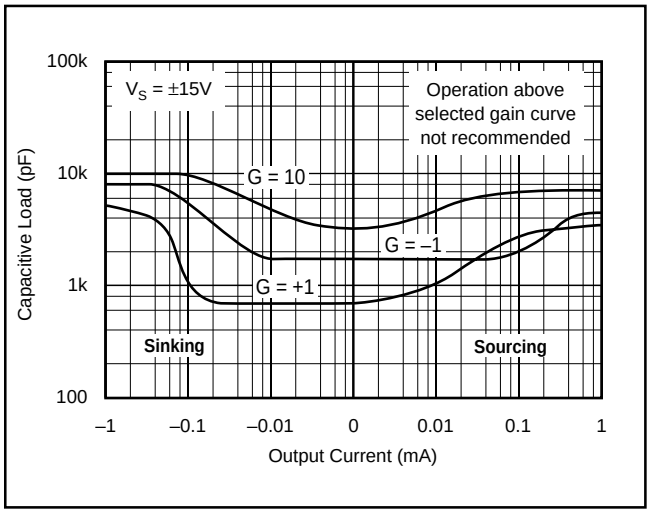


FIGURE 3. Stability—Capacitive Load versus Output Current for ±15V Supplies.

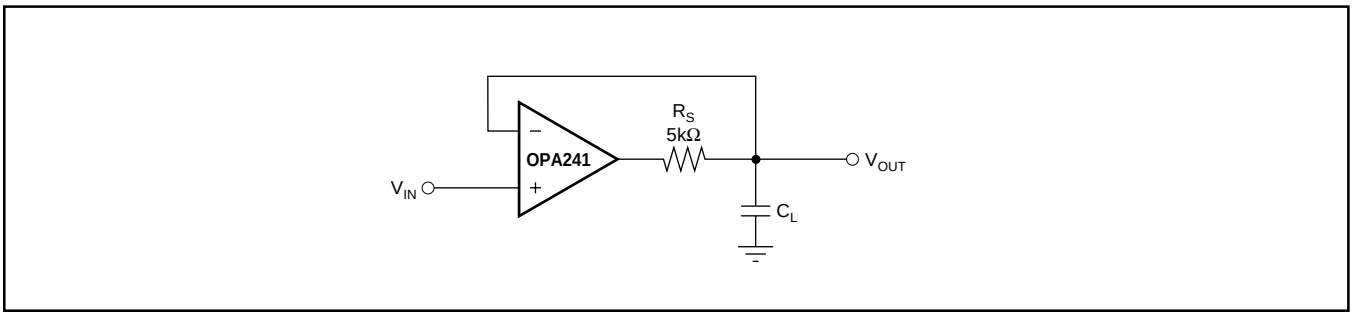
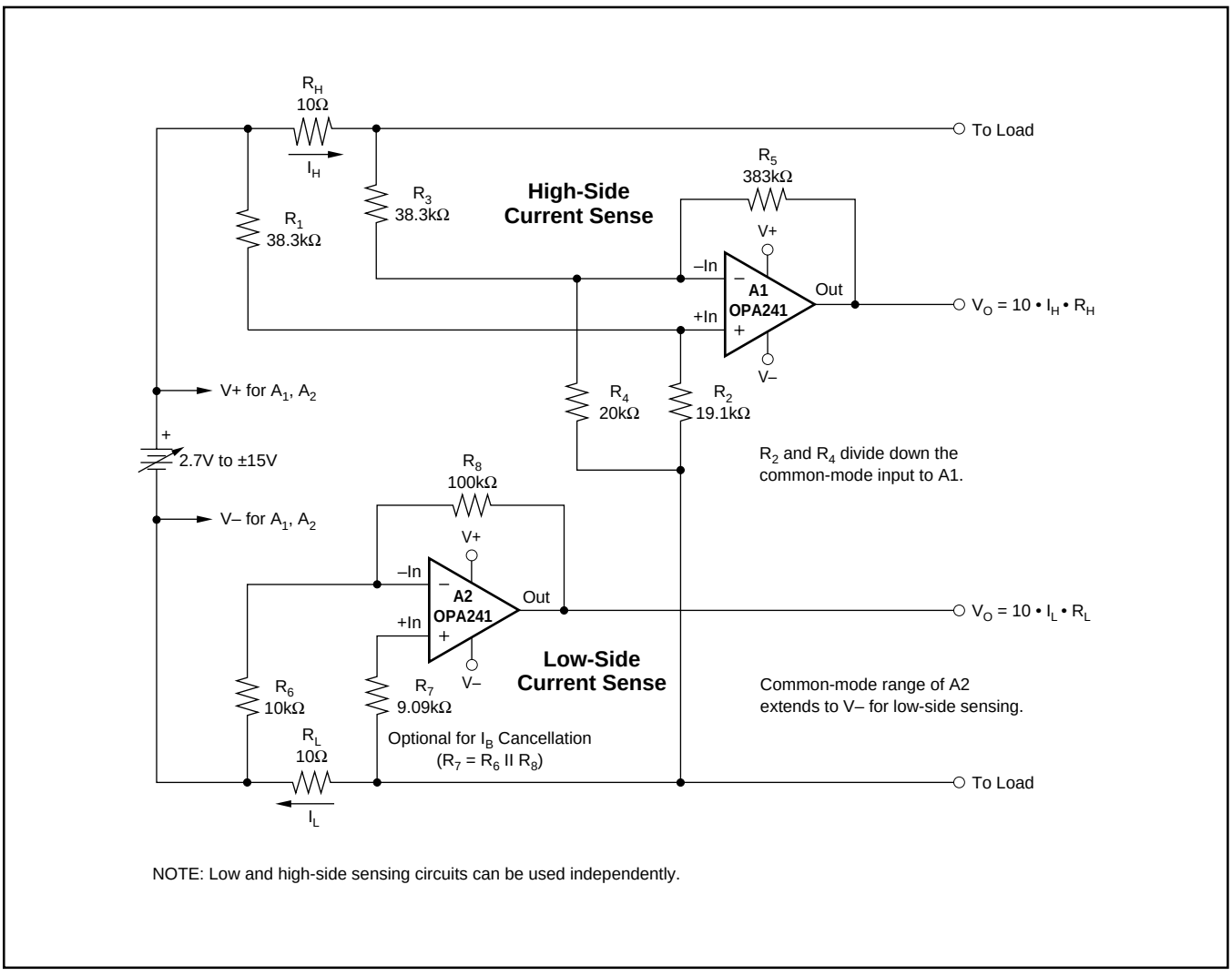


FIGURE 4. Series Resistor in Unity Gain Configuration Improves Capacitive Load Drive.



NOTE: Low and high-side sensing circuits can be used independently.

FIGURE 5. Low and High-Side Battery Current Sensing.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2241PA	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA2241PA	Samples
OPA2241PAG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA2241PA	Samples
OPA2241UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2241UA	Samples
OPA2241UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2241UA	Samples
OPA2241UAG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2241UA	Samples
OPA2251PA	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA2251PA	Samples
OPA2251PAG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA2251PA	Samples
OPA2251UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2251UA	Samples
OPA2251UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2251UA	Samples
OPA2251UAG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2251UA	Samples
OPA241PA	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		OPA241PA	Samples
OPA241PAG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		OPA241PA	Samples
OPA241UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 241UA	Samples
OPA241UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 241UA	Samples
OPA241UAG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 241UA	Samples
OPA251UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 251UA	Samples
OPA251UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 251UA	Samples
OPA251UA/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										251UA	
OPA4241PA	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA4241PA	Samples
OPA4241UA	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4241UA	Samples
OPA4241UA/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4241UA	Samples
OPA4251UA	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4251UA	Samples
OPA4251UA/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4251UA	Samples
OPA4251UA/2K5G4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4251UA	Samples
OPA4251UAG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4251UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

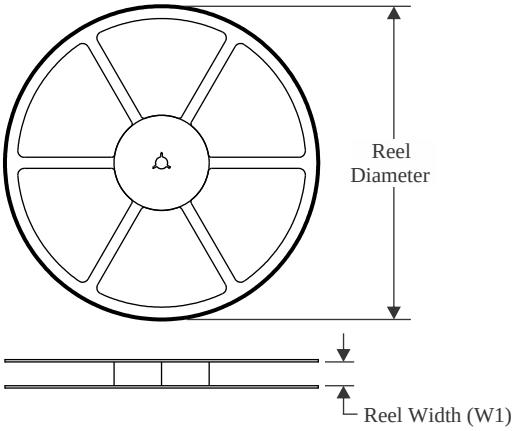
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

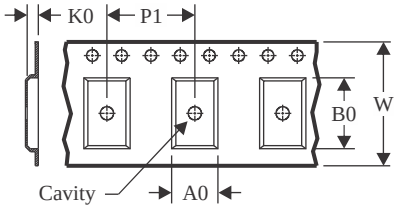
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

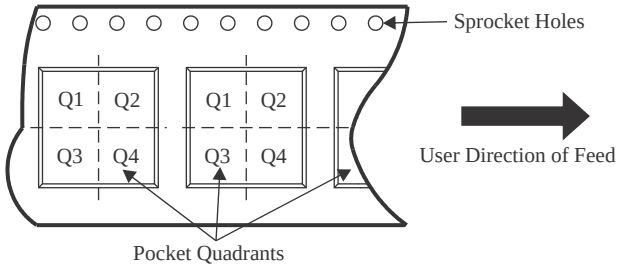


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

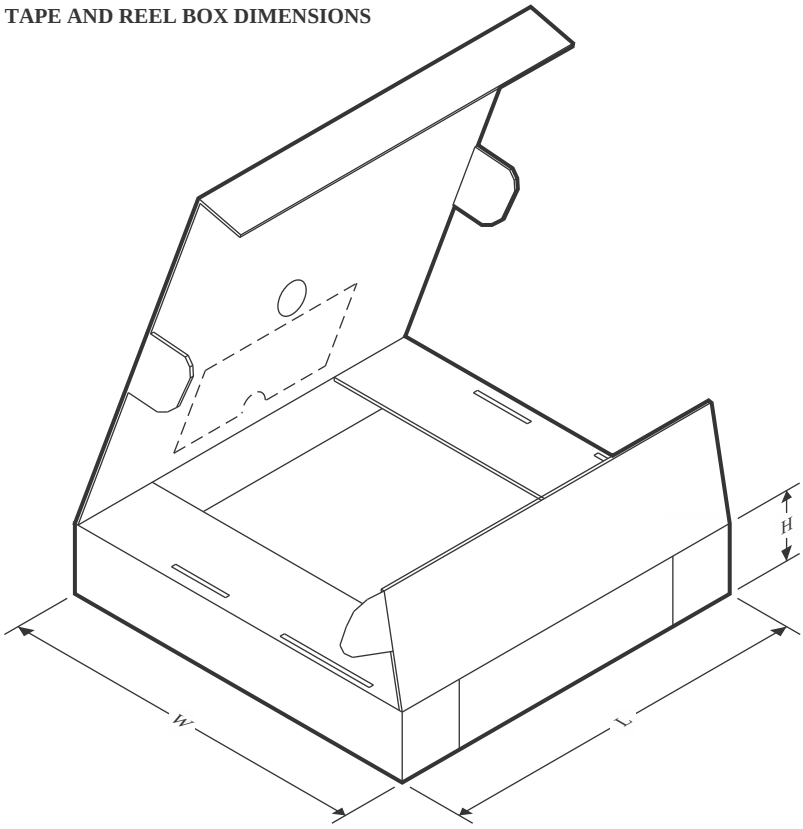
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2241UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2251UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA241UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA251UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4241UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4251UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

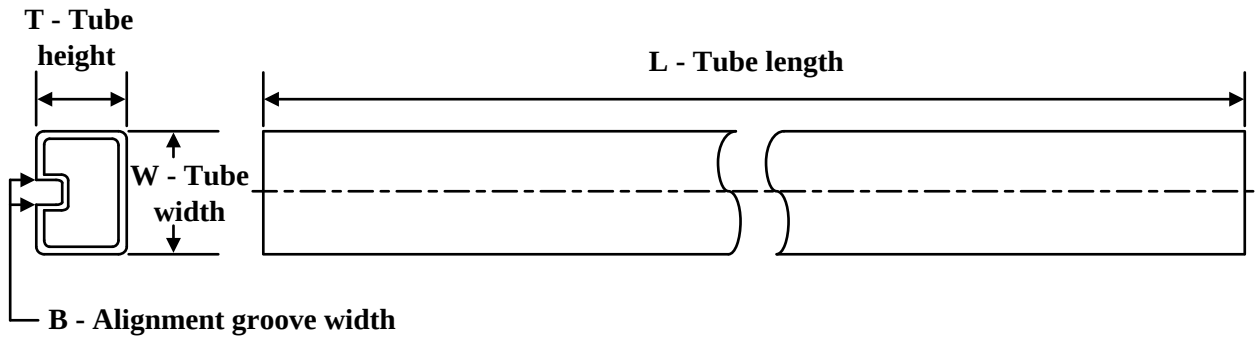
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2241UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2251UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA241UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA251UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA4241UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0
OPA4251UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0

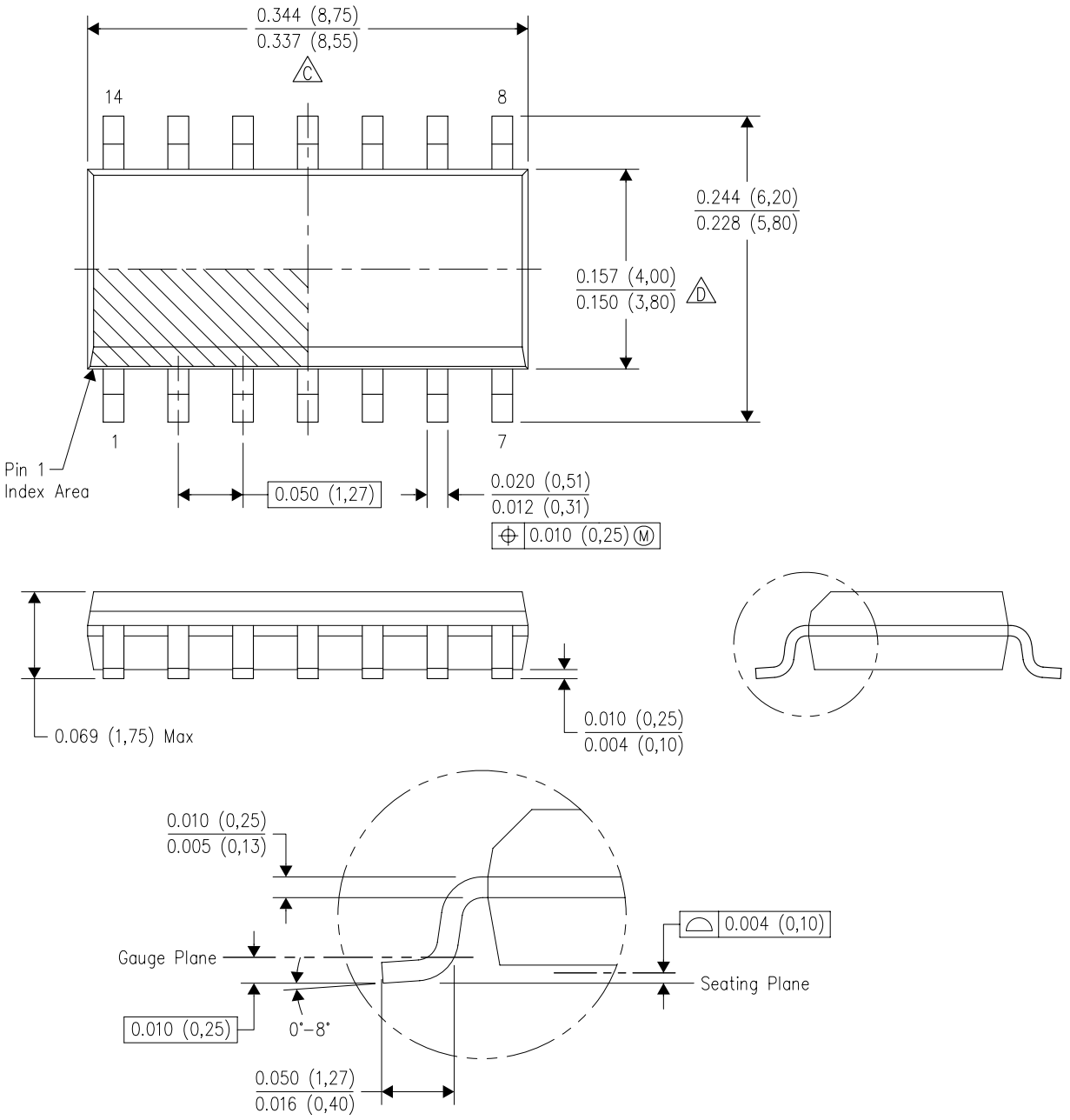
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2241PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2241PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA2241UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2241UAG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA2251PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2251PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA2251UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2251UAG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA241PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA241PAG4	P	PDIP	8	50	506	13.97	11230	4.32
OPA241UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA241UAG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA251UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA4241PA	N	PDIP	14	25	506	13.97	11230	4.32
OPA4241UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4251UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4251UAG4	D	SOIC	14	50	506.6	8	3940	4.32

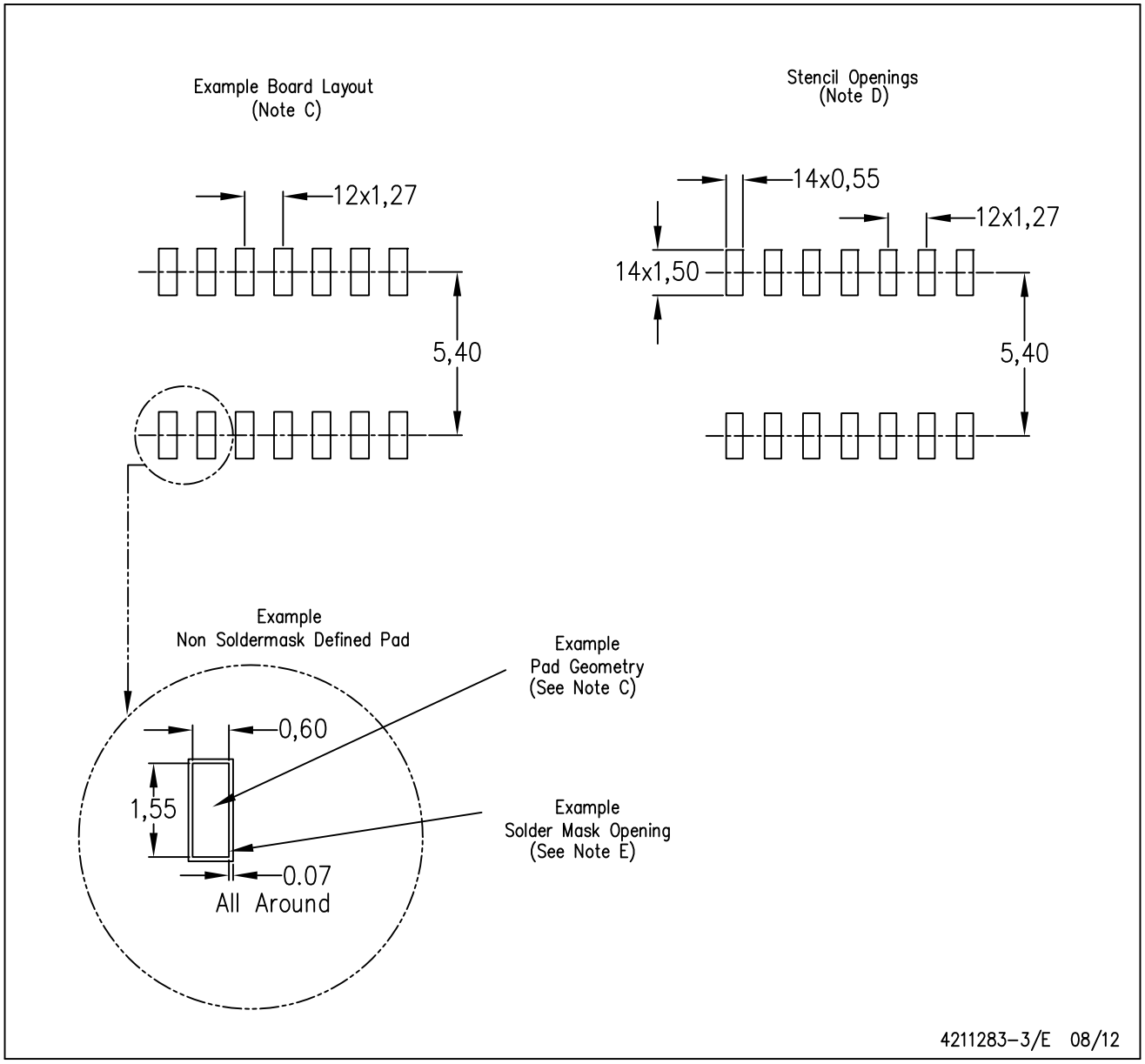
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



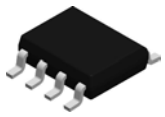
4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

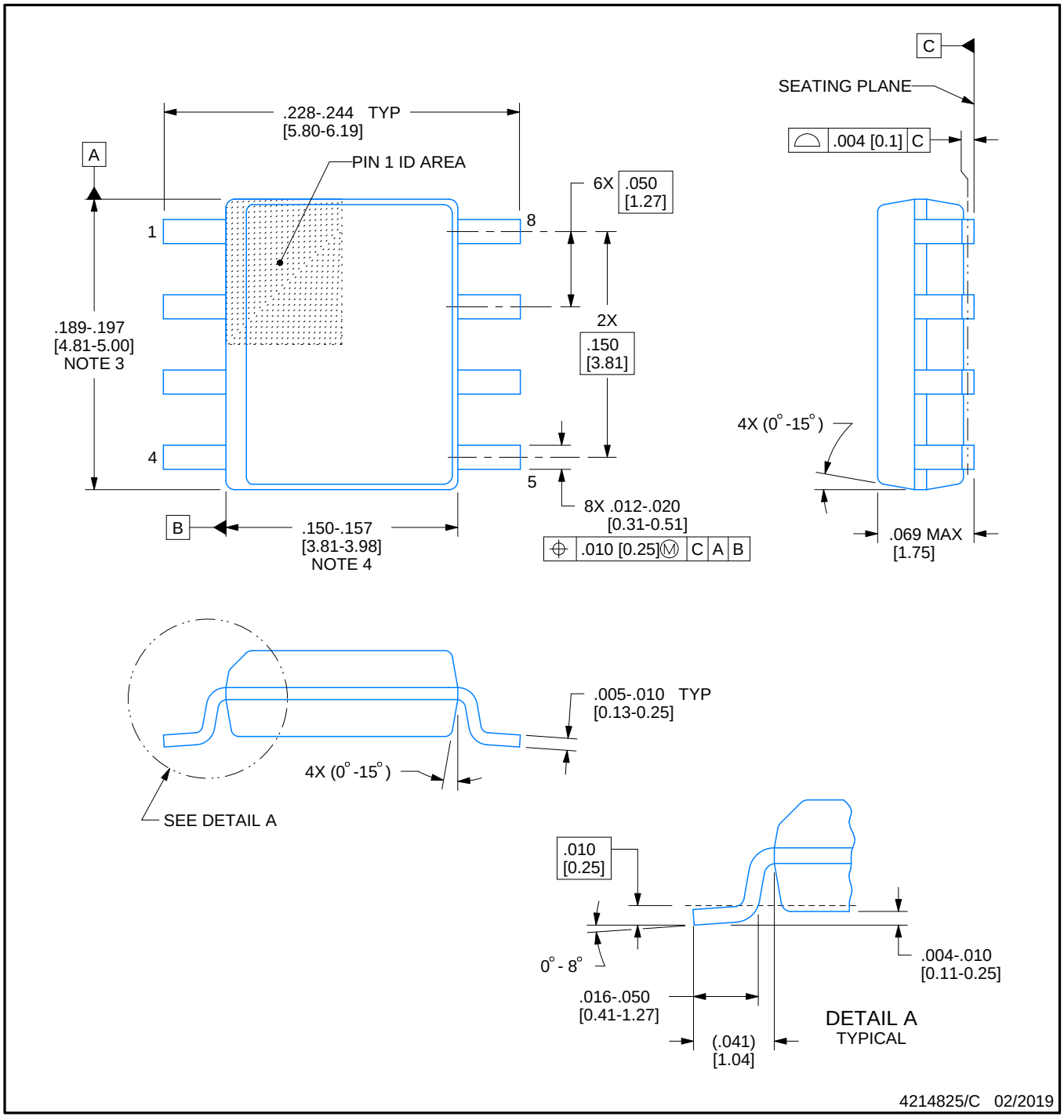


PACKAGE OUTLINE

D0008A

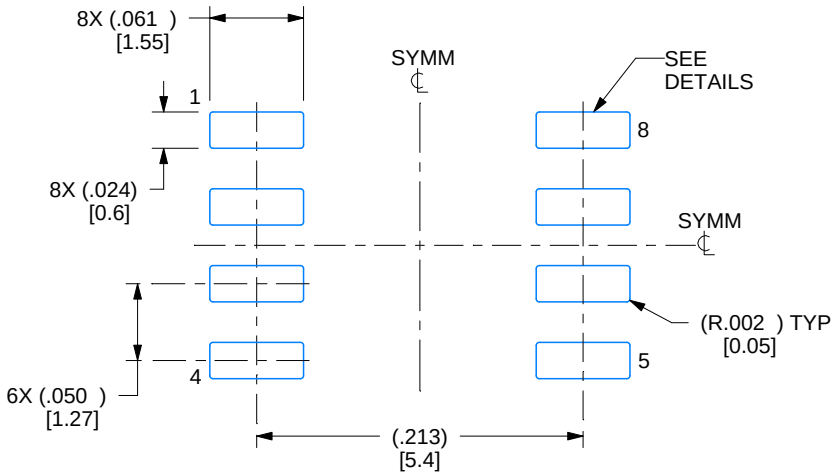
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

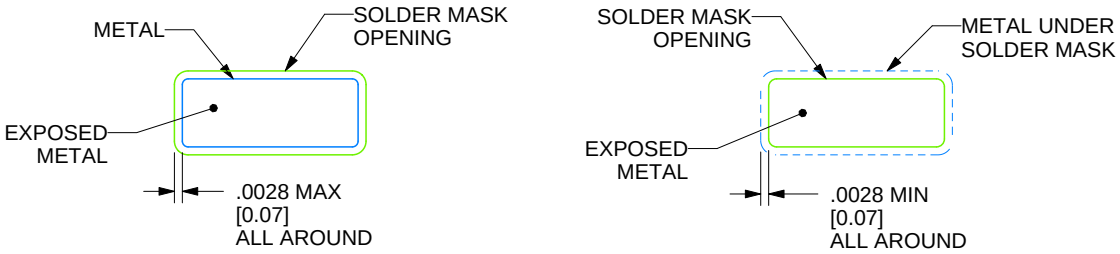


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

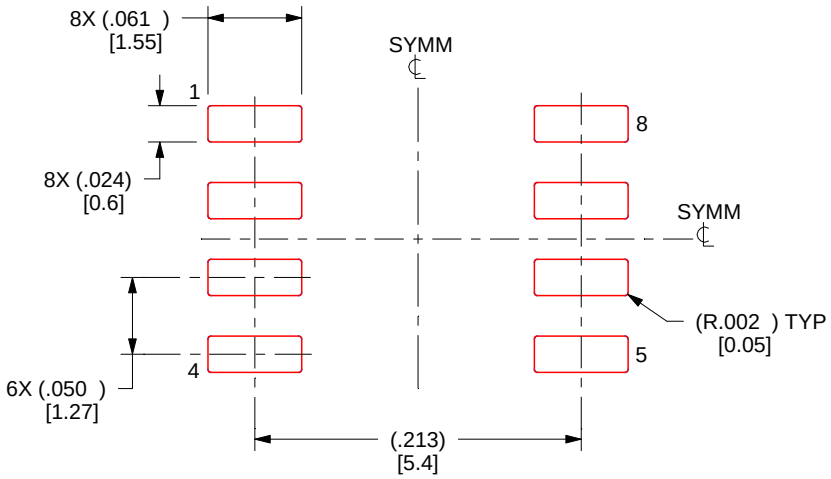
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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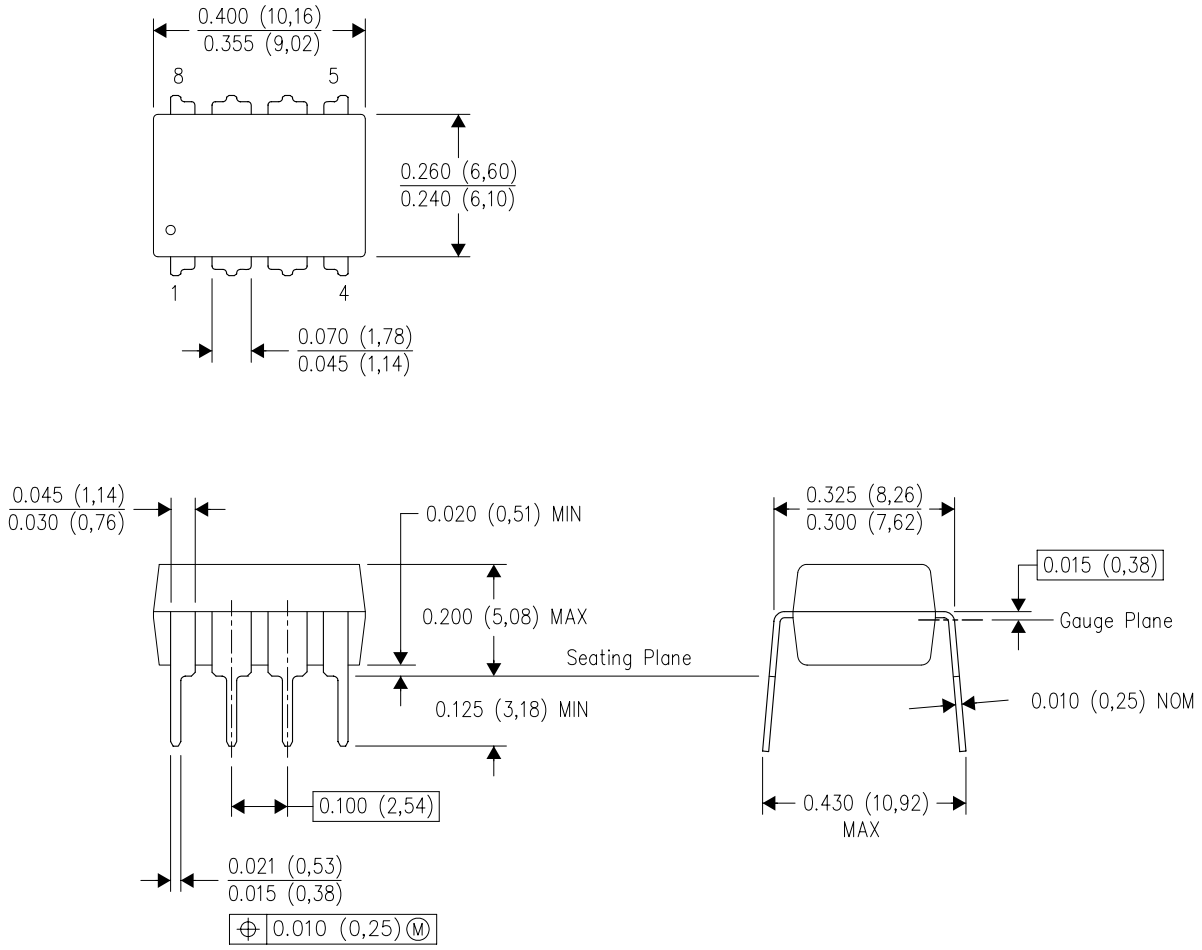
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

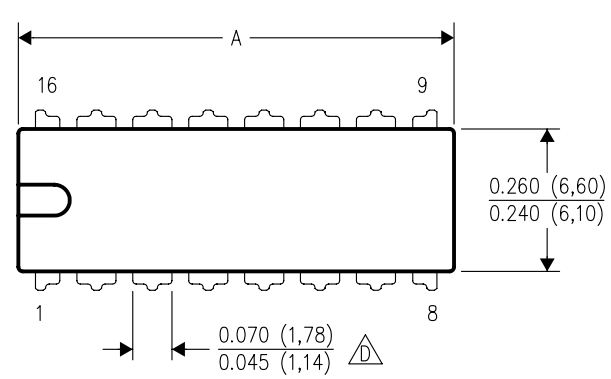


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

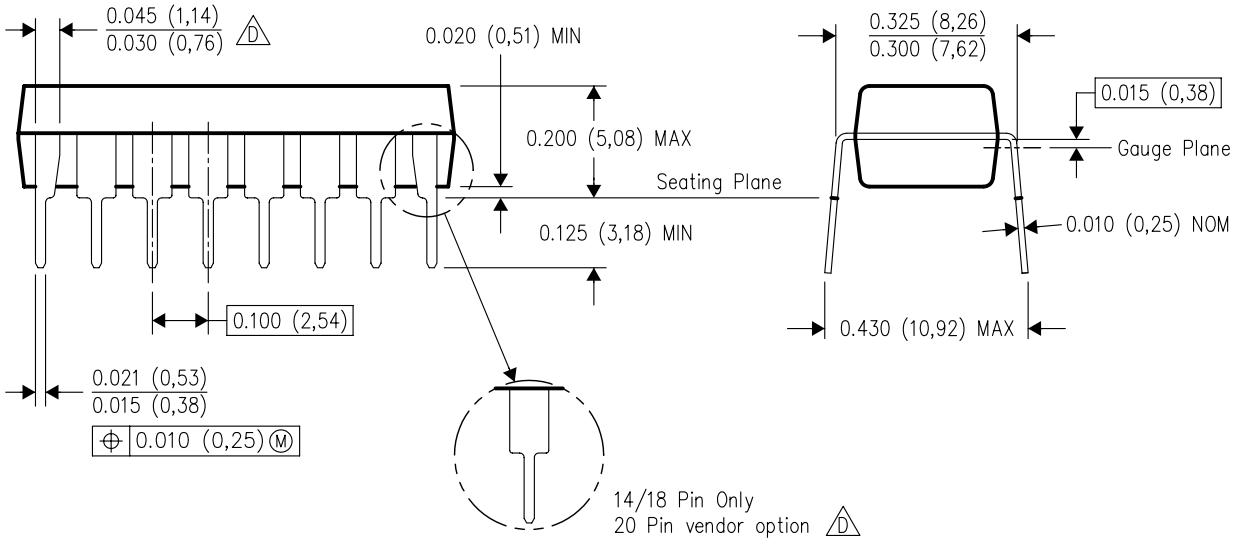
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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