FEATURES
- LOW OFFSET VOLTAGE: 5μV (max)
- ZERO DRIFT: 0.05μV/°C (max)
- QUIESCENT CURRENT: 285µA
- SINGLE-SUPPLY OPERATION
- SINGLE AND DUAL VERSIONS
- SHUTDOWN
- MicroSIZE PACKAGES

APPLICATIONS
- TRANSDUCER APPLICATIONS
- TEMPERATURE MEASUREMENT
- ELECTRONIC SCALES
- MEDICAL INSTRUMENTATION
- BATTERY-POWERED INSTRUMENTS
- HANDHELD TEST EQUIPMENT

DESCRIPTION
The OPA334 and OPA335 series of CMOS operational amplifiers use auto-zeroing techniques to simultaneously provide very low offset voltage (5μV max), and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high input impedance and rail-to-rail output swing. Single or dual supplies as low as +2.7V (±1.35V) and up to +5.5V (±2.75V) may be used. These op amps are optimized for low-voltage, single-supply operation.

The OPA334 family includes a shutdown mode. Under logic control, the amplifiers can be switched from normal operation to a standby current of 2µA. When the Enable pin is connected high, the amplifier is active. Connecting Enable low disables the amplifier, and places the output in a high-impedance state.

The OPA334 (single version with shutdown) comes in MicroSIZE SOT23-6. The OPA335 (single version without shutdown) is available in SOT23-5, and SO-8. The OPA2334 (dual version with shutdown) comes in MicroSIZE MSOP-10. The OPA2335 (dual version without shutdown) is offered in the MSOP-8 and SO-8 packages. All versions are specified for operation from –40°C to +125°C.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.
### ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE/ORDERING INFORMATION

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>PACKAGE-LEAD</th>
<th>PACKAGE DESIGNATOR(1)</th>
<th>SPECIFIED TEMPERATURE RANGE</th>
<th>PACKAGE MARKING</th>
<th>ORDERING NUMBER</th>
<th>TRANSPORT MEDIA, QUANTITY</th>
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**NOTES:** (1) For the most current specifications and package information, refer to our web site at www.ti.com.

### PIN CONFIGURATIONS

**OPA335**

![Pin Configuration Diagram](image)

**OPA334**

![Pin Configuration Diagram](image)

**OPA2334**

![Pin Configuration Diagram](image)

**OPA2335**

![Pin Configuration Diagram](image)

**NOTES:** (1) NC indicates no internal connection. (2) Pin 1 of the SOT23-6 is determined by orienting the package marking as indicated in the diagram.
ELECTRICAL CHARACTERISTICS

**Boldface limits apply over the specified temperature range, \( T_A = -40^\circ C \) to \( +125^\circ C \).**

At \( T_A = +25^\circ C, V_S = +5V, R_L = 10k\Omega \) connected to \( V_S/2 \), and \( V_{OUT} = V_S/2 \), unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
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<th>OPA2334AI, OPA2335AI</th>
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<td>( V_{OS} ) vs Temperature ( V_{CM} = V_S/2 )( T_A = -40^\circ C ) to ( +125^\circ C )</td>
<td>( \pm 0.02 )</td>
<td>( +0.05 )</td>
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<td>( I_B ) vs Temperature ( V_{CM} = V_S/2 )</td>
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<td>( \pm 200 )</td>
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<tr>
<td><strong>NOISE</strong></td>
<td>( \eta_n ) vs Power Supply</td>
<td>( 1.4 )</td>
<td>( \mu V_p/pA )</td>
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<tr>
<td><strong>INPUT VOLTAGE RANGE</strong></td>
<td>( V_{CM} ) vs Power Supply ( V_{CM} = 0 )</td>
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<td>( 130 )</td>
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<td>( pF )</td>
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<tr>
<td><strong>OPEN-LOOP GAIN</strong></td>
<td>( A_{OL} ) vs Power Supply</td>
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<td>( 130 )</td>
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<tr>
<td><strong>FREQUENCY RESPONSE</strong></td>
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<td>MHz</td>
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<td><strong>OUTPUT</strong></td>
<td>Voltage Output Swing from Rail</td>
<td>( 50mV )</td>
<td>( 100 )</td>
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<tr>
<td><strong>SHUTDOWN</strong></td>
<td>( t_{OFF} ) (shutdown) ( V_L )</td>
<td>( +0.8 )</td>
<td>V</td>
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<tr>
<td><strong>POWER SUPPLY</strong></td>
<td>Current ( I_D )</td>
<td>( 2.7 )</td>
<td>V</td>
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<tr>
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<td>Specified Range ( \theta_J )</td>
<td>( -40 )</td>
<td>°C</td>
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</table>

Notes: (1) 500-hour life test at 150°C demonstrated randomly distributed variation approximately equal to measurement repeatability of \( 1\mu V \). (2) Device requires one complete cycle to return to \( V_{OS} \) accuracy.
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ C$, $V_S = +5V$, $R_L = 10k\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

INPUT BIAS CURRENT vs TEMPERATURE

QUIESCENT CURRENT (per channel) vs TEMPERATURE

V S  = +5.5V

V S  = +2.7V

V S  = +5.5V

V S  = +2.7V
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ C$, $V_S = +5V$, $R_L = 10k\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

**OPEN-LOOP GAIN/PHASE vs FREQUENCY**

- $A_V$ (dB)
  - 140
  - 120
  - 100
  - 80
  - 60
  - 40
  - 20
  - 0
  - $-20$
- Phase (°)
  - $-80$
  - $-90$
  - $-100$
  - $-110$
  - $-120$
  - $-130$
  - $-140$
  - $-150$
  - $-160$
- Frequency (Hz)
  - 0.1
  - 1
  - 10
  - 100
  - 1k
  - 10k
  - 100k
  - 1M
  - 10M

**LARGE-SIGNAL RESPONSE**

- $G = -1$
- $C_L = 300pF$
- Time (5μs/div)
- Output Voltage (1V/div)

**SMALL-SIGNAL RESPONSE**

- $G = +1$
- $C_L = 50pF$
- Time (5μs/div)
- Output Voltage (50mV/div)

**POSITIVE OVER-VOLTAGE RECOVERY**

- Input
- Output
- Time (25μs/div)
- 200mV/div
- 1V/div

**NEGATIVE OVER-VOLTAGE RECOVERY**

- Input
- Output
- Time (25μs/div)
- 200mV/div
- 1V/div

**COMMON-MODE REJECTION vs FREQUENCY**

- Common-Mode Rejection (dB)
  - 1
  - 140
  - 120
  - 100
  - 80
  - 60
  - 40
  - 20
  - 0
- Frequency (Hz)
  - 0.1
  - 1
  - 10
  - 100
  - 1k
  - 10k
  - 100k
  - 1M
  - 10M
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ C$, $V_S = +5V$, $R_L = 10k\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

**POWER-SUPPLY REJECTION RATIO vs FREQUENCY**

**NOISE vs FREQUENCY**

**SAMPLING FREQUENCY vs TEMPERATURE**

**SAMPLING FREQUENCY vs SUPPLY VOLTAGE**

**0.01Hz TO 10Hz NOISE**

**SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE**

$V_S = 2.7V$ to $5V$

$R_L = 10k\Omega$

**POWER-SUPPLY REJECTION RATIO**

**Frequency (Hz)**

$10$ to $1000$ kHz

**Noise (nV/√Hz)**

$1000$ to $10$ nV/√Hz

**Frequency (Hz)**

$1$ to $100$ kHz

**Frequency (kHz)**

$2.7$ to $5.5$

**Supply Voltage (V)**

$–10$ to $+50$ kHz

**Temperature (°C)**

$–40$ to $125$

**Sampling Frequency (kHz)**

$8$ to $13$

**Sampling Frequency (kHz)**

$50$ to $55$

**Overload (%)**

$0$ to $50$

**Load Capacitance (pF)**

$10$ to $1000$ pF
APPLICATIONS INFORMATION

The OPA334 and OPA335 series op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and very low drift over time and temperature.

Good layout practice mandates use of a 0.1 μF capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals.

- Use low thermoelectric-coefficient connections (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat-sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 μV/°C or higher, depending on materials used.

OPERATING VOLTAGE

The OPA334 and OPA335 series op amps operate over a power-supply range of +2.7V to +5.5V (±1.35V to ±2.75V). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

OPA334 ENABLE FUNCTION

The enable/shutdown digital input is referenced to the V– supply voltage of the amp. A logic high enables the op amp. A valid logic high is defined as > 75% of the total supply voltage. The valid logic high signal can be up to 5.5V above the negative supply, independent of the positive supply voltage. A valid logic low is defined as < 0.8V above the V– supply pin. If dual or split power supplies are used, be sure that logic input signals are properly referred to the negative supply voltage. The Enable pin must be connected to a valid high or low voltage, or driven, not left open circuit.

The logic input is a high-impedance CMOS input, with separate logic inputs provided on the dual version. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life.

The enable time is 150 μs, which includes one full auto-zero cycle required by the amplifier to return to VOS accuracy. Prior to this time, the amplifier functions properly, but with unspecified offset voltage.

Disable time is 1 μs. When disabled, the output assumes a high-impedance state. This allows the OPA334 to be operated as a gated amplifier, or to have the output multiplexed onto a common analog output bus.

INPUT VOLTAGE

The input common-mode range extends from (V–) – 0.1V to (V+) – 1.5V. For normal operation, the inputs must be limited to this range. The common-mode rejection ratio is only valid within the valid input common-mode range. A lower supply voltage results in lower input common-mode range; therefore, attention to these values must be given when selecting the input bias voltage. For example, when operating on a single 3V power supply, common-mode range is from 0.1V below ground to half the power-supply voltage.
Normally, input bias current is approximately 70pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supplies can be tolerated if the input current is limited to 10mA. This is easily accomplished with an input resistor, as shown in Figure 1.

**INTERNAL OFFSET CORRECTION**

The OPA334 and OPA335 series op amps use an auto-zero topology with a time-continuous 2MHz op amp in the signal path. This amplifier is zero-corrected every 100us using a proprietary technique. Upon power-up, the amplifier requires one full auto-zero cycle of approximately 100us to achieve specified \( V_{OS} \) accuracy. Prior to this time, the amplifier functions properly but with unspecified offset voltage.

This design has remarkably little aliasing and noise. Zero correction occurs at a 10kHz rate, but there is virtually no fundamental noise energy present at that frequency. For all practical purposes, any glitches have energy at 20MHz or higher and are easily filtered, if required. Most applications are not sensitive to such high-frequency noise, and no filtering is required.

Unity-gain operation demands that the auto-zero circuitry correct for common-mode rejection errors of the main amplifier. Because these errors can be larger than 0.01% of a full-scale input step change, one calibration cycle (100\( \mu \)s) can be required to achieve full accuracy. This behavior is shown in the typical characteristic section, see *Settling Time vs Closed-Loop Gain*.

**ACHIEVING OUTPUT SWING TO THE OP AMP’S NEGATIVE RAIL**

Some applications require output voltage swing from 0V to a positive full-scale voltage (such as +2.5V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach ground. The output of the OPA334 or OPA335 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires use of another resistor and an additional, more negative, power supply than the op amp’s negative supply. A pull-down resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 2.

**LAYOUT GUIDELINES**

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1\( \mu \)F capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI (electromagnetic-interference) susceptibility.
FIGURE 3. Temperature Measurement Circuit.


FIGURE 5. Single Op Amp Bridge Amplifier Circuits.
FIGURE 6. Dual Op Amp IA Bridge Amplifier.

FIGURE 7. Low-Side Current Measurement.
FIGURE 8. High Dynamic Range Transimpedance Amplifier.

NOTE: (1) Pull-down resistors to allow accurate swing to 0V.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
A. Falls within JEDEC MO-187
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion.  
D. Falls within JEDEC MO-178
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187
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<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
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<th>Eco Plan</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
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<td>250</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
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<td>-40 to 125</td>
<td>OPA 335</td>
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</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA2335:

Military: OPA2335M

NOTE: Qualified Version Definitions:

Military - QML certified for Military and Defense Applications
### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

![Reel Dimensions Diagram]

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

![Quadrant Assignments Diagram]

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
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## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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<td>2500</td>
<td>853.0</td>
<td>449.0</td>
<td>35.0</td>
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.
NOTES:
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.
5. Reference JEDEC MO-178.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
EXAMPLE STENCIL DESIGN

DBV0006A
SOT-23 - 1.45 mm max height
SMALL OUTLINE TRANSISTOR

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
   > Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
   > Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.
NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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