1 Features
• Unity-Gain Bandwidth: 250 MHz
• Wide Bandwidth: 100-MHz GBW
• High Slew Rate: 150 V/µs
• Low Noise: 6.5 nV/√Hz
• Rail-to-Rail I/O
• High Output Current: > 100 mA
• Excellent Video Performance:
  – Differential Gain: 0.02%, Differential Phase: 0.09°
  – 0.1-dB Gain Flatness: 40 MHz
• Low Input Bias Current: 3 pA
• Quiescent Current: 4.9 mA
• Thermal Shutdown
• Supply Range: 2.5 V to 5.5 V
• MicroSIZE and PowerPAD™ Packages

2 Applications
• Video Processing
• Ultrasound
• Optical Networking, Tunable Lasers
• Photodiode Transimpedance Amps
• Active Filters
• High-Speed Integrators
• Analog-to-Digital (A/D) Converter Input Buffers
• Digital-to-Analog (D/A) Converter Output Amplifiers
• Barcode Scanners
• Communications

3 Description
The OPAx354 series of high-speed, voltage-feedback CMOS operational amplifiers are designed for video and other applications requiring wide bandwidth. They are unity-gain stable and can drive large output currents. Differential gain is 0.02% and differential phase is 0.09°. Quiescent current is only 4.9 mA per channel.

The OPAx354 series of op amps are optimized for operation on single or dual supplies as low as 2.5 V (±1.25 V) and up to 5.5 V (±2.75 V). Common-mode input range extends beyond the supplies. The output swing is within 100 mV of the rails, supporting wide dynamic range.

For applications requiring the full 100-mA continuous output current, single and dual 8-pin HSOP PowerPAD versions are available.

The single version (OPA354) is available in the tiny 5-pin SOT-23 and 8-pin HSOP PowerPAD packages. The dual version (OPA2354) comes in the miniature 8-pin VSSOP and 8-pin HSOP PowerPAD packages. The quad version (OPA4354) is offered in 14-pin TSSOP and 14-pin SOIC packages.

Multichannel version features completely independent circuitry for lowest crosstalk and freedom from interaction. All features are specified over the extended –40°C to +125°C temperature range.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA354</td>
<td>HSOP (8)</td>
<td>4.89 mm x 3.90 mm</td>
</tr>
<tr>
<td></td>
<td>SOT-23 (5)</td>
<td>2.90 mm x 1.60 mm</td>
</tr>
<tr>
<td>OPA2354</td>
<td>VSSOP (8)</td>
<td>3.00 mm x 3.00 mm</td>
</tr>
<tr>
<td></td>
<td>HSOP (8)</td>
<td>4.89 mm x 3.90 mm</td>
</tr>
<tr>
<td>OPA4354</td>
<td>SOIC (14)</td>
<td>8.65 mm x 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>TSSOP (14)</td>
<td>5.00 mm x 4.40 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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2 Applications .......................................................... 1
3 Description ............................................................ 1
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   7.2 ESD Ratings ....................................................... 6
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4 Revision History

Changes from Revision F (June 2016) to Revision G

- Deleted table note about input pins and input signals from Absolute Maximum Ratings table ................................. 6

Changes from Revision E (March 2002) to Revision F

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ........................................... 1
- Deleted Package/Ordering Information table, see POA at the end of the data sheet .................................................... 1
- Renamed OPAx354 Related Products table to Device Comparison Table ................................................................. 3
5  Device Comparison Table

<table>
<thead>
<tr>
<th>FEATURES</th>
<th>PRODUCT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shutdown Version of OPAx354 Family</td>
<td>OPAx357</td>
</tr>
<tr>
<td>200-MHz GBW, Rail-to-Rail Output, CMOS, Shutdown</td>
<td>OPAx355</td>
</tr>
<tr>
<td>200-MHz GBW, Rail-to-Rail Output, CMOS</td>
<td>OPAx356</td>
</tr>
<tr>
<td>38-MHz GBW, Rail-to-Rail Input/Output, CMOS</td>
<td>OPAx350/OPA353</td>
</tr>
<tr>
<td>75-MHz BW G = 2, Rail-to-Rail Output</td>
<td>OPA2631</td>
</tr>
<tr>
<td>150-MHz BW G = 2, Rail-to-Rail Output</td>
<td>OPA2634</td>
</tr>
<tr>
<td>100-MHz BW, Differential Input/Output, 3.3-V Supply</td>
<td>THS412x</td>
</tr>
</tbody>
</table>

6  Pin Configuration and Functions

Pin Functions: OPA354

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>–IN</td>
<td>I</td>
<td>Inverting input</td>
</tr>
<tr>
<td>+IN</td>
<td>I</td>
<td>Noninverting input</td>
</tr>
<tr>
<td>NC</td>
<td>—</td>
<td>No internal connection (can be left floating)</td>
</tr>
<tr>
<td>OUT</td>
<td>O</td>
<td>Output</td>
</tr>
<tr>
<td>V–</td>
<td>—</td>
<td>Negative (lowest) supply</td>
</tr>
<tr>
<td>V+</td>
<td>—</td>
<td>Positive (highest) supply</td>
</tr>
<tr>
<td>SOT-23</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>1, 5, 8</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>HSOP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>7</td>
<td></td>
</tr>
</tbody>
</table>
(1) PowerPAD must be connected to $V_-$ or left floating.

## Pin Functions: OPA2354

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT A</td>
<td>O</td>
<td>Output, channel A</td>
</tr>
<tr>
<td>OUT B</td>
<td>O</td>
<td>Output, channel B</td>
</tr>
<tr>
<td>V–</td>
<td></td>
<td>Negative (lowest) supply</td>
</tr>
<tr>
<td>V+</td>
<td></td>
<td>Positive (highest) supply</td>
</tr>
<tr>
<td>–IN A</td>
<td>I</td>
<td>Inverting input, channel A</td>
</tr>
<tr>
<td>+IN A</td>
<td>I</td>
<td>Noninverting input, channel A</td>
</tr>
<tr>
<td>–IN B</td>
<td>I</td>
<td>Inverting input, channel B</td>
</tr>
<tr>
<td>+IN B</td>
<td>I</td>
<td>Noninverting input, channel B</td>
</tr>
</tbody>
</table>
Pin Functions: OPA4354

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>–IN A</td>
<td>2</td>
<td>I Inverting input, channel A</td>
</tr>
<tr>
<td>+IN A</td>
<td>3</td>
<td>I Noninverting input, channel A</td>
</tr>
<tr>
<td>–IN B</td>
<td>6</td>
<td>I Inverting input, channel B</td>
</tr>
<tr>
<td>+IN B</td>
<td>5</td>
<td>I Noninverting input, channel B</td>
</tr>
<tr>
<td>–IN C</td>
<td>9</td>
<td>I Inverting input, channel C</td>
</tr>
<tr>
<td>+IN C</td>
<td>10</td>
<td>I Noninverting input, channel C</td>
</tr>
<tr>
<td>–IN D</td>
<td>13</td>
<td>I Inverting input, channel D</td>
</tr>
<tr>
<td>+IN D</td>
<td>12</td>
<td>I Noninverting input, channel D</td>
</tr>
<tr>
<td>OUT A</td>
<td>1</td>
<td>O Output, channel A</td>
</tr>
<tr>
<td>OUT B</td>
<td>7</td>
<td>O Output, channel B</td>
</tr>
<tr>
<td>OUT C</td>
<td>8</td>
<td>O Output, channel C</td>
</tr>
<tr>
<td>OUT D</td>
<td>14</td>
<td>O Output, channel D</td>
</tr>
<tr>
<td>V–</td>
<td>11</td>
<td>— Negative (lowest) supply</td>
</tr>
<tr>
<td>V+</td>
<td>4</td>
<td>— Positive (highest) supply</td>
</tr>
</tbody>
</table>
7 Specifications

7.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Voltage</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply voltage, V+ to V−</td>
<td>7.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Signal input terminals</td>
<td>(V−) − (0.5)</td>
<td>(V+) + 0.5</td>
<td></td>
</tr>
<tr>
<td><strong>Current</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signal input terminals</td>
<td>−10</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Output short circuit(2)</td>
<td>Continuous</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Temperature</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating, T_a</td>
<td>−55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Junction, T_J</td>
<td>150</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage, T_stg</td>
<td>−65</td>
<td>150</td>
<td></td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th></th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{(ESD)} ESD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Electrostatic discharge</td>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)</td>
<td>±2000</td>
</tr>
<tr>
<td></td>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(2)</td>
<td>±250</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{S} Supply voltage, V− to V+</td>
<td>2.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Specified temperature</td>
<td>−40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>
### 7.4 Thermal Information: OPA354

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>OPA354</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DBV (SOT-23)</td>
<td>DDA (HSOP)</td>
</tr>
<tr>
<td></td>
<td>5 PINS</td>
<td>8 PINS</td>
</tr>
<tr>
<td>$R_{\theta JA}$</td>
<td>Junction-to-ambient thermal resistance</td>
<td>216.3</td>
</tr>
<tr>
<td>$R_{\theta JC(top)}$</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>84.3</td>
</tr>
<tr>
<td>$R_{\theta JB}$</td>
<td>Junction-to-board thermal resistance</td>
<td>43.1</td>
</tr>
<tr>
<td>$\psi_{JT}$</td>
<td>Junction-to-top characterization parameter</td>
<td>3.8</td>
</tr>
<tr>
<td>$\psi_{JB}$</td>
<td>Junction-to-board characterization parameter</td>
<td>42.3</td>
</tr>
<tr>
<td>$R_{\theta JC(bot)}$</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>—</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](https://www.ti.com) application report.

### 7.5 Thermal Information: OPA2354

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>OPA2354</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DDA (HSOP)</td>
<td>DGK (VSSOP)</td>
</tr>
<tr>
<td></td>
<td>8 PINS</td>
<td>8 PINS</td>
</tr>
<tr>
<td>$R_{\theta JA}$</td>
<td>Junction-to-ambient thermal resistance</td>
<td>40.6</td>
</tr>
<tr>
<td>$R_{\theta JC(top)}$</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>46</td>
</tr>
<tr>
<td>$R_{\theta JB}$</td>
<td>Junction-to-board thermal resistance</td>
<td>20.7</td>
</tr>
<tr>
<td>$\psi_{JT}$</td>
<td>Junction-to-top characterization parameter</td>
<td>5.6</td>
</tr>
<tr>
<td>$\psi_{JB}$</td>
<td>Junction-to-board characterization parameter</td>
<td>20.6</td>
</tr>
<tr>
<td>$R_{\theta JC(bot)}$</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>2.5</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](https://www.ti.com) application report.

### 7.6 Thermal Information: OPA4354

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>OPA4354</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>D (SOIC)</td>
<td>PW (TSSOP)</td>
</tr>
<tr>
<td></td>
<td>14 PINS</td>
<td>14 PINS</td>
</tr>
<tr>
<td>$R_{\theta JA}$</td>
<td>Junction-to-ambient thermal resistance</td>
<td>83.8</td>
</tr>
<tr>
<td>$R_{\theta JC(top)}$</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>70.7</td>
</tr>
<tr>
<td>$R_{\theta JB}$</td>
<td>Junction-to-board thermal resistance</td>
<td>59.5</td>
</tr>
<tr>
<td>$\psi_{JT}$</td>
<td>Junction-to-top characterization parameter</td>
<td>11.6</td>
</tr>
<tr>
<td>$\psi_{JB}$</td>
<td>Junction-to-board characterization parameter</td>
<td>37.7</td>
</tr>
<tr>
<td>$R_{\theta JC(bot)}$</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>—</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](https://www.ti.com) application report.
7.7 Electrical Characteristics: \( V_S = 2.7 \) V to 5.5 V (Single-Supply)

at \( T_A = 25^\circ\text{C}, R_F = 0 \, \Omega, R_L = 1 \, k\Omega \), and connected to \( V_S / 2 \), (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFFSET VOLTAGE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OS} )</td>
<td>Input offset voltage</td>
<td>( V_S = 5 ) V ( T_A = 25^\circ\text{C} )</td>
<td>±2</td>
<td>±8</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = 5 ) V ( T_A = -40^\circ\text{C} ) to (+125^\circ\text{C} )</td>
<td>±10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( dV_{OS}/dT )</td>
<td>Input offset voltage vs temperature</td>
<td>( V_S = 5 ) V ( T_A = -40^\circ\text{C} ) to (+125^\circ\text{C} )</td>
<td>±4</td>
<td></td>
<td>µV/^\circ\text{C}</td>
</tr>
<tr>
<td>PSRR</td>
<td>Input offset voltage vs power supply</td>
<td>( V_S = 2.7 ) V to 5.5 V ( V_{CM} = (V_S / 2) - 0.55 ) V ( T_A = -40^\circ\text{C} ) to (+125^\circ\text{C} )</td>
<td>±200</td>
<td>±800</td>
<td>µV/V</td>
</tr>
<tr>
<td>INPUT BIAS CURRENT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_B )</td>
<td>Input bias current</td>
<td></td>
<td>3</td>
<td>±50</td>
<td>pA</td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>Input offset current</td>
<td></td>
<td>±1</td>
<td>±50</td>
<td>pA</td>
</tr>
<tr>
<td>NOISE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( e_n )</td>
<td>Input voltage noise density</td>
<td>( f = 1 ) MHz</td>
<td>6.5</td>
<td></td>
<td>nV/√Hz</td>
</tr>
<tr>
<td>( i_n )</td>
<td>Current noise density</td>
<td>( f = 1 ) MHz</td>
<td>50</td>
<td></td>
<td>fA/√Hz</td>
</tr>
<tr>
<td>INPUT VOLTAGE RANGE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{CM} )</td>
<td>Common-mode voltage</td>
<td>( (V^-) - 0.1 )</td>
<td>( (V^+) + 0.1 )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-mode rejection ratio</td>
<td>( V_S = 5.5 ) V ( T_A = 25^\circ\text{C} )</td>
<td>66</td>
<td>80</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = 5.5 ) V ( T_A = -40^\circ\text{C} ) to (+125^\circ\text{C} )</td>
<td>64</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = 5.5 ) V ( T_A = -40^\circ\text{C} ) to (+125^\circ\text{C} ) ( V_{CM} &lt; 5.6 ) V</td>
<td>56</td>
<td>68</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = 5.5 ) V ( T_A = -40^\circ\text{C} ) to (+125^\circ\text{C} ) ( V_{CM} &lt; 3.5 ) V</td>
<td>55</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INPUT IMPEDANCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential</td>
<td></td>
<td>( 10^{13}</td>
<td></td>
<td>2 )</td>
<td>( \Omega</td>
</tr>
<tr>
<td>Common-mode</td>
<td></td>
<td>( 10^{13}</td>
<td></td>
<td>2 )</td>
<td>( \Omega</td>
</tr>
<tr>
<td>OPEN-LOOP GAIN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( A_{OL} )</td>
<td>Open-loop gain</td>
<td>( V_S = 5 ) V ( T_A = 25^\circ\text{C} )</td>
<td>94</td>
<td>110</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_S = 5 ) V ( T_A = -40^\circ\text{C} ) to (+125^\circ\text{C} ) ( V_{D} &lt; 4.7 ) V</td>
<td>90</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FREQUENCY RESPONSE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_{3dB} )</td>
<td>Small-signal bandwidth</td>
<td>At ( G = +1 ) ( V_O = 100 ) mVpp</td>
<td>250</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_F = 25 ) ( \Omega )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>At ( G = +2 ) ( V_O = 100 ) mVpp</td>
<td>90</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GBW</td>
<td>Gain-bandwidth product</td>
<td>( G = +10 )</td>
<td>100</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{0.1dB} )</td>
<td>Bandwidth for 0.1-dB gain flatness</td>
<td>At ( G = +2 ) ( V_O = 100 ) mVpp</td>
<td>40</td>
<td></td>
<td>MHz</td>
</tr>
</tbody>
</table>
Electrical Characteristics: $V_S = 2.7 \text{ V to } 5.5 \text{ V (Single-Supply)}$ (continued)

at $T_A = 25^\circ\text{C}$, $R_C = 0 \Omega$, $R_L = 1 \text{ k}\Omega$, and connected to $V_S / 2$, (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR Slew rate</td>
<td>$V_S = 5 \text{ V}, G = +1$, 4-V step</td>
<td>150</td>
<td></td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td></td>
<td>$V_S = 5 \text{ V}, G = +1$, 2-V step</td>
<td>130</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_S = 3 \text{ V}, G = +1$, 2-V step</td>
<td>110</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rise-and-fall time</td>
<td>At $G = +1$, $V_O = 200 \text{ mV}_{\text{PP}}, 10%$ to $90%$</td>
<td>2</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>At $G = +1$, $V_O = 2 \text{ V}_{\text{PP}}, 10%$ to $90%$</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Settling time</td>
<td>0.1%, $V_S = 5 \text{ V}, G = +1$, 2-V output step</td>
<td>30</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>0.01%, $V_S = 5 \text{ V}, G = +1$, 2-V output step</td>
<td>60</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overload recovery time</td>
<td>$V_{IN} \times \text{Gain} = V_S$</td>
<td>5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
Electrical Characteristics: $V_S = 2.7$ V to 5.5 V (Single-Supply) (continued)

at $T_A = 25^\circ C$, $R_F = 0 \, \Omega$, $R_L = 1 \, k\Omega$, and connected to $V_S / 2$, (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>FREQUENCY RESPONSE (CONTINUED)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Harmonic distortion</td>
<td>Second harmonic</td>
<td>$G = +1$, $f = 1 , MHz$, $V_O = 2 , V_{PP}$, $R_L = 200 , \Omega$, $V_{CM} = 1.5 , V$</td>
<td>$-75$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Third harmonic</td>
<td>$G = +1$, $f = 1 , MHz$, $V_O = 2 , V_{PP}$, $R_L = 200 , \Omega$, $V_{CM} = 1.5 , V$</td>
<td>$-83$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Differential gain error</td>
<td>NTSC, $R_L = 150 , \Omega$</td>
<td>0.02%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Differential phase error</td>
<td>NTSC, $R_L = 150 , \Omega$</td>
<td>0.09°</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Channel-to-channel crosstalk</td>
<td>OPA2354, $f = 5 , MHz$</td>
<td>$-100$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>OPA4354</td>
<td>$-84$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OUTPUT</td>
<td>Voltage output swing from rail</td>
<td>$V_S = 5 , V$, $R_L = 1 , k\Omega$, $A_{OL} &gt; 94 , dB$</td>
<td>$0.1$</td>
<td>$0.3$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = 25^\circ C$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = 5 , V$, $R_L = 1 , k\Omega$, $A_{OL} &gt; 90 , dB$</td>
<td></td>
<td></td>
<td>$0.4$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = -40^\circ C \ to \ +125^\circ C$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_O$</td>
<td>Output current, single, dual, quad$^{(1),(2)}$</td>
<td>$V_S = 5 , V$</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_S = 3 , V$</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Closed-loop output impedance</td>
<td>$f &lt; 100 , kHz$</td>
<td>0.05</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_O$</td>
<td>Open-loop output resistance</td>
<td></td>
<td>35</td>
<td></td>
<td></td>
</tr>
<tr>
<td>POWER SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_S$</td>
<td>Specified voltage</td>
<td></td>
<td>2.7</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Operating voltage</td>
<td></td>
<td>2.5</td>
<td>5.5</td>
<td></td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Quiescent current (per amplifier)</td>
<td>$T_A = 25^\circ C$, $V_S = 5 , V$ (enabled)</td>
<td>4.9</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_Q = 0$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_A = -40^\circ C \ to \ +125^\circ C$</td>
<td></td>
<td>7.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>THERMAL SHUTDOWN: JUNCTION TEMPERATURE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shutdown</td>
<td></td>
<td></td>
<td>160</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reset from shutdown</td>
<td></td>
<td></td>
<td>140</td>
<td></td>
<td></td>
</tr>
<tr>
<td>THERMAL RANGE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Specified</td>
<td></td>
<td></td>
<td>$-40$</td>
<td>125</td>
<td></td>
</tr>
<tr>
<td>Operating</td>
<td></td>
<td></td>
<td>$-55$</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>Storage</td>
<td></td>
<td></td>
<td>$-65$</td>
<td>150</td>
<td></td>
</tr>
</tbody>
</table>

$^{(1)}$ See typical characteristic curves, *Output Voltage Swing vs Output Current* (Figure 20 and Figure 22).

$^{(2)}$ Specified by design.
7.8 Typical Characteristics

at \( T_A = 25^\circ C, V_S = 5 \text{ V}, G = +1, R_F = 0 \Omega, R_L = 1 \text{ k}\Omega \), and connected to \( V_S / 2 \), (unless otherwise noted)
Typical Characteristics (continued)

at $T_A = 25°C$, $V_S = 5 \text{ V}$, $G = +1$, $R_F = 0 \Omega$, $R_L = 1 \text{ k}Ω$, and connected to $V_S / 2$, (unless otherwise noted)

**Figure 7. Harmonic Distortion vs Noninverting Gain**

**Figure 8. Harmonic Distortion vs Inverting Gain**

**Figure 9. Harmonic Distortion vs Frequency**

**Figure 10. Harmonic Distortion vs Load Resistance**

**Figure 11. Input Voltage and Current Noise Spectral Density vs Frequency**

**Figure 12. Frequency Response for Various $R_L$ Values**
Typical Characteristics (continued)

at $T_A = 25^\circ$C, $V_S = 5$ V, $G = +1$, $R_F = 0$ Ω, $R_L = 1$ kΩ, and connected to $V_S / 2$, (unless otherwise noted)

![Frequency Response for Various $C_L$ Values](image1)

![Recommended $R_S$ vs Capacitive Load](image2)

![Frequency Response vs Capacitive Load](image3)

![Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency](image4)

![Open-Loop Gain and Phase](image5)

![Composite Video Differential Gain and Phase](image6)
Typical Characteristics (continued)

at $T_A = 25^\circ C$, $V_S = 5\, V$, $G = +1$, $R_F = 0\, \Omega$, $R_L = 1\, k\, \Omega$, and connected to $V_S / 2$, (unless otherwise noted)

- **Figure 19. Input Bias Current vs Temperature**
- **Figure 20. Output Voltage Swing vs Output Current**
- **Figure 21. Supply Current vs Temperature**
- **Figure 22. Output Voltage Swing vs Output Current**
- **Figure 23. Closed-Loop Output Impedance vs Frequency**
- **Figure 24. Maximum Output Voltage vs Frequency**
Typical Characteristics (continued)

at $T_A = 25^\circ C$, $V_S = 5$ V, $G = +1$, $R_E = 0$ $\Omega$, $R_L = 1$ k$\Omega$, and connected to $V_S / 2$, (unless otherwise noted)
8 Detailed Description

8.1 Overview
The OPAx354 is a CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifier designed for video, high-speed, and other applications. It is available as a single, dual, or quad op amp.

The amplifier features a 100-MHz gain bandwidth, and 150-V/µs slew rate, but the amplifier is unity-gain stable and can operate as a 1-V/V voltage follower.

8.2 Functional Block Diagram
8.3 Feature Description

8.3.1 Operating Voltage

The OPAx354 is specified over a power-supply range of 2.7 V to 5.5 V (±1.35 V to ±2.75 V). However, the supply voltage may range from 2.5 V to 5.5 V (±1.25 V to ±2.75 V). Supply voltages higher than 7.5 V (absolute maximum) can permanently damage the amplifier.

Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

8.3.2 Rail-to-Rail Input

The specified input common-mode voltage range of the OPAx354 extends 100 mV beyond the supply rails. This extended range is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the Functional Block Diagram. The N-channel pair is active for input voltages close to the positive rail, typically (V+) − 1.2 V to 100 mV above the positive supply, while the P-channel pair is on for inputs from 100 mV below the negative supply to approximately (V+) − 1.2 V. There is a small transition region, typically (V+) − 1.5 V to (V+) − 0.9 V, in which both pairs are on. This 600-mV transition region vary ±500 mV with process variation. Therefore, the transition region (both input stages on) range from (V+) − 2 V to (V+) − 1.5 V on the low end, up to (V+) − 0.9 V to (V+) − 0.4 V on the high end.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage.

8.3.3 Rail-to-Rail Output

A class AB output stage with common-source transistors achieves rail-to-rail output. For high-impedance loads (> 200 Ω), the output voltage swing is typically 100 mV from the supply rails. With 10-Ω loads, a useful output swing is achieved while maintaining high open-loop gain. See the typical characteristic curves, Output Voltage Swing vs Output Current (Figure 20 and Figure 22).

8.3.4 Output Drive

The OPAx354 output stage supplies a continuous output current of ±100 mA and yet provide approximately 2.7 V of output swing on a 5-V supply, as shown in Figure 30. For maximum reliability, TI does not recommend running a continuous DC current in excess of ±100 mA. See the typical characteristic curves, Output Voltage Swing vs Output Current (Figure 20 and Figure 22). For supplying continuous output currents greater than ±100 mA, the OPAx354 may be operated in parallel, as shown in Figure 31.

Figure 30. Laser Diode Driver
Feature Description (continued)

The OPAx354 provides peak currents up to 200 mA, which corresponds to the typical short-circuit current. Therefore, an on-chip thermal shutdown circuit is provided to protect the OPAx354 from dangerously high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below 140°C.

![Parallel Operation Diagram]

**Figure 31. Parallel Operation**

8.3.5 Video

The OPAx354 output stage is capable of driving standard back-terminated 75-Ω video cables, as shown in Figure 32. By back-terminating a transmission line, the output stage does not exhibit a capacitive load to the driver. A properly back-terminated 75-Ω cable does not appear as capacitance; the cable presents a 150-Ω resistive load to the OPAx354 output.

![Single-Supply Video Line Driver Diagram]

**Figure 32. Single-Supply Video Line Driver**

The OPAx354 is used as an amplifier for RGB graphic signals, which feature a voltage of zero at the video black level, by offsetting and AC-coupling the signal. See Figure 33.
Figure 33. RGB Cable Driver

(1) Source video signal offset 300 mV above ground to accommodate op amp swing-to-ground capability.
Feature Description (continued)

8.3.6 Driving Analog-to-Digital converters

The OPAx354 series op amps offer 60 ns of settling time to 0.01%, making the series a good choice for driving high- and medium-speed sampling A/D converters and reference circuits. The OPAx354 series provide an effective means of buffering the A/D converter input capacitance and resulting charge injection while providing signal gain. For applications requiring high DC accuracy, the OPA350 series is recommended.

Figure 34 shows the OPAx354 driving an A/D converter. With the OPAx354 in an inverting configuration, a capacitor across the feedback resistor is used to filter high-frequency noise in the signal.

![Figure 34. The OPAx354 in Inverting Configuration Driving the ADS7816](image)

8.3.7 Capacitive Load and Stability

The OPAx354 series op amps drives a wide range of capacitive loads. However, all op amps may become unstable under certain conditions. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in unity-gain configuration is most susceptible to the effects of capacitive loading. The capacitive load reacts with the device output resistance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin. See the Frequency Response for Various $C_L$ typical characteristic curve (Figure 13) for details.

The OPAx354 topology enhances its ability to drive capacitive loads. In unity gain, these op amps perform well with large capacitive loads. See the Recommended $R_S$ vs Capacitive Load (Figure 14) and Frequency Response vs Capacitive Load (Figure 15) typical characteristic curves for details.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10-$\Omega$ to 20-$\Omega$ resistor in series with the output, as shown in Figure 35. This configuration significantly reduces ringing with large capacitive loads; see the Frequency Response vs Capacitive Load typical characteristic curve (Figure 15). However, if there is a resistive load in parallel with the capacitive load, $R_S$ creates a voltage divider. This voltage division introduces a DC error at the output and slightly reduces output swing. This error may be insignificant. For instance, with $R_L = 10\, k\Omega$ and $R_S = 20\, \Omega$, there is an error of approximately 0.2% at the output.

![Figure 35. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive](image)
Feature Description (continued)

8.3.8 Wideband Transimpedance Amplifier

Wide bandwidth, low input bias current, low input voltage, and current noise make the OPAx354 a preferred wideband photodiode transimpedance amplifier for low-voltage single-supply applications. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design (as shown in Figure 36) are the expected diode capacitance [including the parasitic input common-mode and differential-mode input capacitance (2 + 2) pF for the OPAx354], the desired transimpedance gain \( R_F \), and the gain-bandwidth product (GBW) for the OPAx354 (100 MHz, typical). With these three variables set, the feedback capacitor value \( C_F \) may be set to control the frequency response.

\[
\frac{1}{2\pi R_F C_F} = \sqrt{\frac{\text{GBP}}{4\pi R_F C_D}} \tag{1}
\]

Typical surface-mount resistors have a parasitic capacitance of approximately 0.2 pF that must be deducted from the calculated feedback capacitance value. Bandwidth is calculated by Equation 2:

\[
f_{3\text{dB}} = \sqrt{\frac{\text{GBP}}{2\pi R_F C_D}} \text{ Hz} \tag{2}
\]

For even higher transimpedance bandwidth, the high-speed CMOS OPA355 (200-MHz GBW) or the OPA655 (400-MHz GBW) may be used.

8.4 Device Functional Modes

The OPAx354 family of devices is powered on when the supply is connected. The devices can operate as single-supply operational amplifiers or dual-supply amplifiers depending on the application. The devices are used with asymmetrical supplies as long as the differential voltage (V– to V+) is at least 1.8 V and no greater than 5.5 V (example: V– set to –3.5 V and V+ set to 1.5 V).
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
The OPAx354 family of devices is a CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifier designed for video, high-speed, and other applications. The OPAx354 family of devices is available as a single, dual, or quad op amp. The amplifier features a 100-MHz gain bandwidth, and 150-V/µs slew rate, but it is unity-gain stable and operates as a 1-V/V voltage follower.

9.2 Typical Application
Wide gain bandwidth, low input bias current, low input voltage, and current noise make the OPAx354 family of devices an ideal wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency. The key elements to a transimpedance design, as shown in Figure 37, are the expected diode capacitance, (which include the parasitic input common-mode and differential-mode input capacitance) the desired transimpedance gain, and the gain-bandwidth (GBW) for the OPAx354 family of devices (20 MHz). With these three variables set, the feedback capacitor value is set to control the frequency response. Feedback capacitance includes the stray capacitance, which is 0.2 pF for a typical surface-mount resistor.

Figure 37. Dual-Supply Transimpedance Amplifier

9.2.1 Design Requirements
For this design example, use the parameters listed in Table 1 as the input parameters.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, (V_{(V_+)})</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Supply voltage, (V_{(V_-)})</td>
<td>-2.5 V</td>
</tr>
</tbody>
</table>
C_{(F)} is optional to prevent gain peaking. C_{(F)} includes the stray capacitance of R_{(F)}.

**9.2.2 Detailed Design Procedure**

To achieve a maximally-flat, second-order Butterworth frequency response, set the feedback pole using Equation 3.

\[
\frac{1}{2 \times \pi \times R_{(F)} \times C_{(F)}} = \sqrt{\frac{GBW}{4 \times \pi \times R_{(F)} \times C_{(D)}}}
\]  

(3)

Calculate the bandwidth using Equation 4.

\[
f_{(-3 \text{ dB})} = \sqrt{\frac{GBW}{2 \times \pi \times R_{(F)} \times C_{(D)}}}
\]  

(4)

**9.2.2.1 Optimizing the Transimpedance Circuit**

To achieve the best performance, components must be selected according to the following guidelines:

1. For lowest noise, select R_{(F)} to create the total required gain. Using a lower value for R_{(F)} and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by R_{(F)} increases with the square-root of R_{(F)}, whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.

2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to amplify (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode reduce the capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.

3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only the required bandwidth. Use a capacitor across the R_{(F)} to limit bandwidth, even if a capacitor not required for stability.

4. Circuit board leakage degrades the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage helps control leakage.

**9.2.3 Application Curve**

![Figure 38. AC Transfer Function](image-url)
10 Power Supply Recommendations

The OPAx354 family of devices is specified for operation from 2.5 V to 5.5 V (±1.25 to ±2.75 V); many specifications apply from −40°C to +125°C. Parameters that exhibit significant variance with regard to operating voltage or temperature are shown Typical Characteristics.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see the Layout Guidelines section.

11 Layout

11.1 Layout Guidelines

Good high-frequency printed-circuit board (PCB) layout techniques must be employed for the OPAx354. Generous use of ground planes, short and direct signal traces, and a suitable bypass capacitor located at the V+ pin ensure clean, stable operation. Large areas of copper provides a means of dissipating heat that is generated in normal operation.

TI does not recommend using sockets with any high-speed amplifier.

A 10-nF ceramic bypass capacitor is the minimum recommended value; adding a 1-µF or larger tantalum capacitor in parallel is beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving low harmonic and intermodulation distortion.

11.2 Layout Example

![Operational Amplifier Board Layout for Noninverting Configuration](image)

**Figure 39. Operational Amplifier Board Layout for Noninverting Configuration**

11.3 Power Dissipation

Power dissipation depends on power-supply voltage, signal and load conditions. With DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor, \( V_{S} - V_{O} \). Power dissipation is minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower. AB-039 Power Amplifier Stress and Power Handling Limitations explains how to calculate or measure power dissipation with unusual signals and loads See www.ti.com for more details.
Power Dissipation (continued)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature must be limited to 150°C (maximum). To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered at 160°C. The thermal protection must trigger more than 35°C above the maximum expected ambient condition of the application.

11.4 PowerPAD Thermally-Enhanced Package

In addition to the regular 5-pin SOT-23 and 9-pin VSSOP packages, the single and dual versions of the OPAx354 also come in an 8-pin SOIC PowerPAD package. The 98-pin SO with PowerPAD is a standard size 8-pin SOIC package where the exposed leadframe on the bottom of the package is soldered directly to the PCB to create a low thermal resistance. This direct attachment enhances the OPA354 power dissipation capability significantly, and eliminates the use of bulky heat sinks and slugs that are traditionally used in thermal packages. This package is easily mounted using standard PCB assembly techniques.

NOTE
Because the 8-pin HSOP PowerPAD is pin-compatible with standard 8-pin SOIC packages, the OPA354 and OPA2354 can directly replace operational amplifiers in existing sockets. Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation. This configuration provides the necessary thermal and mechanical connection between the leadframe die pad and the PCB.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the device, as shown in Figure 40. This exposed die provides an extremely low thermal resistance ($R_{\text{JC}}$) path between the die and the exterior of the package. The thermal pad on the bottom of the device can then be soldered directly to the PCB, using the PCB as a heat sink. In addition, plated-through holes (vias) provide a low thermal resistance heat flow path to the back side of the PCB.

![Figure 40. Section View of a PowerPAD Package](image)

11.5 PowerPAD Assembly Process

The PowerPAD must be connected to the most negative supply voltage for the device, which is ground in single-supply applications and $V_{-}$ in split-supply applications.

Prepare the PCB with a top-side etch pattern, as shown in Figure 41. The exact land design may vary based on the specific assembly process requirements. There must be etch for the leads and etch for the thermal land.

Place the recommended number of plated-through holes (or thermal vias) in the area of the thermal pad. These holes must be 13 mils (.013 in) in diameter. The holes are small so that solder wicking through the holes is not a problem during reflow. TI recommends a minimum of five holes for the 8-pin HSOP PowerPAD package, as shown in Figure 41.
PowerPAD Assembly Process (continued)

TI recommends, but does not require, placing a small number of additional holes under the package and outside the thermal pad area. These holes provide additional heat paths between the copper thermal land and the ground plane. The holes may be larger because the holes are not in the area to be soldered, so wicking is not a problem. This technique is shown in Figure 41.

Connect all holes, including those within the thermal pad area and outside the pad area, to the internal ground plane or other internal copper plane for single-supply applications, and to V− for split-supply applications.

When laying out these holes, do not use the typical web or spoke via connection methodology, as shown in Figure 42. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This feature makes soldering the vias that have ground plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the PowerPAD package must make connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.

The top-side solder mask must leave the pad connections and the thermal pad area exposed. The thermal pad area must leave the 13-mil holes exposed. The larger holes outside the thermal pad area may be covered with a solder mask.

Apply solder paste to the exposed thermal pad area and all of the package pins.

With these preparatory steps in place, the PowerPAD device is placed in position and run through the solder reflow operation as any standard surface-mount component. This preparation and processing results in a part that is properly installed.

For detailed information on the PowerPAD package, including thermal modeling considerations and repair procedures, see PowerPAD Thermally Enhanced Package on www.ti.com.
12 Device and Documentation Support

12.1 Documentation Support

For related documentation see the following:

- Texas Instruments, *ADS8326 16-Bit, High-Speed, 2.7V to 5.5V microPower Sampling ANALOG-TO-DIGITAL CONVERTER*
- Texas Instruments, *Circuit Board Layout Techniques*
- Texas Instruments, *Compensate Transimpedance Amplifiers Intuitively*
- Texas Instruments, *FilterPro™ User’s Guide*
- Texas Instruments, *Noise Analysis for High-Speed Op Amps*
- Texas Instruments, *OPA380 and OPA2380 Precision, High-Speed Transimpedance Amplifier*
- Texas Instruments, *OPA355, OPA2355, and OPA3355 200MHz, CMOS OPERATIONAL AMPLIFIER WITH SHUTDOWN*
- Texas Instruments, *OPA656 Wideband, Unity-Gain Stable, FET-Input OPERATIONAL AMPLIFIER*
- Texas Instruments, *POWER AMPLIFIER STRESS AND POWER HANDLING LIMITATIONS*
- Texas Instruments, *PowerPAD Thermally Enhanced Package*

12.2 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

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</tr>
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<td>OPA2354</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>OPA4354</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
</tbody>
</table>

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E Online Community**  *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support**  *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.
12.7 Glossary

SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## Packaging Information

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</tr>
</thead>
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<tr>
<td>OPA2354AIDDA</td>
<td>ACTIVE</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>75</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>OPA 2354A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA2354AIDDAG3</td>
<td>ACTIVE</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>75</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>OPA 2354A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA2354AIDDAR</td>
<td>ACTIVE</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>OPA 2354A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA2354AIDDARG3</td>
<td>ACTIVE</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>OPA 2354A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA2354AIDGKR</td>
<td>ACTIVE</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>Call TI</td>
<td>NIPDAUAG</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OACI</td>
</tr>
<tr>
<td>OPA2354AIDGKT</td>
<td>ACTIVE</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>Call TI</td>
<td>NIPDAUAG</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OACI</td>
</tr>
<tr>
<td>OPA2354AIDGKTG4</td>
<td>ACTIVE</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>Call TI</td>
<td>NIPDAUAG</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OACI</td>
</tr>
<tr>
<td>OPA354AIDBVR</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OABI</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA354AIDBVT</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OABI</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA354AIDBVTG4</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OABI</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA354AIDDDA</td>
<td>ACTIVE</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>75</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>OPA 354A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA354AIDDAG3</td>
<td>ACTIVE</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>75</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>OPA 354A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA354AIDDAR</td>
<td>ACTIVE</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>OPA 354A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA4354AID</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>50</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA4354A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA4354AIDR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA4354A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA4354AIPWR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA4354A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA4354AIPWRG4</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA4354A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA4354AIPWT</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA4354A</td>
<td>Samples</td>
</tr>
</tbody>
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The marketing status values are defined as follows:

**ACTIVE**: Product device recommended for new designs.
**LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE**: TI has discontinued the production of the device.

TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF OPA4354**:
- Automotive : OPA4354-Q1

**NOTE**: Qualified Version Definitions:
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

- **Reel Diameter**
- **Reel Width (W1)**

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Pocket Quadrants**
- **Sprocket Holes**
- **User Direction of Feed**

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*All dimensions are nominal*

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<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
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<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA2354AIDDAR</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>OPA2354AIDGKR</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>5.3</td>
<td>3.4</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>OPA2354AIDGKT</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>250</td>
<td>178.0</td>
<td>9.0</td>
<td>3.23</td>
<td>3.17</td>
<td>1.37</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>OPA354AIDBVR</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>178.0</td>
<td>9.0</td>
<td>3.2</td>
<td>3.14</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q3</td>
</tr>
<tr>
<td>OPA354AIDBVT</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>250</td>
<td>178.0</td>
<td>9.0</td>
<td>3.5</td>
<td>3.15</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q3</td>
</tr>
<tr>
<td>OPA354AIDDAR</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>OPA4354AIDR</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>330.0</td>
<td>16.4</td>
<td>6.5</td>
<td>9.0</td>
<td>2.1</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>OPA4354AIPWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.9</td>
<td>5.6</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>OPA4354AIPWT</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>250</td>
<td>180.0</td>
<td>12.4</td>
<td>6.9</td>
<td>5.6</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA2354AIDDAR</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
</tr>
<tr>
<td>OPA2354AIDGKR</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>2500</td>
<td>366.0</td>
<td>364.0</td>
<td>50.0</td>
</tr>
<tr>
<td>OPA2354AIDGKT</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>250</td>
<td>366.0</td>
<td>364.0</td>
<td>50.0</td>
</tr>
<tr>
<td>OPA354AIDBVR</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>180.0</td>
<td>180.0</td>
<td>18.0</td>
</tr>
<tr>
<td>OPA354AIDBVT</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>250</td>
<td>180.0</td>
<td>180.0</td>
<td>18.0</td>
</tr>
<tr>
<td>OPA354AIDDAR</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
</tr>
<tr>
<td>OPA4354AIDR</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
</tr>
<tr>
<td>OPA4354AIPWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2500</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
</tr>
<tr>
<td>OPA4354AIPWT</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
**TUBE**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Name</th>
<th>Package Type</th>
<th>Pins</th>
<th>SPQ</th>
<th>L (mm)</th>
<th>W (mm)</th>
<th>T (µm)</th>
<th>B (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA2354AIDDA</td>
<td>DDA</td>
<td>HSOIC</td>
<td>8</td>
<td>75</td>
<td>506.6</td>
<td>8</td>
<td>3940</td>
<td>4.32</td>
</tr>
<tr>
<td>OPA2354AIDDAG3</td>
<td>DDA</td>
<td>HSOIC</td>
<td>8</td>
<td>75</td>
<td>506.6</td>
<td>8</td>
<td>3940</td>
<td>4.32</td>
</tr>
<tr>
<td>OPA354AIDDA</td>
<td>DDA</td>
<td>HSOIC</td>
<td>8</td>
<td>75</td>
<td>506.6</td>
<td>8</td>
<td>3940</td>
<td>4.32</td>
</tr>
<tr>
<td>OPA354AIDDAG3</td>
<td>DDA</td>
<td>HSOIC</td>
<td>8</td>
<td>75</td>
<td>506.6</td>
<td>8</td>
<td>3940</td>
<td>4.32</td>
</tr>
<tr>
<td>OPA4354AID</td>
<td>D</td>
<td>SOIC</td>
<td>14</td>
<td>50</td>
<td>506.6</td>
<td>8</td>
<td>3940</td>
<td>4.32</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*

---

**Diagrams:**

- **T - Tube height**
- **L - Tube length**
- **W - Tube width**
- **B - Alignment groove width**
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
\[\text{Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.}\]
C. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
D. Falls within JEDEC MO-187 variation AA, except interlead flash.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
MECHANICAL DATA

D (R-PDSO-G14) PLASTIC SMALL OUTLINE

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AB.
NOTES:  
A. All linear dimensions are in millimeters. 
B. This drawing is subject to change without notice. 
C. Publication IPC-7351 is recommended for alternate designs. 
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations. 
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.

E. Falls within JEDEC MO-153
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.

PowerPAD is a trademark of Texas Instruments.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

11. Board assembly site may have different recommendations for stencil design.
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