



# SPECIFICATIONS

## ELECTRICAL

At  $T_C = +25^\circ\text{C}$  and  $V_S = \pm 35\text{VDC}$ , unless otherwise noted.

PARAMETER	CONDITIONS	OPA2541AM			OPA2541BM, SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUT OFFSET VOLTAGE</b>								
$V_{OS}$ vs Temperature vs Supply Voltage vs Power	Specified Temperature Range $V_S = \pm 10\text{V}$ to $\pm V_{MAX}$		$\pm 2$ $\pm 20$ $\pm 2.5$ $\pm 20$	$\pm 10$ $\pm 40$ $\pm 10$ $\pm 60$		$\pm 0.25$ $\pm 15$ * *	$\pm 1$ $\pm 30$ * *	mV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/\text{V}$ $\mu\text{V}/\text{W}$
<b>INPUT BIAS CURRENT</b>								
$I_B$	Specified Temperature Range		15 Note 1	50		*	*	pA
<b>INPUT OFFSET CURRENT</b>								
$I_{OS}$	Specified Temperature Range		$\pm 5$ Note 1	$\pm 30$		*	*	pA
<b>INPUT CHARACTERISTICS</b>								
Common-Mode Voltage Range Common-Mode Rejection Input Capacitance Input Impedance, DC	Specified Temperature Range $V_{CM} = (\pm V_S) - 6\text{V}$	$\pm( V_S  - 6)$ 95	$\pm( V_S  - 3)$ 106 5 1		*	*		V dB pF $10^{12}\Omega$
<b>GAIN CHARACTERISTICS</b>								
Open Loop Gain at 10Hz Gain-Bandwidth Product	$R_L = 6\Omega$	90	96 1.6		*	*		dB MHz
<b>OUTPUT</b>								
Voltage Swing  Current, Continuous	$I_O = 5\text{A}$ $I_O = 2\text{A}$ $I_O = 0.5\text{A}$ +25°C +85°C +125°C (SM grade only)	$\pm( V_S  - 5.5)$ $\pm( V_S  - 4.5)$ $\pm( V_S  - 4)$ 5 4	$\pm( V_S  - 4.5)$ $\pm( V_S  - 3.6)$ $\pm( V_S  - 3.2)$ 7.0 5.0		*	*		V V V A A A
<b>AC PERFORMANCE</b>								
Slew Rate Power Bandwidth Settling Time to 0.1%  Capacitive Load  Phase Margin Channel Separation	$R_L = 8\Omega$ , $V_O = 20\text{Vrms}$ 2V Step  Specified Temperature Range, $G = 1$ Specified Temperature Range, $G > 10$ Specified Temperature Range, $R_L = 8\Omega$ 1kHz, $R_L = 6\Omega$	6 45    40 80	8 55 2   40 80	3.3 SOA	*	*	*	V/ $\mu\text{s}$ kHz $\mu\text{s}$ nF Degrees dB
<b>POWER SUPPLY</b>								
Power Supply Voltage, $\pm V_S$ Current, Quiescent	Specified Temperature Range Total—Both Amplifiers	$\pm 10$	$\pm 30$ 40	$\pm 35$ 50	*	$\pm 35$ *	$\pm 40$ *	V mA
<b>THERMAL RESISTANCE</b>								
$\theta_{JC}$ , (Junction-to-Case) $\theta_{JC}$ $\theta_{JC}$ $\theta_{JC}$ $\theta_{JA}$ , (Junction-to-Ambient)	Both Amplifiers <sup>(2)</sup> , AC Output $f > 60\text{Hz}$ Both Amplifiers <sup>(2)</sup> , DC Output One Amplifier, AC Output $f > 60\text{Hz}$ One Amplifier, DC Output No Heat Sink		0.8 0.9 1.25 1.4 30	1.0 1.2 1.5 1.9		*	*	$^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$
<b>TEMPERATURE RANGE</b>								
Case	AM, BM SM	-25		+85	*		*	$^\circ\text{C}$ $^\circ\text{C}$

\*Specification same as OPA2541AM.

NOTES: (1) Input bias and offset current approximately doubles for every  $10^\circ\text{C}$  increase in temperature. (2) Assumes equal dissipation in both amplifiers.

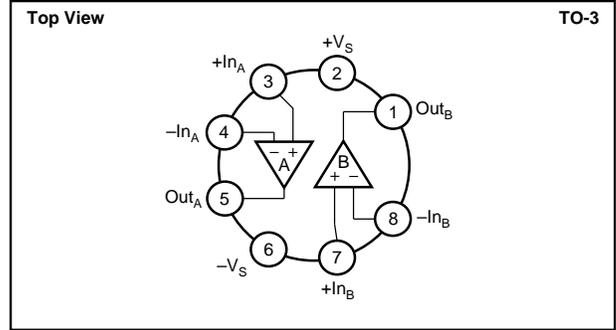
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## ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ .....	80V
Output Current .....	see SOA
Power Dissipation, Internal <sup>(1)</sup> .....	125W
Input Voltage: Differential .....	$\pm V_S$
Common-mode .....	$\pm V_S$
Temperature: Pin Solder, 10s .....	+300°C
Junction <sup>(1)</sup> .....	+150°C
Temperature Range:	
Storage .....	-65°C to +150°C
Operating (Case) .....	-55°C to +125°C

NOTE: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

## CONNECTION DIAGRAM



## PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>
OPA2541AM	TO-3	030
OPA2541BM	TO-3	030
OPA2541SM	TO-3	030

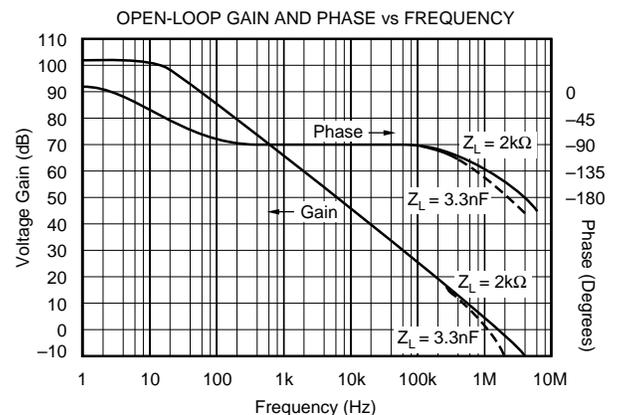
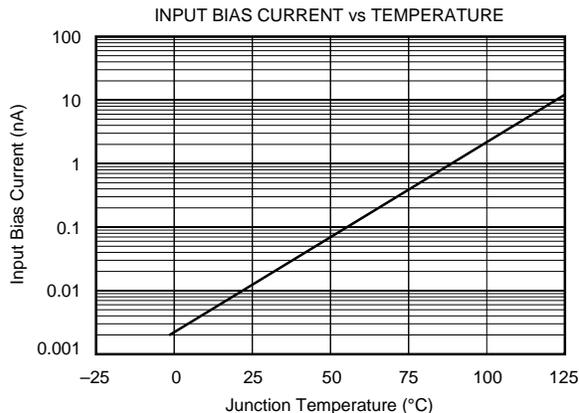
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

## ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA2541AM	TO-3	-25°C to +85°C
OPA2541BM	TO-3	-25°C to +85°C
OPA2541SM	TO-3	-55°C to +125°C

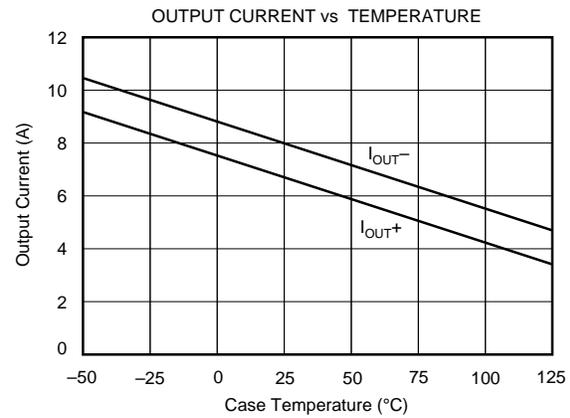
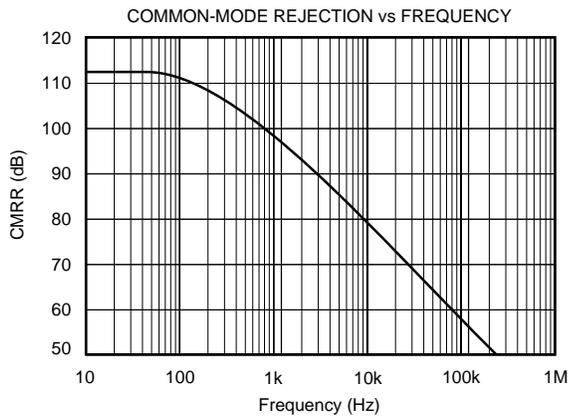
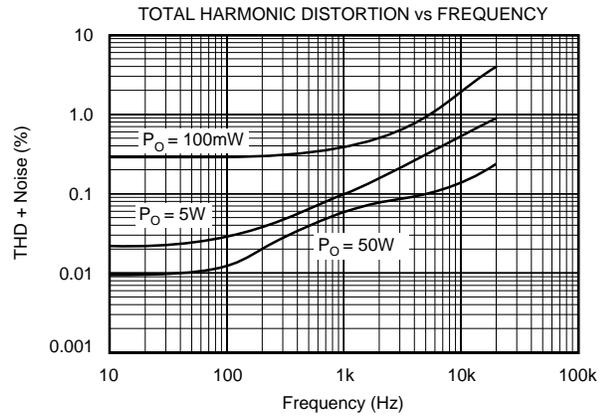
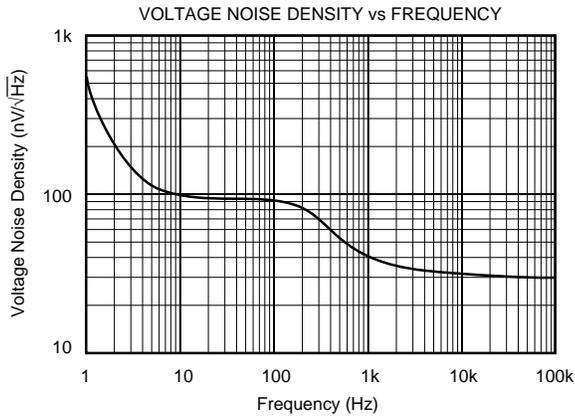
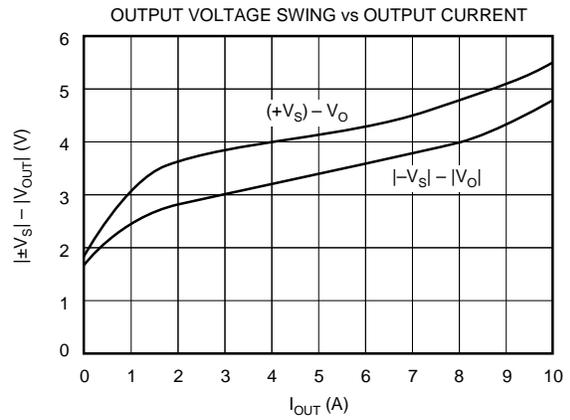
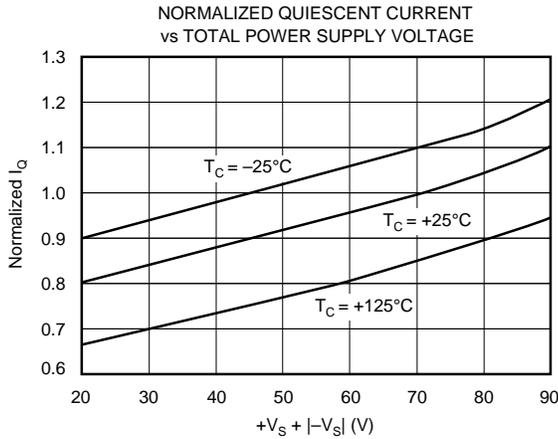
## TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$  and  $V_S = \pm 35\text{VDC}$ , unless otherwise noted.



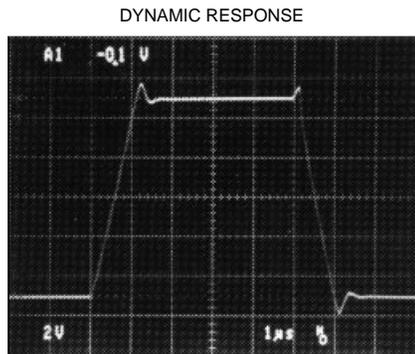
# TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$  and  $V_S = \pm 35\text{VDC}$ , unless otherwise noted.

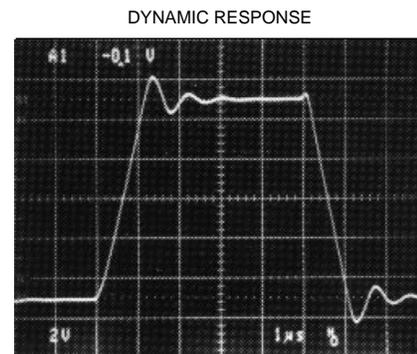


## TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$  and  $V_S = \pm 35\text{VDC}$ , unless otherwise noted.



$Z_{\text{LOAD}} = \infty$ ,  $V_S = \pm 35\text{V}$ ,  $A_V = +1$



$Z_{\text{LOAD}} = 4700\text{pF}$ ,  $V_S = \pm 35\text{V}$ ,  $A_V = +1$

## INSTALLATION INSTRUCTIONS

### POWER SUPPLIES

The OPA2541 is specified for operation from power supplies up to  $\pm 40\text{V}$ . It can also be operated from an unbalanced or a single power supply so long as the total power supply voltage does not exceed  $80\text{V}$  ( $70\text{V}$  for “AM” grade). The power supplies should be bypassed with low series impedance capacitors such as ceramic or tantalum. These should be located as near as practical to the amplifier’s power supply pins. Good power amplifier circuit layout is, in general, like good high-frequency layout. Consider the path of large power supply and output currents. Avoid routing these connections near low-level input circuitry to avoid waveform distortion and instability.

Signal dependent load current can modulate the power supply voltage with inadequate power supply bypassing. This can affect both amplifiers’ outputs. Since the second amplifier’s signal may not be related to the first, this will degrade the inherent channel separation of the OPA2541.

### HEAT SINKING

Most applications will require a heat sink to prevent junction temperatures from exceeding the  $150^\circ\text{C}$  maximum rating. The type of heat sink required will depend on the output signals, power dissipation of each amplifier, and ambient temperature. The thermal resistance from junction-to-case,  $\theta_{\text{JC}}$ , depends on how the power dissipation is distributed on the amplifier die.

DC output concentrates the power dissipation in one output transistor. AC output distributes the power dissipation equally between the two output transistors and therefore has lower thermal resistance. Similarly, the power dissipation may be all in one amplifier (worst case) or equally distributed between the two amplifiers (best case). Thermal resistances are provided for each of these possibilities. The case-to-junction temperature rise is the product of the power dissi-

pation (total of both amplifiers) times the appropriate thermal resistance—

$$\Delta T_{\text{JC}} = (P_{\text{D total}}) (\theta_{\text{JC}}).$$

Sufficient heat sinking must be provided to keep the case temperature within safe limits for the maximum ambient temperature and power dissipation. The thermal resistance of the heat sink required may be calculated by:

$$\theta_{\text{HS}} = (150^\circ\text{C} - \Delta T_{\text{JC}} - T_A) / P_{\text{D}}.$$

Commercially available heat sinks usually specify thermal resistance. These ratings are often suspect, however, since they depend greatly on the mounting environment and air flow conditions. Actual thermal performance should be verified by measurement of case temperature under the required load and environmental conditions.

No insulating hardware is required when using the OPA2541. Since mica and other similar insulators typically add  $0.7^\circ\text{C}/\text{W}$  thermal resistance, this is a significant advantage. See Burr-Brown Application Note AN-83 for further details on heat sinking.

### SAFE OPERATING AREA

The Safe Operating Area (SOA) curve provides comprehensive information on the power handling abilities of the OPA2541. It shows the allowable output current as a function of the voltage across the conducting output transistor (see Figure 1). This voltage is equal to the power supply voltage minus the output voltage. For example, as the amplifier output swings near the positive power supply voltage, the voltage across the output transistor decreases and the device can safely provide large output currents demanded by the load.

The internal current limit will not provide short-circuit protection in most applications. When the amplifier output is shorted to ground, the full power supply voltage is impressed across the conducting output transistor. For instance, with  $V_s = \pm 35V$ , a short circuit to ground would impress 35V across the conducting power transistor. The maximum safe output current at this voltage is 1.8A, so the internal current limit would not protect the amplifier. The unit-to-unit variation and temperature dependence of the internal current limit suggest that it be used to handle abnormal conditions and not activated in commonly encountered circuit operation.

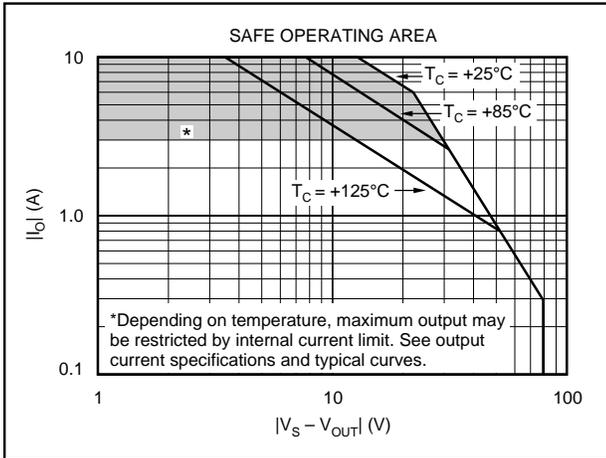


FIGURE 1. Safe Operating Area.

Reactive, or EMF generating loads such as DC motors can present demanding SOA requirements. With a purely reactive load, output voltage current occurs when the output voltage is zero and the voltage across the conducting transistor is equal to the full power supply voltage. See Burr-Brown Application Note AN-123 for further information on evaluating SOA.

Applications with inductive or EMF-generating loads which can produce “kick back” voltage surges to the amplifiers should include clamp diodes from the output terminals to the power supplies. These diodes should be chosen to limit the peak amplifier output voltage surges to less than 2V beyond the power supply rail voltage. Common 1A rated rectifier diodes will suffice in most applications.

## APPLICATIONS CIRCUITS

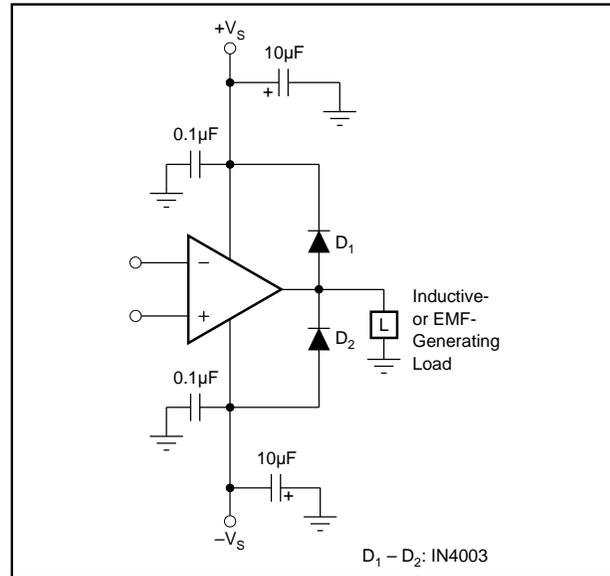


FIGURE 2. Clamping Output for EMF-Generating Loads.

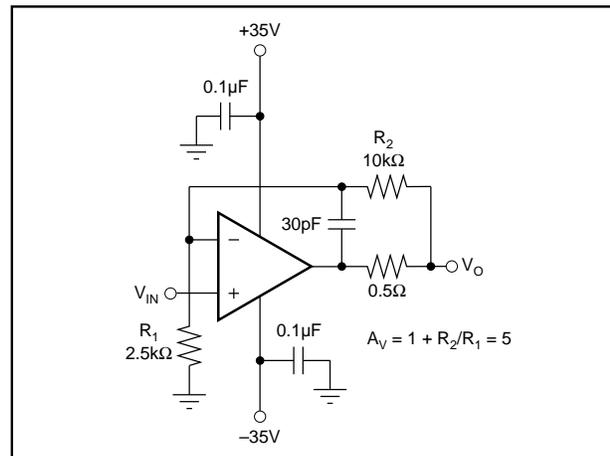


FIGURE 3. Isolating Capacitive Loads.

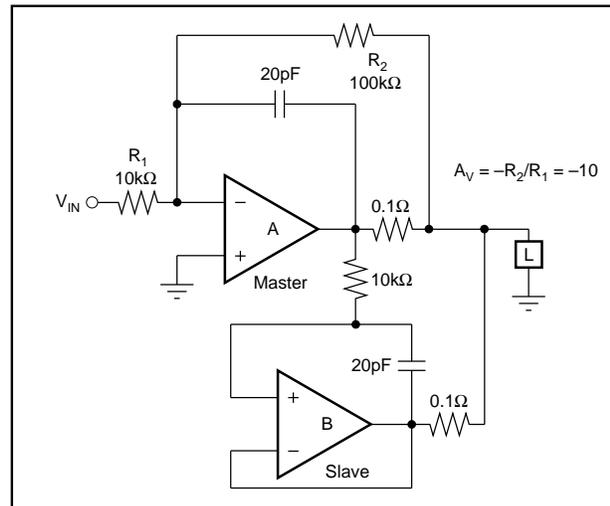


FIGURE 4. Paralleled Operation, Extended SOA.

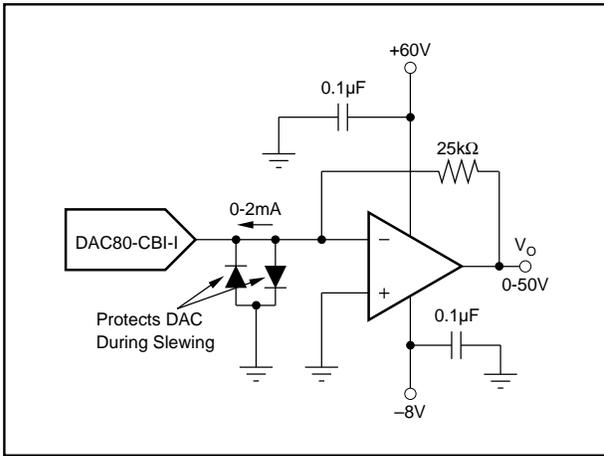


FIGURE 5. Programmable Voltage Source.

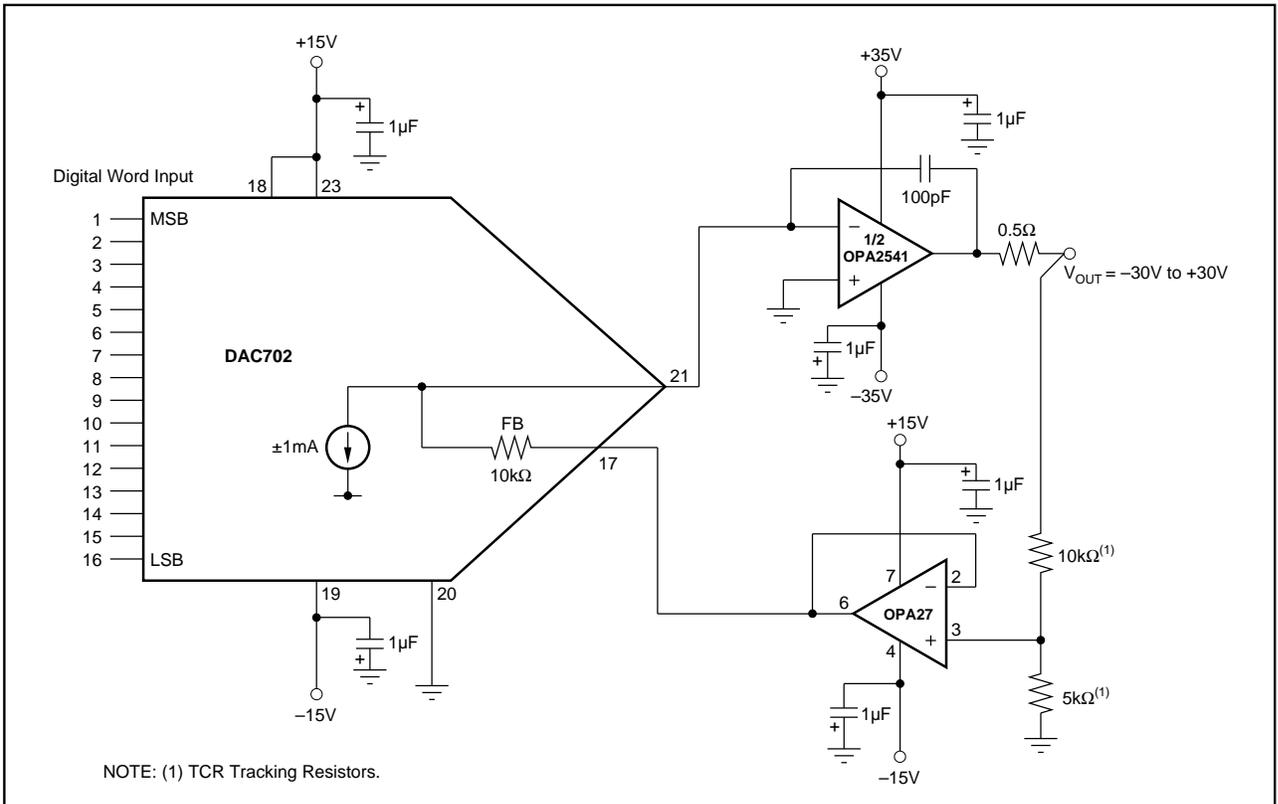


FIGURE 6. 16-Bit Programmable Voltage Source.

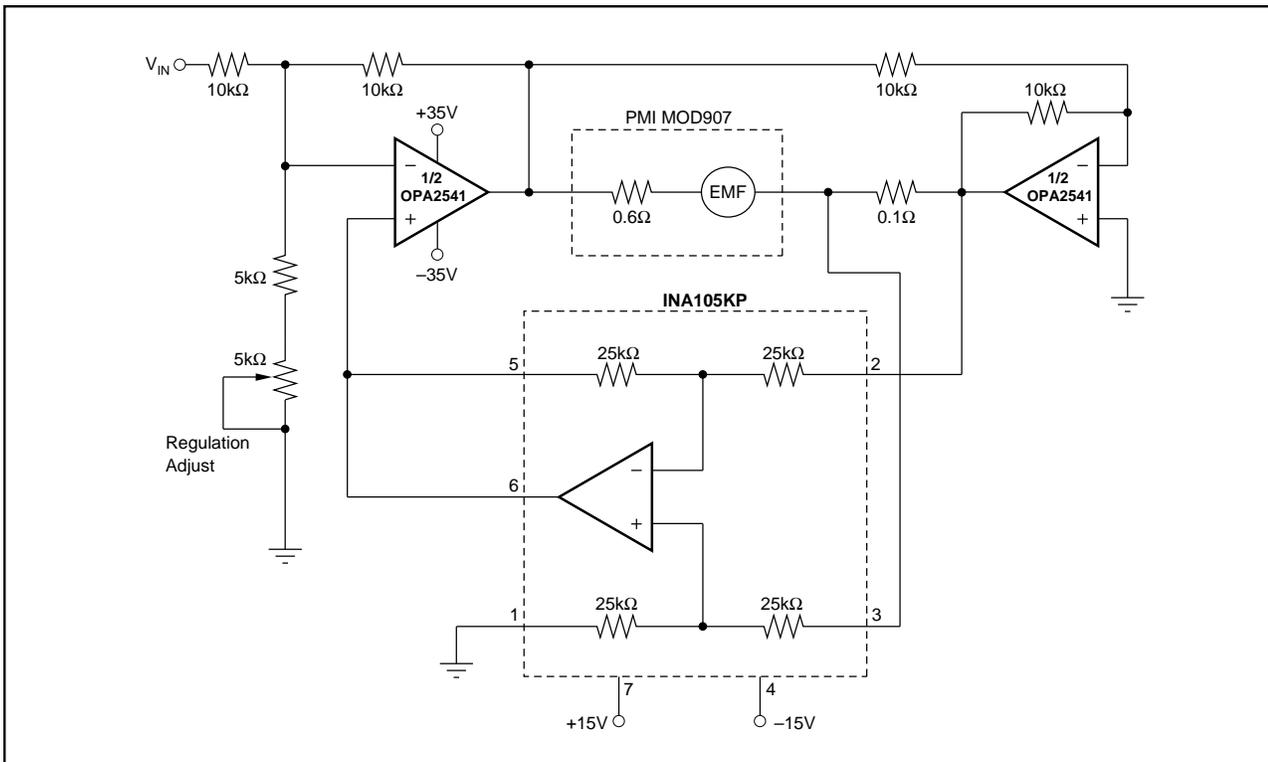


FIGURE 7. Bridge Amplifier Motor-Speed Controller.

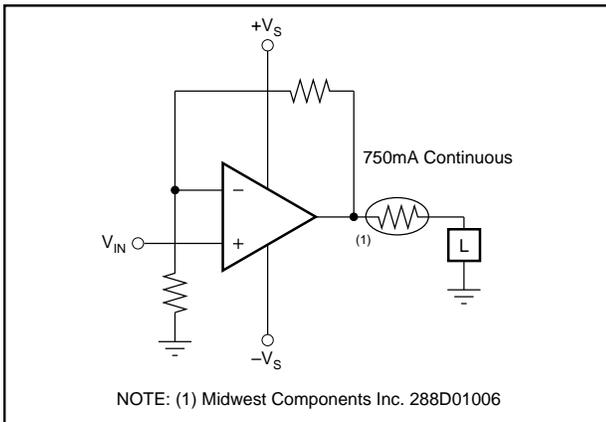


FIGURE 8. Limiting Output Current.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2541AM	ACTIVE	TO-3	LMF	8	18	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125	OPA2541AM	<a href="#">Samples</a>
OPA2541BM	ACTIVE	TO-3	LMF	8	18	Non-RoHS & Green	NI	N / A for Pkg Type	-55 to 125	OPA2541BM	<a href="#">Samples</a>
OPA2541SM	ACTIVE	TO-3	LMF	8	18	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125	OPA2541SM	<a href="#">Samples</a>
OPA2541SMQ	ACTIVE	TO-3	LMF	8	18	RoHS & Green	NI	N / A for Pkg Type	-40 to 125	OPA2541 OPA2541SMQ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

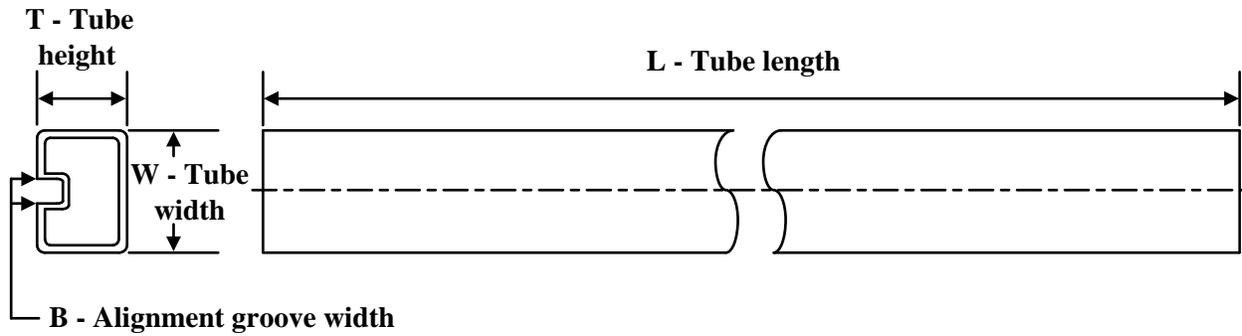
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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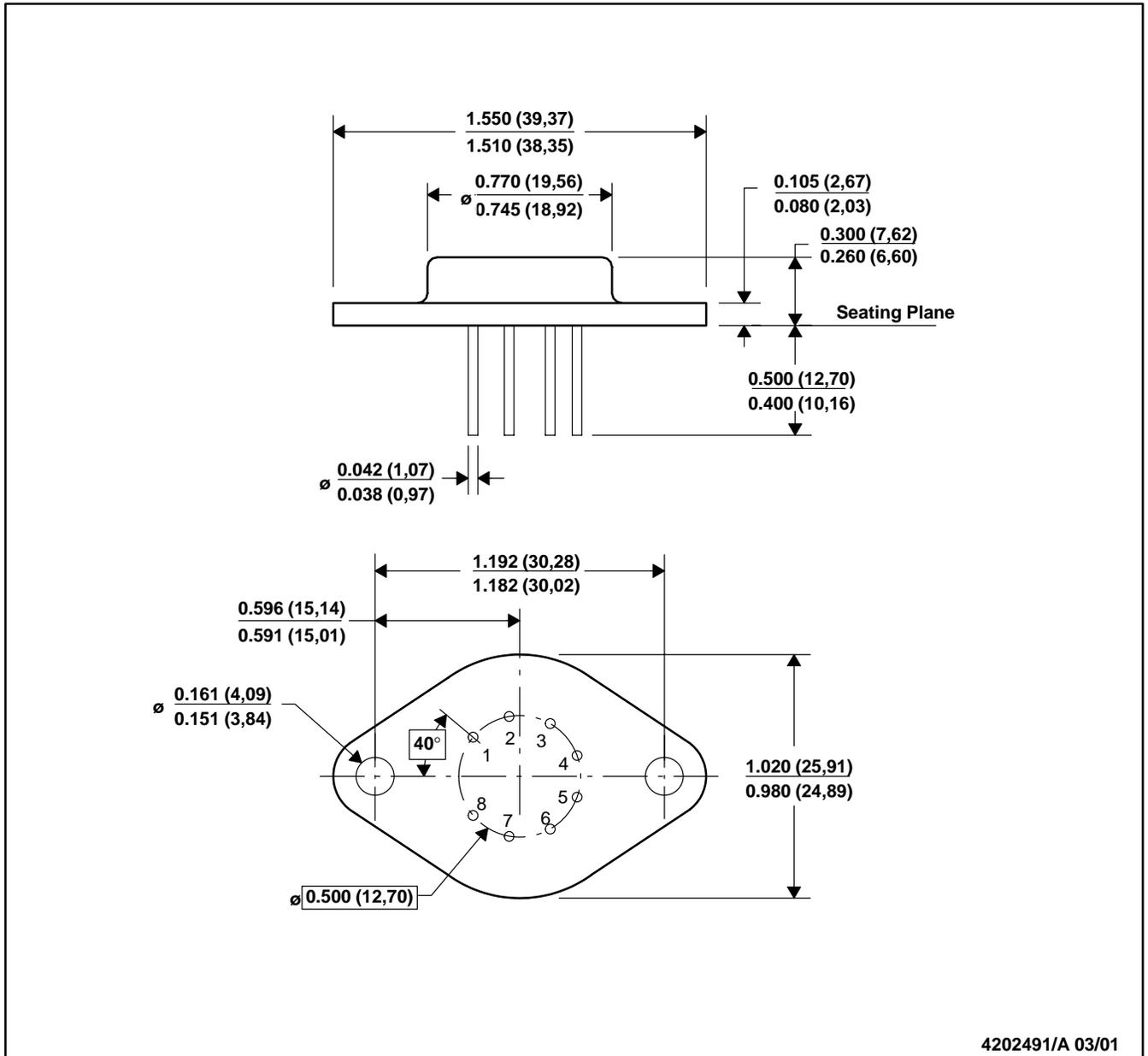
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA2541AM	LMF	TO-CAN	8	18	532.13	21.59	889	NA
OPA2541BM	LMF	TO-CAN	8	18	532.13	21.59	889	NA
OPA2541SM	LMF	TO-CAN	8	18	532.13	21.59	889	NA
OPA2541SMQ	LMF	TO-CAN	8	18	532.13	21.59	889	NA

LMF (O-MBCY-W8)

METAL CYLINDRICAL PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
  - D. Pin numbers shown for reference only. Numbers may not be marked on package.

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