OPAx863 Low-Power, 100-MHz, Rail-to-Rail Input and Output, Voltage-Feedback Amplifier

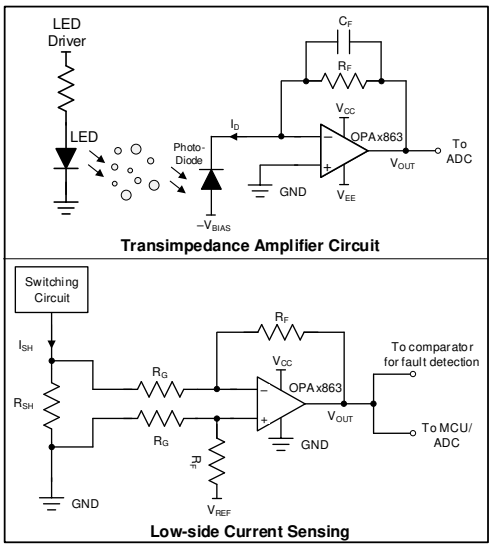
1 Features

- Wide-Bandwidth
  - Unity-Gain Bandwidth: 100-MHz (A_V= 1 V/V)
  - Gain-Bandwidth Product: 50-MHz
- Low Power
  - Quiescent Current: 720-µA/ch (Typical)
  - Power Down Mode: 1.5-µA (Maximum)
  - Supply Voltage: 2.7-V to 12.6-V
- Input Voltage Noise: 5.9-nV/√Hz
- Slew Rate: 100-V/µs
- Rail-to-Rail Input and Output
- HD_2/HD_3: –105 dBc/–125 dBc at 100 kHz (2-V_{PP})
- Operating Temperature Range: –40°C to +125°C
- Additional Features:
  - Overload Power Limit
  - Output Short-Circuit Protection

2 Applications

- Low-Power SAR and ΔΣ ADC Driver
- ADC Reference Buffer
- Low-Side Current Sensing
- Photodiode TIA Interface
- Inductive Sensing
- Ultrasonic Flow Meters
- Multi-Function Printers
- MDAC Output Buffer
- Gain & Active Filter Stages

Application Circuits Using OPAx863



Transimpedance Amplifier Circuit

Low-side Current Sensing

3 Description

The OPAx863 devices are low-power, unity-gain stable, rail-to-rail input/output, voltage-feedback operational amplifiers designed to operate over a power supply range of 2.7-V to 12.6-V. Consuming only 750-µA per channel, the OPAx863 devices offer a gain-bandwidth product of 50-MHz, slew rate of 100-V/µs with a voltage noise density of 5.9-nV/√Hz.

The rail-to-rail input stage with 2.7-V supply operation is useful in portable battery powered applications. The differential input stages are well matched for gain-bandwidth product and noise across the full input common-mode voltage range, enabling superior performance with wide-input dynamic range. The OPAx863 devices feature a power-down (PD) mode with a PD quiescent current of 1.5-µA (maximum) with turn-on or turn-off within 10-µs (typical).

The OPAx863 devices include overload power limiting to limit the increase in quiescent current with saturated outputs, thereby preventing excessive dissipation critical in battery-powered systems. The output stage is short-circuit protected, making it a rugged amplifier for general-purpose usage.

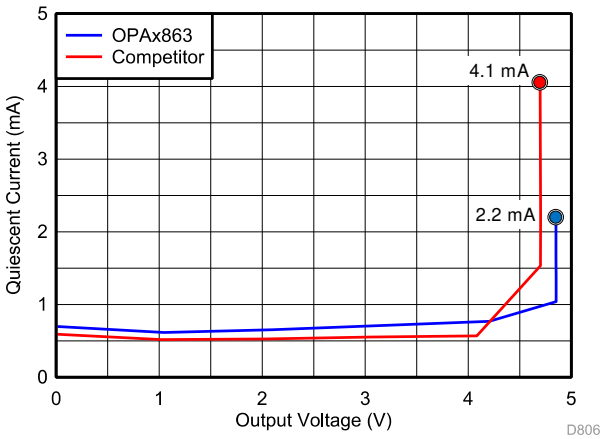
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA863	SOT23 (6)(2)	2.90 mm × 1.60 mm
OPA2863	VSSOP (8)	3.00 mm × 3.00 mm
	USON (10)(2)	3.00 mm × 3.00 mm
OPA4863	TSSOP (14)(2)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Preview packages

Increase in Quiescent Current with Output Saturation



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

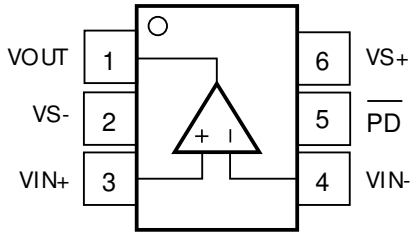
Changes from Original (June 2020) to Revision A	Page
• Updated links to product folder.	1

5 Device Comparison Table

DEVICE	$V_{S\pm}$ (V)	I_Q / CHANNEL (mA)	GBWP (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
OPAx863	±6.3	0.72	50	100	5.9	Unity-gain stable RRIO Bipolar Amplifier
LMH6643	±6.4	2.7	65	130	17	Unity-gain stable NRI/RRO Bipolar Amplifier
OPAx810	±13.5	3.6	70	200	6.3	Unity-gain stable RRIO FET-Input Amplifier
OPAx837	±2.7	0.6	50	105	4.7	Unity-gain stable NRI/RRO Bipolar Amplifier
OPAx607	±2.75	0.9	50	24	3.8	Decompensated Gain of 6V/V stable CMOS Amplifier

6 Pin Configuration and Functions

DBV Package (Preview)
6-Pin SOT-23
Top View



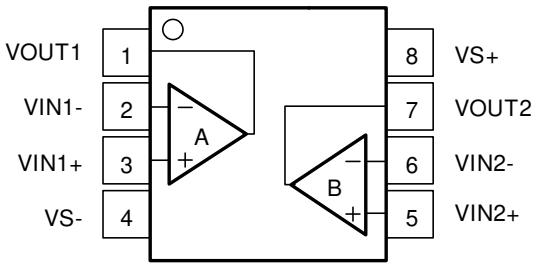
Pin Functions

PIN		FUNCTION(1)	DESCRIPTION
NAME	OPA863 SOT-23		
VOUT	1	O	Output pin
VS–	2	P	Negative power-supply pin
VIN+	3	I	Noninverting input pin
VIN–	4	I	Inverting input pin
$\overline{PD}$	5	I	Power down. Low = disabled, high = normal operation (pin must be driven).
VS+	6	P	Positive power-supply input

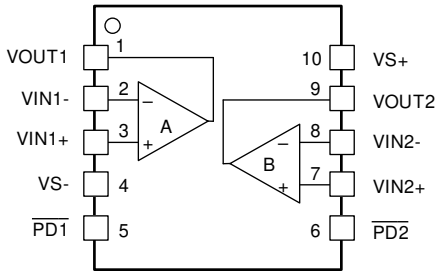
(1) I = input, O = output, and P = power.

ADVANCE INFORMATION

DGK Package
8-Pin VSSOP
Top View



DSN Package (Preview)
10-Pin USON
Top View



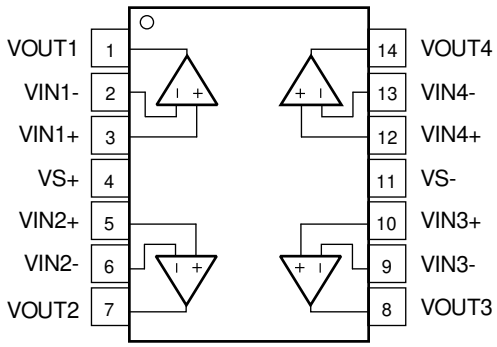
Pin Functions

PIN			FUNCTION[1]	DESCRIPTION
NAME	OPA2863			
	VSSOP	USON		
$\overline{PD1}$	-	5	I	Amplifier 1 power down. Low = disabled, high = normal operation (pin must be driven).
$\overline{PD2}$	-	6	I	Amplifier 2 power down. Low = disabled, high = normal operation (pin must be driven).
VIN1–	2	2	I	Amplifier 1 inverting input pin
VIN1+	3	3	I	Amplifier 1 noninverting input pin
VIN2–	6	8	I	Amplifier 2 inverting input pin
VIN2+	5	7	I	Amplifier 2 noninverting input pin
VOUT1	1	1	O	Amplifier 1 output pin
VOUT2	7	9	O	Amplifier 2 output pin
VS–	4	4	P	Negative power-supply pin
VS+	8	10	P	Positive power-supply input

(1) I = input, O = output, and P = power.

ADVANCE INFORMATION

PW Package (Preview)
14-Pin TSSOP
Top View



Pin Functions

PIN		FUNCTION(1)	DESCRIPTION
NAME	OPA4863 TSSOP		
VOUT1	1	O	Amplifier 1 output pin
VIN1–	2	I	Amplifier 1 inverting input pin
VIN1+	3	I	Amplifier 1 noninverting input pin
VS+	4	P	Positive power-supply input
VIN2+	5	I	Amplifier 2 noninverting input pin
VIN2–	6	I	Amplifier 2 inverting input pin
VOUT2	7	O	Amplifier 2 output pin
VOUT3	8	O	Amplifier 3 output pin
VIN3–	9	I	Amplifier 3 inverting input pin
VIN3+	10	I	Amplifier 3 noninverting input pin
VS–	11	P	Negative power-supply pin
VIN4+	12	I	Amplifier 4 noninverting input pin
VIN4–	13	I	Amplifier 4 inverting input pin
VOUT4	14	O	Amplifier 4 output pin

(1) I = input, O = output, and P = power.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$V_{S–}$ to V_{S+}	Supply voltage		13	V
V_I	Input voltage	$V_{S–}$ – 0.5	V_{S+} + 0.5	V
V_{ID}	Differential input voltage		±1	V
I_I	Continuous input current(2)		±10	mA
I_O	Continuous output current(3)		±30	mA
	Continuous power dissipation	See *Thermal Information*		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Continuous input current limit for both the ESD diodes to supply pins and amplifier differential input clamp diode. The differential input clamp diode limits the voltage across it to 1 V with this continuous input current flowing through it.
(3) Long-term continuous current for electromigration limits.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S+}	Single-supply positive voltage	2.7	10	12.6	V
T_A	Ambient temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		OPA2863 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	101.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.8	°C/W
Y_{JB}	Junction-to-board characterization parameter	100.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics: 10 V

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_F = 0 Ω for Gain =1, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)

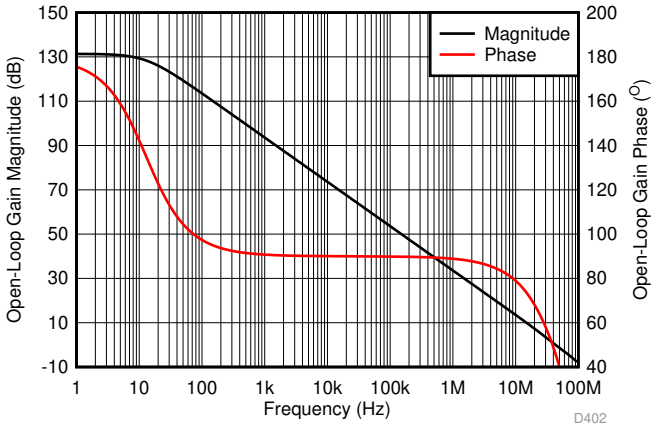
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1, < 1 dB peaking		100		MHz
GBWP	Gain-bandwidth product			50		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		17		MHz
SR	Slew rate	V_{OUT} = 2–V step, G = –1		100		V/µs
	Rise, fall time	V_{OUT} = 200–mV step		10		ns
	Settling time to 0.1%	V_{OUT} = 2–V step		60		ns
	Settling time to 0.01%	V_{OUT} = 2–V step		70		ns
HD2	Second-order harmonic distortion	f = 20 kHz, V_{OUT} = 2 V_{PP}		–115		dBc
HD3	Third-order harmonic distortion	f = 20 kHz, V_{OUT} = 2 V_{PP}		–130		dBc
e_N	Input voltage noise	1/f corner at 30 Hz		5.9		nV/√Hz
i_N	Input current noise			0.4		pA/√Hz
z_O	Closed-loop output impedance	f = 1 MHz		0.2		Ω
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_O = ±2.5 V	110	130		dB
V_{OS}	Input-referred offset voltage		–1.5	±0.3	1.5	mV
	Input offset voltage drift(1)	T_A = –40°C to +125°C	–6	±1.5	6	µV/°C
	Input bias current	V_{CM} = mid-supply	0.15	0.3	0.73	µA
	Input offset current		-30	±10	30	nA
INPUT						
	Input common-mode voltage range		$V_{S–}$–0.2		V_{S+}+0.2	V
CMRR	Common-mode rejection ratio	V_{CM}=$V_{S–}$ – 0.2 V to V_{S+} + 0.2 V		110		dB
		V_{CM} = $V_{S–}$ to V_{S+} – 1.4 V		120		
	Input impedance common-mode			650 || 0.8		MΩ || pF
	Input impedance differential mode			200 || 0.5		kΩ || pF
OUTPUT						
V_{OL}	Output voltage, low			$V_{S–}$+0.2	$V_{S–}$+0.2	V
V_{OH}	Output voltage, high		V_{S+}–0.2	V_{S+}–0.2		V
	Linear output drive (sourcing/sinking)	V_{OUT} = ±2.5 V, ΔV_{IO} < 1 mV		30		mA
	Short-circuit current			40		mA
POWER SUPPLY						
I_Q	Quiescent current per amplifier	T_A ≈ 25°C		720	970	µA
PSRR	Power-supply rejection ratio	ΔV_S = 2 V		120		dB
POWER DOWN (Pin Must be Driven)						
	Enable voltage threshold	Specified *on* above V_{S+}–0.5 V			4.5	V
	Disable voltage threshold	Specified *off* below V_{S+}–1.5 V	3.5			V
	Power-down quiescent current per channel	$\overline{PD}$ ≤ V_{S+}–1.5 V		0.5	1.5	µA
	Turn-on/off time delay			10		µs
AUXILIARY INPUT STAGE						
	Gain-bandwidth product			50		MHz
	Input voltage noise			5.9		nV/√Hz
	Input-referred offset voltage		–1.5	±0.3	1.5	mV

(1) Based on electrical characterization of 32 devices. Typical specifications are ±1sigma.

ADVANCE INFORMATION

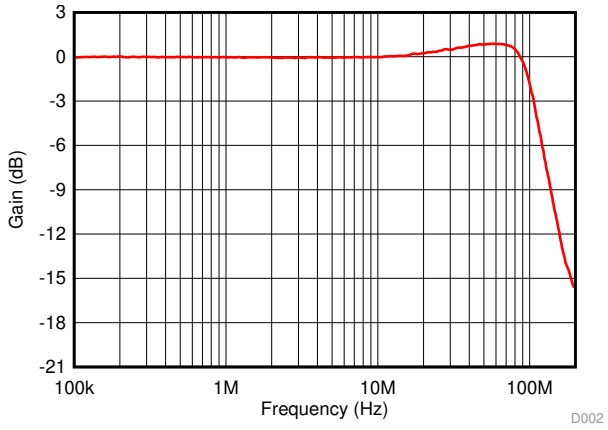
7.6 Typical Characteristics: V_S = 10 V

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to midsupply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≈ 25°C (unless otherwise noted)



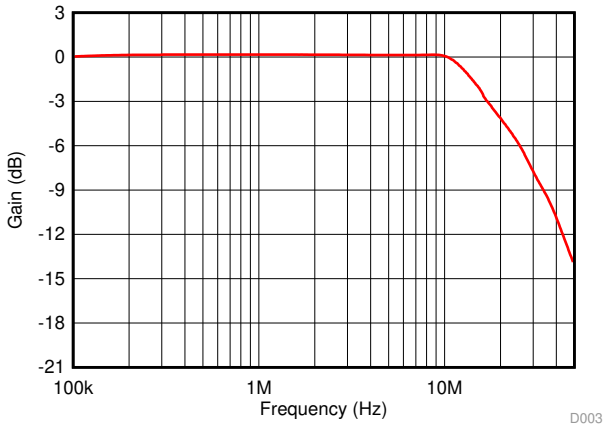
Small-signal response

Figure 1. Open-Loop Gain and Phase vs Frequency



See Figure 8, V_{OUT} = 20 mV_{PP}

Figure 2. Small-Signal Frequency Response



See Figure 8, V_{OUT} = 2 V_{PP}

Figure 3. Large-Signal Frequency Response

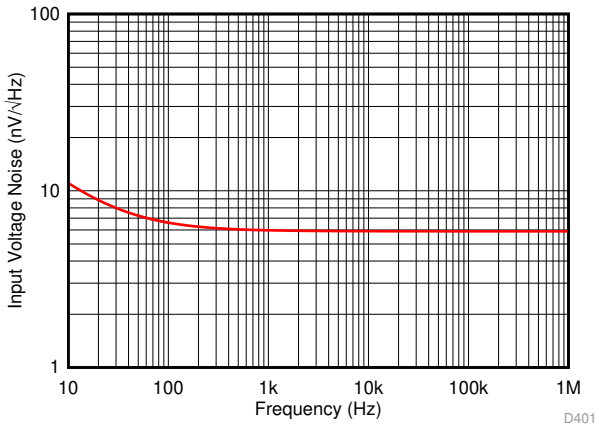
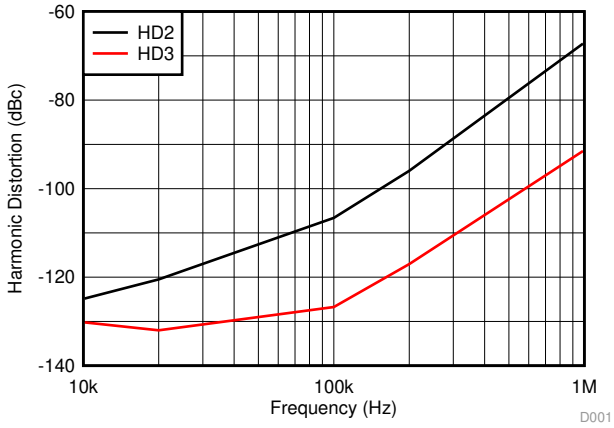


Figure 4. Input Voltage Noise Density vs Frequency



Gain = 1 V/V, V_{OUT} = 2 V_{PP}

Figure 5. Harmonic Distortion vs Frequency

ADVANCE INFORMATION

8 Detailed Description

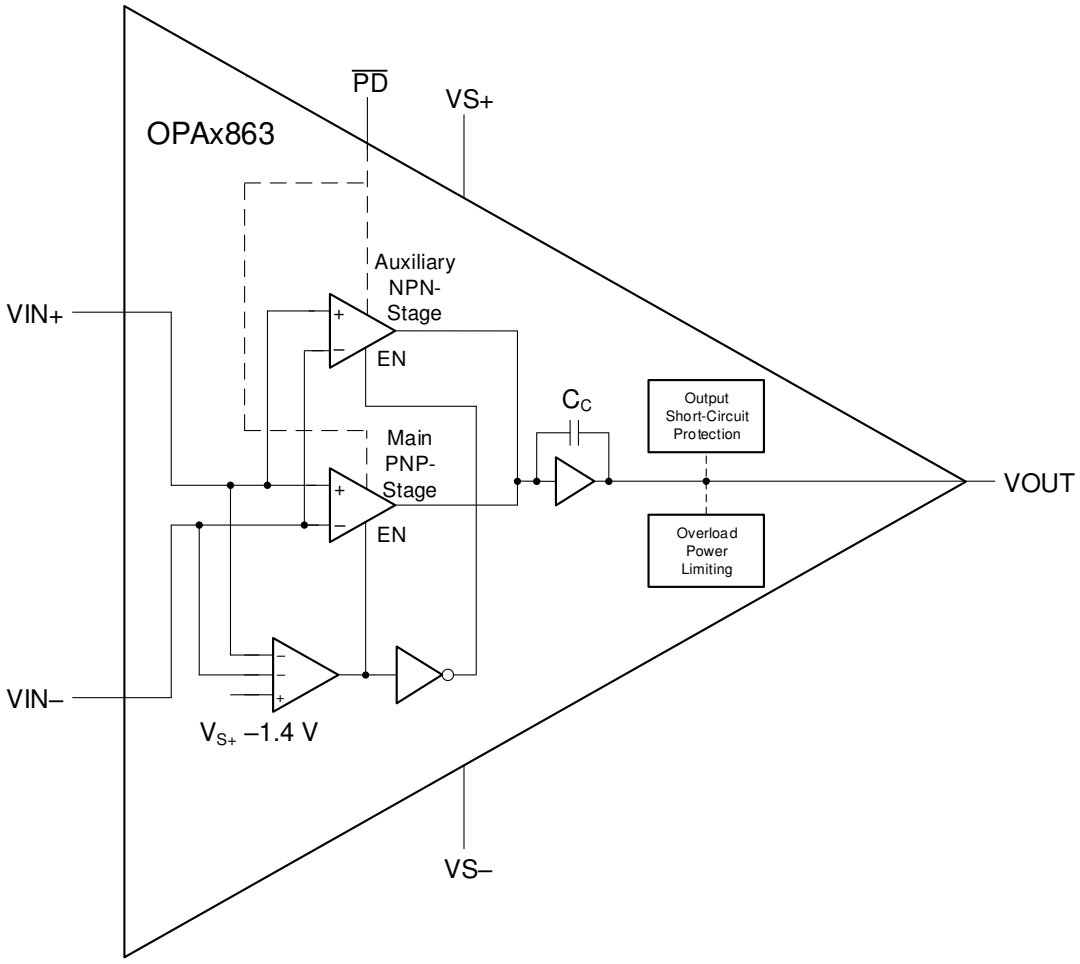
8.1 Overview

The OPAx863 devices are low-power, 50 MHz, rail-to-rail input and output (RRIO) bipolar voltage-feedback operational amplifiers with a voltage noise density of 5.9 nV/√Hz and 1/f noise corner at 30 Hz. The OPAx863 devices work in a wide-supply voltage range from 2.7 V to 12.6 V and consumes only 750 µA quiescent current. The OPAx863 devices operate with 2.7-V supply, are RRIO capable, consume low-power and offer a power-down mode, which makes them ideal amplifiers for 3.3-V or lower voltage applications that need superior AC performance. The amplifier's two input stages are well-matched for gain bandwidth product (GBW), noise and offset voltage especially for applications which require wide dynamic input range and good SNR.

The device includes an overload power limit feature which limits the increase in quiescent current with over-driven and saturated outputs to either of the supply rails. See Overload Power Limit for more details of this overload power limit feature. The amplifier's output is protected against short-circuit fault conditions.

The OPAx863 devices feature a power-down (PD) mode with a PD quiescent current of 1.5-µA (maximum) with turn-on and turn-off within less than 10-µs.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Input Stage

The OPAx863 devices include a rail-to-rail input stage. The main stage differential pair using PNP bipolar transistors operates for common-mode input voltages from $V_{S–}$ – 0.2 V till V_{S+} – 1.4 V. The amplifier inputs transition into the auxiliary stage using NPN transistors for common-mode input voltages from V_{S+} – 1.4 V till V_{S+} + 0.2 V. The PNP and NPN input stages offer a gain-bandwidth product of 50 MHz and a voltage noise density of 5.9 nV/√Hz. The offset voltage for the two input stages is matched to lie within the device specifications. The NPN input stage does not use the slew boost circuit during large-signal transient response. The input bias current for the PNP and NPN input stages is opposite in polarity, which adds an additional offset based on the values of the gain-setting and feedback resistors. A common-mode input voltage transition between these input stages will cause a crossover distortion which needs to be considered in high-frequency applications requiring superior linearity. Limit the common-mode input voltage to V_{S+} – 1.5 V (maximum) for main-stage operation across process and ambient temperature .

Since the OPAx863 devices are bipolar amplifiers, the two inputs are protected with anti-parallel back-to-back diodes between them, which limits the maximum input differential voltage to 1 V. In very fast input or output transient conditions, the amplifier is slew limited and the two inputs are puled apart up to 1 V when the anti-parallel diodes begin to conduct. Care must be taken to use gain-setting and feedback resistors large enough to limit the current through these diodes in such conditions.

8.3.2 Output Stage

The OPAx863 devices feature a rail-to-rail output stage with signal swing possible from $V_{S–}$ + 0.2 V to V_{S+} – 0.2 V. Violating the output headroom to either of the supplies will cause output signal clipping and degrade linear performance.

The OPAx863 devices integrate an output short-circuit protection circuit which makes the device rugged for use in real-world applications.

8.3.2.1 Overload Power Limit

The OPAx863 devices include overload power limiting which limits the increase in device quiescent current with output saturated to either of the supplies. Typically, when an amplifier's output saturates, its two inputs are pulled apart which may enable the slew boost circuit. The input differential voltage is an error voltage in negative feedback, which the amplifier core nullifies by engaging the slew boost circuit and driving the output stage deeper into saturation. As the output stage transistor is pushed deeper into saturation, its h_{FE} (base-to-collector current gain) drops with increase in its base and collector current, increasing the device quiescent current. This may cause a catastrophic failure in multi-channel, high-gain, high-density front-end designs and reduce operating lifetime in portable battery powered systems. The OPAx863 devices overload power limiting includes an intelligent output saturation detection circuit which limits the devices quiescent current to 2.2-mA per channel under DC overload condition. This increase in quiescent current is smaller with AC input or output with output saturation duration for only a fraction of the overall signal time period.

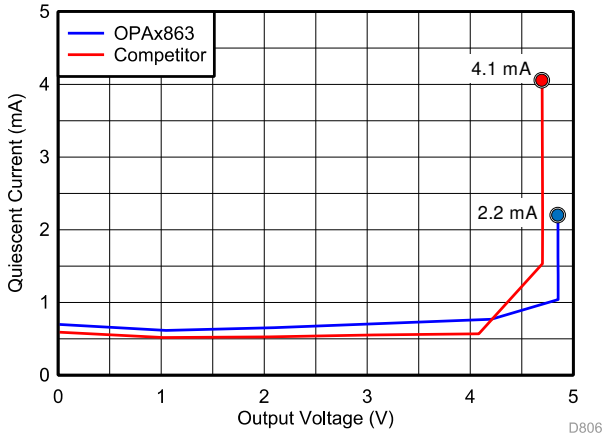

Figure 6. Increase in Quiescent Current with Output Saturation

Feature Description (continued)

8.3.3 ESD Protection

As Figure 7 shows, all device pins are protected with internal ESD protection diodes to the power supplies. These diodes provide moderate protection to input overdrive voltages above the supplies. The protection diodes can typically support 10-mA continuous input and output currents. Use series current limiting resistors if input voltages exceeding the supply voltages occur at the amplifier inputs, which ensures the current through the ESD diodes remains within their rated value. Keep these resistor values as low as possible because using high values degrades noise performance and frequency response.

Since OPAx863 is a bipolar amplifier, the two inputs are protected with anti-parallel back-to-back diodes between them which limits the maximum input differential voltage to approximately 1 V. In very fast input or output transient conditions, the amplifier is slew limited and the two inputs are pulled apart up to 1 V, when the anti-parallel diodes begin to conduct. Care must be taken to use gain-setting and feedback resistors large enough to limit the current through these diodes in such conditions.

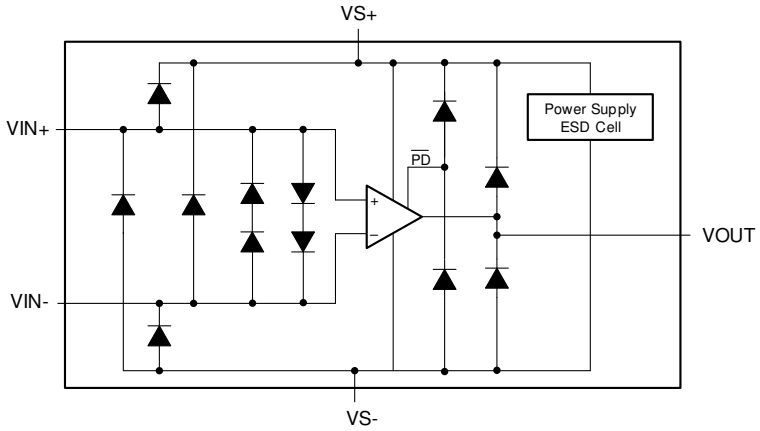

Figure 7. Internal ESD Protection

8.4 Device Functional Modes

8.4.1 Power-Down Mode

The OPAx863 devices include a power-down mode for low-power standby operation with a quiescent current of only 1.5 μA (maximum). Many applications, such as battery powered systems, are active for only a small time interval when the parameters of interest are measured and remain in low-power standby mode for a majority of the time. This results in an overall small average power consumption. The OPAx863 device enable such a low-power operation with quick turn-on that the device turns on within less than 10 μsec. The device remains in power-down mode with $\overline{PD}$ pin voltage less than V_{S+}– 1.5 V (disabled up to $V_{S–}$) and returns to active-mode with PD pin voltage greater than V_{S+}– 0.5 V up to V_{S+}. The intermediate $\overline{PD}$ pin voltage range from V_{S+}– 1.5 V to V_{S+}– 0.5 V should be avoided to prevent erratic device turn-on and turn-off behavior.

8.4.2 Split-Supply Operation (±1.35 V to ±6.3 V)

See the *OPA2863DGK Evaluation Module* user guide for more information on how the OPAx863 devices can be configured to allow for split-supply operation to facilitate testing with common lab equipment. This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers, and other lab equipment reference the inputs and outputs to ground. Figure 8 depicts the OPAx863 devices configured as a noninverting amplifier and Figure 9 illustrates the OPAx863 devices configured as an inverting amplifier. For split-supply operation referenced to ground, the power supplies V_{S+} and V_{S-} are symmetrical around ground and V_{REF} is at GND. Split-supply operation is preferred in systems where the signals swing around ground because of the ease-of-use; however, the system requires two supply rails.

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Device Functional Modes (continued)

8.4.3 Single-Supply Operation (2.7 V to 12.6 V)

Many newer systems use a single power supply to improve efficiency and reduce the cost of the extra power supply. The OPAx863 devices can be used with a single supply (with the negative supply set to ground) with no change in performance if the input and output are biased within the linear operation of the device. To change the circuit from split supply to a balanced, single-supply configuration, level shift all voltages by half the difference between the power-supply rails. An additional advantage of configuring an amplifier for single-supply operation is that the effects of PSRR are minimized because the low-supply rail is grounded. See the *Single-Supply Op Amp Design Techniques* application report for examples of single-supply designs.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Amplifier Gain Configurations

The OPAx863 devices are classic voltage-feedback amplifiers with each channel having two high-impedance inputs and a low-impedance output. Standard application circuits (as shown in Figure 8 and Figure 9) include the noninverting and inverting gain configurations. The DC operating point for each configuration is level-shifted by the reference voltage VREF that is typically set to midsupply in single-supply operation. VREF is often connected to ground in split-supply applications.

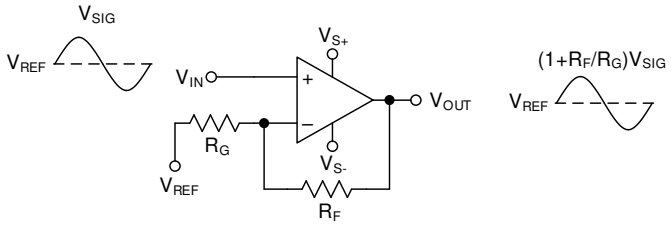

Figure 8. Noninverting Amplifier

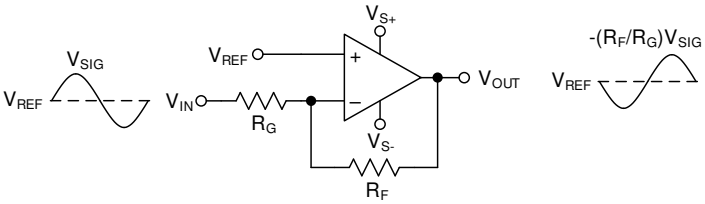

Figure 9. Inverting Amplifier

Figure 11 shows the closed-loop gain of an amplifier in a noninverting configuration.

$$V_O = V_{IN}\left(1 + \frac{R_F}{R_G}\right) + V_{REF}$$

shows the closed-loop gain of an amplifier in an inverting configuration.

$$V_O = V_{IN}\left(-\frac{R_F}{R_G}\right) + V_{REF}$$

9.2 Low-Side Current Sensing

Power converters use current-mode feedback control for superior transient response and multi-phase load sharing. Inverter stages control the phase currents for torque control in motor drives. Due to its simplicity and low-cost, many of these topologies use difference amplifier based low-side current sensing. Figure 10 shows the use of OPAx863 in a difference amplifier circuit for low-side current sensing.

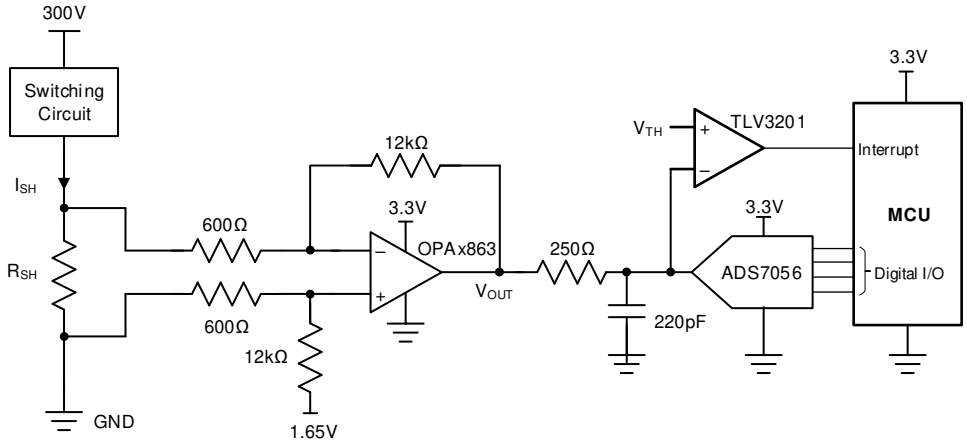

Figure 10. Low-Side Current Sensing in Power Converters

9.2.1 Design Requirements

Table 1. Design Requirements

PARAMETER	DESIGN REQUIREMENT
Shunt resistor	10 mΩ
Input current	15 A_{PP}
Output voltage	3 V_{PP}
Switching frequency	50 kHz
Data acquisition	1 MSPS with 0.1% accuracy
Input voltage due to ground bounce	10 Vpk

In a difference amplifier circuit, the output voltage is given by,

$$V_O = \frac{R_F}{R_G} I_{SH} R_{SH} + V_{REF}$$

For lowest system noise, small values of R_F and R_G are preferred. The smallest value of R_G is limited by the input transient voltage (10V here) seen by the circuit, and is given by,

$$R_G = \frac{V_{IN(max.)} - V_D - V_S}{I_{D(max.)}}$$

Where,

- $V_{IN(maximum)}$ is the maximum input transient voltage seen by the circuit
- V_D is the forward voltage drop of ESD diodes at the amplifier input
- $I_{D(maximum)}$ is the maximum current rating of the ESD diodes at the amplifier input

For a difference amplifier gain of 20 V/V, R_F and R_G of 12kΩ and 600Ω are used, respectively. With a clock frequency of 40 MHz and ADS7056 sampling at 1 MSPS, the available acquisition time for amplifier output settling is 550 ns. Figure 11 shows the simulation results for the circuit in Figure 10. The worst-case peak-to-peak input transient condition is simulated. The OPAx863 devices output settles to within 0.1% accuracy within 543 ns. If use of a slower clock frequency with the ADC is desired, the acquisition time reduces for the same sampling rate which worsens measurement accuracy. Alternatively, the sampling rate may be reduced to recover the required acquisition time and 0.1% accuracy.

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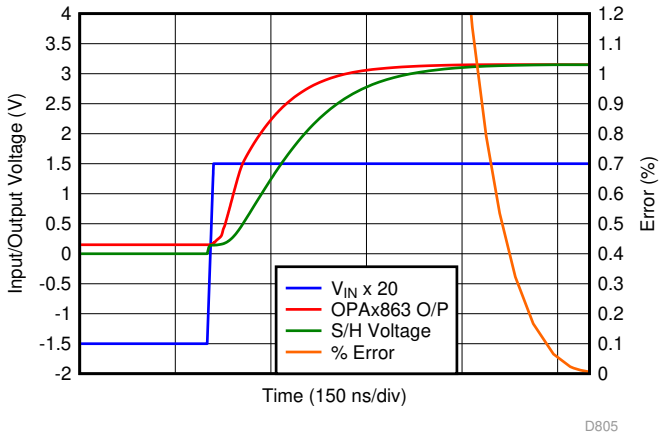

Figure 11. 0.1% Settling Performance

9.3 Transimpedance Amplifier

The high GBWP and small input capacitance of the OPAx863 devices make them an ideal wideband transimpedance amplifier for high-frequency, mid to high transimpedance gain applications.

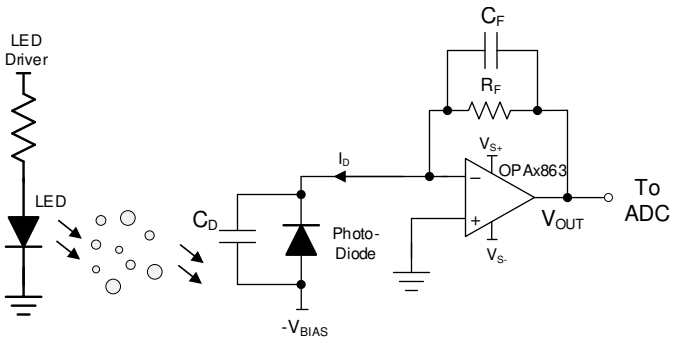

Figure 12. Wideband, High-Sensitivity, Transimpedance Amplifier

9.3.1 Design Requirements

Table 2 lists the design requirements for a high-bandwidth, high-gain transimpedance amplifier circuit.

Table 2. Design Requirements

PARAMETER	DESIGN REQUIREMENT
Target bandwidth	> 2.5 MHz
Transimpedance gain	100 kΩ
Photodiode capacitance	10 pF

9.3.2 Detailed Design Procedure

Figure 12 shows how the OPAx863 devices can be used as a transimpedance amplifier (TIA) for converting a photodiode current into an output voltage. The factors which determine the minimum required gain-bandwidth product (GBW) of the amplifier are the transimpedance gain, small-signal bandwidth and the photodiode capacitance. Increase in the values of any of these three parameters requires higher GBW. Large-area photodiodes with higher sensitivity have a relatively larger photodiode capacitance, sometimes up to 100 pF, which impacts the small-signal bandwidth, which is given below.

$$f_{-3dB} = \sqrt{\frac{GBW}{2\pi R_F C_{IN}}}$$

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The small input capacitance of OPAx863 helps to achieve a wider small-signal bandwidth, mainly limited by the photodiode capacitance. The feedback resistor RF introduces a zero in the noise gain with the total input capacitance CIN and a 40 dB/dec rate of closure. Figure 12 shows the feedback capacitor CF that is needed to cancel the zero due to RF, CIN with a pole in the noise gain, whose value is given below for a 65° phase margin and butterworth response.

$$C_F = \frac{1}{2\pi(0.707)R_F f_{-3dB}}$$

estimates a closed-loop bandwidth of 2.6 MHz. Figure 13 and Figure 14 show the closed-loop gain and phase plots from TINA-TI simulation of the TIA circuit of Figure 12. The 1/β gain curve has a zero from R_F and C_{IN} at 142 kHz and a pole from R_F and C_F cancelling the 1/β zero at 1.87 MHz, resulting in a 20-dB per decade rate-of-closure at the loop-gain crossover frequency (the frequency where A_{OL} equals 1/β), ensuring a stable circuit. A phase margin of 65° is obtained with a closed-loop bandwidth of 2.6 MHz and a 100-kΩ transimpedance gain.

9.3.3 Application Curves

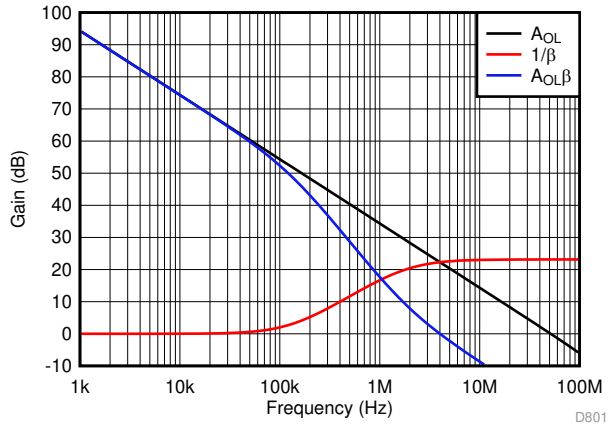

Figure 13. Loop-Gain Magnitude vs Frequency for the Transimpedance Amplifier Circuit of Figure 12

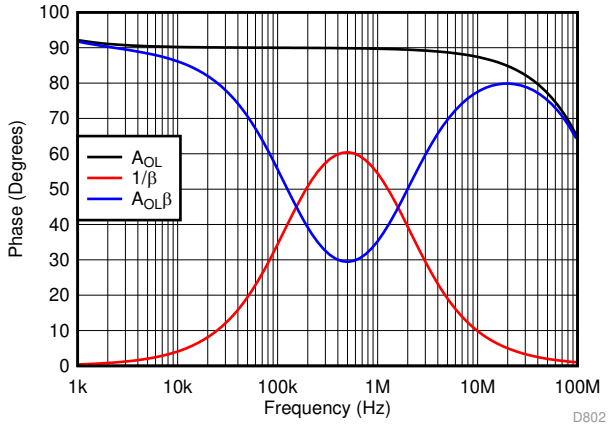

Figure 14. Loop-Gain Phase vs Frequency for the Transimpedance Amplifier Circuit of Figure 12

ADVANCE INFORMATION

9.4 Low-Power SAR ADC Driver and Reference Buffer

Figure 15 shows the use of the OPAx863 devices as a SAR ADC input driver and reference buffer driving the ADS7945. Sensors, which are used for interface with real-world, exhibit high output impedance, and cannot drive SAR ADC inputs directly. A wide-GBW amplifier like the OPAx863 devices are needed to charge the switching capacitors at the SAR ADC input and to settle fast to the required accuracy within the given acquisition time. During the conversion (digitization) phase, the ADC core draws transient current from the reference input which needs to be driven with a wide-GBW amplifier to offer fast settling and maintain a stable reference voltage for superior digitization performance. Due to limitations in precision performance of wide-GBW amplifiers, the OPAx863 devices reference buffer is used in a composite loop with the OPA378 precision amplifier. The precision amplifier maintains low-offset output whereas the OPAx863 devices provide the output drive and fast-settling performance.

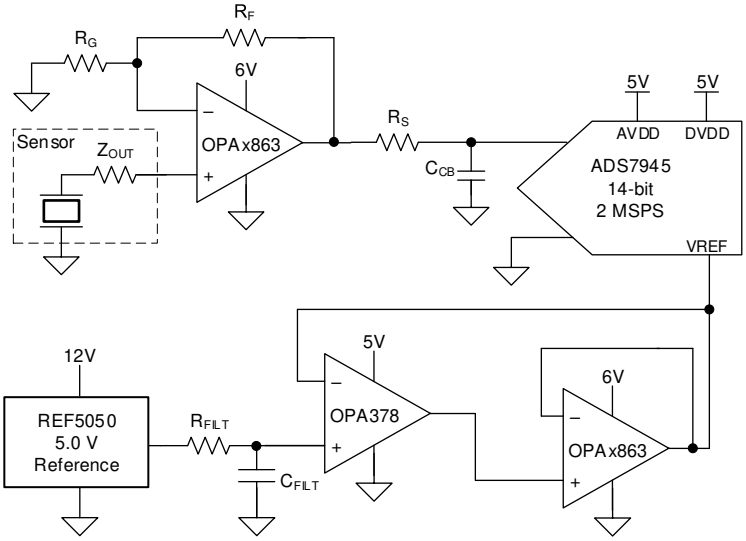

Figure 15. OPAx863 as Low-Power SAR ADC Driver

9.5 Front-End Gain and Filtering

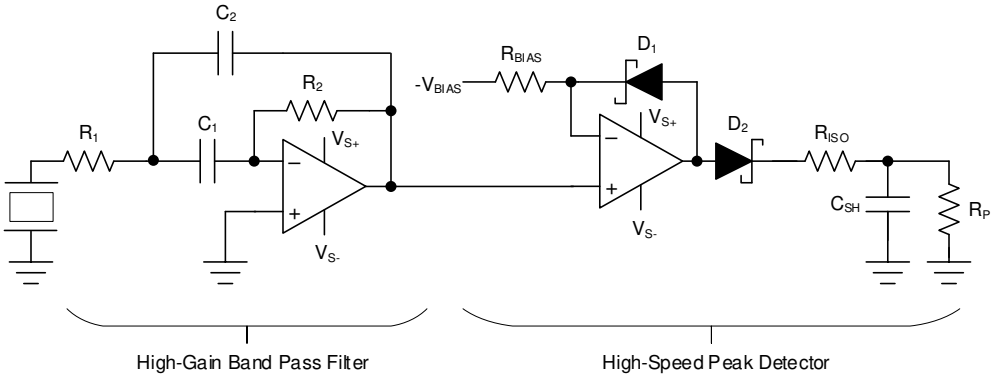

Figure 16. High-Gain Narrow Bandpass Filter and Peak Detector Circuit

Ultrasonic signaling is used for proximity and obstacle detection, level sensing, sonars, and so forth. Such signal chains detect the amplitude of received ultrasonic signal at a particular center frequency. Figure 16 shows a high-gain narrow bandpass filter and peak detector circuit using any of the OPAx863 devices. The signal at the frequency of interest is filtered out, gained and peak detected to report the amplitude at the output of this circuit. The phase information is lost in this circuit. The OPAx863 devices are used with its 50-MHz GBW to add a single-stage gain, and the peak detection capability is easily made with the RRIO capability of these amplifiers.

9.6 Clamp-On Ultrasonic Flow Meter

Ultrasonic flow meters measure rate of flow of a liquid using transit-time difference, t_{12}–t_{21} in Figure 17 which changes with and used to determine the flow rate. Figure 17 shows a representative schematic for a non-intrusive ultrasonic flow meter using the OPAx863 devices and 12-V transducer excitation. For the forward path, the OPAx863 devices are used as a unity-gain buffer for 12-V pulsed transducer excitation at Node 1. At the same time, the receiver circuit at Node 2, also using the OPAx863 devices, first provides an AC-gain followed by a DC-level shift to lead to the PGA, ADC and processing within the MSP430 microcontroller.

For the reverse path, Node 2 and Node 1 use similar transmit and receive circuits discussed above. The OPAx863 devices wide GBW of 50 MHz introduces minimal phase-delay and low-noise for superior flow rate measurement. In battery powered systems, the amplifier stays in power-down mode for a majority of the time, resulting in very small average system-level power consumption and prolonged battery lifetime with its 1.5 µA (maximum) power-down mode quiescent current. Since the transmit and receive signal chains are connected to the same point at the respective node transducers, the OPAx863 devices 12.6-V supply voltage capability enables 12-V transducer excitation capability with damage to the front-end and need for external switches to make a compact solution. This makes the OPAx863 devices suitable for flow measurements in large diameter pipes and non-intrusive flow meters.

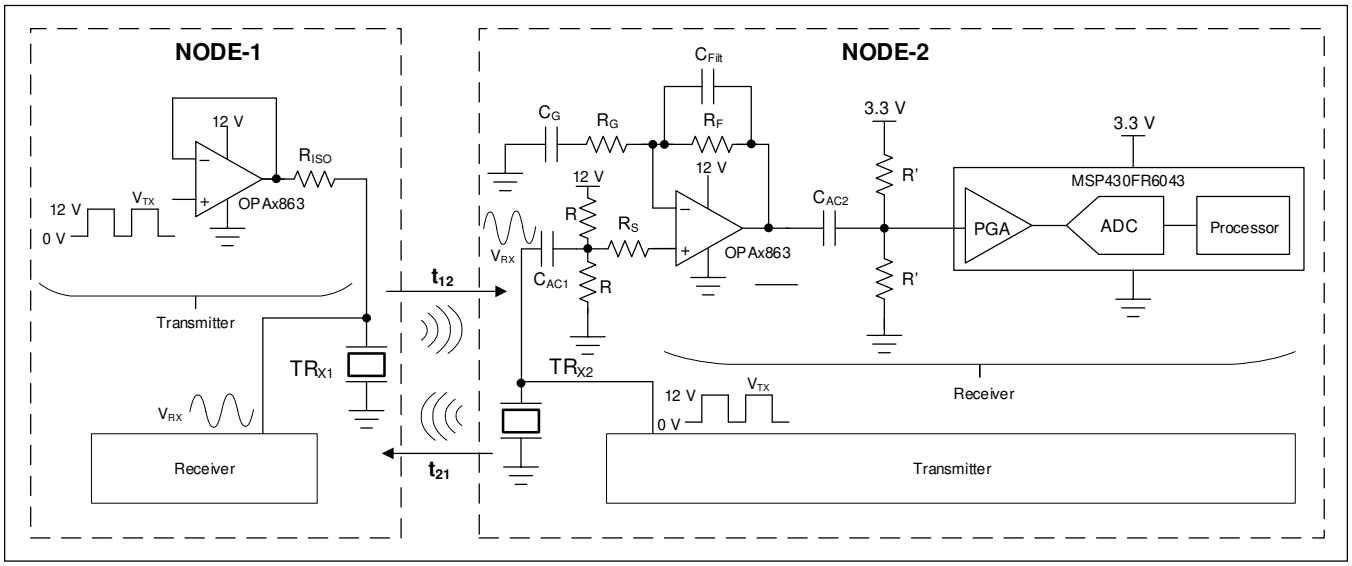

Figure 17. Non-Intrusive Ultrasonic Flow Meter

9.7 Variable Reference Generator Using MDAC

High-speed amplifiers may be used as a voltage buffer at MDAC output to generate a fast settling variable reference voltage. Figure 18 shows a representative circuit using DAC8801 and OPAx863.

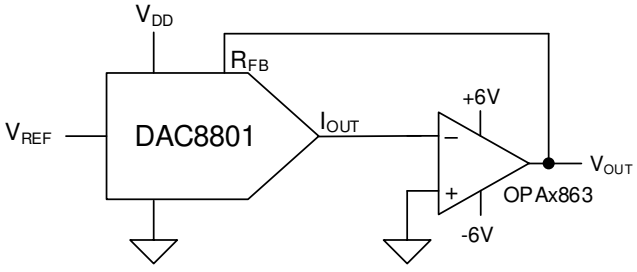

Figure 18. Variable Reference Generator Using MDAC and OPAx863

ADVANCE INFORMATION

10 Power Supply Recommendations

The OPAx863 devices are intended for operation on supplies ranging from 2.7 V to 12.6 V. The OPAx863 devices may operate on single-sided supplies, split and balanced bipolar supplies, or unbalanced bipolar supplies. Operating from a single supply can have numerous advantages. With the negative supply at ground, the DC errors due to the –PSRR term can be minimized. Typically, AC performance improves slightly at 10-V operation with minimal increase in supply current. Minimize the distance (< 0.1 in) from the power supply pins to high-frequency, 0.01-µF decoupling capacitors. A larger capacitor (2.2 µF typical) is used along with a high-frequency, 0.01-µF supply-decoupling capacitor at the device supply pins. For single-supply operation, only the positive supply has these capacitors. When a split-supply is used, use these capacitors from each supply to ground. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the printed circuit board (PCB). An optional supply decoupling capacitor across the two power supplies (for split-supply operation) reduces second harmonic distortion.

11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPAx863 devices require careful attention to board layout parasitics and external component types. The *OPA2863EVM* can be used as a reference when designing the circuit board. Recommendations that optimize performance include:

1. **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability—on the noninverting input, it can react with the source impedance to cause unintentional band-limiting. To reduce unwanted capacitance, open a window around the signal I/O pins in all of the ground and power planes around those pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.
2. **Minimize the distance** (< 0.1 in) from the power-supply pins to high-frequency 0.01-µF decoupling capacitors. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, must also be used on the supply pins. These can be placed somewhat farther from the device and shared among several devices in the same area of the PC board.
3. **Careful selection and placement of external components preserve the high frequency performance of the OPAx863 devices.** Resistors must be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wirewound type resistors in a high frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, must also be placed close to the package. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 10 kΩ, this parasitic capacitance can add a pole or zero close to the GBWP of 50 MHz and subsequently affects circuit operation. Keep resistor values as low as possible consistent with load driving considerations. Lowering the resistor values keep the resistor noise terms low, and minimize the effect of its parasitic capacitance, however lower resistor values increase the dynamic power consumption because R_F and R_G become part of the amplifiers output load network. Transimpedance applications (see the *Transimpedance Amplifier* section) can use whatever feedback resistor is required by the application as long as the feedback compensation capacitor is set considering all parasitic capacitance terms on the inverting node.
4. **Connections to other wideband devices** on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) must be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S for sufficient phase margin and stability. Low parasitic capacitive loads (< 2.5 pF) may not need an R_S because the OPAx863 devices are nominally compensated to operate with a 2.5-pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin) If a long

Layout Guidelines (continued)

trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary onboard, and a higher impedance environment improves distortion. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPAx863 devices are used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device— this total effective impedance must be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value to obtain sufficient phase margin and stability. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, the signal attenuates because of the voltage divider formed by the series output into the terminating impedance.

5. **Take care to design the PCB layout for optimal thermal dissipation.** For the extreme case of 125°C operating ambient, using the approximate maximum 180.3°C/W for the DGK package, and an internal power of 12-V supply × 2.6-mA 125°C supply current (both amplifiers together) gives a maximum internal power dissipation of 31.2 mW. This power gives a 5.6°C increase from ambient to junction temperature. Load power adds to this value and this dissipation must also be calculated to determine the worst-case safe operating point.
6. **Socketing a high speed part like the OPAx863 devices are not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPAx863 devices onto the board.

11.1.1 Thermal Considerations

The OPA2863 does not require heat sinking or airflow in most applications. Maximum allowed junction temperature sets the maximum allowed internal power dissipation. Do not allow the maximum junction temperature to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to half of either supply voltage (for equal split-supplies). Under this condition $P_{DL} = V_S{}^2 / (4 \times R_L)$ where R_L includes feedback network loading.

The power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA2863-DGK (VSSOP package) configured as a unity gain buffer, operating on ±6-V supplies at an ambient temperature of 25°C and driving a grounded 500-Ω load.

$P_D = 12\ V \times 2\ mA + 6^2 / (4 \times 500\ \Omega) = 42\ mW$

Maximum $T_J = 25°C + (0.042\ W \times 180.3°C/W) = 33°C$, which is well below the maximum allowed junction temperature of 150°C.

ADVANCE INFORMATION

11.2 Layout Example

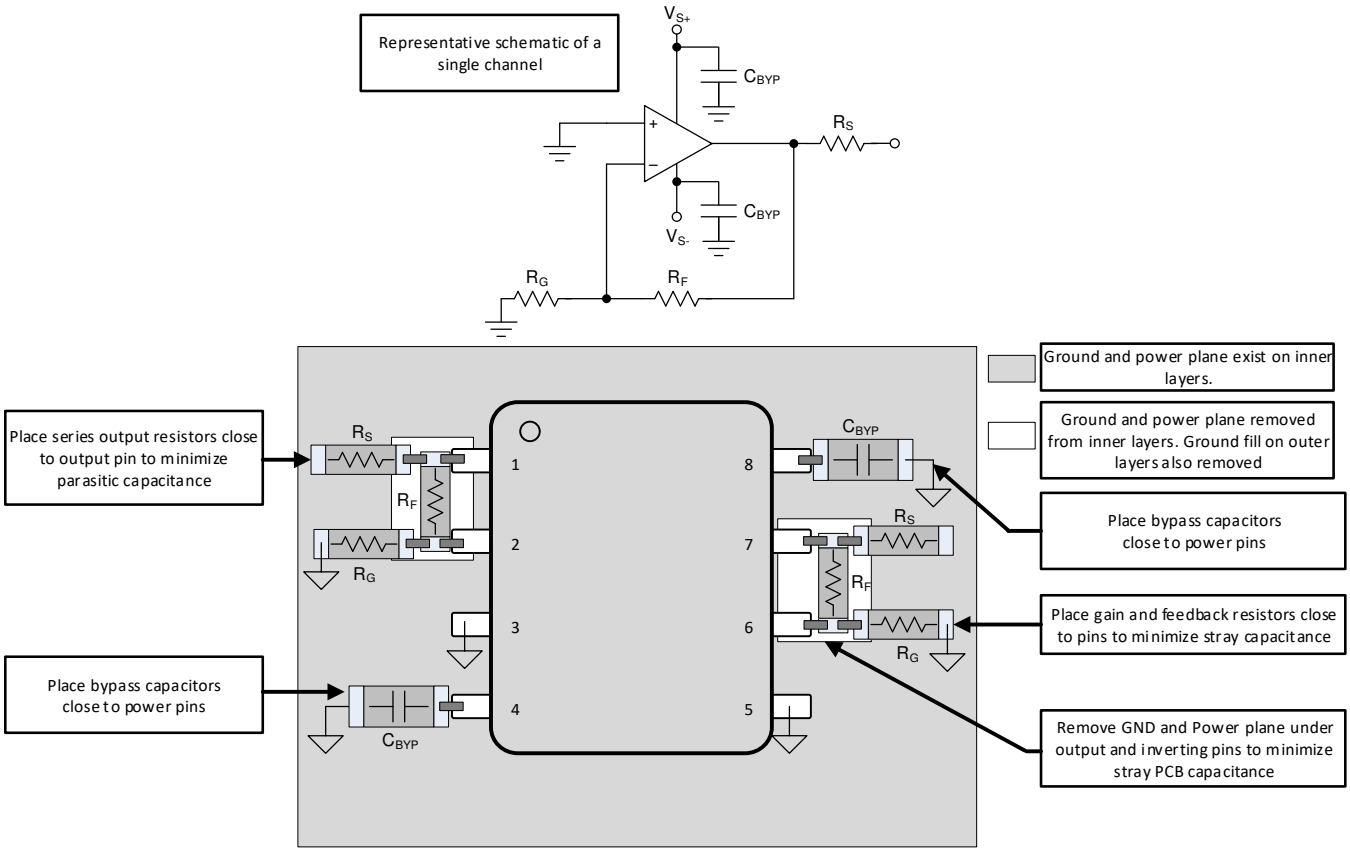

Figure 19. Layout Recommendation

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, OPA2863DGK Evaluation Module.
- Texas Instruments, Semiconductor and IC package Thermal Metrics.
- Texas Instruments, Single-Supply Op Amp Design Techniques.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 3. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA2863	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2863IDGKR	PREVIEW	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2FJ4	
XOPA2863IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS (In work) & Non-Green	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

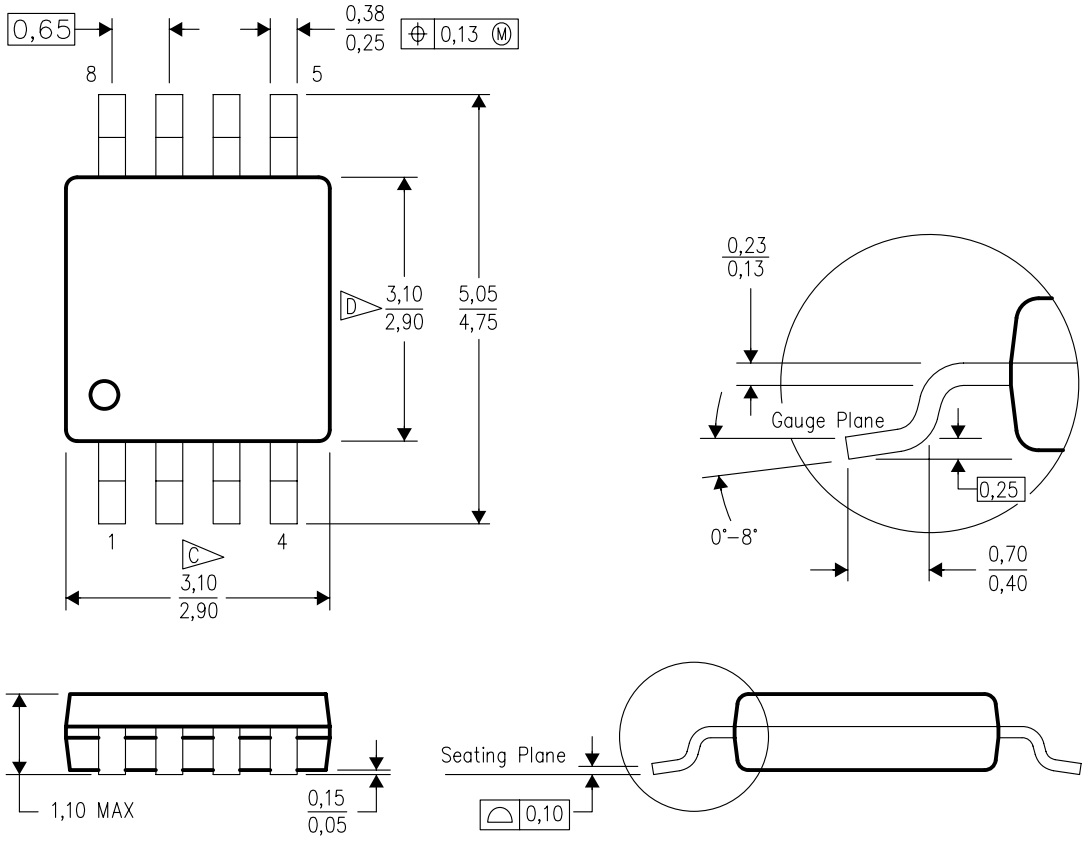
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

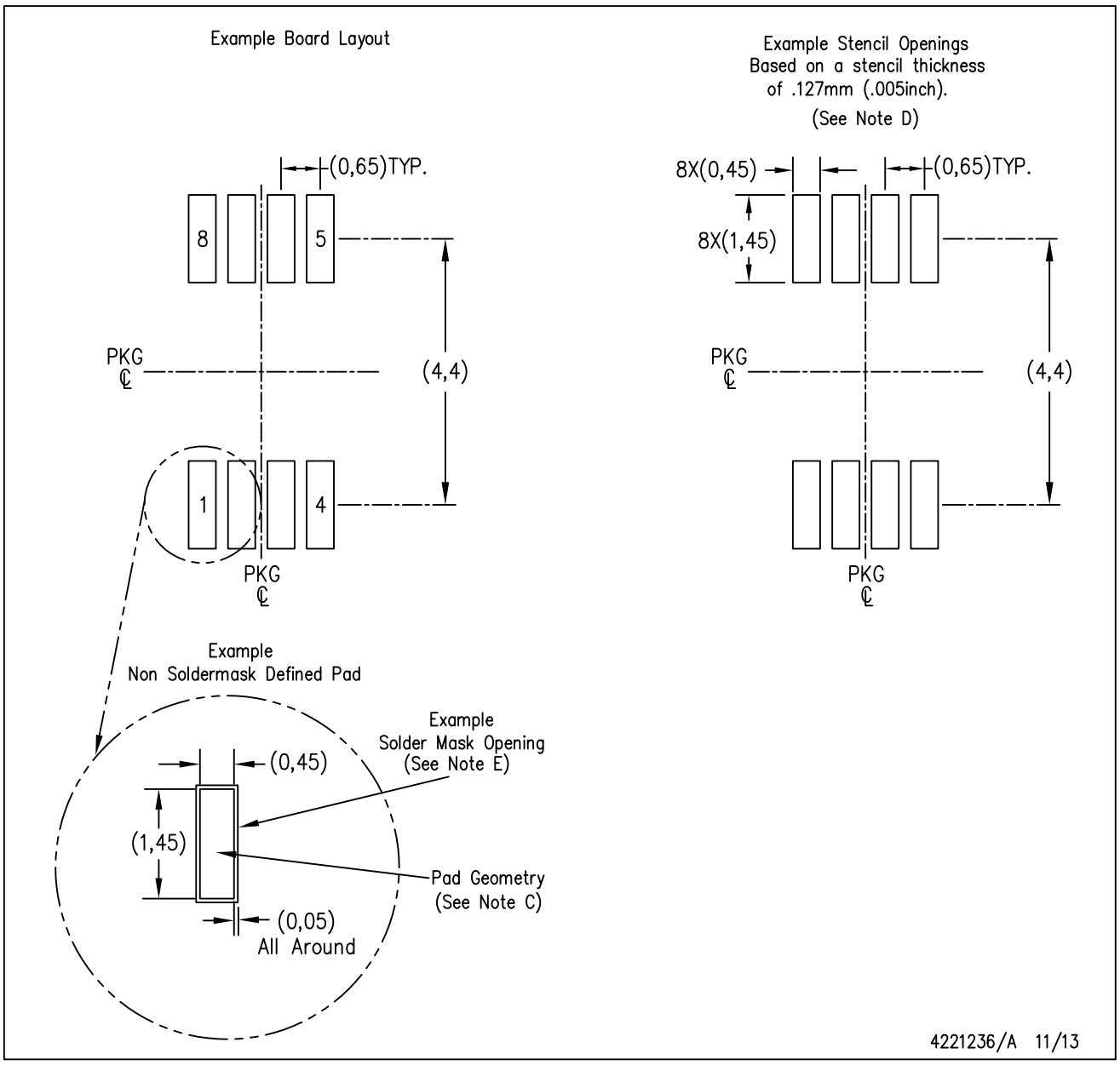
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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