Rail-to-Rail I/O, 2A
POWER AMPLIFIER

FEATURES

- HIGH OUTPUT CURRENT: 2A
- OUTPUT SWINGS TO: 150mV of Rails with I_o = 2A
- THERMAL PROTECTION
- ADJUSTABLE CURRENT LIMIT
- TWO FLAGS: Current Limit and Temperature Warning
- LOW SUPPLY VOLTAGE OPERATION: 2.7V to 5.5V
- SHUTDOWN FUNCTION WITH OUTPUT DISABLE
- SMALL POWER PACKAGE

APPLICATIONS

- THERMOELECTRIC COOLER DRIVER
- LASER DIODE PUMP DRIVER
- VALVE, ACTUATOR DRIVER
- SYNCHRO, SERVO DRIVER
- TRANSDUCER EXCITATION
- GENERAL LINEAR POWER BOOSTER FOR OP AMPS

DESCRIPTION

The OPA567 is a low-cost, high-current, operational amplifier designed for driving a wide variety of loads while operating on low-voltage supplies. It operates from either single or dual supplies for design flexibility and has rail-to-rail swing on the input and output. Output swing is within 300mV of the supply rails, with output current of 2A. Smaller loads allow an output swing closer to the rails.

The OPA567 is unity gain stable, easy to use, and free from the phase inversion problems found in some power amplifiers. High performance is maintained at voltage swings near the output rails.

The OPA567 provides an accurate user-selected current limit set with an external resistor, or digitally adjusted via a Digital-to-Analog Converter (DAC).

The output of the OPA567 can be independently disabled using the Enable pin. This feature saves power and protects the load.

Two flags are provided. The current limit flag, I_FLAG, warns of current limit conditions. T_FLAG is a thermal flag that warns of thermal overstress. The T_FLAG pin can be connected to the Enable pin to provide a thermal shutdown solution.

The OPA567 is available in a tiny 5mm x 5mm Quad Flatpack No-lead (QFN) package and features an exposed thermal pad that enhances thermal and electrical characteristics. It is small and easy to heat sink. The OPA567 is specified for operation over the industrial temperature range, −40°C to +85°C.

OPA567 RELATED PRODUCTS

<table>
<thead>
<tr>
<th>FEATURES</th>
<th>PRODUCT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Same features as the OPA567, plus current monitor output and paralleling ability in SO-20 PowerPAD™ package.</td>
<td>OPA569</td>
</tr>
</tbody>
</table>

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ABSOLUTE MAXIMUM RATINGS\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>(+7.5) V</td>
</tr>
<tr>
<td>Output Current</td>
<td>See SOA Curves</td>
</tr>
<tr>
<td>Voltage (pins 8 and 9):</td>
<td>(V_{\text{O}}) (-0.5) V to ((V+) + 0.5) V</td>
</tr>
<tr>
<td>Current (pins 8 and 9):</td>
<td>(\pm0.5) mA</td>
</tr>
<tr>
<td>Output Short-Circuit (pin 6):</td>
<td>Continuous when thermal protection enabled</td>
</tr>
<tr>
<td>Enable Pin (pin 11):</td>
<td>((V-) - 0.5) V to ((V+) + 7.5) V</td>
</tr>
<tr>
<td>Current Limit Set Pin (pin 6):</td>
<td>(0.5) V to ((V+) + 0.5) V</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>(-55) °C to (+125) °C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>(-65) °C to (+150) °C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>(+150) °C</td>
</tr>
<tr>
<td>ESD Rating:</td>
<td>Human Body Model: (3) kV</td>
</tr>
<tr>
<td></td>
<td>Charged Device Model: (1500) V</td>
</tr>
</tbody>
</table>

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than \(0.5\) V beyond the supply rails should be current limited to \(10\) mA or less. (3) Short-circuit to ground.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

PIN CONFIGURATION

```
+IN
V+, Enable T_FLAG

V+ 1 12 10
V_O 2 11

Metal heat sink (located on bottom)

V_O 3

IN

V+ V_O T_FLAG

\(\text{QFN}\)
```

PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>PIN #</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 12</td>
<td>(V_+)</td>
<td>Positive Power-Supply Voltage</td>
</tr>
<tr>
<td>2, 3</td>
<td>(V_O)</td>
<td>Output</td>
</tr>
<tr>
<td>4, 5</td>
<td>(V_-)</td>
<td>Negative Power-Supply Voltage</td>
</tr>
<tr>
<td>6</td>
<td>(I_{\text{SET}})</td>
<td>Current Limit Set Pin(^{(1)})</td>
</tr>
<tr>
<td>7</td>
<td>(I_{\text{FLAG}})</td>
<td>Current Limit Flag—Indicates when part is in current limit (active LOW).</td>
</tr>
<tr>
<td>8</td>
<td>(\text{IN})</td>
<td>Inverting Input</td>
</tr>
<tr>
<td>9</td>
<td>(\text{+IN})</td>
<td>Noninverting Input</td>
</tr>
<tr>
<td>10</td>
<td>(T_{\text{FLAG}})</td>
<td>Thermal Flag—Indicates thermal stress (active LOW).</td>
</tr>
<tr>
<td>11</td>
<td>ENABLE</td>
<td>Enabled HIGH, shut down LOW.</td>
</tr>
</tbody>
</table>

NOTE: (1) This pin limits the output current. The limited value, \(I_{\text{LIMIT}}\), is \(9800(I_{\text{SET}})\), where \(I_{\text{SET}}\) is the current flowing through the \(I_{\text{SET}}\) pin. This current is programmed by the resistor \(R_{\text{SET}}\) connected to \(V_-\).
ELECTRICAL CHARACTERISTICS: $V_S = +2.7V$ to $+5.5V$

**Boldface limits apply over the specified temperature range, $T_A = -40^\circ C$ to $+85^\circ C$.**

At $T_{CASE} = +25^\circ C$, $R_L = 1k\Omega$, and connected to $V_S/2$, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>OP567</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFFSET VOLTAGE</td>
<td>$V_{OS}$</td>
<td>$V_{OFF}$, $V_S = +5V$</td>
</tr>
<tr>
<td>vs Power Supply</td>
<td>$dV_{OS}/dT$</td>
<td>$T_A = -40^\circ C$ to $+85^\circ C$</td>
</tr>
<tr>
<td>PSRR</td>
<td>$0.5$</td>
<td>$1.3$</td>
</tr>
<tr>
<td>vs Temperature</td>
<td>$12$</td>
<td>$60$</td>
</tr>
</tbody>
</table>

| INPUT BIAS CURRENT | $I_B$ | $\pm 1$ | $\pm 10$ | pA |
| vs Power Supply | $I_{OS}$ | $\pm 2$ | $\pm 10$ | pA |

**NOTES:**

(1) See typical characteristic, **Maximum Output Voltage vs Frequency**.

(2) See typical characteristic, **Total Harmonic Distortion + Noise vs Frequency**.

(3) Swing to the rail is measured in final test. Under those conditions, the $A_{OL}$ is derived from characterization.

(4) See **Safe Operating Area (SOA)** plots.

(5) See the **Typical Characteristics** section. Higher frequency output impedance can affect frequency stability.

(6) External current limit setting resistor is required; see Figure 1.

(7) $I_{SET}$ is the value of the desired current limit and is equal to $9800(I_{SET})$, where $I_{SET}$ is the current through the $I_{SET}$ pin. $I_{LIMT}$ tolerance is proportional to the ratio of $I_{LIMT}/I_{SET}$. Errors from this parameter can be calibrated out—see the Applications Information section.

(8) $V_{SET}$ is a voltage reference that equals the difference between the voltage of the $I_{SET}$ pin and $V-$, and is referenced to the negative rail. Errors from this parameter can be calibrated out—see the Applications Information section.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFFSET VOLTAGE</td>
<td>$V_{OS}$</td>
<td>$\pm 0.5$</td>
<td>$\pm 2$</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>vs Power Supply</td>
<td>$dV_{OS}/dT$</td>
<td>$\pm 1.3$</td>
<td>$\pm 2$</td>
<td>$\mu V/\degree C$</td>
<td></td>
</tr>
<tr>
<td>vs Temperature</td>
<td>$V_S = +5V$, $V_{CM} = (V-) + 0.55V$</td>
<td>$V_S = +2.7V$ to $+5V$, $V_{CM} = (V-) + 0.55V$</td>
<td>$V_S = +2.7V$ to $+5V$, $V_{CM} = (V-) + 0.55V$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>$12$</td>
<td>$60$</td>
<td>$\mu V/\degree C$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>vs Power Supply</td>
<td>$\pm 0.6$</td>
<td>$\pm 1.3$</td>
<td>$\mu V/\degree C$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| INPUT BIAS CURRENT | $I_B$ | $\pm 1$ | $\pm 10$ | pA |
| vs Power Supply | $I_{OS}$ | $\pm 2$ | $\pm 10$ | pA |

| INPUT VOLTAGE RANGE | $V_{CM}$ | $V_S = +5V$, $V_{CM} = (V-) + 0.55V$ | $V_S = +2.7V$ to $+5V$, $V_{CM} = (V-) + 0.55V$ |
| Common-Mode Voltage Range | $80$ | $100$ | $\mathrm{dB}$ |
| Common-Mode Rejection Ratio | $80$ | $80$ | $\mathrm{dB}$ |

| INPUT IMPEDANCE | Differential | $10^{13}$ | $4.5$ | $\Omega$ |
| Common-Mode | $10^{13}$ | $9$ | $\Omega$ |

| OPEN-LOOP GAIN | $A_{OL}$ | $0.2V < V_O < 4.8V$, $R_L = 1k\Omega$, $V_S = +5V$ | $V_S = +2.7V$ to $+5V$, $V_{CM} = (V-) + 0.55V$ |
| Common-Mode Voltage Gain | $100$ | $126$ | $\mathrm{dB}$ |
| $V_S = +5V$, $-0.1V < V_{CM} < 3.2V$ | $60$ | $90$ | $\mathrm{dB}$ |

| FREQUENCY RESPONSE | Gain Bandwidth Product | $GBW$ | $1.2$ | MHz |
| Slew Rate | $SR$ | $1.2$ | $V/\mu s$ |
| Full-Power Bandwidth | $1.2$ | $V/\mu s$ |
| Settling Time: $\pm 0.1\%$ | $G = +1$, $V_O = 4.0V$ Step | $5$ | $\mu s$ |
| Total Harmonic Distortion + Noise | $THD+N$ | See Typical Characteristics | See Typical Characteristics |

| OUTPUT | Voltage Output Swing from Rail | $V_O$ | $V_S = +5V$, $A_{OL} > 100\mathrm{dB}$ | $V_S = +2.7V$ to $+5V$, $A_{OL} > 80\mathrm{dB}$ |
| Maximum Continuous Current Output: dc | $0.2V < V_O < 4.8V$, $R_L = 1k\Omega$, $V_S = +5V$ |
| Capacitive Load Drive | $0.3V < V_O < 4.7V$, $R_L = 1.15k\Omega$, $V_S = +5V$ |
| Closed-Loop Output Impedance | $G = 1$, $f = 10kHz$ | $0.1$ | $\Omega$ |
| | $G = 1$, $f = 1.2MHz$ | $0.44$ | $\Omega$ |
| Output Disabled Output Impedance | $G = 1$, $f = 1.2MHz$ | $12M || 0.25$ | $\Omega$ |

| CURRENT LIMIT ($I_{SET}$ Pin) | Output Current Limit | $I_{LIMT}$ | Externally Adjustable | $\pm 0.2$ to $\pm 2.2$ | $A$ |
| Current Limit Equation | $R_{SET}$ | $R_{SET} = 9800(1.18V/I_{LIMT})$ | $A$ |
| Current Limit Tolerance | $I_{LIMT} = 1A$ | $\pm 3$ | $\%$ |
| Negative | $I_{LIMT} = 1A$ | $\pm 10$ | $\%$ |
| $V_{SET}$ Tolerance | $V = 0.2$ to $V_O = 4.8V$ | $V_O = +5V$, $A_{OL} > 100\mathrm{dB}$ | $V$ |
| $V_O = 0.2$ to $+3.2V$ | $V_O = +5V$, $A_{OL} > 80\mathrm{dB}$ |

| ENABLE-SHUTDOWN INPUT | Enable Pin Bias Current | $V_{IS}$ (High) | $V_{OD}$, Pin Open or Forcex HIGH | $0.2$ | $\mu A$ |
| LOW (Output disabled) | $V_{IS}$ (Low) | $V_{OD}$, Pin Forcex LOW | $V_O = +2.5$ | $V$ |
| Output Disable Time | $R_L = 1\Omega$ | $V_O = +0.8$ | $\mu s$ |
| Output Enable Time | $R_L = 1\Omega$ | $V_O = +1.3$ | $\mu s$ |

**NOTES:**

(1) See typical characteristic, **Maximum Output Voltage vs Frequency**.

(2) See typical characteristic, **Total Harmonic Distortion + Noise vs Frequency**.

(3) Swing to the rail is measured in final test. Under these conditions, the $A_{OL}$ is derived from characterization.

(4) See Safe Operating Area (SOA) plots.

(5) See typical characteristic, **Overshoot vs Load Capacitance**.

(6) See the **Typical Characteristics** section. Higher frequency output impedance can affect frequency stability.

(7) External current limit setting resistor is required; see Figure 1.

(8) $I_{LIMT}$ is the value of the desired current limit and is equal to $9800(I_{SET})$, where $I_{SET}$ is the current through the $I_{SET}$ pin. $I_{LIMT}$ tolerance is proportional to the ratio of $I_{LIMT}/I_{SET}$. Errors from this parameter can be calibrated out—see the Applications Information section.

(9) $V_{SET}$ is a voltage reference that equals the difference between the voltage of the $I_{SET}$ pin and $V-$, and is referenced to the negative rail. Errors from this parameter can be calibrated out—see the Applications Information section.
**ELECTRICAL CHARACTERISTICS: \( V_S = +2.7 \text{V} \) to +5.5V (Cont.)**

**Boldface** limits apply over the specified temperature range, \( T_A = -40^\circ \text{C} \) to +85°C.

At \( T_{CASE} = +25^\circ \text{C} \), \( R_L = 1k\Omega \), and connected to \( V_S/2 \), unless otherwise noted.

### THERMAL FLAG PIN (T FLAG)

<table>
<thead>
<tr>
<th>CONDITION</th>
<th>( T_J ) Limit</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal overstress</td>
<td>147 (^\circ \text{C})</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Normal operation</td>
<td>130 (^\circ \text{C})</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Normal operation: ( (V+) - 0.8V )</th>
<th>Low: ( V_- )</th>
<th>Overstress: ( (V-) + 0.8V )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Flag Pin Voltage</td>
<td>( T_{\text{FLAG}} ) pin sourcing 25(\mu\text{A} )</td>
<td>( V_- )</td>
<td>( (V-) + 0.8V )</td>
</tr>
<tr>
<td>Thermal Flag Pin Voltage</td>
<td>( T_{\text{FLAG}} ) pin sinking 25(\mu\text{A} )</td>
<td>( V_- )</td>
<td>( (V-) + 0.8V )</td>
</tr>
</tbody>
</table>

### CURRENT LIMIT FLAG PIN (I FLAG)

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Normal operation: ( (V+) - 0.8V )</th>
<th>Low: ( V_- )</th>
<th>Overstress: ( (V-) + 0.8V )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Limit Flag Pin Voltage</td>
<td>( I_{\text{FLAG}} ) pin sourcing 25(\mu\text{A} )</td>
<td>( V_- )</td>
<td>( (V-) + 0.8V )</td>
</tr>
<tr>
<td>Current Limit Flag Pin Voltage</td>
<td>( I_{\text{FLAG}} ) pin sinking 25(\mu\text{A} )</td>
<td>( V_- )</td>
<td>( (V-) + 0.8V )</td>
</tr>
</tbody>
</table>

### POWER SUPPLY

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>( V_S )</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specified Voltage Range</td>
<td>( V_S )</td>
<td>+2.7</td>
<td></td>
<td>+5.5</td>
<td>\text{V}</td>
<td></td>
</tr>
<tr>
<td>Operating Voltage Range</td>
<td>( V_S )</td>
<td>+2.5</td>
<td></td>
<td>+5.5</td>
<td>\text{V}</td>
<td></td>
</tr>
<tr>
<td>Quiescent Current(^{(10)})</td>
<td>( I_O )</td>
<td>+0.01</td>
<td></td>
<td></td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Condition</th>
<th>( I_O )</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_O ) = 0, ( I_{\text{LMT}} ) = 200mA, ( V_S = 5V )</td>
<td>+3.4</td>
<td></td>
<td>+6</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_O ) = 0, ( I_{\text{LMT}} ) = 2A, ( V_S = 5V )</td>
<td>+9</td>
<td></td>
<td>+11</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_O ) = 0, ( V_S = 0.8V ), ( V_S = 5V )</td>
<td>+0.01</td>
<td></td>
<td></td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

### TEMPERATURE RANGE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specified Range</td>
<td>Junction Temperature</td>
<td>–40</td>
<td></td>
<td>+85</td>
<td>\text{°C}</td>
</tr>
<tr>
<td>Operating Range</td>
<td>Junction Temperature</td>
<td>–55</td>
<td></td>
<td>+125</td>
<td>\text{°C}</td>
</tr>
<tr>
<td>Storage Range</td>
<td>Junction Temperature</td>
<td>–65</td>
<td></td>
<td>+150</td>
<td>\text{°C}</td>
</tr>
<tr>
<td>Thermal Resistance: Junction-to-Case</td>
<td>( \theta_{JC} )</td>
<td>6</td>
<td></td>
<td>38</td>
<td>\text{°C/W}</td>
</tr>
<tr>
<td>Thermal Resistance: Junction-to-Ambient</td>
<td>( \theta_{JA} )</td>
<td>38</td>
<td></td>
<td></td>
<td>\text{°C/W}</td>
</tr>
</tbody>
</table>

**NOTES:** (10) Quiescent current is a function of the current limit setting. See Adjustable Current Limit and Current Limit Flag Pin in the Applications Information section.
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ C$, $V_S = +5V$, unless otherwise noted.

**OPEN-LOOP GAIN AND PHASE vs FREQUENCY**

**POWER-SUPPLY AND COMMON-MODE REJECTION RATIO vs FREQUENCY**

**OUTPUT SWING TO POSITIVE RAIL vs SUPPLY VOLTAGE**

**OUTPUT SWING TO NEGATIVE RAIL vs SUPPLY VOLTAGE**

**OUTPUT SWING TO POSITIVE RAIL vs TEMPERATURE**

**OUTPUT SWING TO NEGATIVE RAIL vs TEMPERATURE**
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ C$, $V_S = +5V$, unless otherwise noted.

**INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY**

- **Frequency (Hz):** 10, 100, 1k, 10k, 100k
- **Input Voltage Noise (nV/√Hz):** 1000, 100, 10, 1

**0.1Hz TO 10Hz INPUT VOLTAGE NOISE**

- **1µV/div**
- **1s/div**

**MAXIMUM OUTPUT VOLTAGE vs FREQUENCY**

- **Frequency (Hz):** 100, 1k, 100k, 10k, 1M
- **Output Voltage (V_{PP}):** 6, 5, 4, 3, 2, 1, 0

**TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY**

- **Frequency (Hz):** 20, 100, 1k, 10k, 20k
- **THD+N (%):** 10, 1, 0.1, 0.01, 0.001

**QUIESCENT CURRENT vs SUPPLY VOLTAGE**

- **Supply Voltage (V):** 2.7, 3.0, 3.5, 4.0, 4.5, 5.0, 5.5
- **Quiescent Current (mA):** Current Limit = 2A, 1A, 200mA

**QUIESCENT CURRENT vs TEMPERATURE**

- **Temperature (°C):** –55, –25, 5, 25, 55, 85, 105, 125
- **Quiescent Current (mA):** $I_Q$ (Limit = 2A), $I_Q$ (Limit = 200mA)
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ C$, $V_S = +5V$, unless otherwise noted.

**SHUTDOWN CURRENT vs SUPPLY VOLTAGE**

- $i_{LIMIT} = 200mA, 1A, and 2A$

**SHUTDOWN CURRENT vs TEMPERATURE**

**QUIESCENT CURRENT vs CURRENT LIMIT SETTING**

**INPUT BIAS CURRENT vs TEMPERATURE**

**SLEW RATE vs LOAD RESISTANCE**

**SLEW RATE vs TEMPERATURE**
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ C$, $V_S = +5V$, unless otherwise noted.

**VOLTAGE ON $I_{SET}$ PIN vs TEMPERATURE**

**VOLTAGE ON $I_{SET}$ PIN vs SUPPLY VOLTAGE**

**OFFSET VOLTAGE**

**OFFSET VOLTAGE DRIFT**

**SMALL-SIGNAL STEP RESPONSE**

(G = +1, $R_L = 1k\Omega$)

**LARGE-SIGNAL STEP RESPONSE**

(G = +1, $R_L = 1k\Omega$)
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ C$, $V_S = +5V$, unless otherwise noted.

**SMALL-SIGNAL STEP RESPONSE**

$G = +1$, $R_L = 10\Omega$

- 50mV/div
- 10µs/div

**LARGE-SIGNAL STEP RESPONSE**

$G = +1$, $R_L = 10\Omega$

- 1V/div
- 20µs/div

**SMALL-SIGNAL STEP RESPONSE**

$G = +1$, $R_L = 1\Omega$

- 50mV/div
- 20µs/div

**LARGE-SIGNAL STEP RESPONSE**

$G = +1$, $R_L = 1\Omega$

- 1V/div
- 20µs/div

**ENABLE**

(10Ω Load)

- 2V/div
- 4µs/div

Enable/Disable 0.8 to 2.5V Above Negative Supply
Output Driven to +2V

**ENABLE**

(1Ω Load)

- 2V/div
- 10µs/div

Enable/Disable 0.8 to 2.5V Above Negative Supply
Output Driven to +2V
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ C$, $V_S = +5V$, unless otherwise noted.

**DISABLE**

(1Ω Load)

![Waveform Diagram]

Enable/Disable 0.8 to 2.5V Above Negative Supply

Output Driven to +2V

200ns/div

**POWER ON**

(1Ω Load)

Supply 0V to 5V

Output Driven to +2V

1ms/div

**POWER OFF**

(1Ω Load)

Supply 5V to 0V

Output Driven to +2V

1ms/div

**IN AND OUT OF CURRENT LIMIT TRANSIENT**

($R_L = 0.75\Omega$, Current Limit = 2A)

![Waveform Diagram]

**IN AND OUT OF CURRENT LIMIT TRANSIENT**

($R_L = 7.5\Omega$, Current Limit = 200mA)

![Waveform Diagram]
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ C$, $V_S = +5V$, unless otherwise noted.

**OVERLOAD RECOVERY**

$\frac{1V}{div}$

$40\mu s/div$

**NO PHASE INVERSION WITH INPUTS LARGER THAN SUPPLY VOLTAGE**

$\frac{1V}{div}$

$1ms/div$

**CURRENT LIMIT ERROR vs SUPPLY VOLTAGE**

<table>
<thead>
<tr>
<th>Current Limit Error (%)</th>
<th>2.7</th>
<th>3.0</th>
<th>3.5</th>
<th>4.0</th>
<th>4.5</th>
<th>5.0</th>
<th>5.5</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**CURRENT LIMIT ERROR vs TEMPERATURE**

<table>
<thead>
<tr>
<th>Current Limit Error (%)</th>
<th>-55</th>
<th>-35</th>
<th>-15</th>
<th>5</th>
<th>25</th>
<th>45</th>
<th>65</th>
<th>85</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**CURRENT LIMIT ERROR vs OUTPUT CURRENT**

<table>
<thead>
<tr>
<th>Current Limit Error (%)</th>
<th>0.2</th>
<th>0.4</th>
<th>0.6</th>
<th>0.8</th>
<th>1.0</th>
<th>1.2</th>
<th>1.4</th>
<th>1.6</th>
<th>1.8</th>
<th>2.0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**OVERSHOOT vs LOAD CAPACITANCE**

$\frac{Overload (%)}{ Load Capacitance (pF)}$
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ C$, $V_S = +5V$, unless otherwise noted.

CLOSED-LOOP OUTPUT IMPEDANCE

vs FREQUENCY

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Output Impedance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10k</td>
<td>100</td>
</tr>
<tr>
<td>100k</td>
<td>10</td>
</tr>
<tr>
<td>1M</td>
<td>1</td>
</tr>
<tr>
<td>2M</td>
<td>0.1</td>
</tr>
</tbody>
</table>

$G = 1$
APPLICATIONS INFORMATION

BASIC CONFIGURATION

Figure 1 shows the OPA567 connected as a basic non-inverting amplifier. However, the OPA567 can be used in virtually any op amp configuration. A current limit setting resistor (RSET, in Figure 1) is essential to the OPA567 operation, and cannot be omitted.

Power-supply terminals should be bypassed with low series impedance capacitors. Using larger tantalum and smaller ceramic type capacitors in parallel is recommended. Power-supply wiring should have low series impedance.

POWER SUPPLIES

The OPA567 operates with excellent performance from a single (+2.7V to +5.5V) supply or from dual supplies. Power supply voltages do not need to be equal as long as the total voltage remains below 5.5V. Parameters that vary significantly with operating voltage are shown in the Typical Characteristics section.

ADJUSTABLE CURRENT LIMIT AND CURRENT LIMIT FLAG PIN

The OPA567 provides over-current protection to the load through its accurate, user-adjustable current limit (pin 6). The current limit value, I_LIMIT, can be set from 0.2A to 2.2A by controlling the current to the I_SET pin. The current limit, I_LIMIT, will be 9800 • I_SET, where I_SET is the current through the I_SET pin. Setting the current limit requires no special power resistors. The output current does not flow through this pin.

Setting the current limit

As illustrated in Figure 2, the simplest method of setting the current limit is to connect a resistor or potentiometer between

\[ I_{\text{LIMIT}} = 9800 \times \frac{1.18V}{R_{\text{SET}}} \]

Alternatively, the output current limit can be set by applying a voltage source in series with a resistance using the equation:

\[ I_{\text{LIMIT}} = 9800 \times \left( \frac{1.18V - V_{\text{ADJUST}}}{R_{\text{SET}}} \right) \]

The voltage source must be referenced to V–.

FIGURE 1. Basic Connections.

the I_SET pin and V–, the negative supply, according to the formula:

\[ I_{\text{LIMIT}} = 9800 \times \frac{1.18V}{R_{\text{SET}}} \]

Putting a set resistor in series with the potentiometer will prevent potential short-circuit on pin.

FIGURE 2. Setting the Current Limit—Resistor Method.
Current Limit Accuracy

Internally separate circuits monitor the positive and negative current limits. Each circuit output is compared to a single internal reference that is set by the user with an external resistor or a resistor/voltage source combination. The OPA567 employs a patented circuit technique to achieve an accurate and stable current limit throughout the full output range. The initial accuracy of the current limit is typically within 3%; however, because of internal matching limitations, the error can be as much as 15%. The variation of the current limit with factors such as output current level, output voltage, and temperature is shown in the Typical Characteristics section.

When the accuracy of one current limit (sourcing or sinking) is more important than the other, it is possible to set its accuracy to better than 1% by adjusting the external resistor or the applied voltage. The accuracy of the other current limit will still be affected by internal matching.

Current Limit Flag Pin

The OPA567 features an I\textsubscript{FLAG} pin (pin 7) that can be monitored to determine when the part is in current limit. The output signal of the I\textsubscript{FLAG} pin is compatible to standard logic in single-supply applications. The output signal is a CMOS logic gate that switches from V+ to V– to indicate that the amplifier is in current limit. The I\textsubscript{FLAG} pin can source and sink up to 25\textmu{A}. Additional parasitic capacitance between pins 6 and 7 can cause instability at the edge of the current limit. Avoid routing these traces in parallel close to each other.

Quiescent Current Dependence on the Current Limit Setting

The OPA567 is a low-power amplifier, with a typical 3.4mA quiescent current (with the current limit configured for 200mA). The quiescent current varies with the current limit setting—it increases 0.5mA for each additional 200mA increase in the current limit, as shown in Figure 3.

![FIGURE 3. Quiescent Current vs Current Limit Setting.](image)

ENABLE PIN—OUTPUT DISABLE

The Enable pin can disable the OPA567 within microseconds. When disabled, the amplifier draws less than 10\textmu{A} and its output enters a high-impedance state that allows multiplexing. It is important to note that when the amplifier is disabled, the Thermal Flag pin (T\textsubscript{FLAG}) circuitry continues to operate. This feature allows use of the T\textsubscript{FLAG} pin output to implement thermal protection strategies. For more details, please see the section on thermal protection.

The OPA567 Enable pin has an internal pull-up circuit, so it does not have to be connected to the positive supply for normal operation. To disable the amplifier, the Enable pin must be connected to no more than (V–) + 0.8V. To enable the amplifier, either allow the Enable pin to float or connect it to at least (V–) + 2.5V.

The Enable pin is referenced to the negative supply (V–). Therefore, shutdown operation is slightly different in single-supply and dual-supply applications.

In single-supply operation, V– typically equals common ground; thus, the enable/disable logic signal and the OPA567 Enable pin are referenced to the same potential. In this configuration, the logic level and the OPA567 Enable pin can simply be tied together. Disabling the OPA567 occurs for voltage levels of less than 0.8V. The OPA567 is enabled at logic levels greater than 2.5V.

In dual-supply operation, the logic level is referenced to a logic ground. However, the OPA567 Enable pin is still referenced to V–. To disable the OPA567, the voltage level of the logic signal needs to be level-shifted. This level-shifting can be done using an optocoupler, as shown in Figure 4.

Examples of output behavior during disabled and enabled conditions with various load impedances are shown in the typical characteristics section. Please note that this behavior is a function of board layout, load impedances, and bypass strategies. For sensitive loads, the use of a low-pass filter or other protection strategy is recommended.
ENSURING MICROCONTROLLER COMPATIBILITY

Not all microcontrollers output the same logic state after power-up or reset. 8051-type microcontrollers, for example, output logic High levels on their ports while other models power up with logic Low levels after reset.

In configuration (a) shown in Figure 4, the enable/disable signal is applied on the cathode side of the photodiode within the optocoupler. A logic High level causes the OPA567 to be enabled, and a logic Low level disables the OPA567. In configuration (b) of Figure 4, with the logic signal applied on the anode side, a high level disables the OPA567 and a low level enables the op amp.

RAIL-TO-RAIL OUTPUT RANGE

The OPA567 has a class AB output stage with common source transistors that are used to achieve rail-to-rail output swing. It was designed to be able to swing closer to the rail than other existing linear amplifiers, even with high output current levels. A quick way to estimate the output swing with various output current requirements is by using the equation:

\[ V_{SWING\ [typical]} = 0.1 \cdot I_O \]

Plots of the Output Swing vs Output Current, Supply Voltage, and Temperature are provided in the Typical Characteristics section.

RAIL-TO-RAIL INPUT RANGE

The input common-mode voltage range of the OPA567 extends 100mV beyond the supply rails. This is achieved by a complementary input stage with an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel input pair is active for input voltages close to the positive rail while the P-channel input pair is active for input voltages close to the negative rail. The transition point is typically at \((V+) - 1.3V\), and there is a small transition region around the switching point where both transistors are on. It is important to note that the two input pairs can have offsets of different signs and magnitudes. Therefore, as the transition point is crossed, the offset of the amplifier changes. This offset shift accounts for the reduced common-mode rejection ratio over the full input common-mode range.

OUTPUT PROTECTION

Reactive and EMF-generating loads can return load current to the amplifier, causing the output voltage to exceed the power-supply voltage. This damaging condition can be avoided with clamp diodes from the output terminal to the power supplies, as shown in Figure 5. Schottky rectifier diodes with a 3A or greater continuous rating are recommended.

FIGURE 5. Output Protection Diode.

THERMAL FLAG PIN

The OPA567 has thermal sensing circuitry that provides a warning signal when the die temperature exceeds safe limits. Unless the T_FLAG pin is connected to the Enable pin, when this flag is triggered, the part continues to operate even though the junction temperature exceeds 150°C. This default operation allows maximum usable operation in very harsh conditions but degrades reliability. The T_FLAG pin can be used to provide for orderly system shutdown before failure occurs. It can be also used to evaluate the thermal environment to determine need for and appropriate design of a shutdown mechanism.

The thermal flag output signal is from a CMOS logic gate that switches from V+ to V− to indicate that the amplifier is in thermal limit. This flag output pin can source and sink up to 25µA. The T_FLAG pin is HIGH during normal operation. Power dissipated in the amplifier will cause the junction temperature to rise. When the junction temperature exceeds 150°C, the T_FLAG pin will go Low, and remain Low until the amplifier has cooled to 130°C. Despite this hysteresis, with a method of orderly shutdown, the T_FLAG pin can cycle on and off, depending on load and signal conditions. This limits the dissipation of the amplifier but may have an undesirable effect on the load.

It is possible to connect the T_FLAG pin directly to the Enable pin for automatic shutdown protection. When both thermal shutdown and the amplifier enable/disable functions are desired, the externally generated control signal and the T_FLAG pin outputs should be combined with an AND gate; see Figure 6. The temperature protection was designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the OPA567 in and out of thermal shutdown will degrade reliability.
Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable, long-term, continuous operation, the junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loading and signal conditions. For good, long-term reliability, thermal protection should trigger more than 25°C above the maximum expected ambient conditions of your application. This produces a junction temperature of 125°C at the maximum expected ambient condition.

Fast transients of large output current swings (for example, switching quickly from sourcing 2A to sinking 2A) may cause a glitch on the T_FLAG pin. When switching large currents is expected, the use of extra bypass between the supplies or a low-pass filter on the T_FLAG pin is recommended.

### POWER DISSIPATION AND SAFE OPERATING AREA

Power dissipation depends on power supply, signal, and load conditions. It is dominated by the power dissipation of the output transistors. For DC signals, power dissipation is equal to the product of output current, I_OUT and the output voltage across the conducting output transistor (V_S – V_OUT). Dissipation with AC signals is lower. Application Bulletin SBOA022 explains how to calculate or measure power dissipation with unusual signals and loads and can be found at the TI web site (www.ti.com).

Output short-circuits are particularly demanding for the amplifier because the full supply voltage is seen across the conducting transistor. It is very important to note that the temperature protection will not shut the part down in over-temperature conditions, unless the T_FLAG pin is connected to the Enable pin; see the section on Thermal Flag.

Figure 7 shows the safe operating area at room temperature with various heatsinking efforts. Note that the safe output current decreases as (V_S – V_OUT) increases. Figure 8 shows the safe operating area at various temperatures with the metal heatsink being soldered to a 2oz copper pad.

The power that can be safely dissipated in the package is related to the ambient temperature and the heatsink design. The QFN package was specifically designed to provide excellent power dissipation, but board layout greatly influences the heat dissipation of the package. Refer to the QFN Package section for further details.

The OPA567 has a junction-to-ambient thermal resistance (θ_JA) value of 38°C/W when soldered to a 2oz copper plane. This value can be further decreased by the addition of forced air. See Figure 9 for the junction-to-ambient thermal resistance of the QFN-12 package.

Junction temperature should be kept below 125°C for reliable operation. The junction temperature can be calculated by:

\[ T_J = T_A + P_D \theta_{JA} \]

where
- \( \theta_{JA} = \theta_{JC} + \theta_{CA} \)
- \( T_J \) = Junction Temperature (°C)
- \( T_A \) = Ambient Temperature (°C)
- \( P_D \) = Power Dissipated (W)
- \( \theta_{JA} \) = Junction-to-Ambient Thermal Resistance
- \( \theta_{JC} \) = Junction-to-Case Thermal Resistance
- \( \theta_{CA} \) = Case-to-Air Thermal Resistance

The Maximum Power Dissipation vs Temperature for the heatsinking methods referenced in Figure 9 is shown in Figure 10.

FIGURE 10. Maximum Power Dissipation vs Temperature.

To appropriately determine required heatsink area, required power dissipation should be calculated and the relationship between power dissipation and thermal resistance should be considered to minimize shutdown conditions and allow for proper long-term operation (junction temperature of 125°C). Once the heatsink area has been selected, worst-case load conditions should be tested to ensure proper thermal protection.

For applications with limited board size, refer to Figure 11 for the approximate thermal resistance relative to the number of thermal vias. The QFN-12 package is well suited for continuous power levels, as shown in Figure 10. Higher power levels may be achieved in applications with a low on/off duty cycle.

FIGURE 11. Thermal Resistance vs Number of Thermal Vias.

FEEDBACK CAPACITOR IMPROVES RESPONSE

For optimum settling time and stability with higher impedance feedback networks ($R_F > 50\, \Omega$), it may be necessary to add a feedback capacitor across the feedback resistor, $R_F$, as shown in Figure 12. This capacitor compensates for the zero created by the feedback network impedance and the input capacitance of the OPA567 (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks.

The size of the capacitor needed is estimated using the equation:

$$R_{IN} \cdot C_{IN} = R_F \cdot C_F$$

where $C_{IN}$ is the sum of the input capacitance of the OPA567 plus the parasitic layout capacitance.

FIGURE 12. Feedback Capacitor for Use with Higher Impedance Networks.
QFN THERMALLY ENHANCED PACKAGE
The OPA567 uses the QFN-12 package, a thermally-enhanced package designed to eliminate the use of bulky heat sinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See QFN/SON PCB Attachment Application Note (SLUA271) located at www.ti.com.

The thermal resistance junction-to-ambient \( (R_{θJA}) \) of the QFN package depends on the PCB layout. Using thermal vias and wide PCB traces improve thermal resistance. The thermal pad must be soldered to the PCB. The thermal pad should either be left floating or connected to V–.

LAYOUT GUIDELINES
The OPA567 is a power amplifier that requires proper layout for best performance. An example layout is appended to the end of this datasheet. Refinements to this layout may be required based on assembly process requirements.

Keep power-supply leads as short as possible. This practice will keep inductance low and resistive losses at a minimum. A minimum of 18 gauge wire thickness is recommended for power-supply leads. The wire length should be less than 8 inches.

Proper power-supply bypassing with low ESR capacitors is essential to achieve good performance. A parallel combination of 100nF ceramic and 47µF tantalum bypass capacitors will provide low impedance over a wide frequency range. Bypass capacitors should be placed as close as practical to the power-supply pins of the OPA567.

PCB traces conducting high currents, such as from output to load or from the power-supply connector to the power-supply pins of the OPA567 should be kept as wide and short as possible. This practice will keep inductance low and resistive losses to a minimum.

The nine holes in the landing pattern for the OPA567 are for the thermal vias that connect the thermal pad of the OPA567 to the heatsink area on the PCB. All traces conducting high currents are very wide for lowest inductance and minimal resistive losses.
FIGURE 13. Grounded Anode LED Driver.


## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (3)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA567AIRHGR</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RHG</td>
<td>12</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-55 to 125</td>
<td>OPA 567AI</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA567AIRHGT</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RHG</td>
<td>12</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-55 to 125</td>
<td>OPA 567AI</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**

- **Reel Diameter**
- **Reel Width (W1)**

**TAPE DIMENSIONS**

- **K0** Dimension designed to accommodate the component thickness
- **B0** Dimension designed to accommodate the component length
- **A0** Overall width of the carrier tape
- **P1** Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- **Pocket Quadrants**
- **Sprocket Holes**
- **User Direction of Feed**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA567AIRHGR</td>
<td>VQFN</td>
<td>RHG</td>
<td>12</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>5.3</td>
<td>5.3</td>
<td>1.5</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
<tr>
<td>OPA567AIRHGT</td>
<td>VQFN</td>
<td>RHG</td>
<td>12</td>
<td>250</td>
<td>180.0</td>
<td>12.4</td>
<td>5.3</td>
<td>5.3</td>
<td>1.5</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA567AIRHGR</td>
<td>VQFN</td>
<td>RHG</td>
<td>12</td>
<td>2500</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
</tr>
<tr>
<td>OPA567AIRHGT</td>
<td>VQFN</td>
<td>RHG</td>
<td>12</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
RHG (S-PVQFN-N12)  PLASTIC QUAD FLATPACK NO-LEAD

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO-220.
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

NOTE: A. All linear dimensions are in millimeters
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA27L, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com.<http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tapping recommendations for vias placed in the thermal pad.
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