OPA827 Low-Noise, High-Precision, JFET-Input Operational Amplifier

1 Features

- Input Voltage Noise Density: 4 nV/√Hz at 1 kHz
- Input Voltage Noise: 0.1 Hz to 10 Hz: 250 nV_{PP}
- Input Bias Current: 10 pA (Maximum)
- Input Offset Voltage: 150 µV (Maximum)
- Input Offset Drift: 2 µV/°C (Maximum)
- Gain Bandwidth: 22 MHz
- Slew Rate: 28 V/µs
- Quiescent Current: 4.8 mA/Ch
- Wide Supply Range: ±4 V to ±18 V
- Packages: 8-Pin SOIC and 8-Pin VSSOP

2 Applications

- ADC Drivers
- DAC Output Buffers
- Test Equipment
- Medical Equipment
- PLL Filters
- Seismic Applications
- Transimpedance Amplifiers
- Integrators
- Active Filters

3 Description

The OPA827 series of JFET operational amplifiers combine outstanding DC precision with excellent AC performance. These amplifiers offer low offset voltage (150 µV, maximum), very low drift over temperature (0.5 µV/°C, typical), low-bias current (3 pA, typical), and very low 0.1-Hz to 10-Hz noise (250 nV_{PP}, typical). The device operates over a wide supply voltage range, ±4 V to ±18 V on a low supply current (4.8 mA/Ch, typical).

Excellent AC characteristics, such as a 22-MHz gain bandwidth product (GBW), a slew rate of 28 V/µs, and precision DC characteristics make the OPA827 series well-suited for a wide range of applications including 16-bit to 18-bit mixed signal systems, transimpedance (I/V-conversion) amplifiers, filters, precision ±10-V front ends, and professional audio applications.

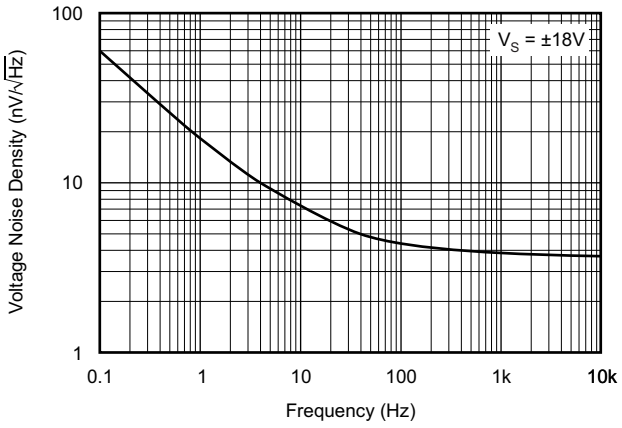
The OPA827 is available in both 8-pin SOIC and 8-pin VSSOP surface-mount packages, and is specified from –40°C to 125°C.

Device Information(1)

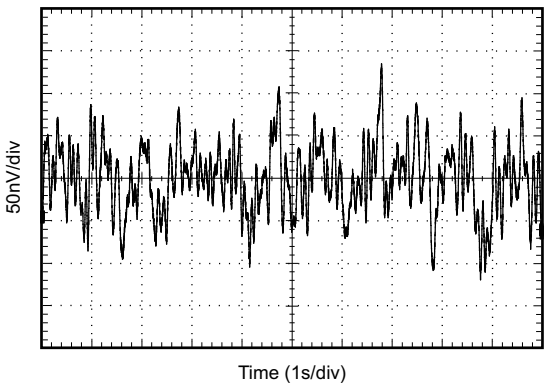
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA827	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Input Voltage Noise Density vs Frequency



0.1-Hz to 10-Hz Noise



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (May 2012) to Revision I — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Package/Ordering Information* table, see POA at the end of the data sheet ... 4
- Changed values in the *Thermal Information* table to align with JEDEC standards ... 5

Changes from Revision G (February 2012) to Revision H — **Page**

- Updated Figure 3 ... 8
- Updated Figure 4 ... 8

Changes from Revision F (March 2009) to Revision G — **Page**

- Changed *Input bias current* and *Input offset drift* Features bullets ... 1
- Changed product status from Mixed Status to Production Data ... 1
- Changed description of amplifier drift and bias current in first paragraph of *Description* section ... 1
- Deleted high grade (OPA827I) option and footnote 2 from *Package/Ordering Information* table ... 4
- Deleted high grade (OPA827I) option from Electrical Characteristics table ... 6
- Changed Offset Voltage, *Input Offset Voltage Drift* parameter typical and maximum specifications in Electrical Characteristics table ... 6
- Changed Input Bias Current section specifications in Electrical Characteristics table ... 6
- Changed -40°C to +85°C *Input Bias Current* parameter unit ... 6
- Added Frequency Response, *Slew Rate* parameter minimum specification to Electrical Characteristics table ... 6
- Added Output, *Short-Circuit Current* parameter minimum specification to Electrical Characteristics table ... 7
- Updated Figure 7 ... 8
- Updated Figure 8 ... 8

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- Updated Figure 9 8
- Updated Figure 11 8
- Updated Figure 12 8
- Updated Figure 14 9

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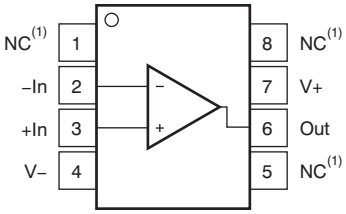
5 Pin Configuration and Functions

D and DGK Packages
8-Pin SOIC and VSSOP
Top View



(1) NC denotes no internal connection.

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
+IN	3	I	Noninverting input
–IN	2	I	Inverting input
NC	1, 5, 8	—	No internal connection (can be left floating)
OUT	6	O	Output
V+	7	—	Positive power supply
V–	4	—	Negative power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		40	V
Input voltage(2)	(V–) – 0.5	(V+) + 0.5	V
Input current(2)		±10	mA
Differential input voltage		$\pm V_S$	V
Output short-circuit(3)	Continuous		
Operating temperature, T_A	–55	150	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current-limited to 10 mA or less.
(3) Short-circuit to $V_S/2$ (ground in symmetrical dual-supply setups).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	±4		±18	V
T_A	Specified temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA827		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60	130	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50	120	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

at V_S = ±4 V to ±18 V, T_A = 25°C, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = ±15 V, V_{CM} = 0 V		75	150	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C		0.1	2	µV/°C
PSRR	Input offset voltage vs power supply			0.2	1	µV/V
		T_A = –40°C to 125°C			3	
INPUT BIAS CURRENT						
I_B	Input bias current			±3	±10	pA
		T_A = –40°C to 85°C			±500	pA
		T_A = –40°C to 125°C			±5	nA
I_{OS}	Input Offset Current			±3	±10	pA
NOISE						
e_n	Input Voltage Noise:	f = 0.1 Hz to 10 Hz, V_S = ±18 V, V_{CM} = 0 V		250		nV_{PP}
	Input Voltage Noise Density	f = 1 kHz, V_S = ±18 V, V_{CM} = 0 V		4		$nV/\sqrt{Hz}$
		f = 10 kHz, V_S = ±18 V, V_{CM} = 0 V		3.8		
i_n	Input current noise density	f = 1 kHz, V_S = ±18 V, V_{CM} = 0 V		2.2		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) + 3		(V+) – 3	V
CMRR	Common-mode rejection ratio	(V–) + 3 V ≤ V_{CM} ≤ (V+) – 3 V, V_S < 10 V	104	114		dB
		(V–) + 3 V ≤ V_{CM} ≤ (V+) – 3 V, V_S ≥ 10 V	114	126		
		(V–) + 3 V ≤ V_{CM} ≤ (V+) – 3 V, V_S < 10 V T_A = –40°C to 125°C	100			
		(V–) + 3 V ≤ V_{CM} ≤ (V+) – 3 V, V_S ≥ 10 V T_A = –40°C to 125°C	110			
INPUT IMPEDANCE						
Differential				10^{13} ‖ 9		Ω ‖ pF
Common-mode				10^{13} ‖ 9		Ω ‖ pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 3 V ≤ V_O ≤ (V+) – 3 V, R_L = 1 kΩ	120	126		dB
		(V–) + 3 V ≤ V_O ≤ (V+) – 3 V, R_L = 1 kΩ T_A = –40°C to 125°C	114			
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	G = +1		22		MHz
SR	Slew rate	G = –1	20	28		V/µs
t_S	Settling time	±0.01%, 10-V step, G = –1, C_L = 100 pF		550		ns
		0.00075% (16-bit), 10-V step, G = –1, C_L = 100 pF		850		ns
	Overload recovery time	Gain = –10		150		ns
THD+N	Total Harmonic Distortion + Noise	G = +1, f = 1 kHz		0.00004%		
		V_O = 3 V_{RMS}, R_L = 600 Ω		–128		dB

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Electrical Characteristics (continued)

at V_S = ±4 V to ±18 V, T_A = 25°C, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing	R_L = 1 kΩ, A_{OL} > 120 dB	(V–) + 3		(V+) – 3	V
		R_L = 1 kΩ, A_{OL} > 114 dB T_A = –40°C to 125°C	(V–) + 3		(V+) – 3	
I_{OUT}	Output current	$\|V_S - V_{OUT}\|$ < 3 V		30		mA
I_{SC}	Short-circuit current		±55	±65		mA
C_{LOAD}	Capacitive load drive		See *Typical Characteristics*			
Z_O	Open-loop output impedance		See *Typical Characteristics*			
POWER SUPPLY						
V_S	Specified voltage		±4		±18	V
I_Q	Quiescent current (per amplifier)	I_{OUT} = 0A		4.8	5.2	mA
		T_A = –40°C to 125°C			6	

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6.6 Typical Characteristics

At T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

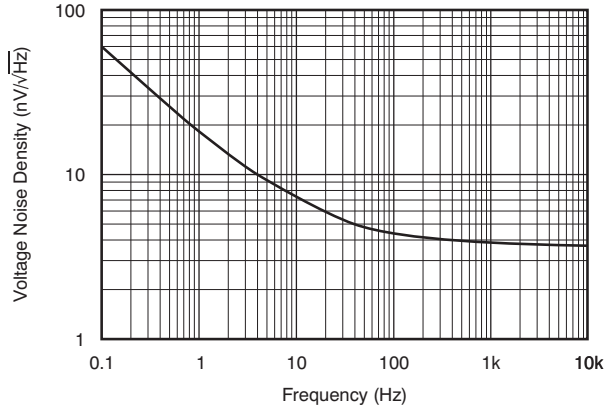

Figure 1. Input Voltage Noise Density vs Frequency

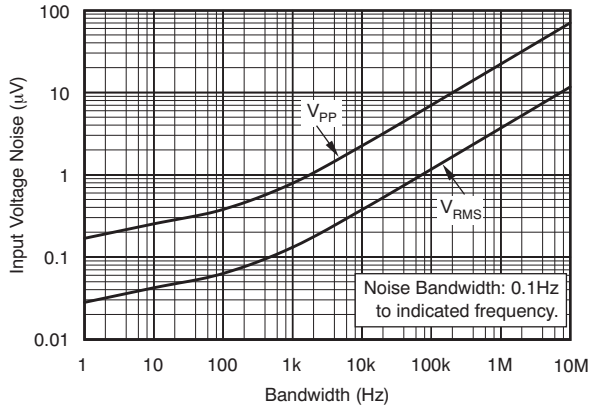

Figure 2. Integrated Input Voltage Noise vs Bandwidth

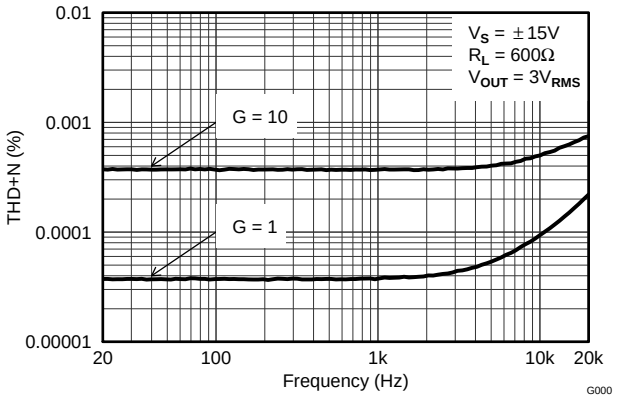

Figure 3. Total Harmonic Distortion + Noise Ratio vs Frequency

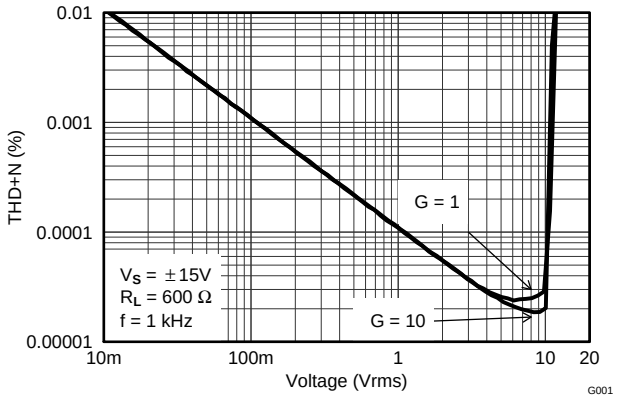

Figure 4. Total Harmonic Distortion + Noise Ratio vs Amplitude

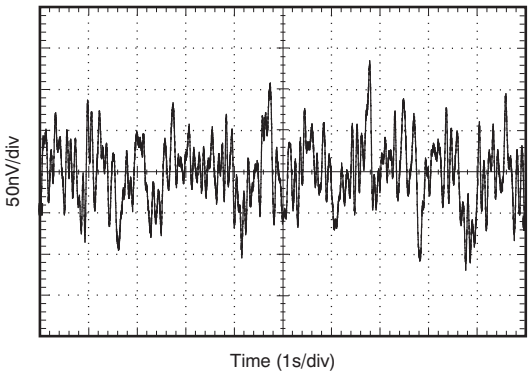

Figure 5. 0.1-Hz to 10-Hz Noise

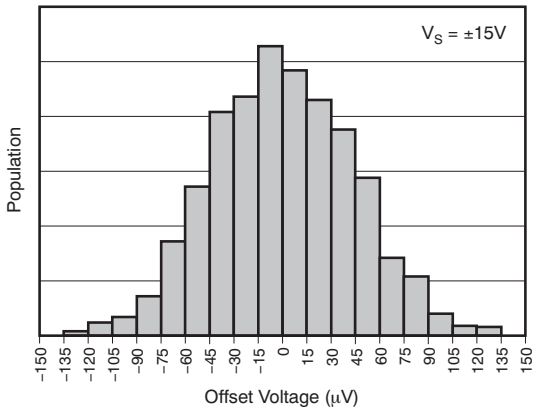

Figure 6. Offset Voltage Production Distribution

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Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

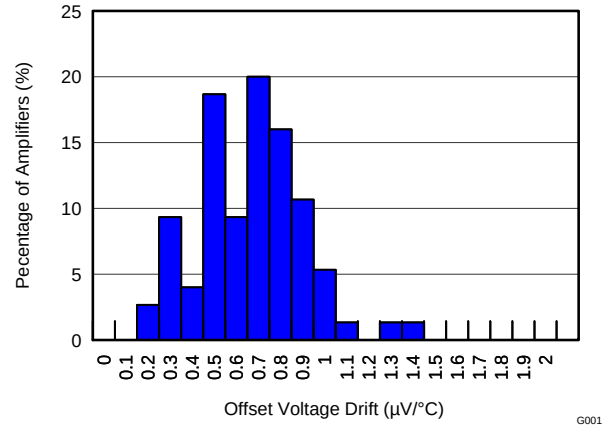

Figure 7. Offset Voltage Drift Production Distribution

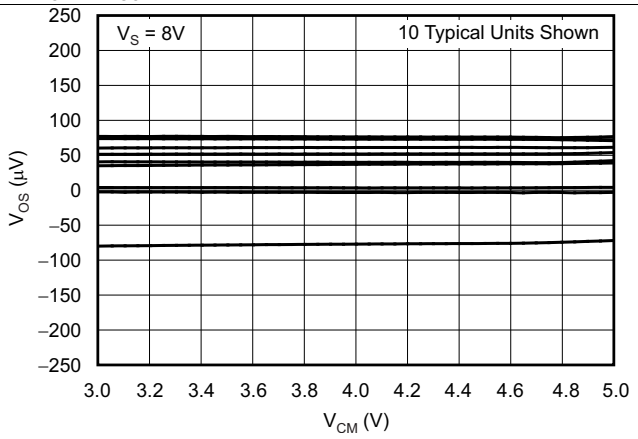

Figure 8. Offset Voltage vs Common-Mode Voltage

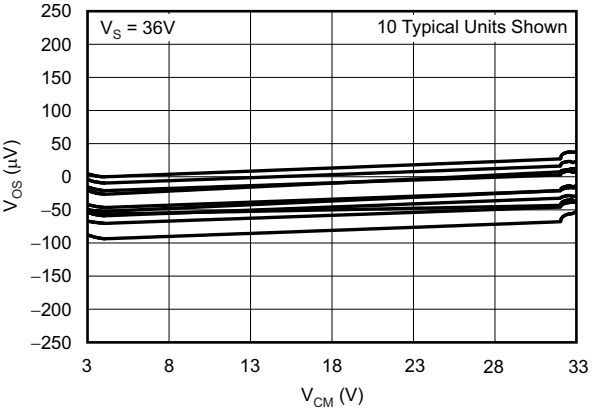

Figure 9. Offset Voltage vs Common-Mode Voltage

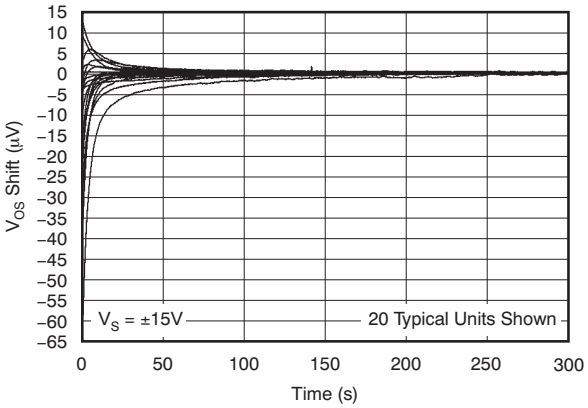

Figure 10. V_{OS} Warmup

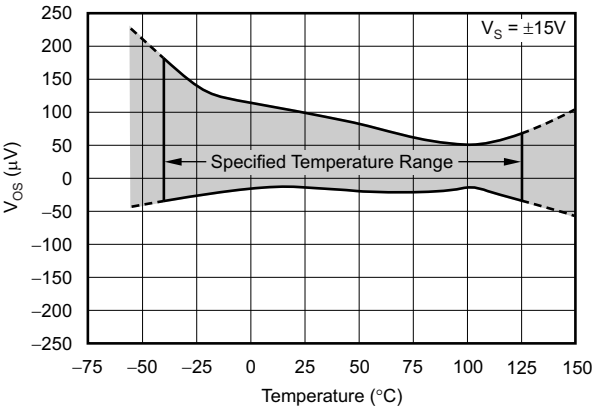

Figure 11. Offset Voltage vs Temperature

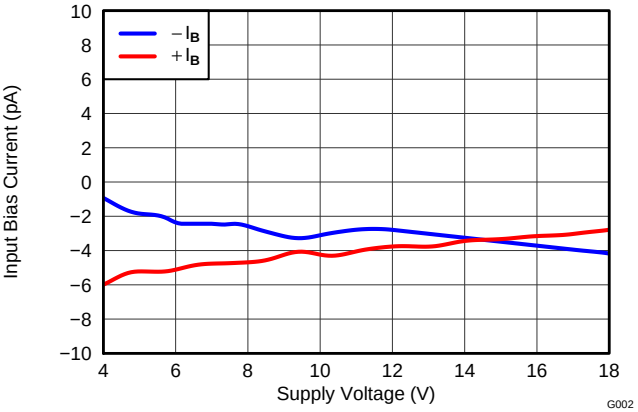

Figure 12. Input Bias Current and Offset Current vs Supply Voltage

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Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

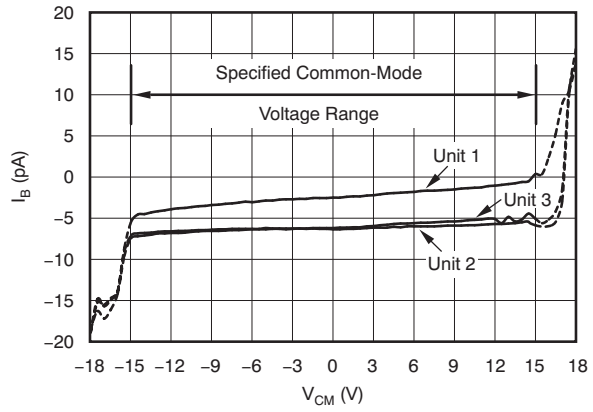

Figure 13. Input Bias Current vs Common-Mode Voltage

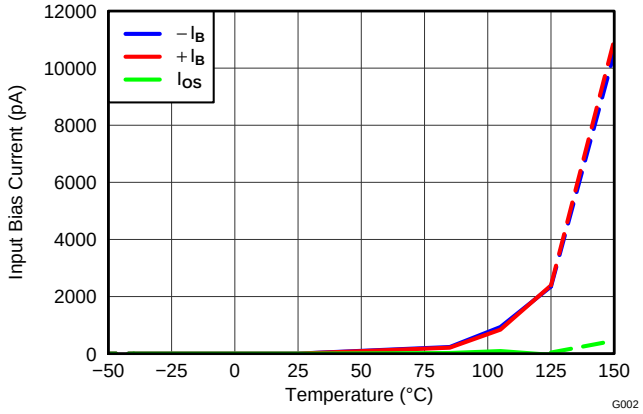

Figure 14. Input Bias Current vs Temperature

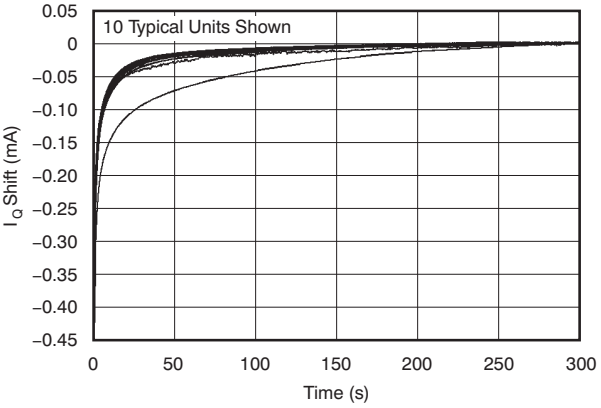

Figure 15. Normalized Quiescent Current vs Time

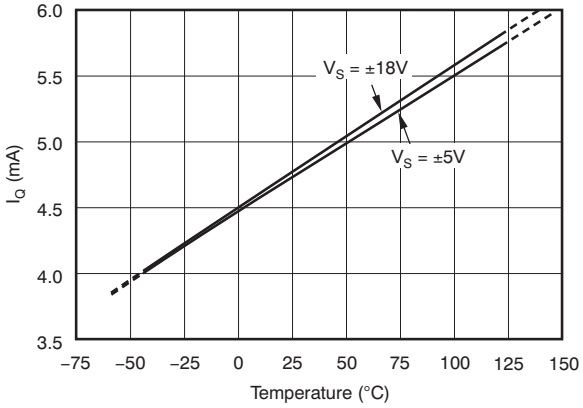

Figure 16. Quiescent Current vs Temperature

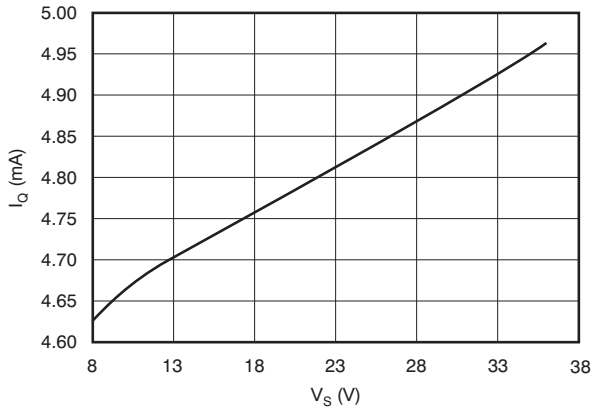

Figure 17. Quiescent Current vs Supply Voltage

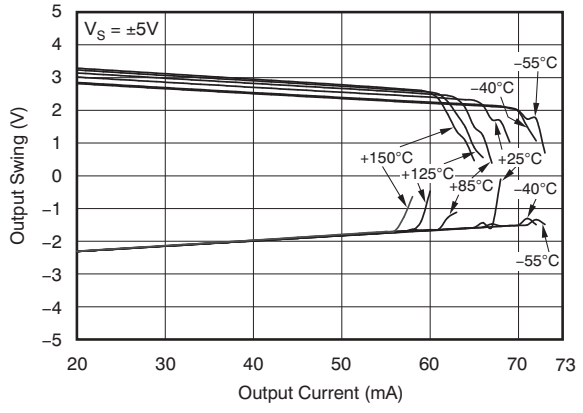

Figure 18. Output Voltage Swing vs Output Current

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Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

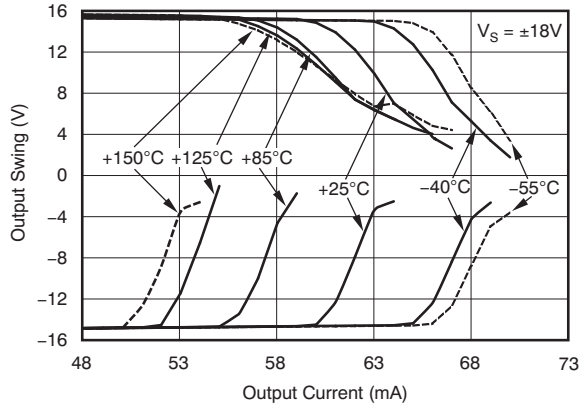

Figure 19. Output Voltage Swing vs Output Current

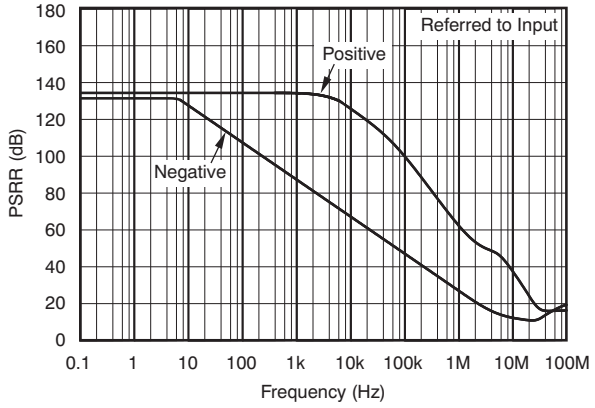

Figure 20. Power-Supply Rejection Ratio vs Frequency

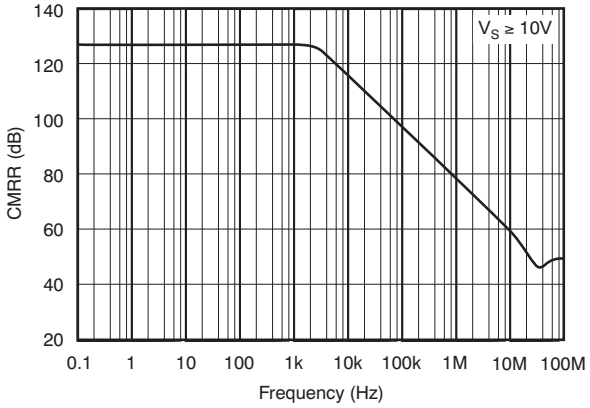

Figure 21. Common-Mode Rejection Ratio vs Frequency

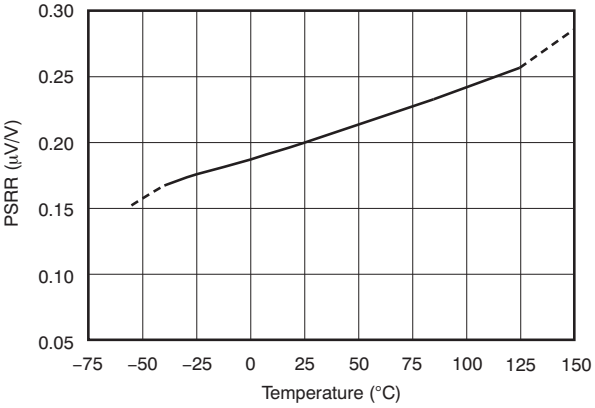

Figure 22. Power-Supply Rejection Ratio vs Temperature

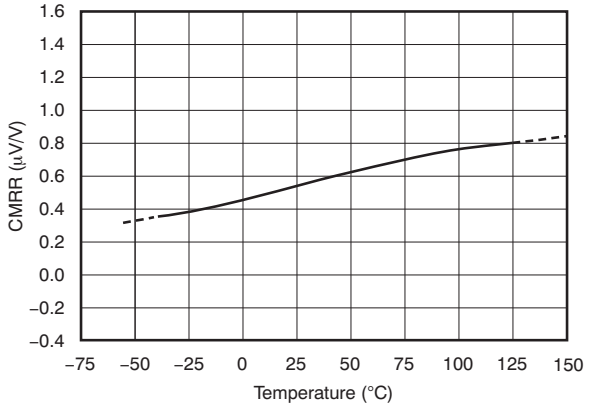

Figure 23. Common-Mode Rejection Ratio vs Temperature

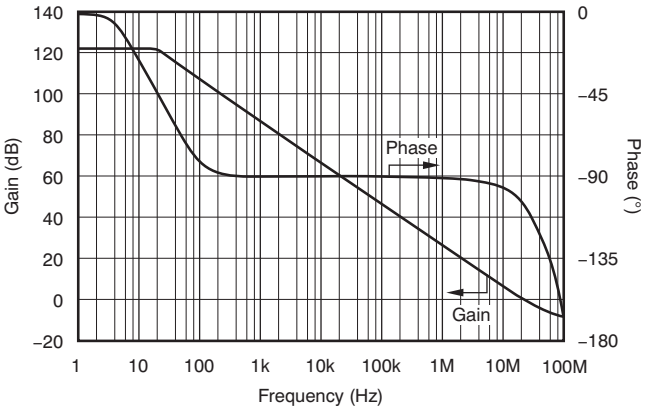

Figure 24. Open-Loop Gain and Phase vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

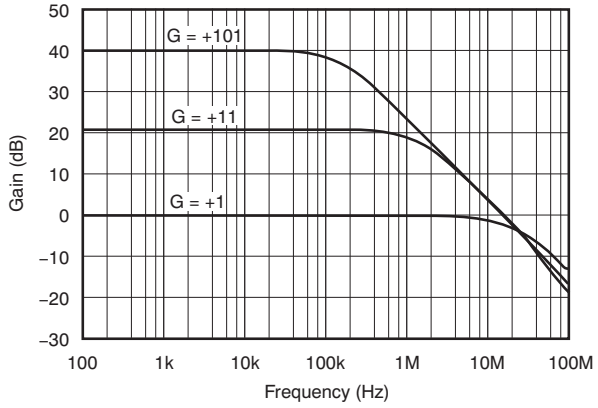

Figure 25. Closed-Loop Gain vs Frequency

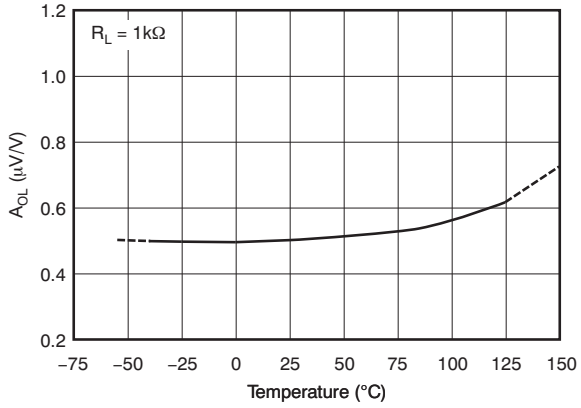

Figure 26. Open-Loop Gain vs Temperature

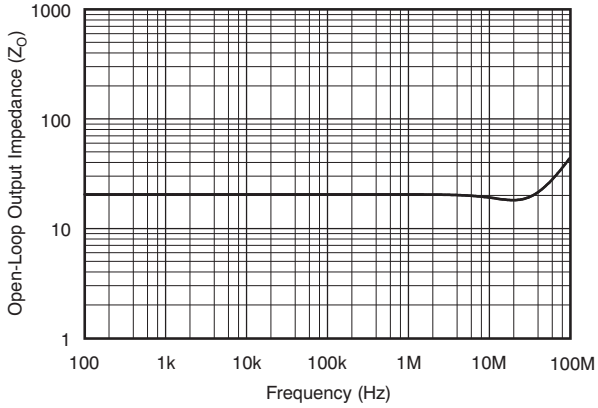

Figure 27. Open-Loop Output Impedance vs Frequency

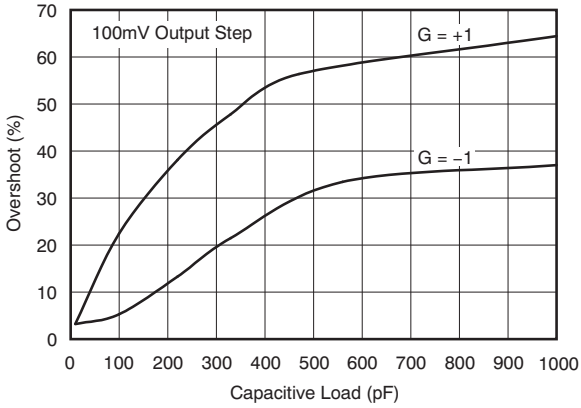

Figure 28. Small-Signal Overshoot vs Capacitive Load

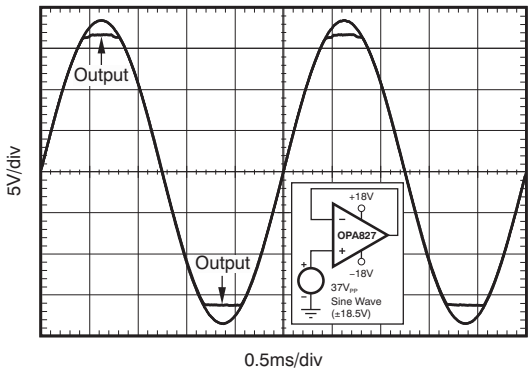

Figure 29. No Phase Reversal

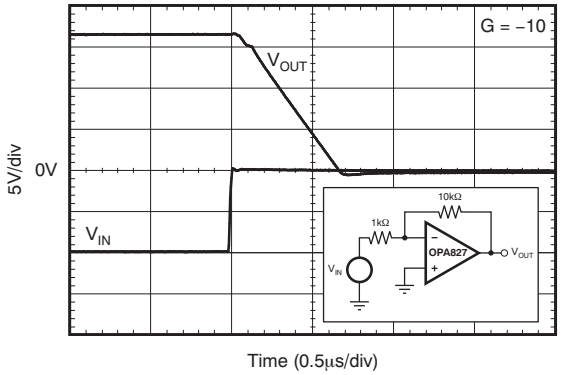

Figure 30. Positive Overload Recovery

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Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

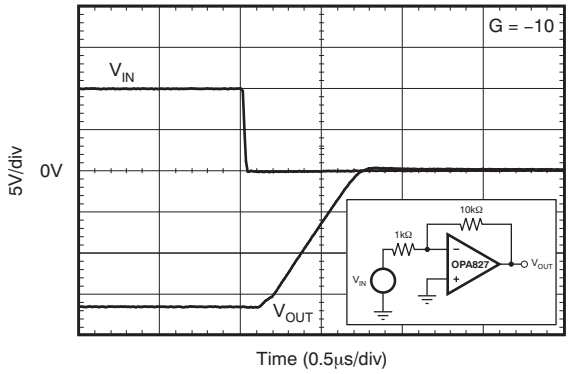


Figure 31. Negative Overload Recovery

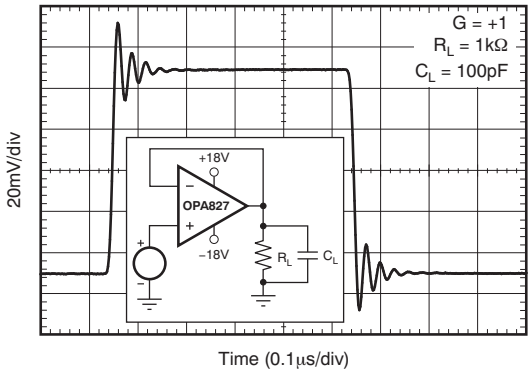


Figure 32. Small-Signal Step Response

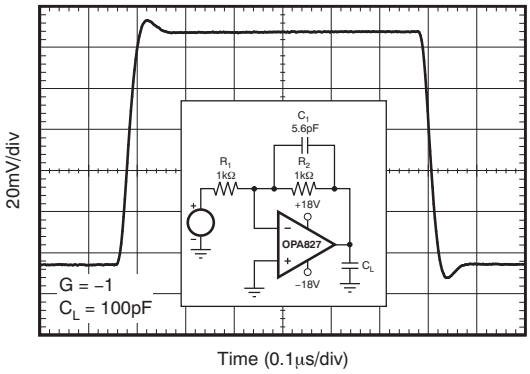


Figure 33. Small-Signal Step Response

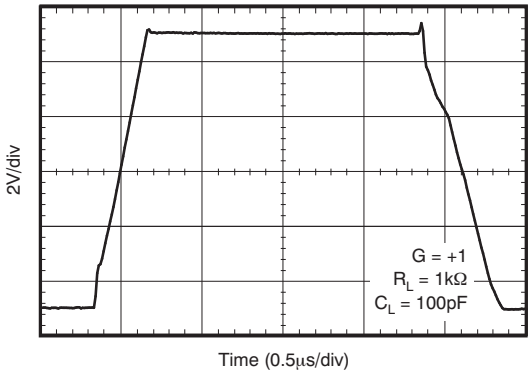


Figure 34. Large-Signal Step Response

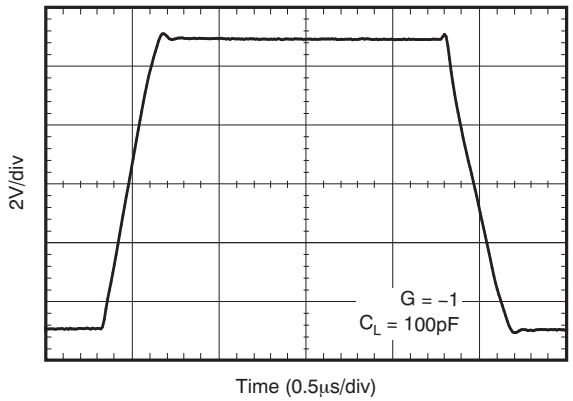
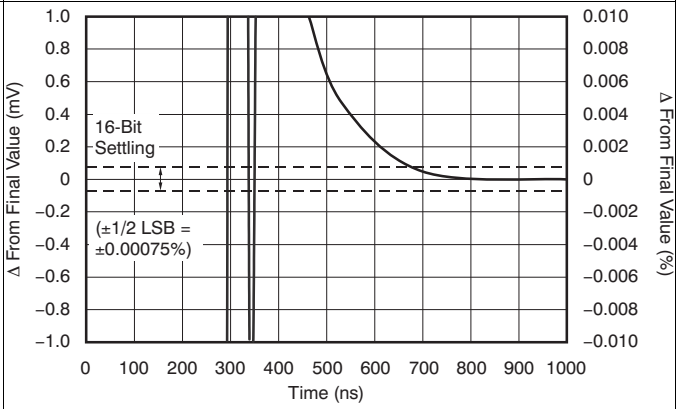


Figure 35. Large-Signal Step Response

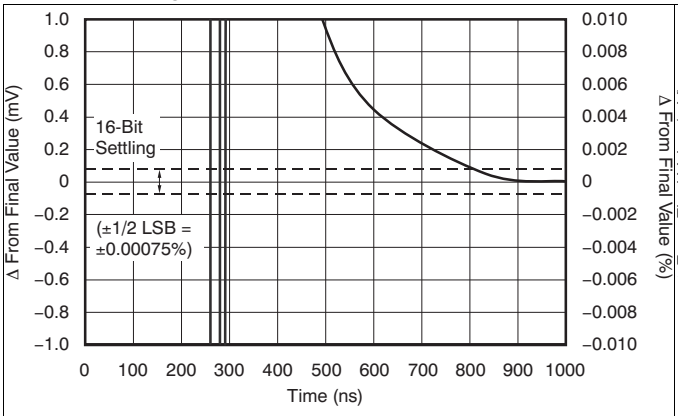


10 V_{PP}, C_L = 100 pF

Figure 36. Large-Signal Positive Settling Time

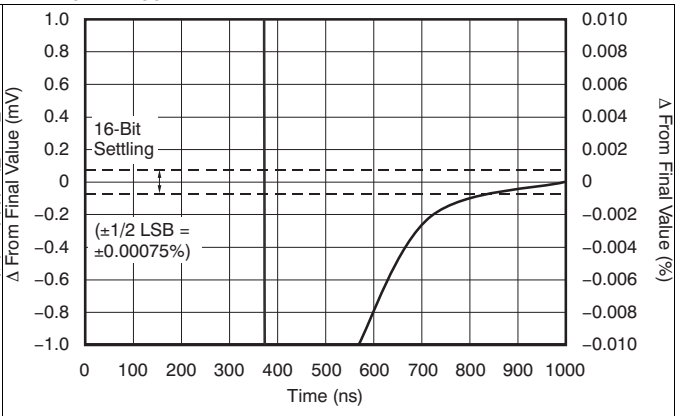
Typical Characteristics (continued)

At T_A = 25°C, V_S = ±18 V, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted.



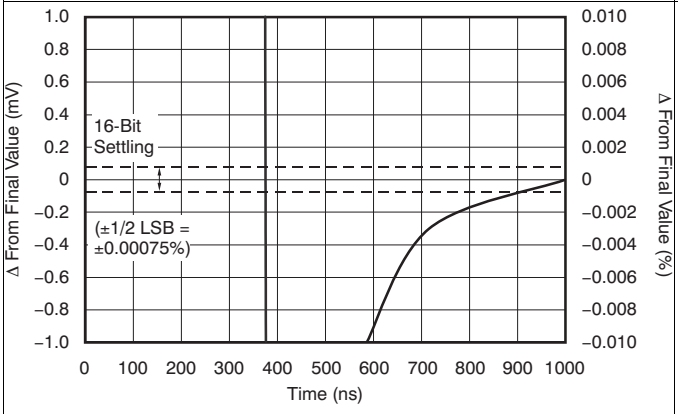
10 V_{PP}, C_L = 10 pF

Figure 37. Large-Signal Positive Settling Time



10 V_{PP}, C_L = 100 pF

Figure 38. Large-Signal Negative Settling Time



10 V_{PP}, C_L = 10 pF

Figure 39. Large-Signal Negative Settling Time

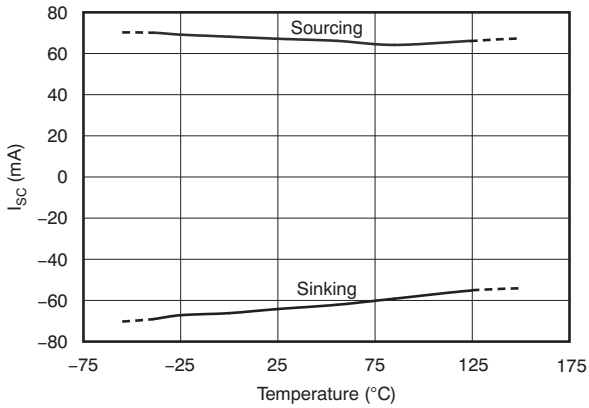


Figure 40. Short-Circuit Current vs Temperature

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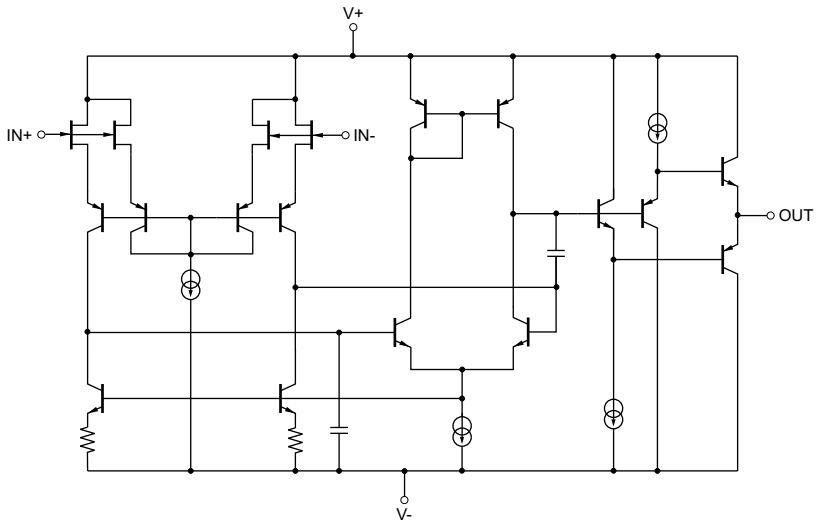
7 Detailed Description

7.1 Overview

The OPA827 is a unity-gain stable, precision operational amplifier with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate.

7.2 Functional Block Diagram



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7.3 Feature Description

The OPA827 is a precision JFET amplifier with low input offset voltage, low input offset voltage drift and low noise. High impedance inputs make the OPA827 ideal for high source impedance applications and transimpedance applications.

7.3.1 Operating Voltage

The OPA827 series of op amps can be used with single or dual supplies from an operating range of V_S = 8 V (±4 V) and up to V_S = 36 V (±18 V). This device does not require symmetrical supplies; it only requires a minimum supply voltage of 8 V. Supply voltages higher than 40 V (±20 V) can permanently damage the device; see *Absolute Maximum Ratings*. Key parameters are specified over the operating temperature range, T_A = –40°C to 125°C. Key parameters that vary over the supply voltage or temperature range are shown in *Typical Characteristics* of this data sheet.

7.3.2 Noise Performance

Figure 41 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The OPA827 (GBW = 22 MHz) and OPA211 (GBW = 80 MHz) are both shown in this example with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPA827 family has both low voltage noise and lower current noise because of the FET input of the op amp. Very low current noise allows for excellent noise performance with source impedances greater than 10 kΩ. OPA211 has lower voltage noise and higher current noise. The low voltage noise makes the OPA211 a better choice for low source impedances (less than 2 kΩ). For high source impedance, current noise may dominate, and makes the OPA827 series amplifier the better choice.

Feature Description (continued)

The equation in Figure 41 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise
- i_n = current noise
- R_S = source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = temperature in kelvins

For more details on calculating noise, see *Basic Noise Calculations*.

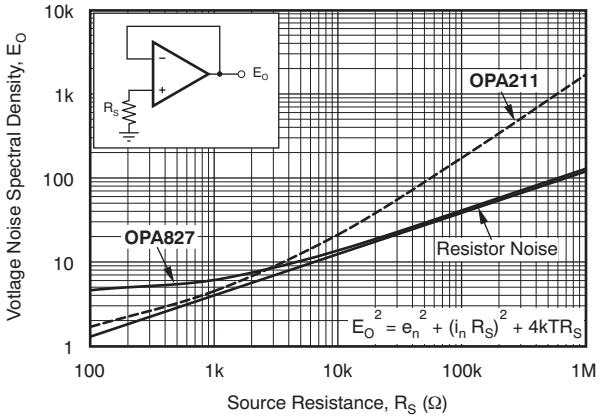

Figure 41. Noise Performance of the OPA827 and OPA211 in Unity-Gain Buffer Configuration

7.3.3 Basic Noise Calculations

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on the overall noise performance of the op amp. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 41. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 42 illustrates both noninverting (*A*) and inverting (*B*) op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components.

The feedback resistor values can generally be chosen to make these noise sources negligible.

NOTE

Low-impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations shown in both configurations in Figure 42.

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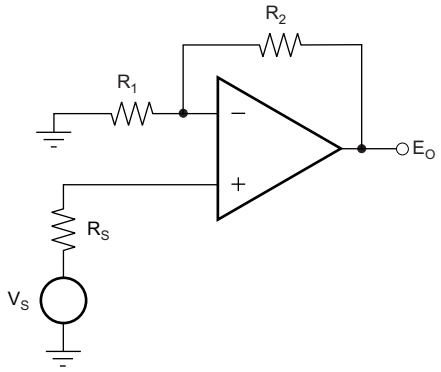
Feature Description (continued)

A) Noise in Noninverting Gain Configuration



Noise at the output:

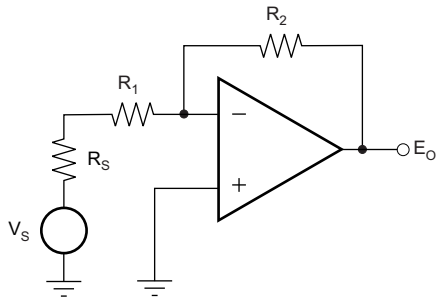
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2 \left(1 + \frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(1 + \frac{R_2}{R_1}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

B) Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA827 series op amps at 1kHz, $e_n = 4nV/\sqrt{Hz}$ and $i_n = 2.2fA/\sqrt{Hz}$.

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Figure 42. Noise Calculation in Gain Configurations

7.3.4 Total Harmonic Distortion Measurements

The OPA827 series op amps have excellent distortion characteristics. THD + Noise is below 0.0001% (G = +1, V_O = 3 V_{RMS}) throughout the audio frequency range, 20 Hz to 20 kHz, with a 600-Ω load (see Figure 3).

The distortion produced by the OPA827 series is below the measurement limit of many commercially available testers. However, a special test circuit (illustrated in Figure 43) can be used to extend the measurement capabilities.

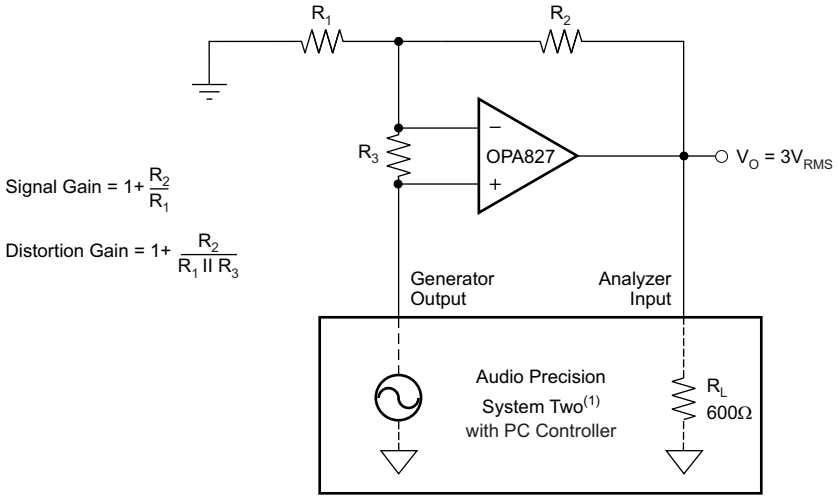
Op amp distortion can be considered an internal error source that can be referred to the input. Figure 43 shows a circuit that causes the op amp distortion to be 101 times greater than that distortion normally produced by the op amp. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101.

NOTE

the input signal and load applied to the op amp are the same as with conventional feedback without R_3. The value of R_3 must be kept small to minimize its effect on the distortion measurements.

Feature Description (continued)

The validity of this technique can be verified by duplicating measurements at high gain and high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion and noise analyzer, which greatly simplifies such repetitive measurements. This measurement technique, however, can be performed with manual distortion measurement instruments.



SIGNAL GAIN	DISTORTION GAIN	R_1	R_2	R_3
1	101	∞	1kΩ	10Ω
11	101	100Ω	1kΩ	11Ω

NOTE: (1) Measurement BW = 80kHz.

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Figure 43. Distortion Test Circuit

7.3.5 Capacitive Load and Stability

The combination of gain bandwidth product (GBW) and near constant open-loop output impedance (Z_O) over frequency gives the OPA827 the ability to drive large capacitive loads. Figure 44 shows the OPA827 connected in a buffer configuration (G = +1) while driving a 2.2-µF ceramic capacitor (with an ESR value of approximately 0 Ω). The small overshoot and fast settling time are results of good phase margin. This feature provides superior performance compared to the competition. Figure 44 and Figure 45 were taken without any resistive load in parallel to shorten the ringing time.

In Figure 45, the OPA827 is driving a 2.2-µF tantalum capacitor. A relatively small ESR that is internal to the capacitor additionally improves phase margin and provides an output waveform with no ringing and minimal overshoot. Figure 45 shows a stable system that can be used in almost any application.

Capacitive load drive depends on the gain and overshoot requirements of the application. Capacitive loads limit the bandwidth of the amplifier. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads (see Figure 28).

7.3.6 Phase-Reversal Protection

The OPA827 family has internal phase-reversal protection. Many FET-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPA827 prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see Figure 29).

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Feature Description (continued)

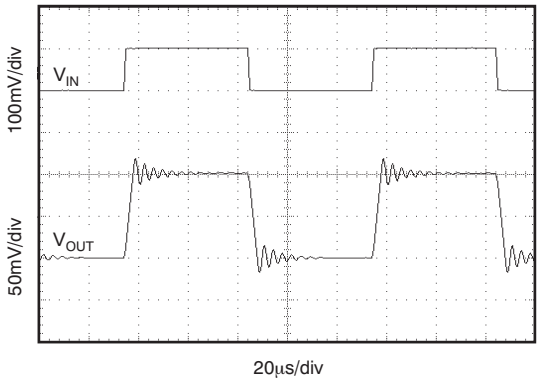


Figure 44. OPA827 Driving 2.2-µF Ceramic Capacitor

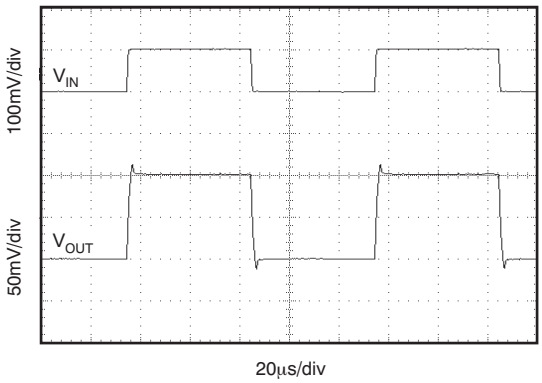


Figure 45. OPA827 Driving 2.2-µF Tantalum Capacitor

7.3.7 Transimpedance Amplifier

The gain bandwidth, low voltage noise, and current noise of the OPA827 series make them ideal wide bandwidth transimpedance amplifiers in a photo-conductive application. High transimpedance gains with feedback resistors greater than 100 kΩ benefit from the low input current noise (2.2 fA/Hz) of the JFET input. Low voltage noise is important because photodiode capacitance causes the effective noise gain in the circuit to increase at high frequencies. Total input capacitance of the circuit limits the overall gain bandwidth of the amplifier and is addressed below. Figure 46 shows a photodiode transimpedance application.

7.3.7.1 Key Transimpedance Points

- The total input capacitance (C_{TOT}) consists of the photodiode junction capacitance, and both the common-mode and differential input capacitance of the operational amplifier.
- The desired transimpedance gain, $V_{OUT} = I_D R_F$.
- The Unity Gain Bandwidth Product (UGBW) (22 MHz for the OPA827).

With these three variables set, the feedback capacitor value (C_F) can be calculated to ensure stability. C_{STRAY} is the parasitic capacitance of the PCB and passive components, which is approximately 0.5 pF.

To ensure 45° phase margin, the minimal amount of feedback capacitance can be calculated using Equation 1.

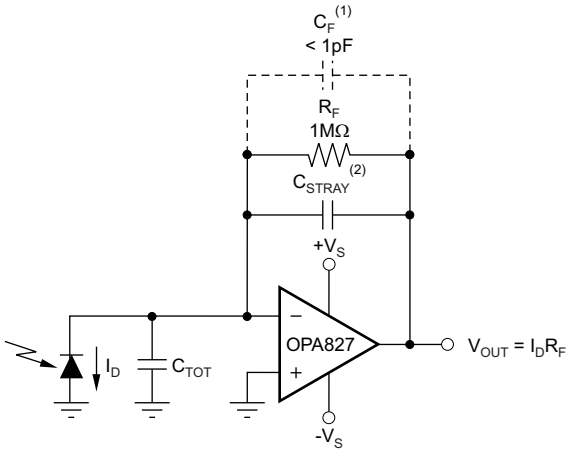
$$C_F \left(\frac{1}{4\pi R_F UGBW} \right) \left(1 + \sqrt{1 + (8\pi C_{TOT} R_F UGBW} \right) \quad (1)$$

Feature Description (continued)

Bandwidth (f_{-3dB}) can be calculated using Equation 2.

$$f_{-3dB} = \sqrt{\frac{UGBW}{2\pi R_F(C_{TOT})}} \text{ Hz} \quad (2)$$

These equations result in maximum transimpedance bandwidth. For additional information, refer to *Compensate Transimpedance Amplifiers Intuitively*, available for download at www.ti.com.



NOTES: (1) C_F is optional to prevent gain peaking.
(2) C_{STRAY} is the stray capacitance of R_F
(typically, 2pF for a surface-mount resistor).

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Figure 46. Transimpedance Amplifier

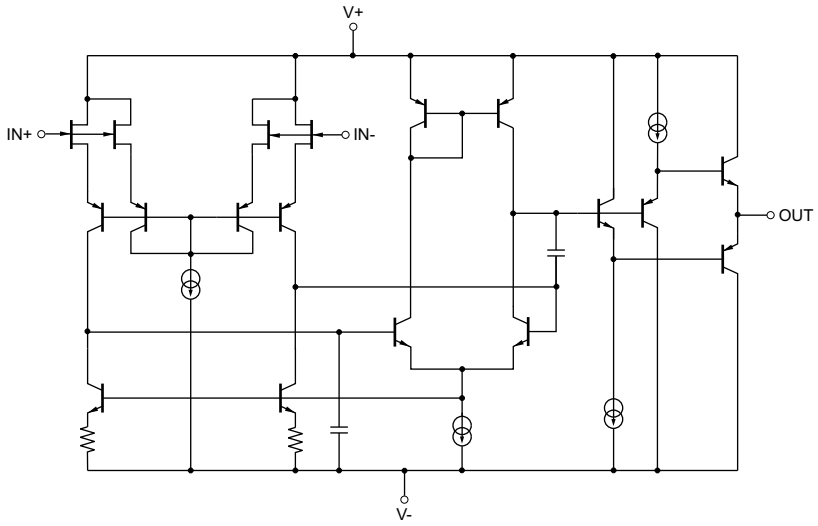

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Figure 47. Equivalent Schematic (Single-Channel)

7.4 Device Functional Modes

The OPA827 has a single functional mode and is operational when the power-supply voltage is greater than 4 V (±2 V). The maximum power supply voltage for the OPA827 is 36 V (±18 V).

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA827 is a unity-gain stable, operational amplifier with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate. Designers can easily take advantage of the low-noise characteristics of JFET amplifiers while also interfacing to modern, single-supply, precision data converters.

8.2 Typical Application

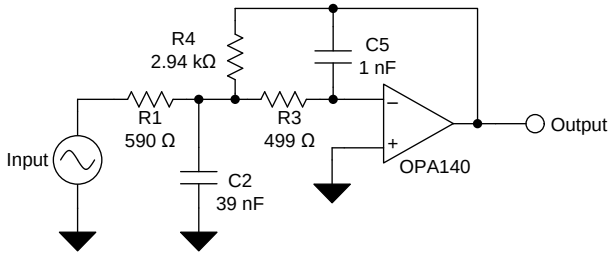

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Figure 48. 25-kHz Low-Pass Filter

8.2.1 Design Requirements

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA827 is ideally suited to construct high-speed, high-precision active filters. Figure 48 shows a second-order, low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the pass band

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in. Use Equation 3 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (3)$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the low-pass cutoff frequency are calculated by Equation 4.

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (4)$$

Typical Application (continued)

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. WEBENCH® Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH Design Center, WEBENCH Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

8.2.3 Application Curve

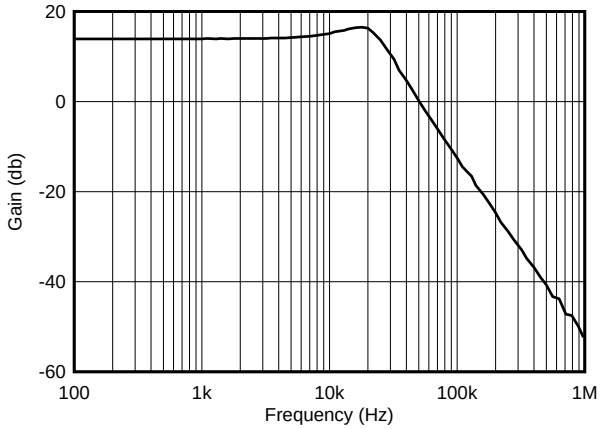

Figure 49. OPA827 Second-Order, 25-kHz, Chebyshev, Low-Pass Filter

8.3 System Examples

The OPA827 is well-suited for phase-lock loop (PLL) applications because of the low voltage offset, low noise, and wide gain bandwidth. Figure 50 illustrates an example of the OPA827 in this application. The first amplifier (OPA827) provides the loop low-pass, active filter function, while the second amplifier (OPA211) serves as a scaling amplifier. This second stage amplifies the DC error voltage to the appropriate level before it is applied to the voltage-controlled oscillator (VCO).

Operational amplifiers used in PLL applications are often required to have low voltage offset. As with other DC levels generated in the loop, a voltage offset applied to the VCO is interpreted as a phase error. An operational amplifier with inherently low voltage offset helps reduce this source of error. Also, any noise produced by the operational amplifiers modulates the voltage applied to the VCO and limits the spectral purity of the oscillator output. The VCO generates noise-related, random phase variations of its own, but this characteristic becomes worse when the input voltage source noise is included. This noise appears as random sideband energy that can limit system performance. The very low flicker noise (1/f) and current noise (In) of the OPA827 help to minimize the operational amplifier contribution to the phase noise.

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System Examples (continued)

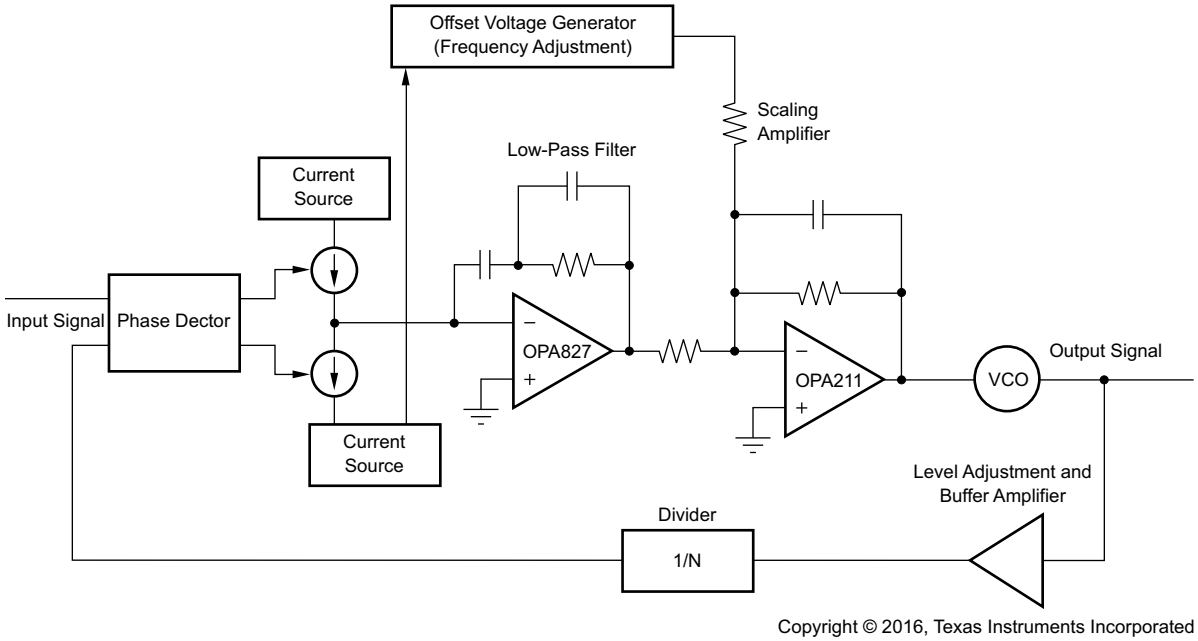

Figure 50. PLL Application

8.3.1 OPA827 Used as an I/V Converter

The OPA827 series of operation amplifiers have low current noise and offset voltage that make these devices a great choice for an I/V converter. DAC8811 is a single-channel, current output, 16-bit digital-to-analog converter (DAC). The I_{OUT} terminal of the DAC is held at a virtual GND potential by the use of the OPA827 as an external I/V converter op amp. The R-2R ladder is connected to an external reference input (V_{REF}) that determines the DAC full-scale current. The external reference voltage can vary in a range of –15 V to 15 V, thus providing bipolar I_{OUT} current operation. By using the OPA827 as an external I/V converter in conjunction with the internal DAC8811 R_{FB} resistor, output voltage ranges of $–V_{REF}$ to $+V_{REF}$ can be generated.

When using an external I/V converter and the DAC8811 R_{FB} resistor, the DAC output voltage is given by Equation 5.

$$V_{OUT} = \frac{-V_{REF} \times CODE}{65536} \quad (5)$$

NOTE

CODE is the digital input into the DAC.

The DAC output impedance as seen looking into the I_{OUT} terminal changes versus code. The low offset voltage of the OPA827 minimizes the error propagated from the DAC.

For a current-to-voltage design (see Figure 51), the DAC8811 I_{OUT} pin and the inverting node of the OPA827 must be as short as possible and adhere to good PCB layout design. For each code change on the output of the DAC, there is a step function. If the parasitic capacitance is excessive at the inverting node, then gain peaking is possible. For circuit stability, two compensation capacitors, C_1 and C_2 (4 pF to 20 pF typical) can be added to the design.

Some applications require full four-quadrant multiplying capabilities or a bipolar output swing. As shown in Figure 51, the OPA827 is added as a summing amp and has a gain of 2x that widens the output span to 20 V. A four-quadrant multiplying circuit is implemented by using a 10-V offset of the reference voltage to bias the OPA827.

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System Examples (continued)

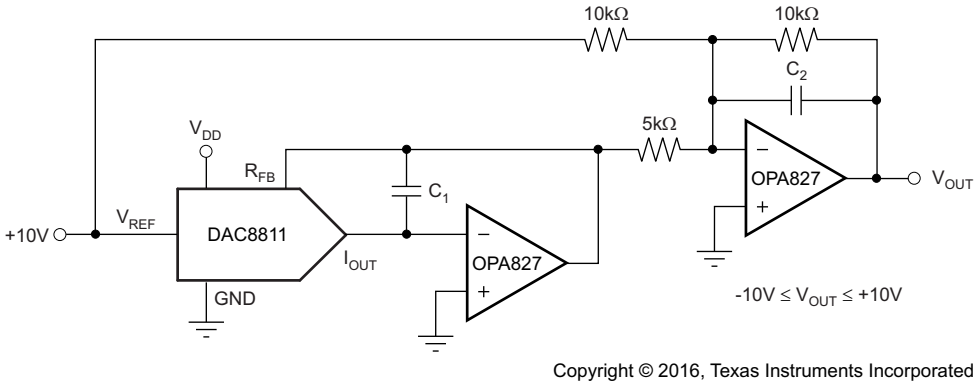

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Figure 51. I/V Converter

9 Power Supply Recommendations

The OPA827 is specified for operation from 4 V to 36 V (±2 V to ±18 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Absolute Maximum Ratings*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout*.

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10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 52, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, TI recommends cleaning the PCB following board assembly.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

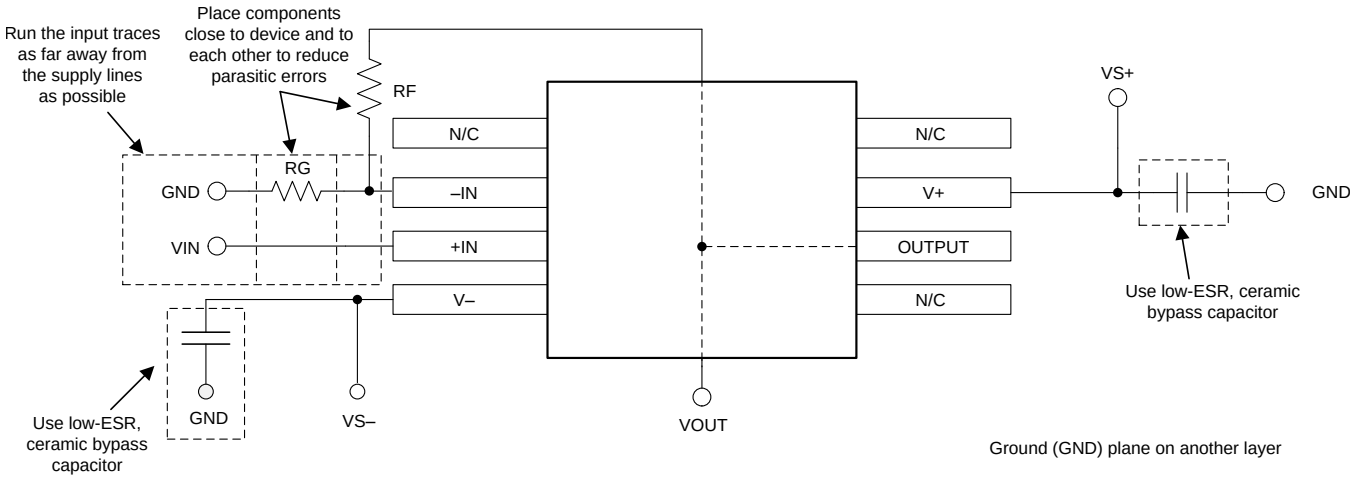

Figure 52. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

For development support see the following:

- WEBENCH® Filter Designer
- OPA211
- DAC8811

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Compensate Transimpedance Amplifiers Intuitively (SBOA055)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

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WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA827AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 827 A
OPA827AID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 827 A
OPA827AIDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 827 A
OPA827AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdauag | Nipdau	Level-2-260C-1 YEAR	-40 to 125	NSP
OPA827AIDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	NSP
OPA827AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI | Nipdauag | Nipdau	Level-2-260C-1 YEAR	-40 to 125	NSP
OPA827AIDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	NSP
OPA827AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 827 A
OPA827AIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 827 A
OPA827AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 827 A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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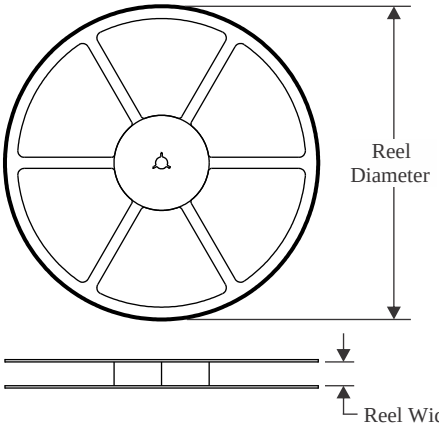
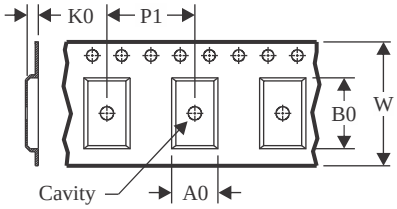
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

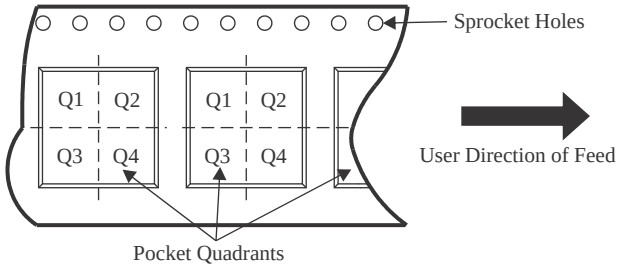


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

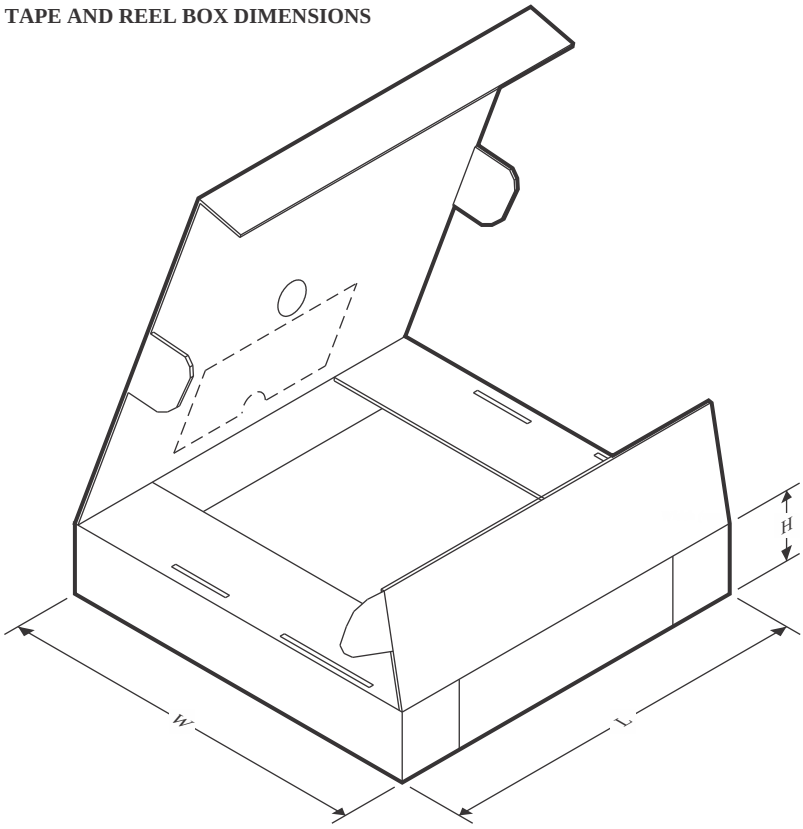
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA827AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA827AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA827AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

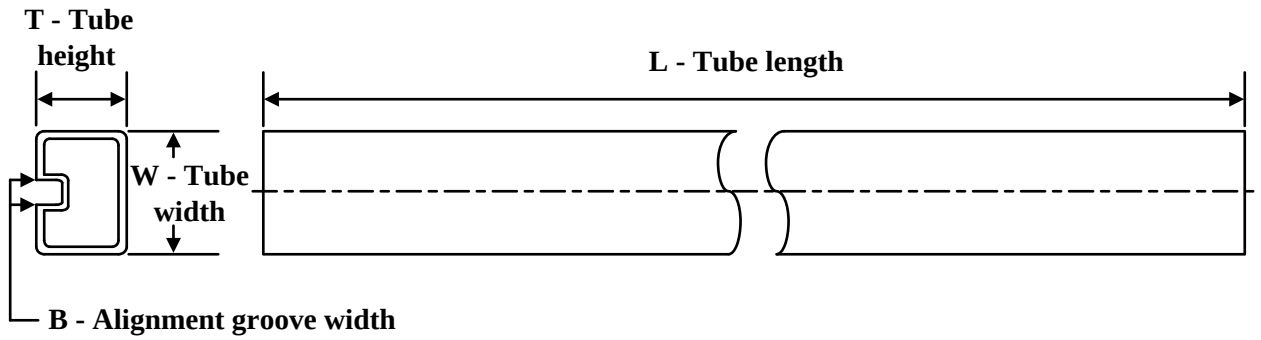
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA827AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA827AIDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA827AIDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

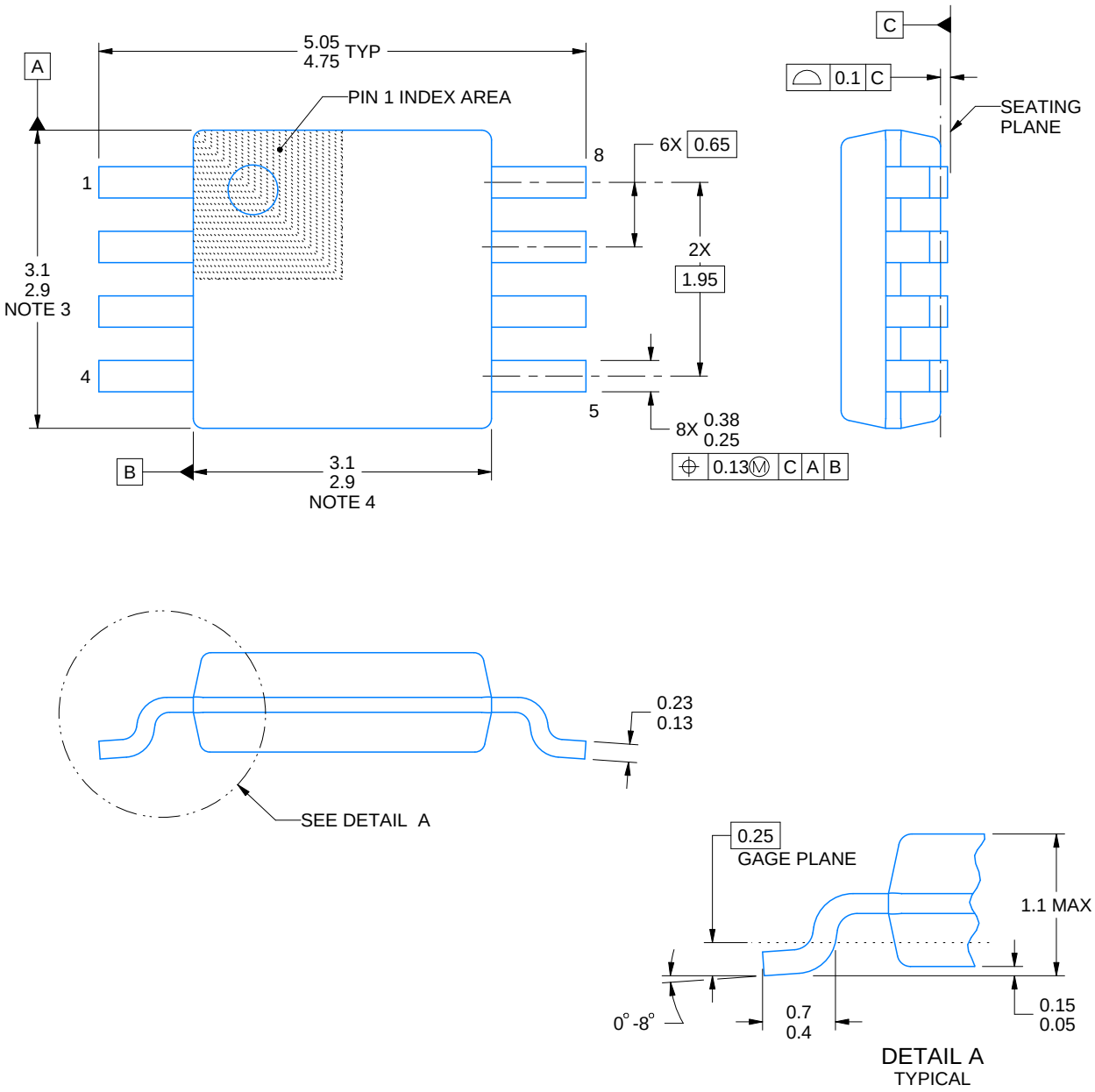
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA827AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA827AID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA827AIDG4	D	SOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

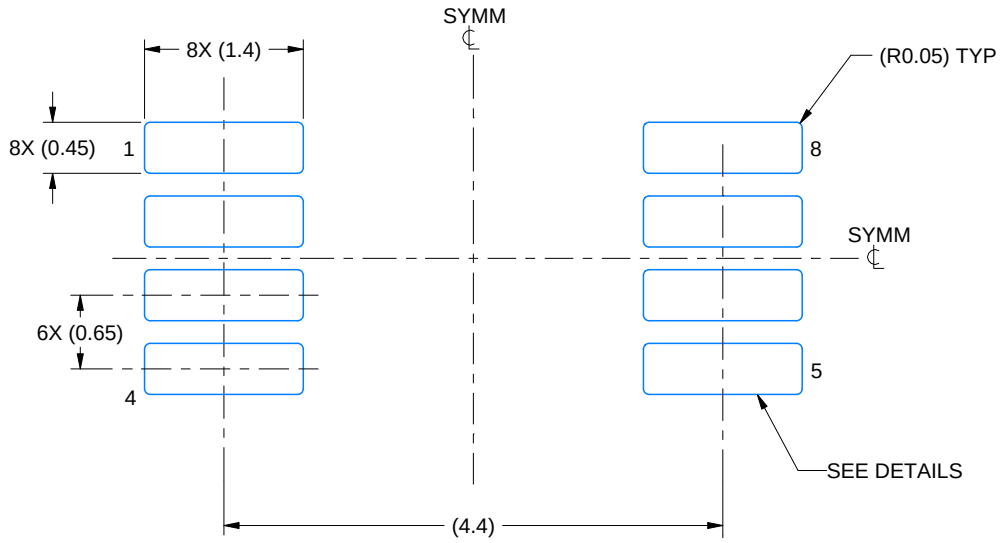
SMALL OUTLINE PACKAGE



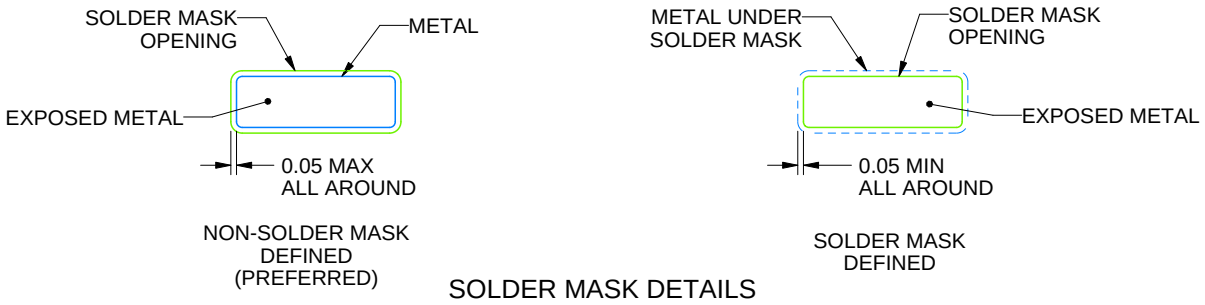
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

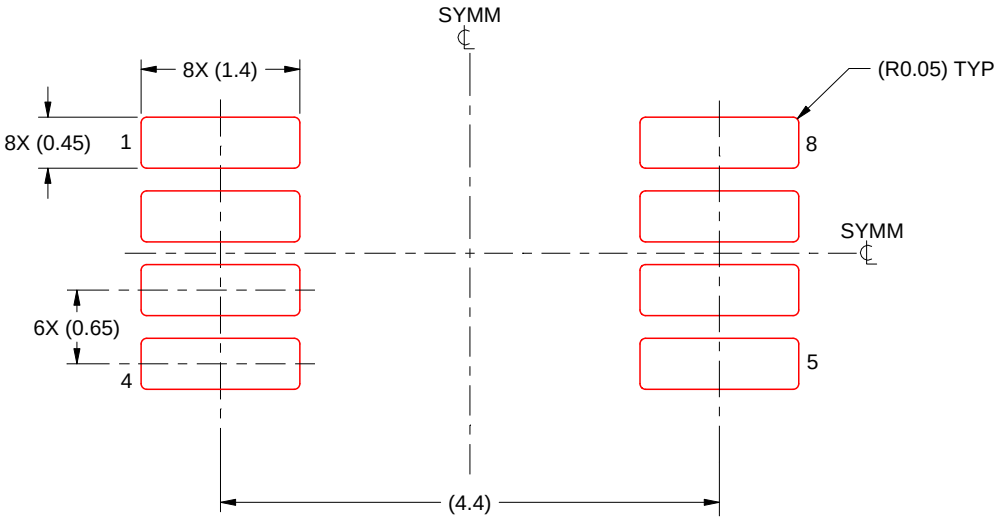


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

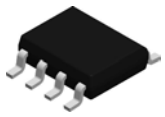


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

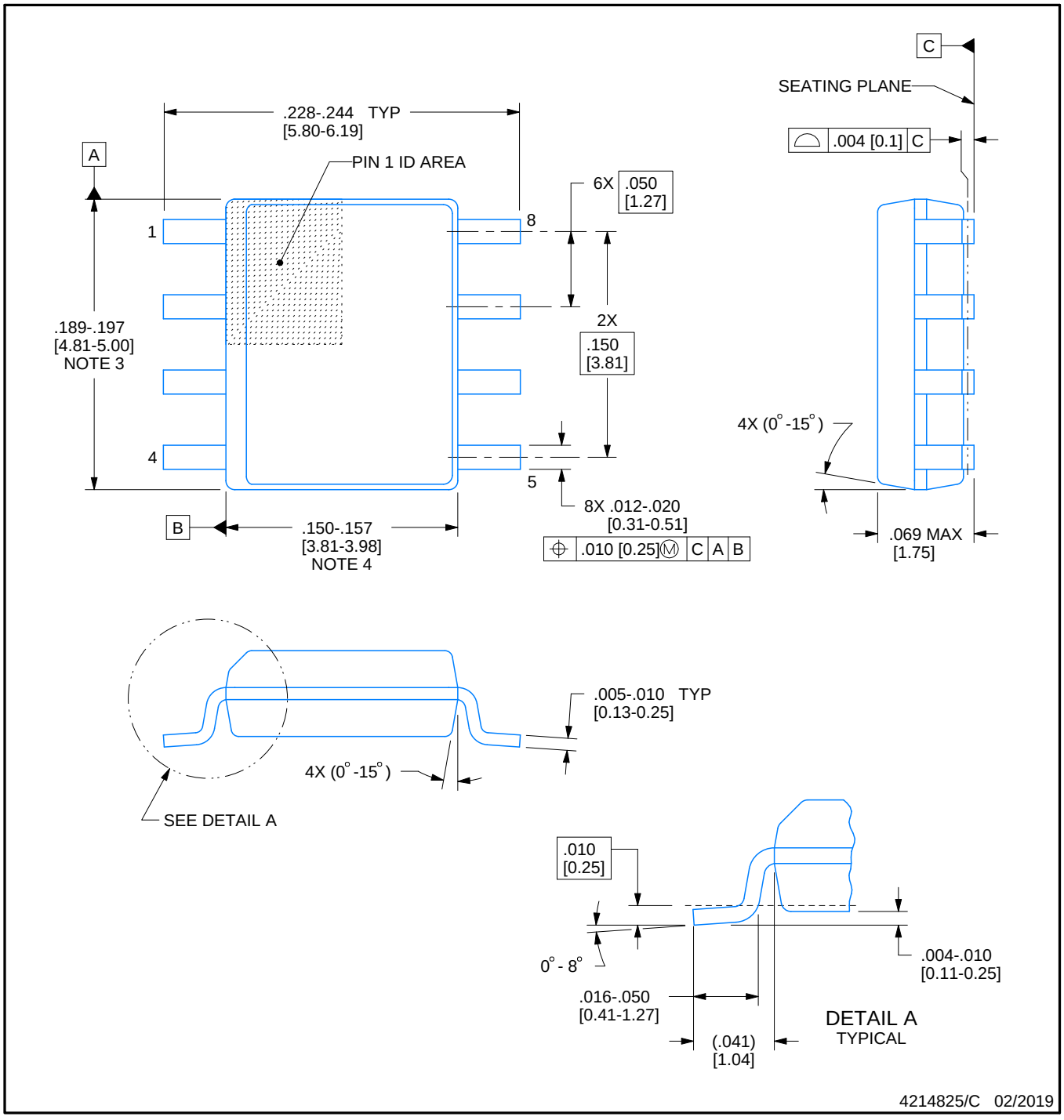


PACKAGE OUTLINE

D0008A

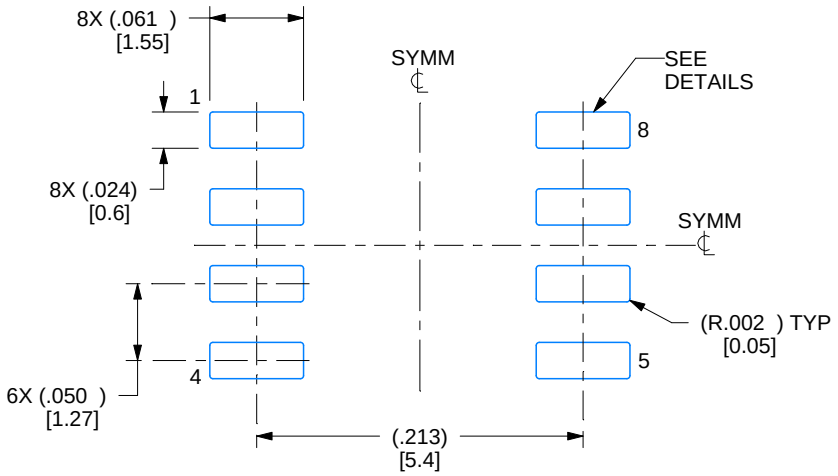
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

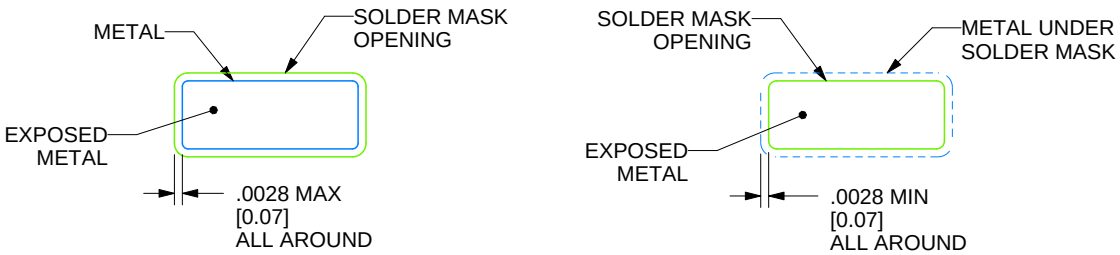


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

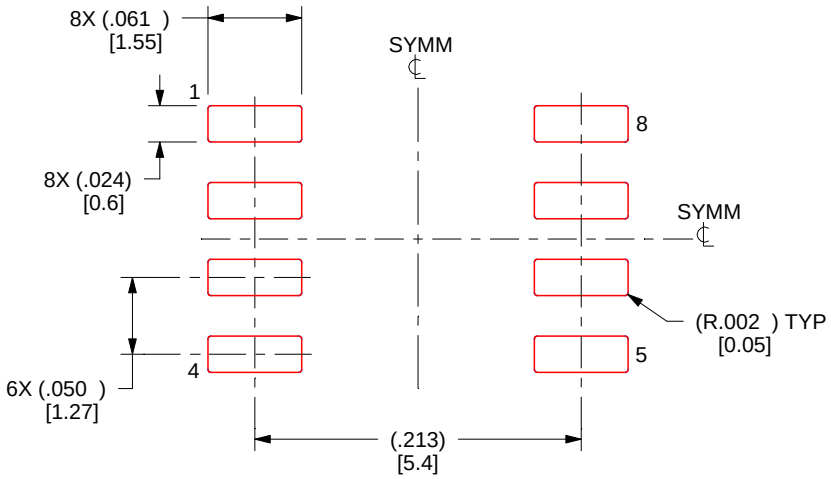
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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