OPT4003-Q1 Automotive High-Speed, Dual-Channel, High-Precision, Digital Ambient Light Sensor

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 2 (USON and SOT-5X3 variant): –40°C to 105°C, T_A
- High-precision, high-speed light-to-digital conversion over high-speed I^{2}C interface
- Visible channel with 28-bits of effective dynamic range:
  - 585µlux to 157klux for SOT-5X3 package variant
  - 535µlux to 143klux for USON package variant
  - Precision optical filtering closely matches human eye with excellent near infrared (NIR) rejection
- Near IR channel with 26-bits of effective dynamic range:
  - 447pW/cm^2 to 30mW/cm^2 for SOT-5X3 package variant
  - 409pW/cm^2 to 27.45mW/cm^2 for USON package variant
  - Precision optical filtering provides high NIR sensitivity with excellent visible rejection
- Semi-logarithmic output:
  - 9 (visible channel) and 7 (NIR channel) binary logarithmic full-scale light ranges
  - Highly linear response within each range
- Built-in automatic full-scale light range selection logic that switches measurement range based on input light condition for best possible resolution at all times
- 12 configurable conversion times:
  - 600µs to 800ms per channel for high-speed and high-precision applications
- External pin interrupt for hardware-synchronized trigger and interrupts
- Error correction code features for improved reliability in automotive use cases
- Internal FIFO for output registers with I^{2}C burst readout
- Low operating current: 30µA
- Ultra-low power standby: 2µA
- Operating temperature range: –40°C to +105°C
- Wide power-supply range: 1.6V to 3.6V
- 5.5V tolerant I/O pins
- Selectable I^{2}C address
- Small-form factor:
  - SOT-5X3: 1.9mm x 2.1mm x 0.6mm
  - USON: 2mm × 2mm × 0.65mm

2 Applications

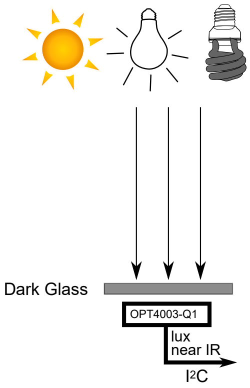
- Automotive interior and exterior lighting
- Infotainment and clusters
- Electrochromatic and smart mirrors
- Head-up display systems
- Automotive camera systems
- Automotive HVAC

Package Information

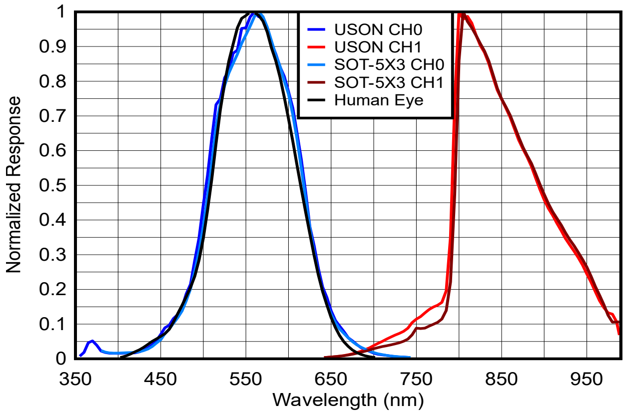
PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
OPT4003-Q1	DTS (SOT-5X3, 8)	1.9mm x 2.1mm x 0.6mm
	DNP (USON, 6)	2mm × 2mm × 0.65mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



OPT4003-Q1 Typical Application Diagram



Spectral Response: The OPT4003-Q1 and the Human Eye

3 Description

The OPT4003-Q1 is a dual-channel, light-to-digital sensor (single-chip lux meter and NIR power meter) that independently measures the intensity of visible and near infrared (NIR) light. To measure accurate visible light intensity, a specially engineered filter on the device tightly matches the photopic response of the human eye and rejects the near-infrared component from common light sources. The NIR channel filter is specially engineered to provide high sensitivity to wavelengths in the near infrared region while achieving high rejection of visible wavelengths with a sharp cutoff at 800nm. The output of the OPT4003-Q1 is semi-logarithmic with binary logarithmic full-scale light ranges along with a highly linear response within each range. The visible channel provides nine binary light ranges, providing measurement capability from 535µlux to 143klux for the USON package variant, 585µlux to 157klux for the SOT-5X3 package variant. The NIR channel provides seven light ranges, providing measurement capability from 409pW/cm^2 to 27.45mW/cm^2 for the USON package variant, 447pW/cm^2 to 30 mW/cm^2 for the SOT-5X3 package variant. The built-in automatic range selection logic dynamically adjusts the device gain settings based on the light level, providing the best possible resolution in all conditions without user input.

The OPT4003-Q1 is equipped with engineered optical filters on both channels, providing strong out-of-band rejection. Strong infrared rejection on the visible channel aids in maintaining high lux accuracy across all light sources, especially when the sensor is placed under dark glass for aesthetic reasons. The NIR channel robust rejection of visible wavelengths and sharp cutoff below 800nm enables precise near-infrared measurements under mixed lighting conditions, including high levels of visible light.

The OPT4003-Q1 is designed for systems that require light level detection to enhance user experience and typically replaces low-accuracy photodiodes, photoresistors, and other ambient light sensors with underwhelming human eye matching and near-infrared rejection.

The OPT4003-Q1 can be configured to operate with light conversion times from 600µs to 800ms per channel in 12 steps, providing system flexibility based on application need. Conversion time includes the light integration time and analog-to-digital (ADC) conversion time. Measurement resolution is determined by a combination of light intensity and integration time, effectively providing the capability to measure down to 535µlux of light intensity changes for the USON package variant, down to 585µlux for the SOT-5X3 package variant.

Digital operation is flexible for system integration. Measurements can be either continuous or triggered in one shot with register writes or a hardware pin . The device features a threshold detection logic, which allows the processor to sleep while the sensor waits for an appropriate wake-up event to report through the interrupt pin.

The sensor reports a digital output representing the light level over an I^{2}C- and SMBus-compatible, two-wire serial interface. An internal first-in-first-out (FIFO) on the output registers is available to read out measurements from the sensor at a slower pace while still preserving all data captured by the device. The OPT4003-Q1 also supports I^{2}C burst mode, thus helping the host read data from the FIFO with minimal I^{2}C overhead.

The low power consumption and low power-supply voltage capability of the OPT4003-Q1 helps enhance the battery life of battery-powered systems.

Table of Contents

4 Pin Configuration and Functions

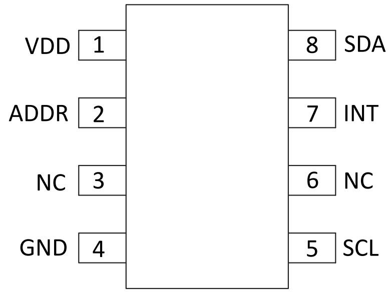
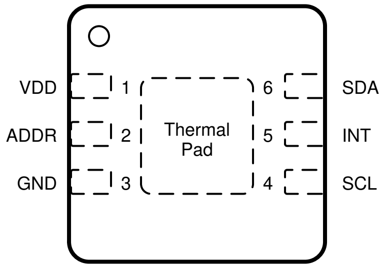


Figure 4-1. DTS Package, 8-Pin SOT-5X3 (Top View)

Table 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NO.	NAME		
1	V_{DD}	I	Device power. Connect to a 1.6-V to 3.6-V supply.
2	ADDR	I	Address pin. This pin sets the LSBs of the I^2C address.
3	NC	No Connection	No Connection
4	GND	P	Ground
5	SCL	I	I^2C clock. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.
6	NC	No Connection	No Connection
7	INT	I/O	Interrupt input/output open-drain. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.
8	SDA	I/O	I^2C data. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.



Not to scale

Figure 4-2. DNP Package, 6-Pin USON (Top View)

Table 4-2. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NO.	NAME		
1	V_{DD}	I	Device power. Connect to a 1.6-V to 3.6-V supply.
2	ADDR	I	Address pin. This pin sets the LSBs of the I^2C address.
3	GND	P	Ground
4	SCL	I	I^2C clock. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.
5	INT	I/O	Interrupt input/output open-drain. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.
6	SDA	I/O	I^2C data. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.

(1) I = Input, O = Output, I/O = Input or Output, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VDD to GND	–0.5	6	V
	SDA and SCL to GND	–0.5	6	V
	Current in to any pin		10	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150(2)	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Long exposure to temperatures higher than 105°C can cause package discoloration, spectral distortion, and measurement inaccuracy.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage	1.6		3.6	V
Operating temperature (USON, SOT-5X3 variant)	–40		105	°C

5.4 Thermal Information

THERMAL METRIC(1)		OPT4003-Q1		UNIT
		DTS (SOT-5X3)	DNP (USON)	
		8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	171.2	71.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	83.1	45.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.2	42.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.7	2.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	65.2	42.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

All specifications at TA = 25°C, VDD = 3.3 V, 800-ms conversion-time per channel, automatic full-scale range, white LED (for channel 0), 850nm LED (for channel 1), normal-angle incidence of light and over operating free-air temperature range, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPTICAL						
SOT-5X3 Variant						
λ_{peak}	Peak wavelength of spectral responsivity	CH0 (ALS)		564		nm
		CH1 (IR)		805		
ER_{lux}	Equivalent resolution CH0 (ALS)	Lowest auto gain range, 100-ms conversion time per channel		4.68		mlux
		Lowest auto gain range, 800-ms conversion time per channel		585		µlux
ER_{IR}	Equivalent Resolution CH1 (IR)	Lowest auto gain range, 100-ms conversion time per channel, 810-nm monochromatic light source		3.58		nW/cm^2
		Lowest auto gain range, 800-ms conversion time per channel, 810-nm monochromatic light source		0.447		
E_{vFS}	Full-scale equivalent Illuminance	CH0 (ALS)		157035		lux
		CH1 (IR), 810-nm monochromatic light source		30		mW/cm^2
R_{CH0}	Responsivity	CH0 (ALS) lowest auto gain range, 800-ms conversion time per channel, 550-nm monochromatic light source		10220		codes per µW/cm^2
R_{CH1}	Responsivity	CH1 (IR) lowest auto gain range, 800-ms conversion time per channel, 810-nm monochromatic light source		2233		codes per µW/cm^2
	Angular response (FWHM)	CH0 (ALS)		120		°
		CH1 (IR), 850nm LED input		128		
E_v	Measurement output result from lux measurement	2000 lux input(1)	1800	2000	2200	lux
E_{IR}	Measurement output result from CH1 (IR) measurement	850-nm LED input, 79.68 µW/cm^2 input irradiance	107910	119900	131890	codes
USON Variant						
λ_{peak}	Peak wavelength of spectral responsivity	CH0 (ALS)		560		nm
		CH1 (IR)		800		
ER_{lux}	Equivalent resolution CH0 (ALS)	Lowest auto gain range, 100-ms conversion time per channel		4.28		mlux
		Lowest auto gain range, 800-ms conversion time per channel		535		µlux
ER_{IR}	Equivalent Resolution CH1 (IR)	Lowest auto gain range, 100-ms conversion time per channel, 810-nm monochromatic light source		3.28		nW/cm^2
		Lowest auto gain range, 800-ms conversion time per channel, 810-nm monochromatic light source		0.409		
E_{vFS}	Full-scale equivalent Illuminance	CH0 (ALS)		143613		lux
		CH1 (IR), 810-nm monochromatic light source		27.45		mW/cm^2
R_{CH0}	Responsivity	CH0 (ALS) lowest auto gain range, 800-ms conversion time per channel, 550-nm monochromatic light source		12800		codes per µW/cm^2

All specifications at TA = 25°C, VDD = 3.3 V, 800-ms conversion-time per channel, automatic full-scale range, white LED (for channel 0), 850nm LED (for channel 1), normal-angle incidence of light and over operating free-air temperature range, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{CH1}	Responsivity	CH1 (IR) lowest auto gain range, 800-ms conversion time per channel, 810-nm monochromatic light source		2441		codes per µW/cm^2
	Angular response (FWHM)	CH0 (ALS)		120		°
		CH1 (IR), 850nm LED input		125		
E_v	Measurement output result from lux measurement	2000 lux input(1)	1800	2000	2200	lux
E_{IR}	Measurement output result from CH1 (IR) measurement	850-nm LED input, 79.68 µW/cm^2 input irradiance	117900	131000	144100	codes
Common Specifications						
	Number of channels			2		
	ADC resolution		9		20	bits
	Range determination	CH0 (ALS)		4		bits
		CH1 (IR)		3		
T_{intg}	Light integration time per channel (4)	Conversion-time CT = 0x6		25		ms
		Conversion-time CT = 0xB		800		
	Relative accuracy between gain ranges (2)	All channels		0.6		%
E_{vIR}	Infrared response(6)	850-nm near-infrared, CH0 (ALS) response		0.2		%
E_{vVIS}	Visible response	550-nm monochromatic light source, CH1 (IR) response		0.2		%
	Light source variation for lux measurement (incandescent, halogen, fluorescent)	Bare device, no cover glass		4		%
	Linearity	EXPONENT > 0, 100-ms conversion-time per channel, all channels		2		%
		EXPONENT = 0, 100-ms conversion-time per channel, all channels		5		
	Dark measurement	All channels		0	10	codes
	Drift across temperature	CH0 (ALS)		0.02		%/°C
		CH1 (IR), 850nm LED input		0.12		
PSRR	Power-supply rejection ratio(3)	CH0 (ALS), VDD at 3.6 V and 1.6 V		0.2		%/V
		CH1 (IR), VDD at 3.6 V and 1.6 V, 850nm LED input		0.8		%/V
POWER SUPPLY						
V_{DD}	Power supply		1.6		3.6	V
V_{I2C}	Power supply for I^{2}C pullup resistor	I^{2}C pullup resistor, $V_{DD} \le V_{I2C}$	1.6		5.5	V
$I_{QACTIVE}$	Active current	Dark		22		µA
		Full-scale lux		30		
I_Q	Quiescent current	Dark		1.6		µA
		Full-scale lux		2		
POR	Power-on-reset threshold			0.8		V
DIGITAL						
C_{IO}	I/O pin capacitance			3		pF
V_{IL}	Low-level input voltage (SDA, SCL, and ADDR)		0		0.3 X V_{DD}	V

All specifications at TA = 25°C, VDD = 3.3 V, 800-ms conversion-time per channel, automatic full-scale range, white LED (for channel 0), 850nm LED (for channel 1), normal-angle incidence of light and over operating free-air temperature range, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage (SDA, SCL, and ADDR)		0.7 X V_{DD}		5.5	V
I_{IL}	Low-level input current (SDA, SCL, and ADDR)			0.01	0.25(5)	µA
V_{OL}	Low-level output voltage (SDA and INT)	I_{OL} = 3 mA			0.32	V
I_{ZH}	Output logic high, high-Z leakage current (SDA, INT)	Measured with V_{DD} at pin		0.01	0.25(5)	µA
TEMPERATURE						
Specified temperature range		USON, SOT-5X3 variant	–40		105	°C

(1) Tested with the white LED calibrated to 2000 lux.
(2) Characterized by measuring fixed near-full-scale light levels on the higher adjacent full-scale range setting.
(3) PSRR is the percent change of the measured lux output from its current value, divided by the change in power supply voltage, as characterized by results from 3.6-V and 1.6-V power supplies.
(4) The conversion time, from start of conversion until the data are ready to be read, is the integration-time plus analog-to-digital conversion time.
(5) The specified leakage current is dominated by the production test equipment limitations. Typical values are much smaller.
(6) Characterized with a near infrared LED of 850-nm wavelength.

5.6 Timing Requirements

see [(1)](#)

		MIN	TYP	MAX	UNIT
I^2C FAST MODE					
f_{SCL}	SCL operating frequency	0.01		0.4	MHz
t_{BUF}	Bus free time between stop and start	1300			ns
t_{HDSTA}	Hold time after repeated start	600			ns
t_{SUSTA}	Setup time for repeated start	600			ns
t_{SUSTO}	Setup time for stop	600			ns
t_{HDDAT}	Data hold time	20		900	ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_{RC} and t_{FC}	Clock rise and fall time			300	ns
t_{RD} and t_{FD}	Data rise and fall time			300	ns
t_{TIMEO}	Bus timeout period. If the SCL line is held low for this duration of time, the bus state machine is reset.		28		ms
I^2C HIGH-SPEED MODE					
f_{SCL}	SCL operating frequency	0.01		2.6	MHz
t_{BUF}	Bus free time between stop and start	160			ns
t_{HDSTA}	Hold time after repeated start	160			ns
t_{SUSTA}	Setup time for repeated start	160			ns
t_{SUSTO}	Setup time for stop	160			ns
t_{HDDAT}	Data hold time	20		140	ns
t_{SUDAT}	Data setup time	20			ns
t_{LOW}	SCL clock low period	240			ns
t_{HIGH}	SCL clock high period	60			ns
t_{RC} and t_{FC}	Clock rise and fall time			40	ns
t_{RD} and t_{FD}	Data rise and fall time			80	ns
t_{TIMEO}	Bus timeout period. If the SCL line is held low for this duration of time, the bus state machine is reset.		28		ms

(1) All timing parameters are referenced to low and high voltage thresholds of 30% and 70%, respectively, of the final settled value.

5.7 Timing Diagram

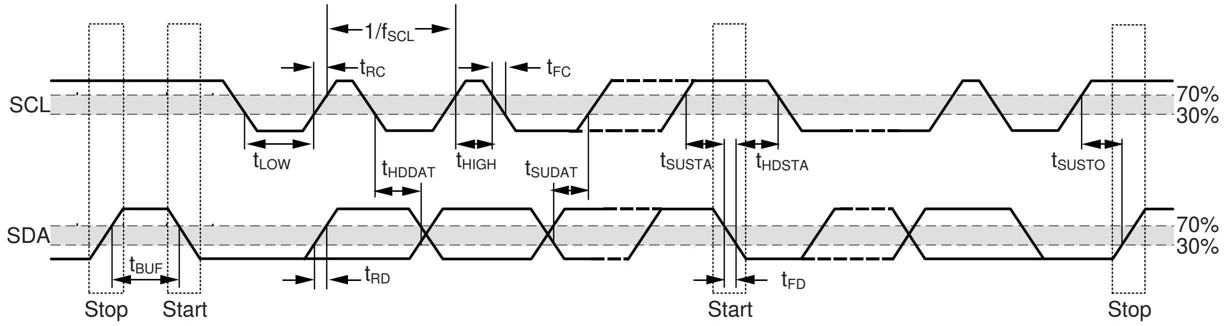


Figure 5-1. I^2C Detailed Timing Diagram

5.8 Typical Characteristics

at T_A = 25°C, V_{DD} = 3.3 V, 800-ms conversion time (CONVERSION_TIME = 0xB), automatic full-scale range (RANGE = 0xC), light source for channel 0 is a white LED and light source for channel 1 is an 850-nm LED, and normal-angle incidence of light (unless otherwise noted)

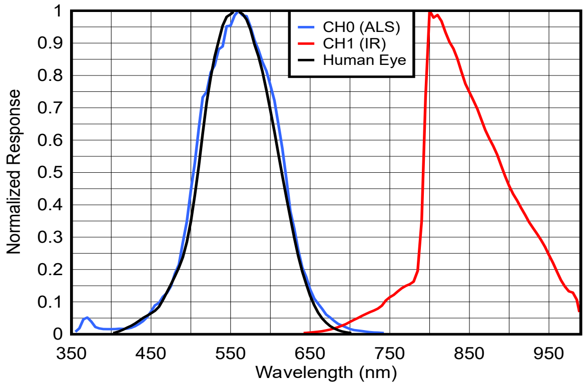


Figure 5-2. Spectral Response vs Wavelength for the USON Variant

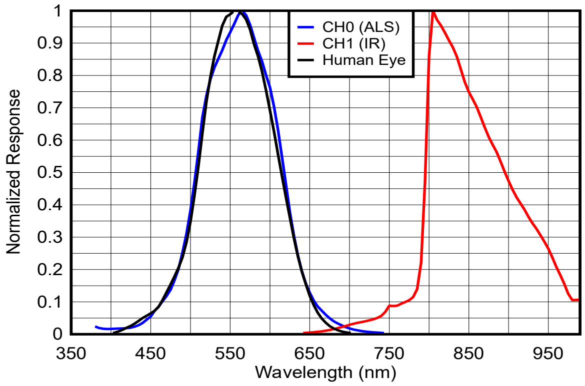
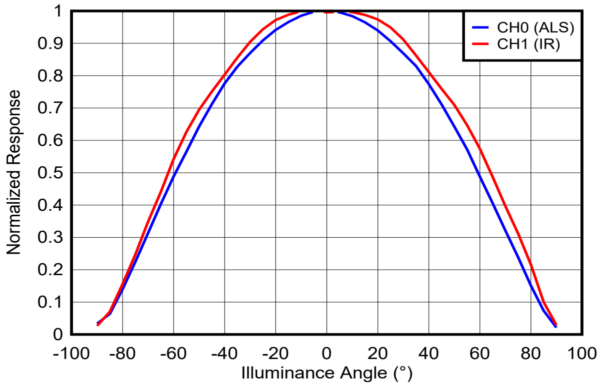
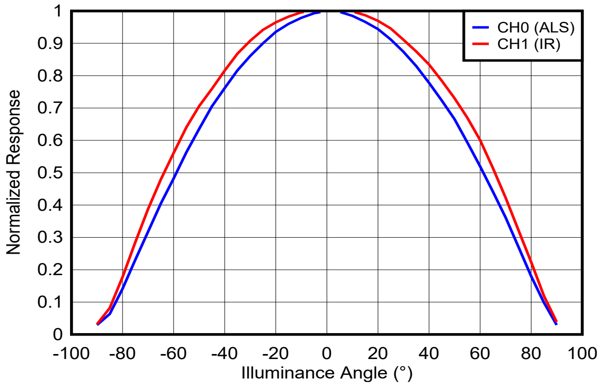


Figure 5-3. Spectral Response vs Wavelength for the SOT-5X3 Variant



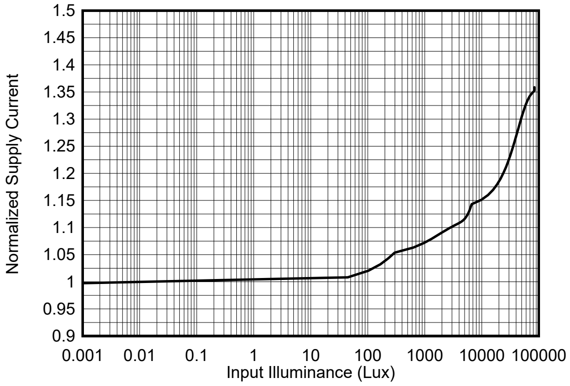
Normalized to 0°

Figure 5-4. Device Response vs Illuminance Angle for the USON Variant



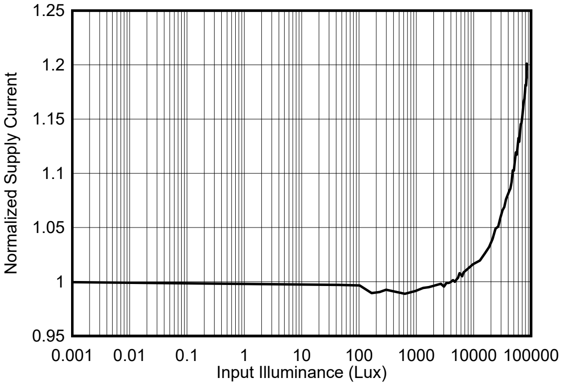
Normalized to 0°

Figure 5-5. Device Response vs Illuminance Angle for the SOT-5X3 Variant



Normalized to dark condition

Figure 5-6. Active Current vs Input Light Level

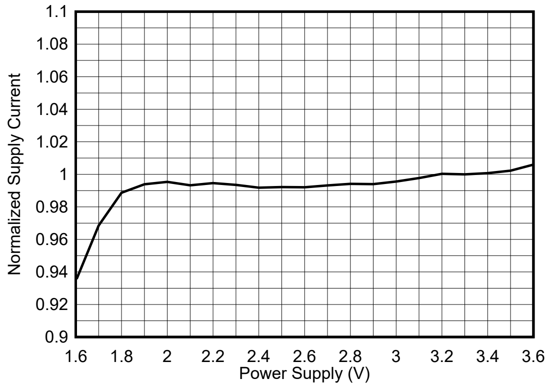


Normalized to dark condition

Figure 5-7. Standby Current vs Input Light Level

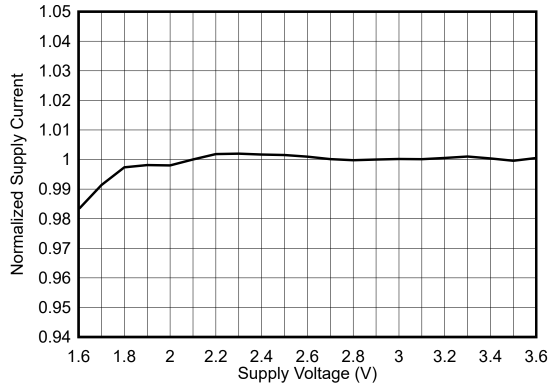
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 3.3 V, 800-ms conversion time (CONVERSION_TIME = 0xB), automatic full-scale range (RANGE = 0xC), light source for channel 0 is a white LED and light source for channel 1 is an 850-nm LED, and normal-angle incidence of light (unless otherwise noted)



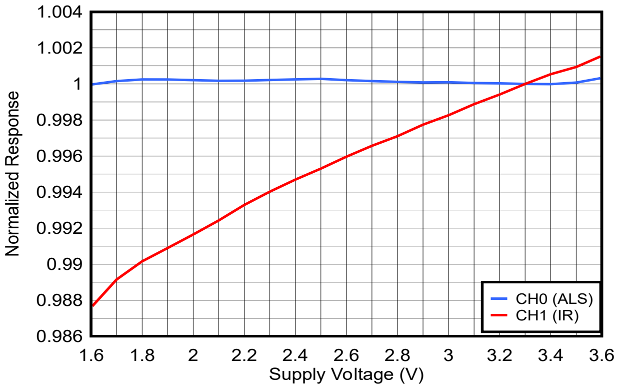
Normalized to 3.3 V

Figure 5-8. Active Current vs Power Supply



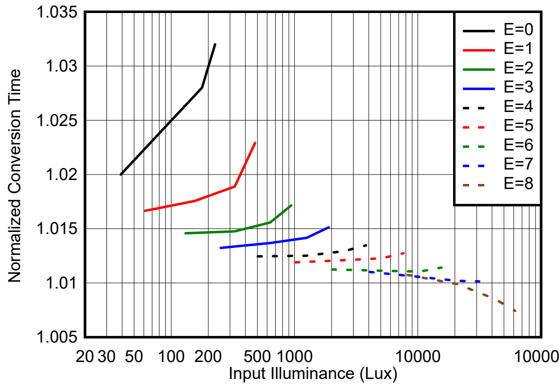
Normalized to 3.3 V

Figure 5-9. Standby Current vs Power Supply



Normalized to 3.3 V

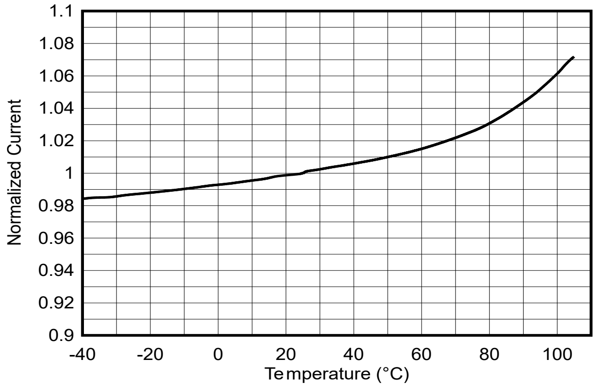
Figure 5-10. Device Response vs Power Supply



Register E (exponent) denotes the full-scale range

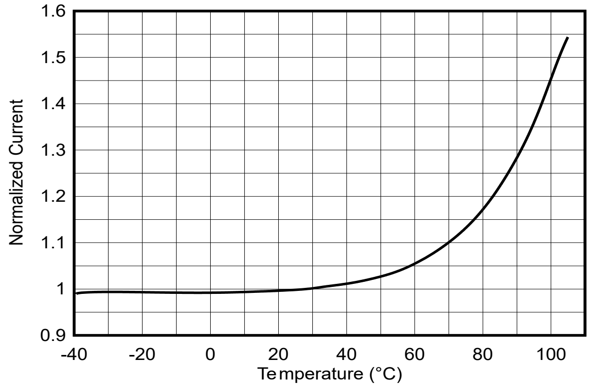
Normalized to 25 ms

Figure 5-11. Conversion Time at 25 ms vs Input Light Level



Normalized to 25°C

Figure 5-12. Active Current vs Temperature



Normalized to 25°C

Figure 5-13. Standby Current vs Temperature

6 Detailed Description

6.1 Overview

The OPT4003-Q1 measures the ambient light that illuminates the device. This device measures light with a spectral response very closely matched to the human eye, and with strong near-infrared rejection.

Matching the sensor spectral response to that of the human eye response is vital because ambient light sensors measure and help create human lighting experiences. Strong rejection of infrared light, which a human does not see, is a crucial component of this matching. This matching makes the OPT4003-Q1 especially good for operation underneath windows that are visibly dark, but infrared transmissive.

The IR channel is sensitive to wavelengths between 800 nm and 1000 nm. This sensitivity enables accurate measurement of NIR sources even in the presence of strong visible light.

The OPT4003-Q1 is fully self-contained to measure the ambient light and report the result in ADC codes directly proportional to lux digitally over the I^{2}C bus. The result can also be used to alert a system and interrupt a processor with the INT pin. The result can also be summarized with a programmable threshold comparison and communicated with the INT pin .

The OPT4003-Q1 is by default configured to operate in automatic, full-scale range detection mode that always selects the best full-scale range setting for the given lighting conditions. There are nine full-scale range settings, one of which can be selected manually as well. Setting the device to operate in automatic, full-scale-range detection mode frees the user from programing software for multiple iterations of measurement and readjustment of the full-scale range until reaching acceptable results for any given measurement. With the device exhibiting excellent linearity over the entire 28-bit dynamic range of measurement, no additional linearity calibration is required at the system level.

The OPT4003-Q1 can be configured to operate in continuous or one-shot measurement mode. The device offers 12 conversion times ranging from 600 µs to 800 ms per channel. The device starts up in a low-power shutdown state, such that the OPT4003-Q1 only consumes active-operation power when the device is programmed into an active state.

The OPT4003-Q1 optical filtering system is not excessively sensitive to small particles and micro-shadows on the optical surface. This reduced sensitivity is a result of the relatively minor device dependency on uniform density optical illumination of the sensor area for infrared rejection. Always follow proper optical surface cleanliness for best results on all optical devices.

6.2 Functional Block Diagram

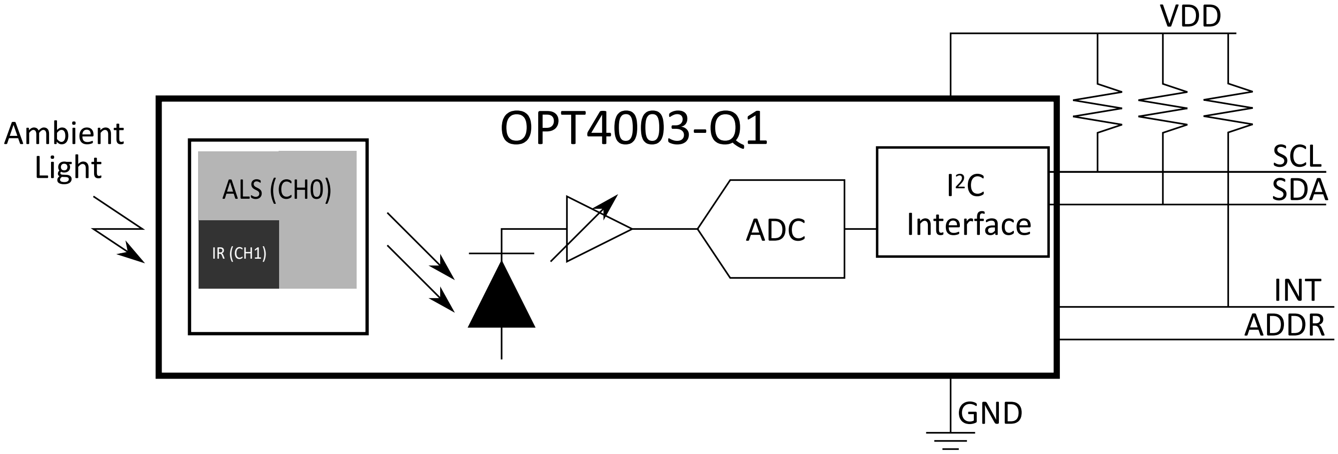


Figure 6-1. Functional Block Diagram of the OPT4003-Q1

6.3 Feature Description

6.3.1 Spectral Response

6.3.1.1 Channel 0: Human Eye Matching

The OPT4003-Q1 spectral response closely matches that of the human eye. If the ambient light sensor measurement is used to help create a good human experience, or create optical conditions that are good for humans, then the sensor must measure the same spectrum of light that a human sees.

The OPT4003-Q1 also has excellent near infrared (NIR) rejection. This NIR rejection is especially important because many real-world lighting sources have significant infrared content that humans do not see. If the sensor measures infrared light that the human eye does not see, then a true human experience is not accurately represented.

If the application demands hiding the OPT4003-Q1 underneath a dark window (such that the end-product user cannot see the sensor), the infrared rejection of the OPT4003-Q1 becomes significantly more important because many dark windows attenuate visible light but transmit infrared light. This attenuation of visible light and lack of attenuation of NIR light amplifies the ratio of the infrared light to visible light that illuminates the sensor. Results can still be well matched to the human eye under this condition because of the high infrared rejection of the OPT4003-Q1.

6.3.1.2 Channel 1: Near Infrared

Channel 1 is able to maintain high near-infrared sensitivity while having excellent visible light rejection. This capability means that even in applications where there are different types of light sources, the OPT4003-Q1 can make accurate near-infrared measurements, regardless of visible light levels. In addition to the accurate measurement of near-infrared sources, the infrared component of common light sources can be measured using the channel 1 data.

6.3.2 Automatic Full-Scale Range Setting

The OPT4003-Q1 has an automatic full-scale range setting feature that eliminates the need to predict and set the best range for the device. In this mode, the device automatically selects the best full-scale range for varying lighting conditions for each measurement. The device has a high degree of result matching between the full-scale range settings. This matching eliminates the problem of varying results or the need for range-specific, user-calibrated gain factors when different full-scale ranges are chosen.

6.3.3 Error Correction Code (ECC) Features

The OPT4003-Q1 features additional error correction code (ECC) bits as part of the output register that helps improves the reliability of light measurements for the application.

6.3.3.1 Output Sample Counter

The OPT4003-Q1 features a COUNTER register as part of the output registers that increment for every successful measurement. This register can be read as part of the output registers, which helps the application keep track of measurements. The 4-bit counter starts at 0 on power-up and counts up to 15, after that the counter resets back to 0 and continues to count up, which is particularly helpful in situations such as the following:

- The host or the controller requires consecutive measurements. Using the COUNTER register allows the controller to compare samples and makes sure that the samples are in the expected order without missing intermediate counter values.
- As a safety feature when light levels are not changing, the controller can make sure that the measurements from the OPT4003-Q1 are not stuck by comparing the values of the COUNTER register between measurements. If the COUNTER values continue to change over samples, the device updates the output register with the most recent measurement of light levels.

6.3.3.2 Output CRC

The CRC register consists of cyclic redundancy checker bits as part of the output registers calculated within the OPT4003-Q1 and is updated on every measurement. This feature helps detect communication-related bit errors during the output readout from the device. Register 1 lists the calculation method for the CRC bits, which can be independently verified in the controller or host firmware and software to validate if communication between the controller and the device is successful without bit errors during transmission.

6.3.3.3 Threshold Detection

The OPT4003-Q1 features a threshold detection logic that can be programmed to indicate and update register flags if measured light levels cross thresholds set by the user. The threshold condition can be programmed to use one of the two channels as a trigger, as determined by the THRESHOLD_CH_SEL register. There are independent low- and high-threshold target registers with independent flag registers to indicate the status of measured light level. Measured light levels reaching below the low threshold and above the high threshold are called *faults*. Users can program a fault count register, which counts the consecutive number of faults before the flag registers are set. Calculations for setting up the threshold are available in the *Threshold Detection Calculations* section.

6.4 Device Functional Modes

6.4.1 Modes of Operation

The OPT4003-Q1 has the following modes of operation:

- **Power-down mode:** This mode is a power-down or standby mode where the device enters a low-power state. There is no active light sensing or conversion in this mode. The device still responds to I^{2}C transactions that can be used to bring the device out of this mode. The OPERATING_MODE register is set to 0.
- **Continuous mode:** In this mode, the OPT4003-Q1 measures and updates the output registers continuously as determined by the conversion time and generates a hardware interrupt on the INT pin for every successful conversion. Configure the INT pin in output mode using the INT_DIR register. The device active circuits are continuously kept active to minimize the interval between measurements. The OPERATING_MODE register is set to 3.
- **One-shot mode:** There are two ways in which the OPT4003-Q1 can be used in one-shot mode of operation with one common theme where the OPT4003-Q1 stays in standby mode and a conversion is triggered either by a register write to the configuration register or by a hardware interrupt on the INT pin .

  There are two types of one-shot modes. Both of these modes operate with auto-range selection logic unless a manual range mode is specified by setting the RANGE bits in the configuration register.

  - **Force auto-range one-shot mode:** Every one-shot trigger forces a full reset on the auto-ranging control logic and a fresh auto-range detection is initiated, ignoring the previous measurements. This mode is particularly useful in situations where lighting conditions are expected to change frequently and the conditions for the one-shot trigger frequency are not expected to change very often. There is a small penalty on conversion time resulting from the auto-ranging logic recovering from a reset state. The full reset cycle on the auto-ranging control logic takes approximately 500 µs, which must be accounted for between measurements when this mode is used. The OPERATING_MODE register is set to 1.
  - **Regular auto-range one-shot mode:** Auto-range selection logic uses the information from the previous measurements to determine the range for the current trigger. Only use this mode when the device needs time-synchronized measurements with frequent triggers from the controller. In other words, this mode can be used as an alternative to continuous mode. The key difference between these modes is that the interval between measurements is determined by the one-shot triggers. The OPERATING_MODE register is set to 2.

  One-shot mode can be triggered by the following:

  - **Hardware trigger :** The INT pin can be configured as an input to trigger a measurement, setting the INT_DIR register to 0. When the INT pin is used as input, there is no hardware interrupt to indicate completion of measurement. The controller must keep time from the trigger mechanism and read out output registers.

  – **Register trigger:** An I^{2}C write to the OPERATING_MODE register triggers a measurement (value of 1 or 2). The register value is reset after the next successful measurement. The INT pin can be configured to indicate measurement completion to read out the output registers by setting the INT_DIR register to 1.

The interval between subsequent triggers must be set to account for all aspects involved in the trigger mechanism, such as the I^{2}C transaction time, device wake-up time, auto-range time (if used), and device conversion time. If a conversion trigger is received before the completion of the current measurement, the device simply ignores the new request until the previous conversion is completed.

The device enters standby after each one-shot trigger; therefore, the measurement interval in the one-shot trigger mechanism must account for additional time (t_{ss} time, as specified in the *Specifications* section for the circuits to recover from standby state. However, setting the quick wake-up register QWAKE eliminates the need for this additional t_{ss} at the cost of not powering down the active circuit with the device not entering standby mode between triggers.

Figure 6-2 illustrates a timing diagram of the various operating modes.

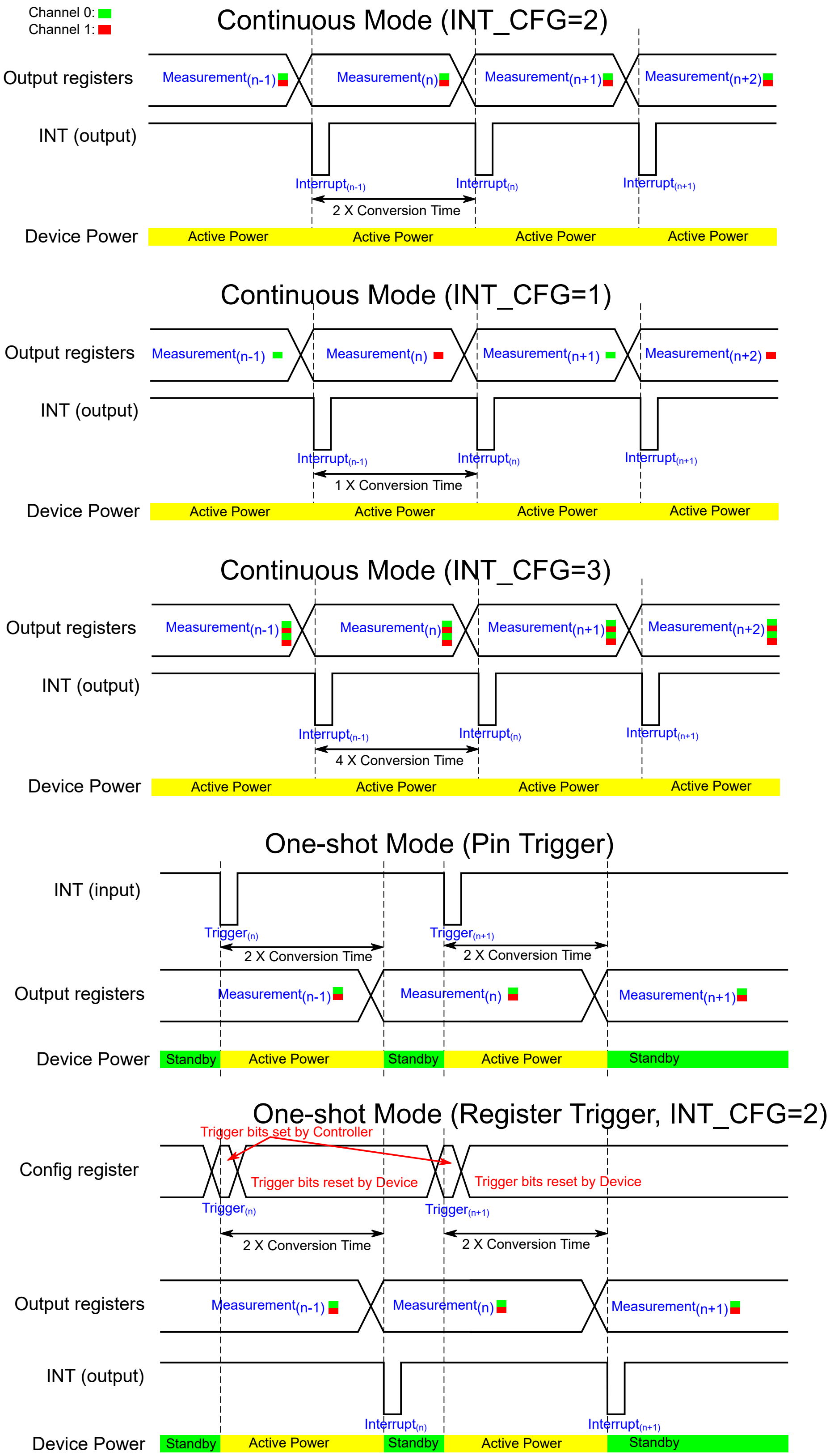


Figure 6-2. Timing Diagrams for Different Operating Modes

6.4.2 Interrupt Modes of Operation

The device has an interrupt reporting system that allows the processor connected to the I^{2}C bus to go to sleep, or otherwise ignore the device results, until a user-defined event occurs that requires possible action. Alternatively, this same mechanism can also be used with any system that can take advantage of a single digital signal that indicates whether the light is above or below levels of interest.

The INT pin has an open-drain output, which requires the use of a pullup resistor. This open-drain output allows multiple devices with open-drain INT pins to connect to the same line, thus creating a logical *NOR* or *AND* function between the devices. The polarity of the INT pin can be controlled by the INT_POL register.

There are two major types of interrupt reporting mechanism modes: latched window comparison mode and transparent hysteresis comparison mode. The LATCH configuration register controls which of these two modes is used. Table 6-1 and Figure 6-3 summarize the function of these two modes. Additionally, the INT pin can either be used to indicate a fault in one of these modes (INT_CFG = 0) or to indicate a conversion completion (INT_CFG > 0). Table 6-2 details this functionality.

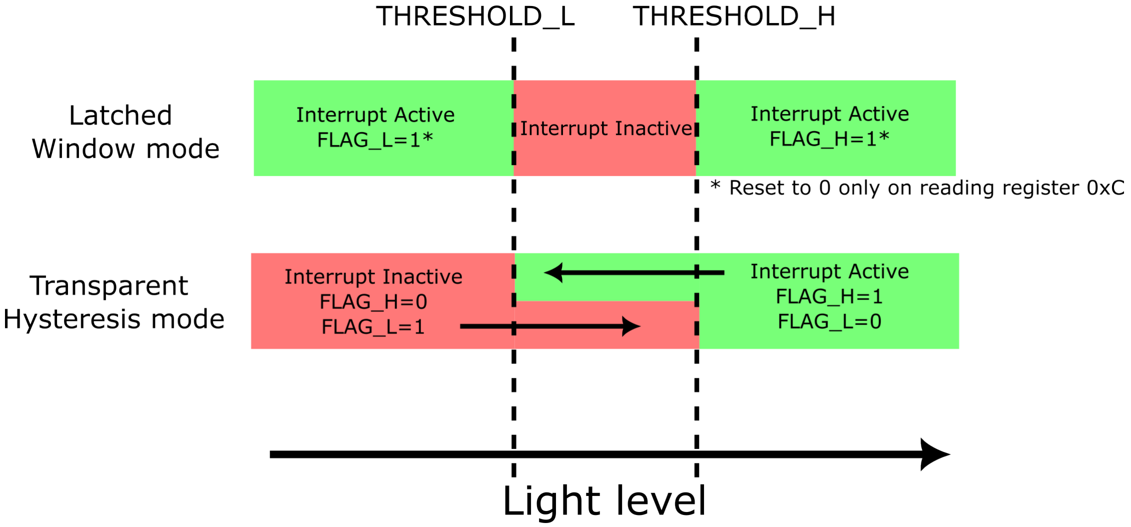


Figure 6-3. Interrupt Pin Status (INT_CFG = 0 Setting) and Register Flag Behavior

Table 6-1. Interrupt Pin Status (INT_CFG = 0 Setting) and Register Flag Behavior

LATCH SETTING	INT PIN STATE (WHEN INT_CFG=0)	FLAG_H VALUE	FLAG_L VALUE	LATCHING BEHAVIOR
0: Transparent hysteresis mode	The INT pin indicates if measurement is above (INT active) or below (INT inactive) the threshold. If measurement is between the high and low threshold values, then the previous INT value is maintained. This mode prevents the INT pin from repeated toggling when the measurement values are close to the threshold.	0: If measurement is below the low limit 1: If measurement is above the high limit If measurement is between the high and low limits, the previous value is maintained.	0: If measurement is above the high limit 1: If measurement is below the low limit If measurement is between the high and low limits, the previous value is maintained.	Not latching: Values are updated after each conversion
1: Latched window mode	The INT pin becomes active if the measurement is outside the window (above the high threshold or below the low threshold). The INT pin does not reset and returns to the inactive state until the 0xC is register read.	1: If measurement is above the high limit	1: If measurement is below the low limit	Latching: The INT pin, FLAG_H, and FLAG_L values do not reset until the 0x0C register is read.

The THRESHOLD_H, THRESHOLD_L, LATCH, and FAULT_COUNT registers control the interrupt behavior. As shown in Table 6-1, the LATCH field setting provides a choice between the latched window mode and transparent hysteresis mode. Interrupt reporting can be observed on the INT pin , the FLAG_H, and the FLAG_L registers.

Results from comparing the current sensor measurements with the THRESHOLD_H and THRESHOLD_L registers are referred to as *fault events*. See the *Threshold Detection Calculations* section for the calculations to set these registers. The FAULT_COUNT register dictates the number of continuous *fault events* required to trigger an interrupt event and subsequently change the state of the interrupt reporting mechanisms. For example, with a FAULT_COUNT value of 2 corresponding to four fault counts, the INT pin , FLAG_H, and FLAG_L states shown in Table 6-1 are not realized unless four consecutive measurements are taken that satisfy the fault condition.

The INT pin function listed in Table 6-1 is valid only when INT_CFG = 0. As described in Table 6-2, the INT pin function can be changed to indicate an end of conversion or FIFO full state. The FLAG_H and FLAG_L registers continue to behave as listed in Table 6-1, even while INT_CFG > 0. The polarity of the INT pin is controlled by the INT_POL register.

Table 6-2. INT_CFG Setting and Resulting INT Pin Behavior

INT_CFG SETTING	INT PIN FUNCTION
0	As per Table 6-1
1	INT pin asserted with a 1-µs pulse duration after every conversion
2	INT pin asserted with a 1-µs pulse duration every two conversions to indicate both channel measurements are complete
3	INT pin asserted with a 1-µs pulse duration every four conversions to indicate the FIFO is full

6.4.3 Light Range Selection

The OPT4003-Q1 has an automatic full-scale-range setting mode that eliminates the need to predict and set the best range for the device. Set the RANGE register to 0xC to enter this mode. The device determines the appropriate full-scale range to take the measurement based on a combination of current lighting conditions and the previous measurement.

If a measurement is towards the low side of full-scale, then the full-scale range is decreased by one or two settings for the next measurement. If a measurement is towards the upper side of full-scale, the full-scale range is increased by one setting for the next measurement.

If the measurement exceeds the full-scale range, resulting from a fast increasing optical transient event, then the current measurement is terminated. This invalid measurement is not reported. If the scale is not at the maximum, then the device increases the scale by one step and a new measurement is retaken with that scale. Therefore, during a fast increasing optical transient in this mode, a measurement can possibly take longer to complete and report than indicated by the CONVERSION_TIME configuration register.

Using this feature is highly recommended by Texas Instruments because the device selects the best range setting based on lighting conditions. However, there is an option to manually set the range. Setting the range manually turns off the automatic full-scale selection logic and the device operates for a particular range setting. The Range Selection Table lists the range selection settings.

The channel 1 irradiance levels are specified with an 810-nm stimulus. The Range Selection Table shows the behavior of channel 0 and channel 1 when setting the RANGE register. Since channel 1 has 7 full-scale light ranges, the exponent register bits are limited to 6, while channel 0 has 9 full-scale light ranges and a maximum exponent value of 8.

Table 6-3. Range Selection Table for SOT-5X3 Variant

RANGE REGISTER SETTING	CH0 TYPICAL FULL-SCALE LIGHT LEVEL FOR SOT-5X3 VARIANT	CH0 EXPONENT	CH1 TYPICAL FULL-SCALE IRRADIANCE FOR SOT-5X3 VARIANT	CH1 EXPONENT
0	613 lux	0	0.469 mW/cm^2	0
1	1227 lux	1	0.937 mW/cm^2	1
2	2454 lux	2	1.87 mW/cm^2	2
3	4907 lux	3	3.75 mW/cm^2	3
4	9815 lux	4	7.50 mW/cm^2	4
5	19629 lux	5	15.00 mW/cm^2	5
6	39259 lux	6	30.00 mW/cm^2	6
7	78517 lux	7	30.00 mW/cm^2	6
8	157035 lux	8	30.00 mW/cm^2	6
12	Determined by automatic full-scale range logic; sets channel 0 and channel 1 independently			

Table 6-4. Range Selection Table for USON Variant

RANGE REGISTER SETTING	CH0 TYPICAL FULL-SCALE LIGHT LEVEL FOR USON VARIANT	CH0 EXPONENT	CH1 TYPICAL FULL-SCALE IRRADIANCE FOR USON VARIANT	CH1 EXPONENT
0	561 lux	0	0.429 mW/cm^2	0
1	1122 lux	1	0.858 mW/cm^2	1
2	2244 lux	2	1.72 mW/cm^2	2
3	4488 lux	3	3.43 mW/cm^2	3
4	8976 lux	4	6.86 mW/cm^2	4
5	17952 lux	5	13.72 mW/cm^2	5
6	35903 lux	6	27.45 mW/cm^2	6
7	71806 lux	7	27.45 mW/cm^2	6
8	143613 lux	8	27.45 mW/cm^2	6
12	Determined by automatic full-scale range logic; sets channel 0 and channel 1 independently			

6.4.4 Selecting Conversion Time

As listed in Table 6-5, the OPT4003-Q1 offers several conversion times that can be selected. Conversion time is defined as the time taken from initiation to completion of one measurement, including the time taken to update the results in the output register. Measurement initiation is determined by the mode of operation, as specified in *Modes of Operation* section.

Table 6-5. Conversion Time Selection

CONVERSION_TIME REGISTER	TYPICAL CONVERSION TIME PER CHANNEL
0	0.6 ms
1	1 ms
2	1.8 ms
3	3.4 ms
4	6.5 ms
5	12.7 ms
6	25 ms
7	50 ms
8	100 ms
9	200 ms
10	400 ms
11	800 ms

6.4.5 Light Measurement in Lux

The OPT4003-Q1 measures light and updates output registers with proportional ADC codes. The output of the device is represented by two parts: by four EXPONENT register bits and by 20 MANTISSA bits. This arrangement of binary logarithmic full-scale ranges with linear representation in a range helps cover a large dynamic range of measurements. MANTISSA represents the linear ADC codes proportional to the measured light within a given full-scale range and the EXPONENT bits represent the current full-scale range selected. The selected range can either be automatically determined by the auto-range selection logic or manually selected as per Section 6.4.3.

The lux level can be determined using the following equations. First, use Equation 1 or Equation 2 to calculate the MANTISSA. Next, use Equation 3 or Equation 4 to calculate the ADC_CODES. Finally, use Equation 6 to calculate the lux.

$$\text{MANTISSA} = (\text{RESULT\_MSB} << 8) + \text{RESULT\_LSB} \tag{1}$$

or

$$\text{MANTISSA} = (\text{RESULT\_MSB} \times 2\text{\textasciicircum}8) + \text{RESULT\_LSB} \tag{2}$$

where:

- The RESULT_MSB, RESULT_LSB, and EXPONENT bits are parts of the output register

The RESULT_MSB register carries the most significant 12 bits of the MANTISSA, and the RESULT_LSB register carries the least significant eight bits of the MANTISSA. Use the previous equations to get the 20-bit MANTISSA number. The four EXPONENT bits are directly read from the register.

After the EXPONENT and MANTISSA portions are calculated, use Equation 3 or Equation 4 to calculate the linearized ADC_CODES.

$$ADC\_CODES = (MANTISSA << E) \quad (3)$$

or

$$ADC\_CODES = (MANTISSA \times 2^E) \quad (4)$$

The maximum value for register E is 8, thus the ADC_CODES is effectively a 28-bit number. As shown in Equation 6, the semi-logarithmic numbers are converted to a linear ADC_CODES representation, which is simple to convert to lux.

(5)

$$lux = ADC\_CODES \times 535E\text{-}6 \text{ for the USON variant} \quad (6)$$

$$lux = ADC\_CODES \times 585E\text{-}6 \text{ for the SOT-5X3 variant} \quad (7)$$

The MANTISSA and ADC_CODES are large numbers with 20 and 28 bits required to represent them. While developing firmware or software for these calculations, allocating appropriate data types to prevent data overflow is important. Some explicit typecasting to a larger data type is recommended, such as 32-bit representation before a left-shift operation (<<).

6.4.6 Threshold Detection Calculations

The THRESHOLD_H_RESULT and THRESHOLD_L_RESULT threshold result registers are 12 bits, whereas the THRESHOLD_H_EXPONENT and THRESHOLD_L_EXPONENT threshold exponent registers are four bits. The threshold is compared at linear ADC_CODES, as given by the following equations. Therefore, the threshold registers are padded with zeros internally to compare with the ADC_CODES.

$$ADC\_CODES\_TH = THRESHOLD\_H\_RESULT << (8 + THRESHOLD\_H\_EXPONENT) \quad (8)$$

or

$$ADC\_CODES\_TH = THRESHOLD\_H\_RESULT \times 2^{(8 + THRESHOLD\_H\_EXPONENT)} \quad (9)$$

and

$$ADC\_CODES\_TL = THRESHOLD\_L\_RESULT << (8 + THRESHOLD\_L\_EXPONENT) \quad (10)$$

or

$$ADC\_CODES\_TL=THRESHOLD\_L\_RESULT \times 2^{(8 + THRESHOLD\_L\_EXPONENT)} \quad (11)$$

Thresholds are then compared as given in the following equations to detect *fault events.*

$$\text{If } ADC\_CODES < ADC\_CODES\_TL \text{ a } \textit{fault low} \text{ is detected} \quad (12)$$

and

$$\text{If } ADC\_CODES > ADC\_CODES\_TH \text{ a } \textit{fault high} \text{ is detected} \quad (13)$$

Based on the FAULT_COUNT register setting, with consecutive *fault high* or *fault low* events, the respective FLAG_H and FLAG_L registers are set. See the *Interrupt Modes of Operation* section for more information. Understanding the relation between the THRESHOLD_H_EXPONENT, THRESHOLD_H_RESULT, THRESHOLD_L_EXPONENT, and THRESHOLD_L_RESULT register bits and the output registers is important to set the appropriate threshold based on application needs.

6.4.7 Light Resolution

The effective resolution of the OPT4003-Q1 is dependent on both the conversion time setting and the full-scale light range. Although the LSB resolution of the linear ADC_CODES does not change, the effective or useful resolution of the device is dependent (as per Table 6-6) on the conversion time setting and the full-scale range. In conversion times where the effective resolution is lower, the LSBs are padded with 0.

Table 6-6. Channel 0 Resolution Table for the USON Variant

CONVERSION_TIME REGISTER	CONVERSION TIME	MANTISSA EFFECTIVE BITS	EXPONENT								
			0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
			FULL-SCALE LUX								
			561	**1122**	**2244**	**4488**	**8976**	**17952**	**35903**	**71806**	**143613**
			Effective Resolution in Lux								
0	600 µs	9	1.096	2.191	4.38	8.77	17.53	35.06	70.12	140.25	280.49
1	1 ms	10	547.84 m	1.096	2.191	4.38	8.77	17.53	35.06	70.12	140.25
2	1.8 ms	11	273.92 m	547.84 m	1.096	2.191	4.38	8.77	17.53	35.06	70.12
3	3.4 ms	12	136.96 m	273.92 m	547.84 m	1.096	2.191	4.38	8.77	17.53	35.06
4	6.5 ms	13	68.48 m	136.96 m	273.92 m	547.84 m	1.096	2.191	4.38	8.77	17.53
5	12.7 ms	14	34.24 m	68.48 m	136.96 m	273.92 m	547.84 m	1.096	2.191	4.38	8.77
6	25 ms	15	17.12 m	34.24 m	68.48 m	136.96 m	273.92 m	547.84 m	1.096	2.191	4.38
7	50 ms	16	8.56 m	17.12 m	34.24 m	68.48 m	136.96 m	273.92 m	547.84 m	1.096	2.191
8	100 ms	17	4.28 m	8.56 m	17.12 m	34.24 m	68.48 m	136.96 m	273.92 m	547.84 m	1.096
9	200 ms	18	2.14 m	4.28 m	8.56 m	17.12 m	34.24 m	68.48 m	136.96 m	273.92 m	547.84 m
10	400 ms	19	1.07 m	2.14 m	4.28 m	8.56 m	17.12 m	34.24 m	68.48 m	136.96 m	273.92 m
11	800 ms	20	0.535 m	1.07 m	2.14 m	4.28 m	8.56 m	17.12 m	34.24 m	68.48 m	136.96 m

Table 6-7. Channel 1 Resolution Table for the USON Variant

CONVERSION_ TIME REGISTER	CONVERSION TIME	MANTISSA EFFECTIVE BITS	EXPONENT						
			0	**1**	**2**	**3**	**4**	**5**	**6**
			FULL-SCALE IRRADIANCE (µW/cm^2)						
			429	**858**	**1715**	**3431**	**6862**	**13724**	**27447**
			Effective Resolution (nW/cm^2)						
0	600 µs	9	837.63	1675.26	3350.53	6701.06	13402.11	26804.22	53608.45
1	1 ms	10	418.82	837.63	1675.26	3350.53	6701.06	13402.11	26804.22
2	1.8 ms	11	209.41	418.82	837.63	1675.26	3350.53	6701.06	13402.11
3	3.4 ms	12	104.7	209.41	418.82	837.63	1675.26	3350.53	6701.06
4	6.5 ms	13	52.35	104.7	209.41	418.82	837.63	1675.26	3350.53
5	12.7 ms	14	26.18	52.35	104.7	209.41	418.82	837.63	1675.26
6	25 ms	15	13.09	26.18	52.35	104.7	209.41	418.82	837.63
7	50 ms	16	6.54	13.09	26.18	52.35	104.7	209.41	418.82
8	100 ms	17	3.27	6.54	13.09	26.18	52.35	104.7	209.41
9	200 ms	18	1.64	3.27	6.54	13.09	26.18	52.35	104.7
10	400 ms	19	0.818	1.64	3.27	6.54	13.09	26.18	52.35
11	800 ms	20	0.409	0.818	1.64	3.27	6.54	13.09	26.18

Table 6-8. Channel 0 Resolution Table for the SOT-5X3 Variant

CONVERSION_TIME REGISTER	CONVERSION TIME	MANTISSA EFFECTIVE BITS	EXPONENT								
			0	1	2	3	4	5	6	7	8
			FULL-SCALE LUX								
			613	1227	2454	4907	9815	19629	39259	78517	157035
			Effective Resolution in Lux								
0	600 µs	9	1.20	2.40	4.79	9.58	19.17	38.34	76.68	153.35	306.71
1	1 ms	10	599.04 m	1.20	2.40	4.79	9.58	19.17	38.34	76.68	153.35
2	1.8 ms	11	299.52 m	599.04 m	1.20	2.40	4.79	9.58	19.17	38.34	76.68
3	3.4 ms	12	149.76 m	299.52 m	599.04 m	1.20	2.40	4.79	9.58	19.17	38.34
4	6.5 ms	13	74.88 m	149.76 m	299.52 m	599.04 m	1.20	2.40	4.79	9.58	19.17
5	12.7 ms	14	37.44 m	74.88 m	149.76 m	299.52 m	599.04 m	1.20	2.40	4.79	9.58
6	25 ms	15	18.72 m	37.44 m	74.88 m	149.76 m	299.52 m	599.04 m	1.20	2.40	4.79
7	50 ms	16	9.36 m	18.72 m	37.44 m	74.88 m	149.76 m	299.52 m	599.04 m	1.20	2.40
8	100 ms	17	4.68 m	9.36 m	18.72 m	37.44 m	74.88 m	149.76 m	299.52 m	599.04 m	1.20
9	200 ms	18	2.34 m	4.68 m	9.36 m	18.72 m	37.44 m	74.88 m	149.76 m	299.52 m	599.04 m
10	400 ms	19	1.17 m	2.34 m	4.68 m	9.36 m	18.72 m	37.44 m	74.88 m	149.76 m	299.52 m
11	800 ms	20	0.585 m	1.17 m	2.34 m	4.68 m	9.36 m	18.72 m	37.44 m	74.88 m	149.76 m

Table 6-9. Channel 1 Resolution Table for the SOT-5X3 Variant

CONVERSION_ TIME REGISTER	CONVERSION TIME	MANTISSA EFFECTIVE BITS	EXPONENT						
			0	1	2	3	4	5	6
			FULL-SCALE IRRADIANCE (µW/cm^2)						
			469	937	1875	3750	7499	14999	29998
			Effective Resolution (nW/cm^2)						
0	600 µs	9	915.46	1830.91	3661.82	7323.65	14647.30	29294.59	58589.18
1	1 ms	10	457.73	915.46	1830.91	3661.82	7323.65	14647.30	29294.59
2	1.8 ms	11	228.86	457.73	915.46	1830.91	3661.82	7323.65	14647.30
3	3.4 ms	12	114.43	228.86	457.73	915.46	1830.91	3661.82	7323.65
4	6.5 ms	13	57.22	114.43	228.86	457.73	915.46	1830.91	3661.82
5	12.7 ms	14	28.61	57.22	114.43	228.86	457.73	915.46	1830.91
6	25 ms	15	14.30	28.61	57.22	114.43	228.86	457.73	915.46
7	50 ms	16	7.15	14.30	28.61	57.22	114.43	228.86	457.73
8	100 ms	17	3.58	7.15	14.30	28.61	57.22	114.43	228.86
9	200 ms	18	1.79	3.58	7.15	14.30	28.61	57.22	114.43
10	400 ms	19	0.894	1.79	3.58	7.15	14.30	28.61	57.22
11	800 ms	20	0.447	1.79	1.79	3.58	7.15	14.30	28.61

6.5 Programming

The OPT4003-Q1 supports the transmission protocol for standard mode (up to 100 kHz), fast mode (up to 400 kHz), and high-speed mode (up to 2.6 MHz). Fast and standard modes are described as the default protocol, referred to as *F/S*. High-speed mode is described in the *High-Speed I2C Mode* section.

6.5.1 I^{2}C Bus Overview

The OPT4003-Q1 offers compatibility with both I^{2}C and SMBus interfaces. The I^{2}C and SMBus protocols are essentially compatible with one another. The I^{2}C interface is used throughout this document as the primary example with the SMBus protocol specified only when a difference between the two protocols is discussed.

The device is connected to the bus with two pins: an SCL clock input pin and an SDA open-drain bidirectional data pin. The bus must have a controller device that generates the serial clock (SCL), controls the bus access, and generates start and stop conditions. To address a specific device, the controller initiates a start condition by pulling the data signal line (SDA) from a high logic level to a low logic level while SCL is high. All targets on the bus shift in the target address byte on the SCL rising edge, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the target being addressed responds to the controller by generating an acknowledge bit by pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition. When all data are transferred, the controller generates a stop condition, indicated by pulling SDA from low to high while SCL is high. The device includes a 28-ms timeout on the I^{2}C interface to prevent locking up the bus. If the SCL line is held low for this duration of time, the bus state machine is reset.

6.5.1.1 Serial Bus Address

To communicate with the OPT4003-Q1, the controller must first initiate an I^{2}C start command. Then, the controller must address target devices through a target address byte. The target address byte consists of a seven bit address and a direction bit that indicates whether the action is to be a read or write operation.

Four I^{2}C addresses are possible by connecting the ADDR pin to one of four pins: GND, VDD, SDA, or SCL. Table 6-10 summarizes the possible addresses with the corresponding ADDR pin configuration. The state of the ADDR pin is sampled on every bus communication and must be driven or connected to the desired level before any activity on the interface occurs.

Table 6-10. ADDR Pin Addresses

ADDR PIN CONNECTION	DEVICE I^{2}C ADDRESS
GND	1000100
VDD	1000101
SDA	1000110
SCL	1000111

6.5.1.2 Serial Interface

The OPT4003-Q1 operates as a target device on both the I^{2}C bus and SMBus. Connections to the bus are made through the SCL clock input line and the SDA open-drain I/O line. The device supports the transmission protocol for standard mode (up to 100 kHz), fast mode (up to 400 kHz), and high-speed mode (up to 2.6 MHz). All data bytes are transmitted most significant bits first.

The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise.

6.5.2 Writing and Reading

Accessing a specific register on the OPT4003-Q1 is accomplished by writing the appropriate register address during the I^{2}C transaction sequence. See the *Register Maps* for a complete list of registers and the corresponding register addresses. The value for the register address (as shown in Figure 6-4) is the first byte transferred after the target address byte with the R/W bit low.

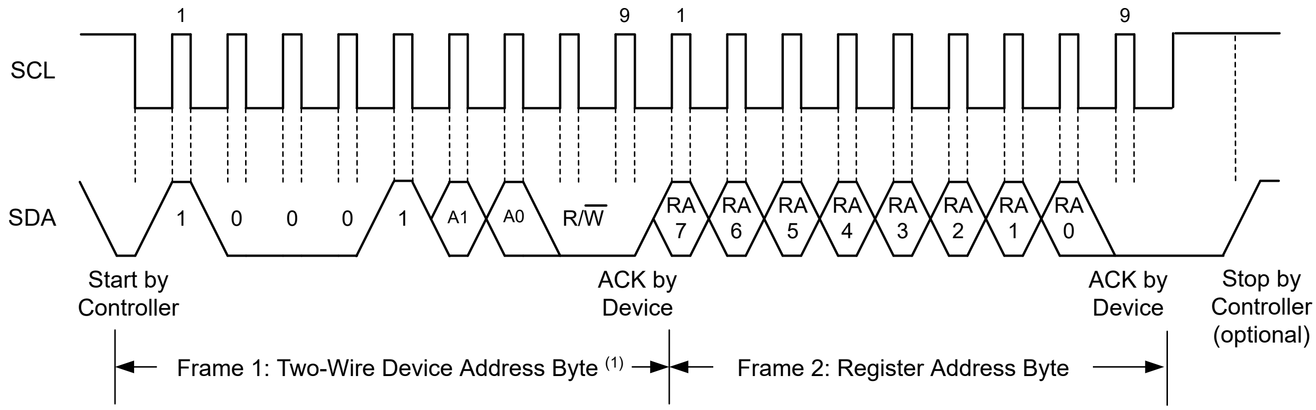


Figure 6-4. Setting the I^{2}C Register Address

Writing to a register begins with the first byte transmitted by the controller. This byte is the target address with the R/W bit low. The device then acknowledges receipt of a valid address. The next byte transmitted by the controller is the address of the register that data are to be written to. The next two bytes are written to the register addressed by the register address. The device acknowledges receipt of each data byte. The controller can terminate the data transfer by generating a start or stop condition.

When reading from the device, the last value stored in the register address by a write operation determines which register is read during a read operation. To change the register address for a read operation, a new partial I^{2}C write transaction must be initiated. This partial write is accomplished by issuing a target address byte with the R/W bit low, followed by the register address byte and a stop command. The controller then generates a start condition and sends the target address byte with the R/W bit high to initiate the read command. The next byte is transmitted by the target and is the most significant byte of the register indicated by the register address. This byte is followed by an acknowledge from the controller, then the target transmits the least significant byte. The controller acknowledges receipt of the data byte. The controller can terminate the data transfer by generating a not-acknowledge after receiving any data byte, or by generating a start or stop condition. If repeated reads from the same register are desired, continually sending the register address bytes is not necessary. The device retains the register address until that number is changed by the next write operation.

Figure 6-5 and Figure 6-6 show the write and read operation timing diagrams, respectively. Register bytes are sent most significant byte first, followed by the least significant byte.

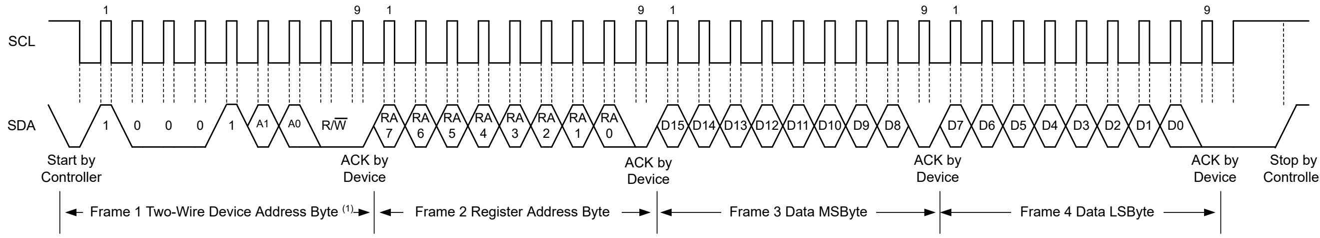
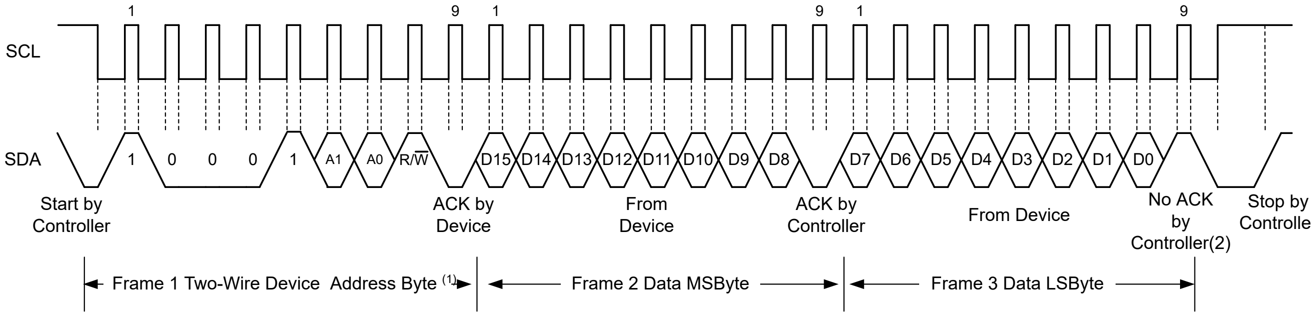


Figure 6-5. I^{2}C Write Example



A. An ACK by the controller can also be sent.

Figure 6-6. I^{2}C Read Example

6.5.2.1 High-Speed I^{2}C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pullup resistors or active pullup devices. The controller generates a start condition followed by a valid serial byte containing the high-speed (HS) controller code 0000 1XXXb. This transmission is made in either standard mode or fast mode (up to 400 kHz). The device does not acknowledge the HS controller code but does recognize the code and switches the internal filters to support a 2.6-MHz operation.

The controller then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.6 MHz are allowed. Instead of using a stop condition, use repeated start conditions to secure the bus in HS mode. A stop condition ends the HS mode and switches all internal filters of the device to support the F/S mode.

6.5.2.2 Burst Read Mode

The OPT4003-Q1 supports I^{2}C burst read mode, which helps minimize the number of transactions on the bus for efficient data transfer from the device to the controller.

Before considering the burst mode, a regular I^{2}C read transaction involves an I^{2}C write operation to the device read pointer, followed by the actual I^{2}C read operation. If regular I^{2}C read transactions are performed when reading from the output registers and FIFO registers, which are in continuous locations, then the register pointer is written every two bytes and this process takes up several clock cycles. With the burst mode enabled, the read pointer address is auto incremented after every register read (two bytes), eliminating the need to write operations to set the pointer for subsequent register reads.

Set the I2C_BURST register to enable burst mode. When a stop command is issued, the pointer resets to the original register address before the auto-increments. Figure 6-7 shows a diagram of the I^{2}C write, single read, and burst mode read operation.

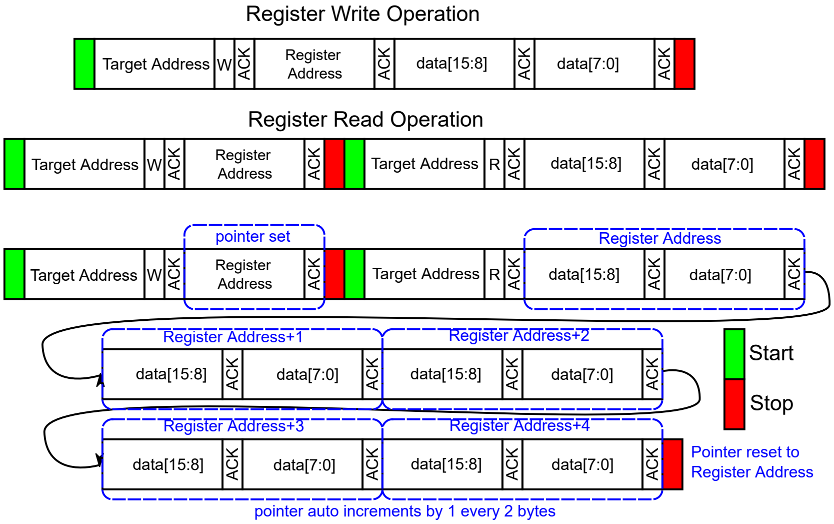


Figure 6-7. I^{2}C Operations

6.5.2.3 General-Call Reset Command

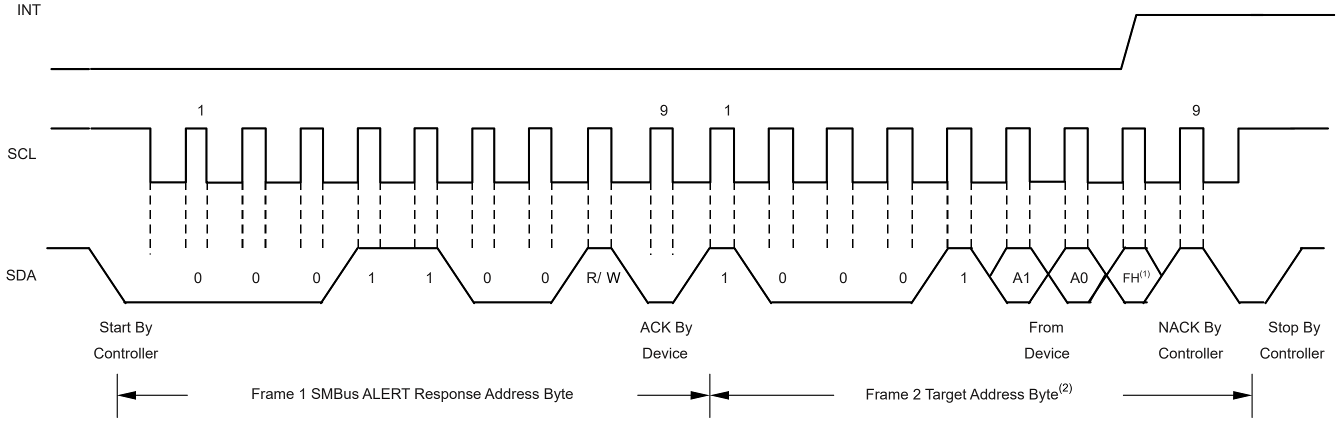
The I^{2}C general-call reset allows the host controller in one command to reset all devices on the bus that respond to the general-call reset command. Write to the I^{2}C address 0 (0000 0000b) to initiate the general call. The reset command is initiated when the subsequent second address byte is 06h (0000 0110b). With this transaction, the device issues an acknowledge bit and sets all registers to the power-on-reset default condition.

6.5.2.4 SMBus Alert Response

The SMBus alert response provides a quick identification for which device issued the interrupt. Without this alert response capability, the processor can not determine which device pulled the interrupt line when there are multiple target devices connected.

The OPT4003-Q1 is designed to respond to the SMBus alert response address when in the latched window-style comparison mode. The OPT4003-Q1 does not respond to the SMBus alert response when in transparent mode.

Figure 6-8 shows the behavior of the device towards the SMBus alert response. When the interrupt line to the processor is pulled to active, the controller can broadcast the alert response target address. Following this alert response, any target devices that generated an alert identify themselves by acknowledging the alert response and sending the respective I^{2}C address on the bus. The alert response can activate several different target devices simultaneously. If more than one target attempts to respond, bus arbitration rules apply. The device with the lowest address wins the arbitration. If the OPT4003-Q1 loses the arbitration, the device does not acknowledge the I^{2}C transaction and the INT pin remains in an active state, prompting the I^{2}C controller processor to issue a subsequent SMBus alert response. When the OPT4003-Q1 wins the arbitration, the device acknowledges the transaction and sets the INT pin to inactive. The controller can issue that same command again, as many times as necessary to clear the INT pin. See the *Interrupt Modes of Operation* section for information on how the flags and INT pin are controlled. The controller can obtain information about the source of the OPT4003-Q1 interrupt from the address broadcast in the above process. The FLAG_H value is sent as the final LSB of the address to provide the controller additional information about the cause of the OPT4003-Q1 interrupt. If the controller requires additional information, the result register or the configuration register can be queried. The FLAG_H and FLAG_L fields are not cleared with an SMBus alert response.



A. FH is the FLAG_H register.

Figure 6-8. Timing Diagram for SMBus Alert Response

7 Register Maps

Figure 7-1. ALL Register Map

<table>
<tr><th>ADD</th><th>D15</th><th>D14</th><th>D13</th><th>D12</th><th>D11</th><th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>00h</td><td colspan="4">EXPONENT_CH0</td><td colspan="12">RESULT_MSB_CH0</td></tr>
<tr><td>01h</td><td colspan="8">RESULT_LSB_CH0</td><td colspan="4">COUNTER_CH0</td><td colspan="4">CRC_CH0</td></tr>
<tr><td>02h</td><td colspan="4">EXPONENT_CH1</td><td colspan="12">RESULT_MSB_CH1</td></tr>
<tr><td>03h</td><td colspan="8">RESULT_LSB_CH1</td><td colspan="4">COUNTER_CH1</td><td colspan="4">CRC_CH1</td></tr>
<tr><td>04h</td><td colspan="4">EXPONENT_FIFO_CH0</td><td colspan="12">RESULT_MSB_FIFO_CH0</td></tr>
<tr><td>05h</td><td colspan="8">RESULT_LSB_FIFO_CH0</td><td colspan="4">COUNTER_FIFO_CH0</td><td colspan="4">CRC_FIFO_CH0</td></tr>
<tr><td>06h</td><td colspan="4">EXPONENT_FIFO_CH1</td><td colspan="12">RESULT_MSB_FIFO_CH1</td></tr>
<tr><td>07h</td><td colspan="8">RESULT_LSB_FIFO_CH1</td><td colspan="4">COUNTER_FIFO_CH1</td><td colspan="4">CRC_FIFO_CH1</td></tr>
<tr><td>08h</td><td colspan="4">THRESHOLD_L_EXPONENT</td><td colspan="12">THRESHOLD_L_RESULT</td></tr>
<tr><td>09h</td><td colspan="4">THRESHOLD_H_EXPONENT</td><td colspan="12">THRESHOLD_H_RESULT</td></tr>
<tr><td>0Ah</td><td>QWAKE</td><td>0</td><td colspan="4">RANGE</td><td colspan="4">CONVERSION_TIME</td><td colspan="2">OPERATING_MODE</td><td>LATCH</td><td>INT_POL</td><td colspan="2">FAULT_COUNT</td></tr>
<tr><td>0Bh</td><td colspan="10">128</td><td>THRESHOLD_CH_SEL</td><td>INT_DIR</td><td colspan="2">INT_CFG</td><td>0</td><td>I2C_BURST</td></tr>
<tr><td>0Ch</td><td colspan="12">0</td><td>OVERLOAD_FLAG</td><td>CONVERSION_READY_FLAG</td><td>FLAG_H</td><td>FLAG_L</td></tr>
<tr><td>11h</td><td colspan="2">0</td><td colspan="2">DIDL</td><td colspan="12">DIDH</td></tr>
</table>

7.1 Register Descriptions

7.1.1 Register 0h (offset = 0h) [reset = 0h]

Figure 7-2. Register 0h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">EXPONENT_CH0</td><td colspan="4">RESULT_MSB_CH0</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="4">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESULT_MSB_CH0</td></tr>
<tr><td colspan="8">R-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-3. Register 00 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	EXPONENT_CH0	R	0h	EXPONENT output CH0. Determines the full-scale range of the light measurement for the channel. Used as a scaling factor for lux calculation.
11-0	RESULT_MSB_CH0	R	0h	Result register MSB (most significant bits) CH0. Used to calculate the MANTISSA representing light level within a given EXPONENT or full-scale range.

7.1.2 Register 1h (offset = 1h) [reset = 0h]

Figure 7-4. Register 1h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESULT_LSB_CH0</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">COUNTER_CH0</td><td colspan="4">CRC_CH0</td></tr>
<tr><td colspan="4">R-0h</td><td colspan="4">R-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-5. Register 01 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESULT_LSB_CH0	R	0h	Result register LSB (least significant bits) CH0. Used to calculate MANTISSA representing light level within a given EXPONENT or full-scale range.
7-4	COUNTER_CH0	R	0h	Sample counter CH0. Rolling counter that increments for every conversion.
3-0	CRC_CH0	R	0h	CRC bits CH0. R[19:0] = MANTISSA = ((RESULT_MSB<<8) + RESULT_LSB X[0] = XOR(E[3:0], R[19:0], C[3:0]) XOR of all bits X[1] = XOR(C[1], C[3], R[1], R[3], R[5], R[7], R[9], R[11], R[13], R[15], R[17], R[19], E[1], E[3]) X[2] = XOR(C[3], R[3], R[7], R[11], R[15], R[19], E[3]) X[3] = XOR(R[3], R[11], R[19])

7.1.3 Register 2h (offset = 2h) [reset = 0h]

Figure 7-6. Register 2h

15	14	13	12	11	10	9	8
EXPONENT_CH1				RESULT_MSB_CH1			
R-0h				R-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESULT_MSB_CH1							
R-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-7. Register 02 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	EXPONENT_CH1	R	0h	EXPONENT output CH1. Determines the full-scale range of the light measurement for the channel. Used as a scaling factor for lux calculation.
11-0	RESULT_MSB_CH1	R	0h	Result register MSB (most significant bits) CH1. Used to calculate the MANTISSA representing light level within a given EXPONENT or full-scale range.

7.1.4 Register 3h (offset = 3h) [reset = 0h]

Figure 7-8. Register 3h

15	14	13	12	11	10	9	8
RESULT_LSB_CH1							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNTER_CH1				CRC_CH1			
R-0h				R-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-9. Register 03 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESULT_LSB_CH1	R	0h	Result register LSB (least significant bits) CH1. Used to calculate MANTISSA representing light level within a given EXPONENT or full-scale range.
7-4	COUNTER_CH1	R	0h	Sample counter CH1. Rolling counter that increments for every conversion.
3-0	CRC_CH1	R	0h	CRC bits CH1. R[19:0] = MANTISSA = ((RESULT_MSB<<8) + RESULT_LSB X[0] = XOR(E[3:0], R[19:0], C[3:0]) XOR of all bits X[1] = XOR(C[1], C[3], R[1], R[3], R[5], R[7], R[9], R[11], R[13], R[15], R[17], R[19], E[1], E[3]) X[2] = XOR(C[3], R[3], R[7], R[11], R[15], R[19], E[3]) X[3] = XOR(R[3], R[11], R[19])

7.1.5 Register 4h (offset = 4h) [reset = 0h]

Figure 7-10. Register 4h

15	14	13	12	11	10	9	8
EXPONENT_FIFO_CH0				RESULT_MSB_FIFO_CH0			
R-0h				R-0h			
7	6	5	4	3	2	1	0
RESULT_MSB_FIFO_CH0							
R-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-11. Register 04 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	EXPONENT_FIFO_CH0	R	0h	EXPONENT register from FIFO CH0
11-0	RESULT_MSB_FIFO_CH0	R	0h	RESULT_MSB Register from FIFO CH0

7.1.6 Register 5h (offset = 5h) [reset = 0h]

Figure 7-12. Register 5h

15	14	13	12	11	10	9	8
RESULT_LSB_FIFO_CH0							
R-0h							
7	6	5	4	3	2	1	0
COUNTER_FIFO_CH0				CRC_FIFO_CH0			
R-0h				R-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-13. Register 05 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESULT_LSB_FIFO_CH0	R	0h	RESULT_LSB register from FIFO CH0
7-4	COUNTER_FIFO_CH0	R	0h	COUNTER register from FIFO CH0
3-0	CRC_FIFO_CH0	R	0h	CRC register from FIFO CH0

7.1.7 Register 6h (offset = 6h) [reset = 0h]

Figure 7-14. Register 6h

15	14	13	12	11	10	9	8
EXPONENT_FIFO_CH1				RESULT_MSB_FIFO_CH1			
R-0h				R-0h			
7	6	5	4	3	2	1	0
RESULT_MSB_FIFO_CH1							
R-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-15. Register 06 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	EXPONENT_FIFO_CH1	R	0h	EXPONENT register from FIFO CH1
11-0	RESULT_MSB_FIFO_CH1	R	0h	RESULT_MSB register from FIFO CH1

7.1.8 Register 7h (offset = 7h) [reset = 0h]

Figure 7-16. Register 7h

15	14	13	12	11	10	9	8
RESULT_LSB_FIFO_CH1							
R-0h							
7	6	5	4	3	2	1	0
COUNTER_FIFO_CH1				CRC_FIFO_CH1			
R-0h				R-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-17. Register 07 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESULT_LSB_FIFO_CH1	R	0h	RESULT_LSB register from FIFO CH1
7-4	COUNTER_FIFO_CH1	R	0h	COUNTER register from FIFO CH1
3-0	CRC_FIFO_CH1	R	0h	CRC register from FIFO CH1

7.1.9 Register 8h (offset = 8h) [reset = 0h]

Figure 7-18. Register 8h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">THRESHOLD_L_EXPONENT</td><td colspan="4">THRESHOLD_L_RESULT</td></tr>
<tr><td colspan="4">R/W-0h</td><td colspan="4">R/W-0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">THRESHOLD_L_RESULT</td></tr>
<tr><td colspan="8">R/W-0h</td></tr>
</table>

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-19. Register 08 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	THRESHOLD_L_EXPONENT	R/W	0h	Threshold low register exponent
11-0	THRESHOLD_L_RESULT	R/W	0h	Threshold low register result

7.1.10 Register 9h (offset = 9h) [reset = BFFFh]

Figure 7-20. Register 9h

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">THRESHOLD_H_EXPONENT</td><td colspan="4">THRESHOLD_H_RESULT</td></tr>
<tr><td colspan="4">R/W-Bh</td><td colspan="4">R/W-Fh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">THRESHOLD_H_RESULT</td></tr>
<tr><td colspan="8">R/W-FFh</td></tr>
</table>

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-21. Register 09 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	THRESHOLD_H_EXPONENT	R/W	Bh	Threshold high register exponent
11-0	THRESHOLD_H_RESULT	R/W	FFFh	Threshold high register result

7.1.11 Register Ah (offset = Ah) [reset = 3208h]

Figure 7-22. Register Ah

15	14	13	12	11	10	9	8
QWAKE	0	RANGE				CONVERSION_TIME	
R/W-0h	R/W-0h	R/W-Ch				R/W-2h	

7	6	5	4	3	2	1	0
CONVERSION_TIME		OPERATING_MODE		LATCH	INT_POL	FAULT_COUNT	
R/W-0h		R/W-0h		R/W-1h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-23. Register 0A Field Descriptions

Bit	Field	Type	Reset	Description
15-15	QWAKE	R/W	0h	Quick wake-up from standby in one-shot mode by not powering down all circuits. Applicable only in one-shot mode and helps get out of standby mode faster with penalty in power consumption compared to full standby mode.
14-14	0	R/W	0h	Must read or write 0
13-10	RANGE	R/W	Ch	Controls the full-scale light level range of the device. The format of this register is same as the EXPONENT register for all values from 0 to 8. For CH0 and CH1 RANGE and corresponding EXPONENT values see Section 6.4.3.
9-6	CONVERSION_TIME	R/W	8h	Controls the device conversion time 0 = 600 µs 1 = 1 ms 2 = 1.8 ms 3 = 3.4 ms 4 = 6.5 ms 5 = 12.7 ms 6 = 25 ms 7 = 50 ms 8 = 100 ms 9 = 200 ms 10 = 400 ms 11 = 800 ms
5-4	OPERATING_MODE	R/W	0h	Controls device mode of operation 0 = Power-down 1 = Forced auto-range one-shot 2 = One-shot 3 = Continuous
3-3	LATCH	R/W	1h	Controls the functionality of the interrupt reporting mechanisms for the INT pin for the threshold detection logic
2-2	INT_POL	R/W	0h	Controls the polarity or active state of the INT pin . 0 = Active low 1 = Active high
1-0	FAULT_COUNT	R/W	0h	Fault count register instructs the device as to how many consecutive fault events are required to trigger the threshold mechanisms: the flag high (FLAG_H) and the flag low (FLAG_L) registers. 0 = One fault count 1 = Two fault counts 2 = Four fault counts 3 = Eight fault counts

7.1.12 Register Bh (offset = Bh) [reset = 8011h]

Figure 7-24. Register Bh

15	14	13	12	11	10	9	8

Figure 7-24. Register Bh (continued)

1	0	0	0	0	0	0	0
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	THRESHOLD_ CH _SEL	INT_DIR	INT_CFG		0	I2C_BURST
R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-25. Register 0B Field Descriptions

Bit	Field	Type	Reset	Description
15-6	128	R/W	200h	Must read or write 128
5-5	THRESHOLD_CH_SEL	R/W	0h	Channel select for threshold logic 0 = CH0 selected 1 = CH1 selected
4-4	INT_DIR	R/W	1h	Determines the direction of the INT pin . 0 = Input 1 = Output
3-2	INT_CFG	R/W	0h	Controls the output interrupt mechanism after end of conversion 0 = SMBus alert 1 = INT pin asserted after every conversion 2 = INT pin asserted after every two conversions 3 = INT pin asserted after every 4 conversions (FIFO full)
1-1	0	R/W	0h	Must read or write 0
0-0	I2C_BURST	R/W	1h	When set, enables I^{2}C burst mode minimizing I^{2}C read cycles by auto incrementing read register pointer by 1 after every register read.

7.1.13 Register Ch (offset = Ch) [reset = 0h]

Figure 7-26. Register Ch

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	OVERLOAD_FLAG	CONVERSION_READY_FLAG	FLAG_H	FLAG_L
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-27. Register 0C Field Descriptions

Bit	Field	Type	Reset	Description
15-4	0	R/W	0h	Must read or write 0
3-3	OVERLOAD_FLAG	R	0h	Indicates when an overflow condition occurs in the data conversion process, typically because the light illuminating the device exceeds the full-scale range.
2-2	CONVERSION_READY_FLAG	R	0h	Conversion-ready flag indicates when a conversion completes. The flag is set to 1 at the end of a conversion and is cleared (set to 0) when register address 0xC is either read or written with any non-zero value. 0 = Conversion in progress 1 = Conversion is complete
1-1	FLAG_H	R	0h	Flag high register identifies that the result of a conversion is the measurement of a specified level of interest. FLAG_H is set to 1 when the result is larger than the level in the THRESHOLD_H_EXPONENT and THRESHOLD_H_RESULT registers for a consecutive number of measurements defined by the FAULT_COUNT register.
0-0	FLAG_L	R	0h	Flag low register identifies that the result of a measurement is smaller than a specified level of interest. FL is set to 1 when the result is smaller than the level in the THRESHOLD_LOW_EXPONENT and THRESHOLD_L_RESULT registers for a consecutive number of measurements defined by the FAULT_COUNT register.

7.1.14 Register 11h (offset = 11h) [reset = 121h]

Figure 7-28. Register 11h

15	14	13	12	11	10	9	8
0	0	DIDL		DIDH			
R/W-0h	R/W-0h	R-0h		R-2h			

7	6	5	4	3	2	1	0
DIDH							
R-21h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 7-29. Register 11 Field Descriptions

Bit	Field	Type	Reset	Description
15-14	0	R/W	0h	Must read or write 0
13-12	DIDL	R	0h	Device ID L
11-0	DIDH	R	221h	Device ID H

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Because ambient light sensors are used in a wide variety of applications that require precise measurement of light as perceived by the human eye, the sensors have a specialized filter that mimics the human eye. The following sections show crucial information about integrating the OPT4003-Q1 in applications.

8.2 Typical Application

8.2.1 Electrical Interface

As shown in Figure 8-1, the electrical interface is quite simple. Connect the OPT4003-Q1 I^2C SDA and SCL pins to the same pins of an applications processor, microcontroller, or other digital processor. If that digital processor requires an interrupt resulting from an event of interest from the OPT4003-Q1, then connect the INT pin to either an interrupt or general-purpose I/O pin of the processor . There are multiple uses for this INT pin, including triggering a measurement on one-shot mode, signaling the system to wake up from low-power mode, processing other tasks while waiting for an ambient light event of interest, or alerting the processor that a sample is ready to be read. Connect pullup resistors between a power supply appropriate for digital communication and the SDA and SCL pins (because the pins have open-drain output structures). If the INT pin is used, connect a pullup resistor to the INT pin. A typical value for these pullup resistors is 10 kΩ. The resistor choice can be optimized in conjunction to the bus capacitance to balance the system speed, power, noise immunity, and other requirements.

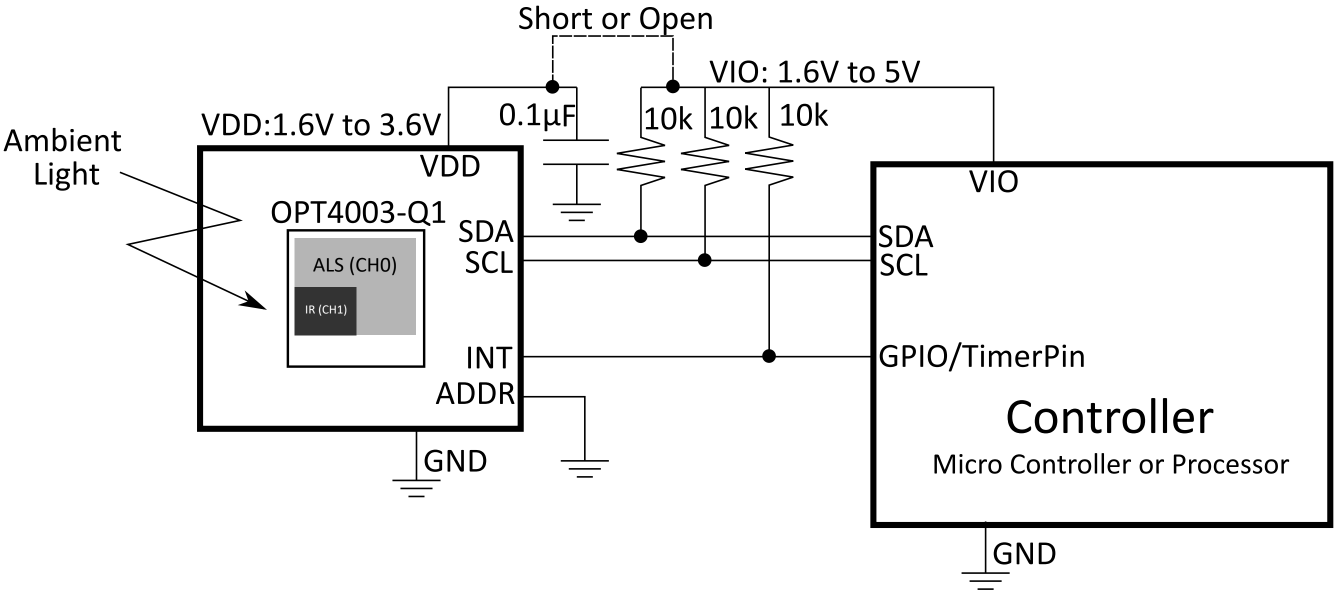


Figure 8-1. Typical Application Schematic

The power-supply and grounding considerations are discussed in the *Power Supply Recommendations* section.

Although spike suppression is integrated in the SDA and SCL pin circuits, use proper layout practices to minimize the amount of coupling into the communication lines. One possible introduction of noise occurs from capacitively coupling signal edges between the two communication lines. Another possible noise introduction comes from other switching noise sources present in the system, especially for long communication lines. In noisy environments, shield communication lines to reduce the possibility of unintended noise coupling into the digital I/O lines that can be incorrectly interpreted.

8.2.1.1 Design Requirements

This section describes the design requirements for a light sensor integrated into a system behind an enclosure cutout with a dark glass. This application is a common example of a light sensor system integration. Key considerations, such as sensor field of view (FoV) and dark glass transmission, are discussed in the *Optical Interface* section.

8.2.1.1.1 Optical Interface

Figure 8-2 shows the dimensions of the optical area.

The light gray area indicates the channel 0 photodiode and the dark gray area indicates the channel 1 photodiode.

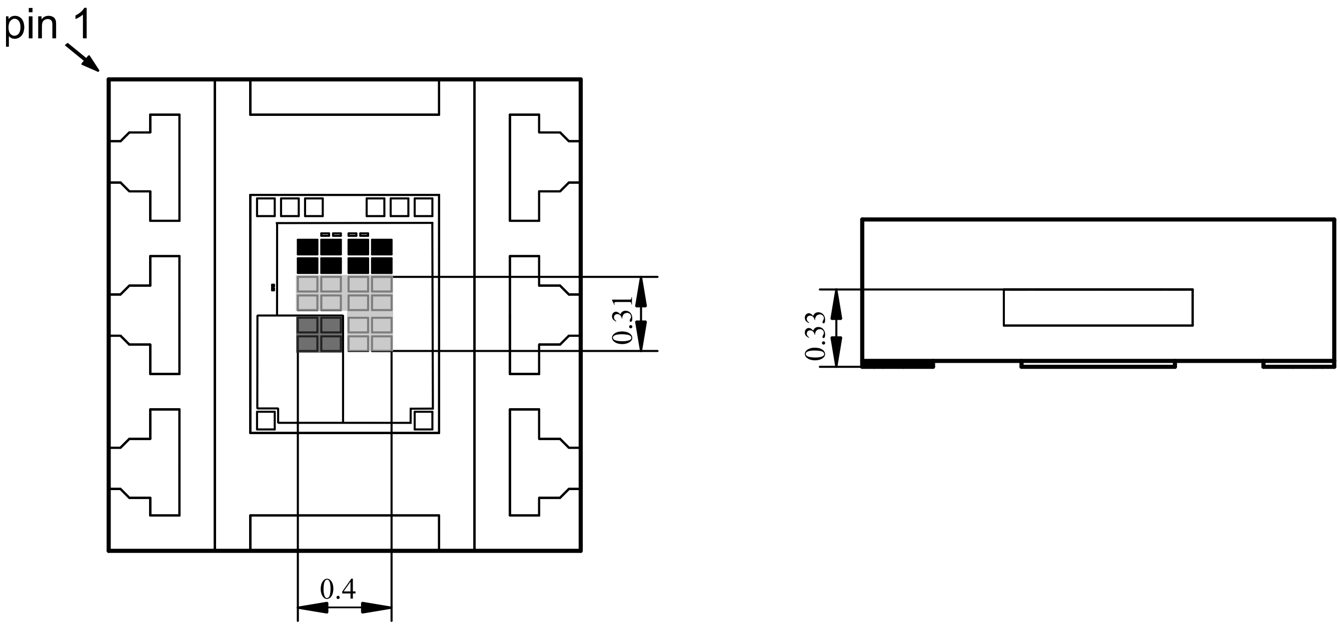


Figure 8-2. USON Sensor Position

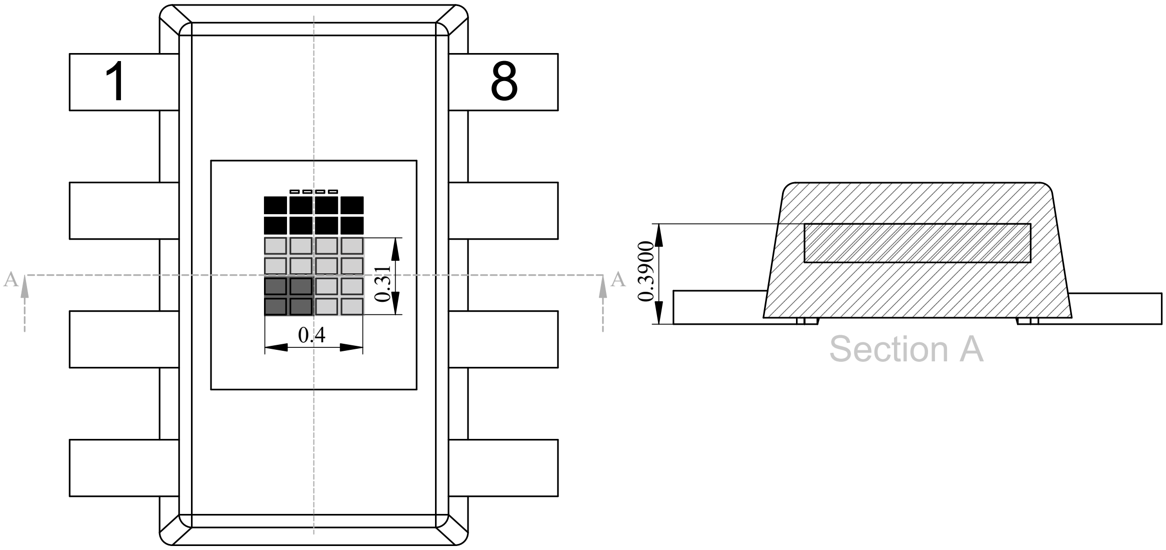


Figure 8-3. SOT-5X3 Sensor Position

Generally, any physical component that affects the light illuminating the sensing area of a light sensor also affects the performance of that light sensor. For example, a dark or opaque window can be used to further enhance the visual appeal of the design by hiding the sensor from view. This window material is typically transparent plastic or glass. Therefore, for the best performance, make sure to understand and control the effect of these components. Design a window width and height to permit light from a sufficient field of view to illuminate the sensor. For best performance, use a field of view of at least ±35°, or preferably ±45° or more. Understanding and designing the field of view is discussed further in the *Ambient Light Sensor Application Guide* application note.

The visible-spectrum transmission for dark windows typically ranges between 5% to 30%, but can be less than 1%. Specify a visible-spectrum transmission as low as, but no more than, necessary to achieve sufficient visual appeal because decreased transmission decreases the available light for the sensor to measure. The windows are made dark by either applying an ink to a transparent window material, or including a dye or other optical substance within the window material. This attenuating transmission in the visible spectrum of the window creates a ratio between the light on the outside of the design and the light that is measured by the device. To accurately measure the light outside of the design, compensate the device measurement for this ratio.

Although the inks and dyes of dark windows serve a primary purpose of being minimally transmissive to visible light, some inks and dyes can also be very transmissive to infrared light. The use of these inks and dyes further decreases the ratio of visible to infrared light, and thus decreases sensor measurement accuracy. However, because of the excellent red and infrared rejection of the device, this effect is minimized, and good results are achieved under a dark window with similar spectral responses.

For best accuracy, avoid grill-like window structures, unless the designer understands the optical effects sufficiently. These grill-like window structures create a nonuniform illumination pattern on the sensor that causes light measurement results to vary with placement tolerances and the angle of incidence of the light. If a grill-like structure is desired, then this device is an excellent sensor choice because the device is minimally sensitive to illumination uniformity issues disrupting the measurement process.

Light pipes can appear attractive for aiding in the optomechanical design that brings light to the sensor; however, do not use light pipes with any light sensor unless the system designer fully understands the ramifications of the optical physics of light pipes within the full context of the design and objectives.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Optomechanical Design (USON, SOT-5X3 Variant)

After completing the electrical design, the next task is the optomechanical design. Window sizing and placement is discussed in more rigorous detail in the *Ambient Light Sensor Application Guide*.

8.2.1.3 Application Curves

The sensor spectral matching to the human eye photopic response (see Figure 5-2 and Figure 5-3) determines the sensor capability of reporting accurate light intensity readings across lighting conditions. The sensitivity of the IR channel allows the sensor to take accurate NIR measurements, even in the presence of visible light. The bare device response over angle for both channels is illustrated in Figure 5-4 and Figure 5-5. The sensor spectral response and response over angle can be affected when the sensor is integrated at the system level. The *OPT3001: Ambient Light Sensor Application Guide* application note gives more details on integrating the light sensor and system level design considerations.

8.3 Best Design Practices

As with any optical product, take special care when handling the OPT4003-Q1. The optical surface of the device must be kept clean for the best performance, both when prototyping with the device and during mass production manufacturing procedures. Keep the optical surface clean of fingerprints, dust, and other optical-inhibiting contaminants. Use a properly-sized vacuum manipulation tool to handle the device.

If the optical surface of the device requires cleaning, then use a few gentle brushes with a soft swab of deionized water or isopropyl alcohol. Avoid potentially abrasive cleaning and manipulating tools and excessive force that can scratch the optical surface.

If the OPT4003-Q1 performance is diminished in any way, then inspect the optical surface for dirt, scratches, or other optical artifacts.

8.4 Power Supply Recommendations

Although the OPT4003-Q1 has low sensitivity to power-supply issues, good practices are always recommended. For best performance, the device VDD pin must have a stable, low-noise power supply with a 100-nF bypass capacitor close to the device and solid grounding. There are many options for powering the device because of the device low current consumption levels.

8.5 Layout

8.5.1 Layout Guidelines

TI highly recommends placing the decoupling capacitor close to the device, but remember that optically reflective surfaces of components also affect the performance of the design. Consider the three-dimensional geometry of all components and structures around the sensor to prevent unexpected results from secondary optical reflections. Placing capacitors and components at a distance of at least twice the height of the component is typically sufficient. The best optical layout is to place all close components on the opposite side of the PCB from the OPT4003-Q1. However, this approach is not practical for the constraints of every design.

The device layout is also critical for good SMT assembly. Two types of land pattern pads can be used for this package: solder mask defined pads (SMD) and non-solder mask defined pads (NSMD). SMD pads have a solder mask opening that is smaller than the metal pads, whereas, NSMD has a solder mask opening that is larger than the metal pad. Figure 8-4 illustrates these types of landing-pattern pads. SMD pads are preferred because these pads provide a more accurate soldering-pad dimension with the trace connections. For further discussion of SMT and PCB recommendations, see the *Soldering and Handling Recommendations (USON, SOT-5X3 Variant)* section.

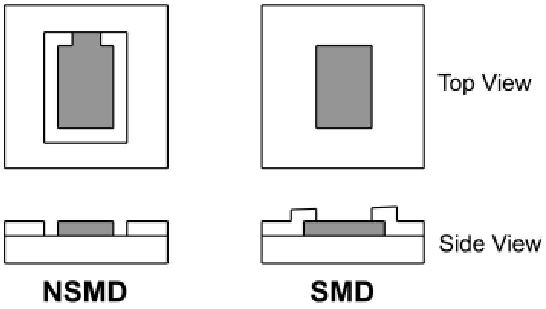


Figure 8-4. Solder Mask Defined Pad (SMD) and Non-Solder Mask Defined Pad (NSMD)

8.5.1.1 Soldering and Handling Recommendations (USON, SOT-5X3 Variant)

The OPT4003-Q1 is qualified for three soldering reflow operations as per JEDEC JSTD-020.

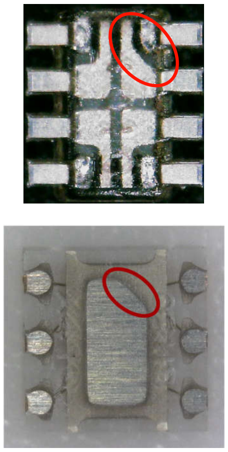
Note

Excessive heat can discolor the device and affect optical performance.

See the *QFN and SON PCB Attachment* application note for details on the soldering thermal profile and other information. Discard the device and do not reattach if the OPT4003-Q1 must be removed from a PCB.

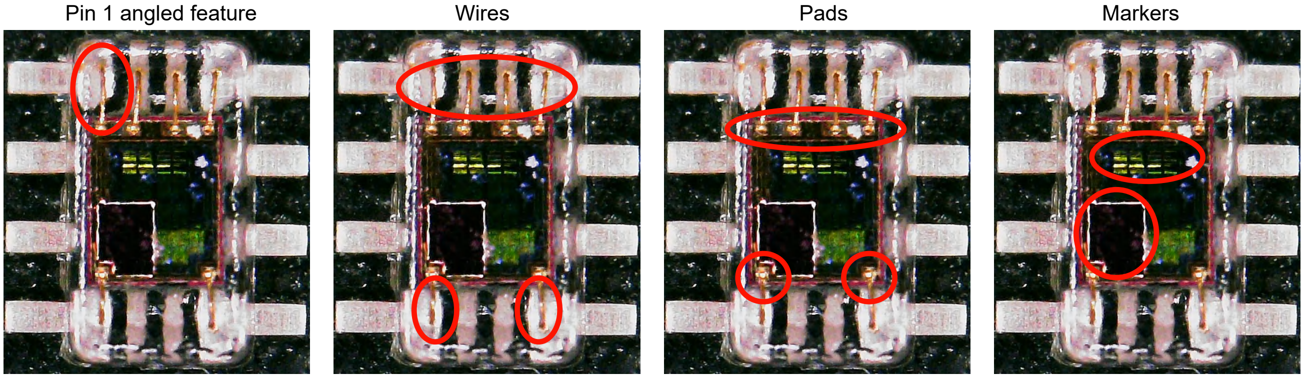
As with most optical devices, take special care to make sure that optical surfaces of the device stay clean and free from damage. See *Section 8.3* for more detailed recommendations. For best optical performance, solder flux and any other possible debris must be cleaned after the soldering processes.

Figure 8-5 shows how to identify pin 1 on the bottom side of the package. Figure 8-7 shows various identification features for pin 1 on the top side of the package.



NOTE: The bottom side of the device features an angled feature to denote pin 1.

Figure 8-5. Identification Feature for Pin 1



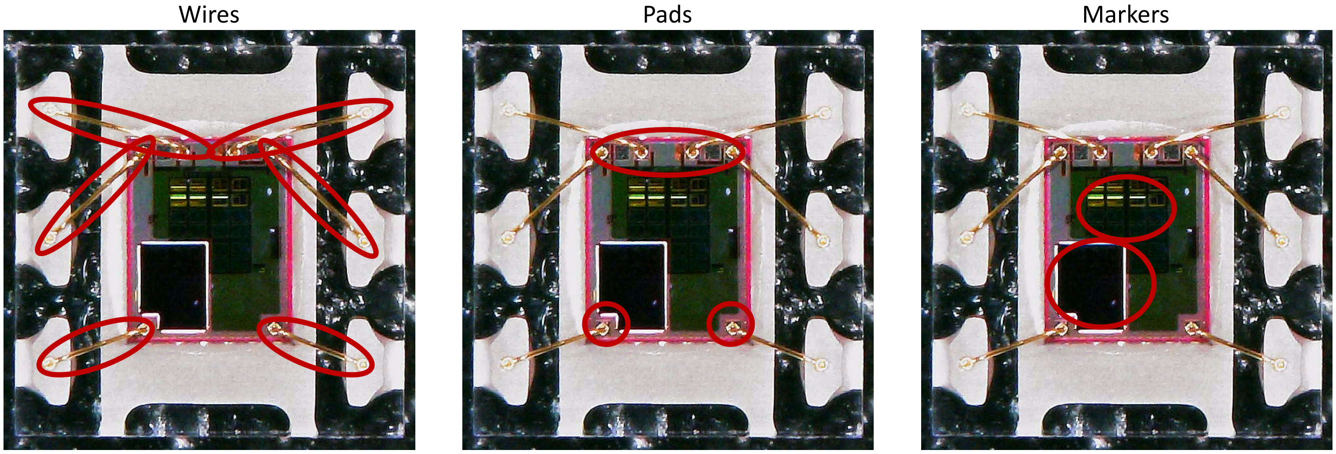
Pin 1 angled feature

Wires

Pads

Markers

Figure 8-6. Pin 1 Identification Features for SOT-5X3 Package



Wires

Pads

Markers

Figure 8-7. Pin 1 Identification Features for USON Package

8.5.2 Layout Example

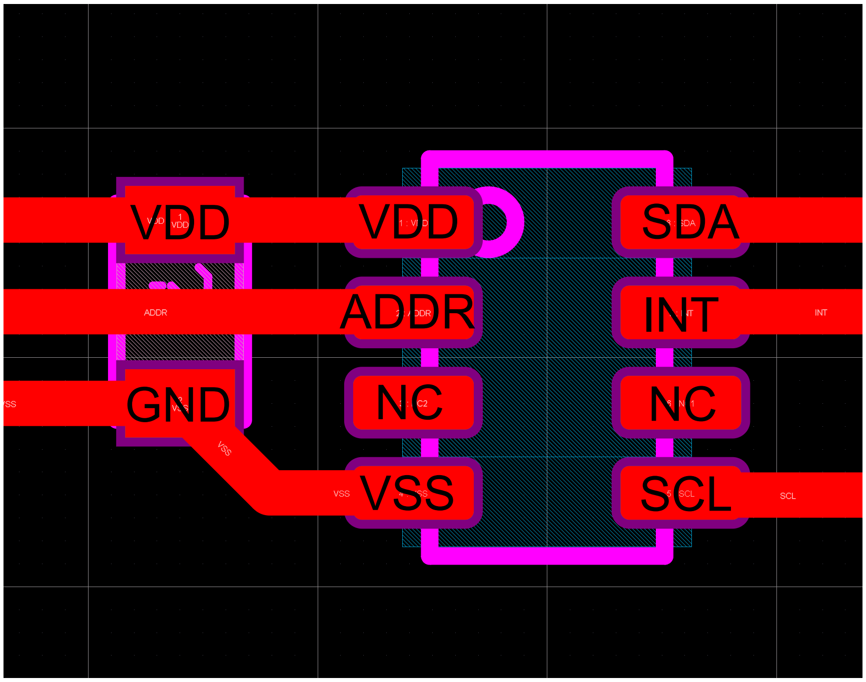


Figure 8-8. Layout Example for DTS Package

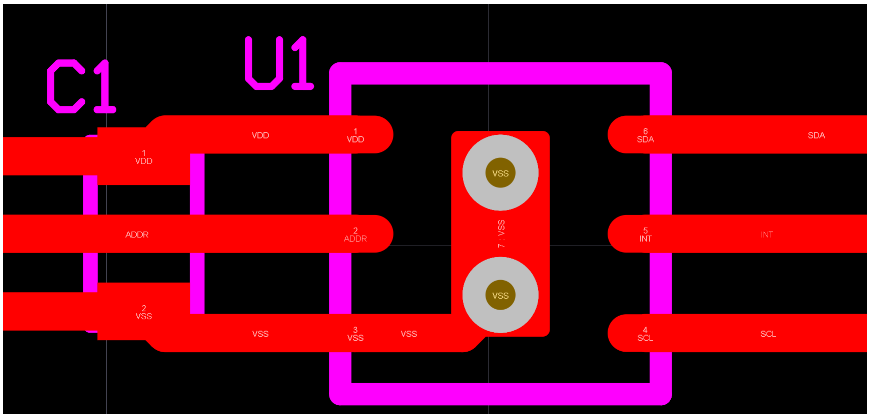


Figure 8-9. Layout Example for DNP Package

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Ambient Light Sensor Application Guide*, application note
- Texas Instruments, *Light Sensor Evaluation Module User's Guide*, user's guide
- Texas Instruments, *QFN and SON PCB Attachment*, application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2024) to Revision C (January 2025) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 2
- Added SOT-5X3 package.. 4
- Changed peak irradiance spectral responsivity of CH0 from 550nm to 560nm and CH1 from from 810nm to 800nm for the USON package.. 5
- Changed CH0 peak responsivity from 1280 codes per $\mu W/cm^2$ to 12800 codes per $\mu W/cm^2$ for the USON package.. 5
- Added CH1 measurement output result for the USON package.. 5
- Added range selection settings for SOT-5X3 package.. 18
- Added *Resolution Table* for the SOT-5X3 package.. 23
- Added SOT-5X3 sensor position... 40
- Added SOT-5X3 package placement view.. 42
- Added layout examples for SOT-5X3 package... 45

Changes from Revision A (December 2023) to Revision B (December 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	2

Changes from Revision * (August 2023) to Revision A (December 2023)	Page
• Changed document status from *Advance Information* to *Production Data*	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPT4003DNPRQ1	ACTIVE	USON	DNP	6	3000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 105	3Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

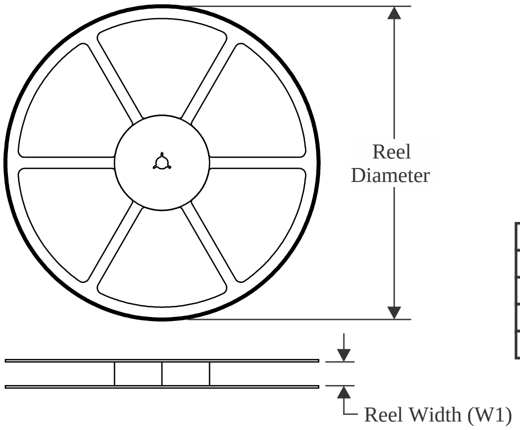
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

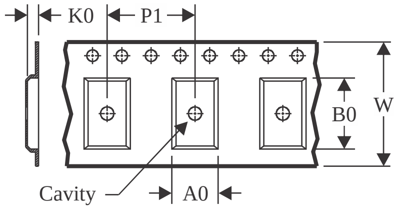
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

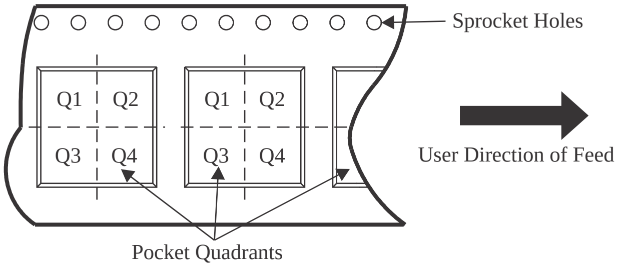


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

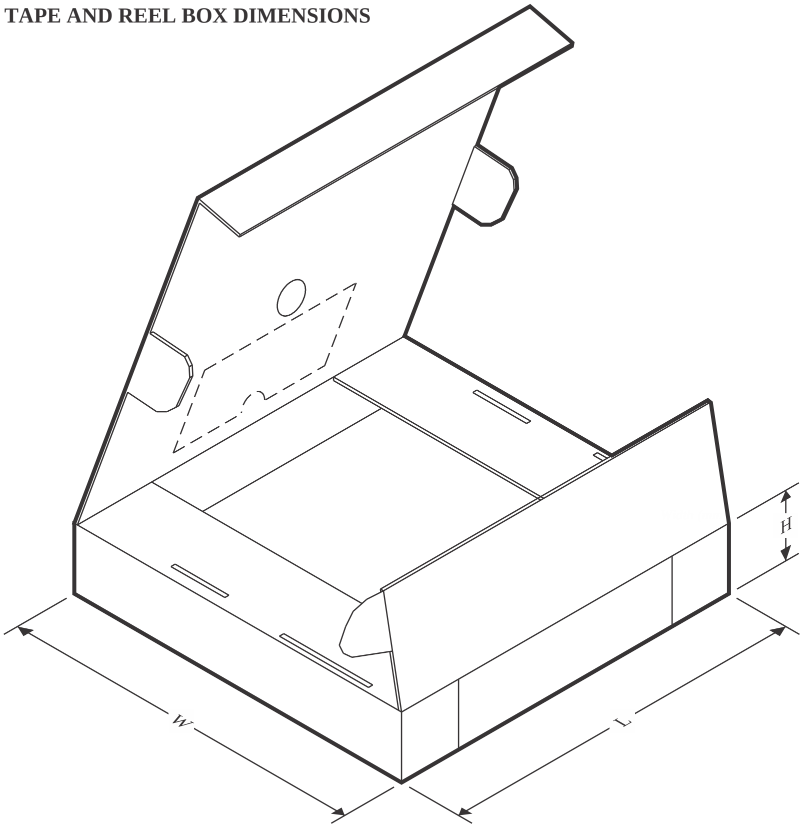
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

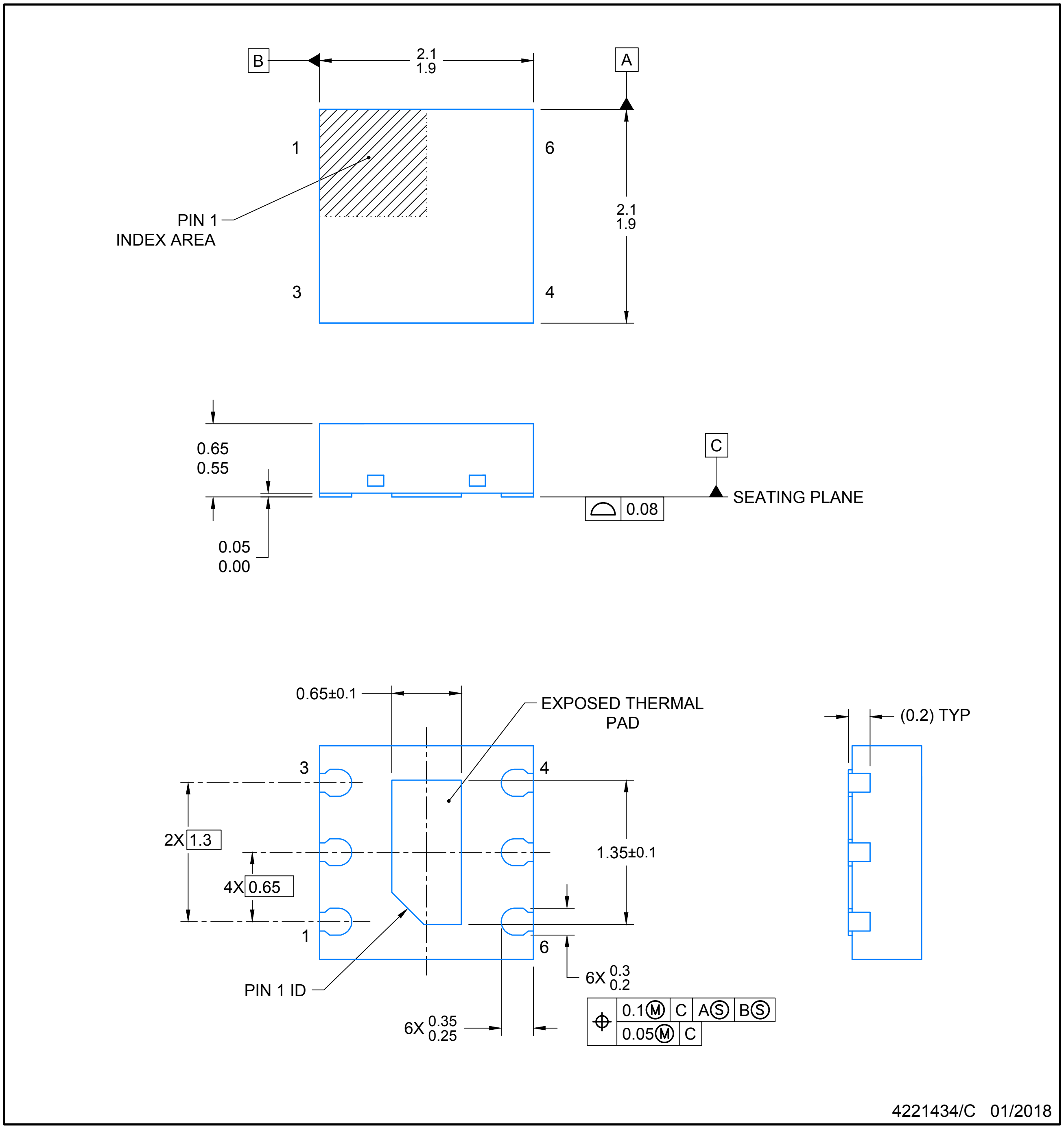
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPT4003DNPRQ1	USON	DNP	6	3000	330.0	12.4	2.3	2.3	0.9	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPT4003DNPRQ1	USON	DNP	6	3000	356.0	338.0	48.0



4221434/C 01/2018

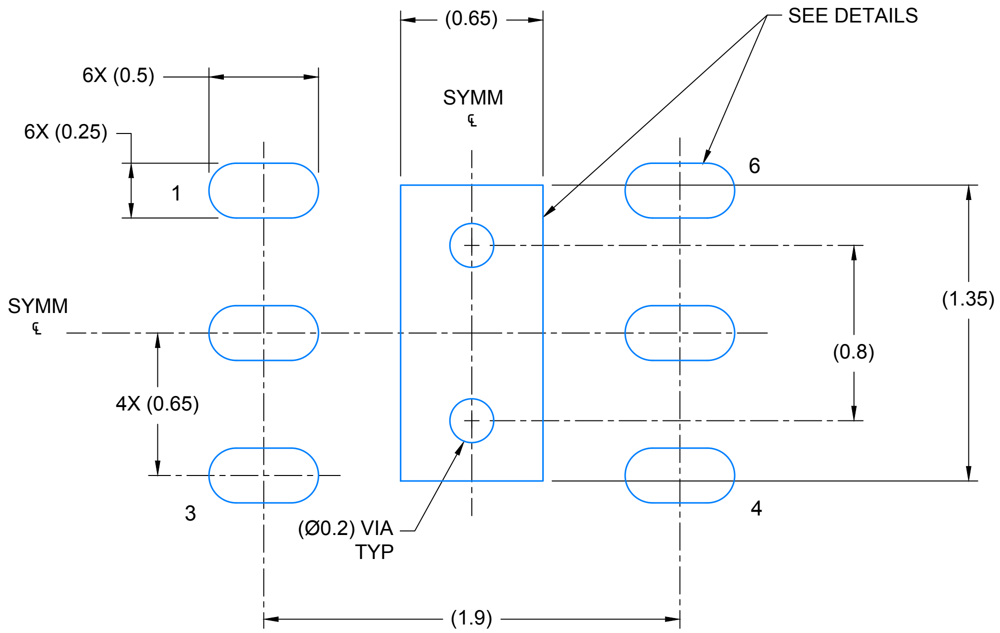
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Optical package with clear mold compound.

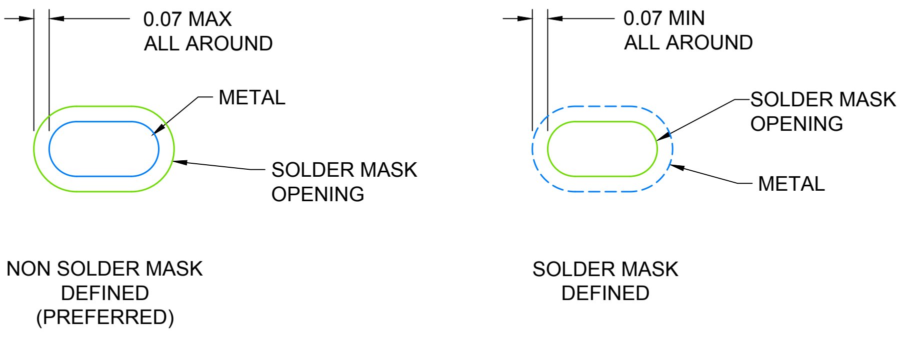
EXAMPLE BOARD LAYOUT

USON - 0.65 mm mm max height

PLASTIC SMALL OUTLINE NO-LEAD



LAND PATTERN EXAMPLE
SCALE: 30X

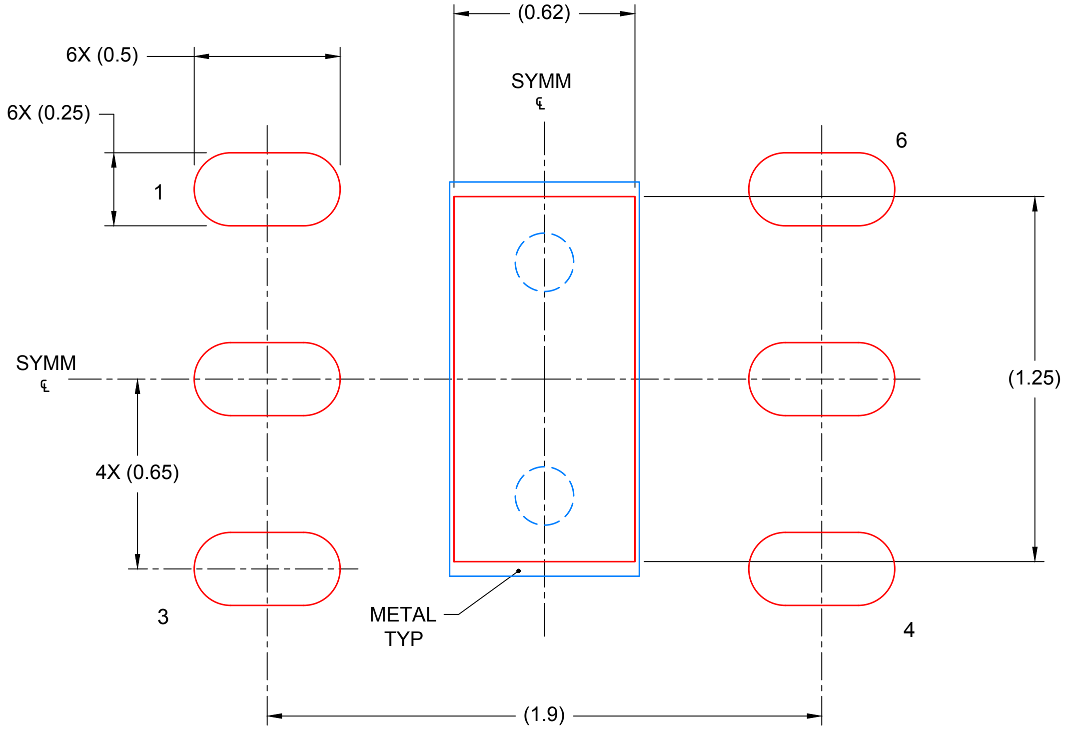


SOLDER MASK DETAILS

4221434/C 01/2018

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .



SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 40X

4221434/C 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated