PCA9545A Low Voltage 4-channel I²C and SMBus Switch With Interrupt Logic and Reset Functions

1 Features
- 1-of-4 Bidirectional Translating Switches
- I²C Bus and SMBus Compatible
- Four Active-Low Interrupt Inputs
- Active-Low Interrupt Output
- Active-Low Reset Input
- Two Address Terminals, Allowing up to Four Devices on the I²C Bus
- Channel Selection via I²C Bus, in Any Combination
- Power-Up With All Switch Channels Deselected
- Low $R_{ON}$ Switches
- Allows Voltage-Level Translation Between 1.8-V, 2.5-V, 3.3-V, and 5-V Buses
- No Glitch on Power-Up
- Supports Hot Insertion
- Low Standby Current
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5.5 V Tolerant Inputs
- 0 to 400-kHz Clock Frequency
- Latch-Up Performance Exceeds 100 mA per JESD 78
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications
- Servers
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products With I²C Slave Address Conflicts (e.g. Multiple, Identical Temp Sensors)

3 Description
The PCA9545A is a quad bidirectional translating switch controlled via the I²C bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register. Four interrupt inputs (INT3–INT0), one for each of the downstream pairs, are provided. One interrupt (INT) output acts as an AND of the four interrupt inputs.

An active-low reset (RESET) input allows the PCA9545A to recover from a situation in which one of the downstream I²C buses is stuck in a low state. Pulling RESET low resets the I²C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the VCC terminal can be used to limit the maximum high voltage, which will be passed by the PCA9545A. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5 V tolerant.

4 Simplified Application Diagram

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1 For all available packages, see the orderable addendum at the end of the data sheet.
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## 5 Revision History

Changes from Revision October 2006 (C) to Revision D Page

- Added **RESET Errata** section ...................................... 12
- Added **Power-On Reset Errata** section ......................... 20
## Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>DGV, DW, PW, AND RGY</th>
<th>RGW</th>
<th>RGY (TOP VIEW)</th>
<th>GQN OR ZQN PACKAGE (TOP VIEW)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>1</td>
<td>19</td>
<td>A2</td>
<td></td>
<td></td>
<td>Address input 0. Connect directly to VCC or ground.</td>
</tr>
<tr>
<td>A1</td>
<td>2</td>
<td>20</td>
<td>A1</td>
<td></td>
<td></td>
<td>Address input 1. Connect directly to VCC or ground.</td>
</tr>
<tr>
<td>RESET</td>
<td>3</td>
<td>1</td>
<td>B3</td>
<td></td>
<td></td>
<td>Active-low reset input. Connect to VDPUM through a pull-up resistor, if not used.</td>
</tr>
<tr>
<td>INT0</td>
<td>4</td>
<td>2</td>
<td>B1</td>
<td></td>
<td></td>
<td>Active-low interrupt input 0. Connect to VDPU0 through a pull-up resistor.</td>
</tr>
<tr>
<td>SD0</td>
<td>5</td>
<td>3</td>
<td>C2</td>
<td></td>
<td></td>
<td>Serial data 0. Connect to VDPU0 through a pull-up resistor.</td>
</tr>
<tr>
<td>SC0</td>
<td>6</td>
<td>4</td>
<td>C1</td>
<td></td>
<td></td>
<td>Serial clock 0. Connect to VDPU0 through a pull-up resistor.</td>
</tr>
<tr>
<td>INT1</td>
<td>7</td>
<td>5</td>
<td>D3</td>
<td></td>
<td></td>
<td>Active-low interrupt input 1. Connect to VDPU1 through a pull-up resistor.</td>
</tr>
<tr>
<td>SD1</td>
<td>8</td>
<td>6</td>
<td>D1</td>
<td></td>
<td></td>
<td>Serial data 1. Connect to VDPU1 through a pull-up resistor.</td>
</tr>
<tr>
<td>SC1</td>
<td>9</td>
<td>7</td>
<td>E2</td>
<td></td>
<td></td>
<td>Serial clock 1. Connect to VDPU1 through a pull-up resistor.</td>
</tr>
<tr>
<td>GND</td>
<td>10</td>
<td>8</td>
<td>E1</td>
<td></td>
<td></td>
<td>Ground</td>
</tr>
<tr>
<td>INT2</td>
<td>11</td>
<td>9</td>
<td>E3</td>
<td></td>
<td></td>
<td>Active-low interrupt input 2. Connect to VDPU2 through a pull-up resistor.</td>
</tr>
<tr>
<td>SD2</td>
<td>12</td>
<td>10</td>
<td>E4</td>
<td></td>
<td></td>
<td>Serial data 2. Connect to VDPU2 through a pull-up resistor.</td>
</tr>
<tr>
<td>SC2</td>
<td>13</td>
<td>11</td>
<td>D2</td>
<td></td>
<td></td>
<td>Serial clock 2. Connect to VDPU2 through a pull-up resistor.</td>
</tr>
<tr>
<td>INT3</td>
<td>14</td>
<td>12</td>
<td>D4</td>
<td></td>
<td></td>
<td>Active-low interrupt input 3. Connect to VDPU3 through a pull-up resistor.</td>
</tr>
<tr>
<td>SD3</td>
<td>15</td>
<td>13</td>
<td>C3</td>
<td></td>
<td></td>
<td>Serial data 3. Connect to VDPU3 through a pull-up resistor.</td>
</tr>
<tr>
<td>SC3</td>
<td>16</td>
<td>14</td>
<td>C4</td>
<td></td>
<td></td>
<td>Serial clock 3. Connect to VDPU3 through a pull-up resistor.</td>
</tr>
<tr>
<td>INT</td>
<td>17</td>
<td>15</td>
<td>B2</td>
<td></td>
<td></td>
<td>Active-low interrupt output. Connect to VDPUM through a pull-up resistor.</td>
</tr>
<tr>
<td>SCL</td>
<td>18</td>
<td>16</td>
<td>B4</td>
<td></td>
<td></td>
<td>Serial clock line. Connect to VDPUM through a pull-up resistor.</td>
</tr>
<tr>
<td>SDA</td>
<td>19</td>
<td>17</td>
<td>A4</td>
<td></td>
<td></td>
<td>Serial data line. Connect to VDPUM through a pull-up resistor.</td>
</tr>
<tr>
<td>VCC</td>
<td>20</td>
<td>18</td>
<td>A3</td>
<td></td>
<td></td>
<td>Supply power</td>
</tr>
</tbody>
</table>

(1) VDPUX is the pull-up reference voltage for the associated data line. VDPUM is the master I2C reference voltage while VDPUX-VDPUS are the slave channel reference voltages.
7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$ Supply voltage range</td>
<td>−0.5</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>$V_I$ Input voltage range(2)</td>
<td>−0.5</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>$I_I$ Input current</td>
<td>±20</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_O$ Output current</td>
<td>±25</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Continuous current through $V_{CC}$</td>
<td>±100</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Continuous current through GND</td>
<td>±100</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$\theta_JA$ Package thermal impedance(3)</td>
<td>92</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>DGV package</td>
<td>58</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DW package</td>
<td>78</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GQN/ZQN package</td>
<td>83</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PW package</td>
<td>TBD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RGW package</td>
<td>47</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RGW package</td>
<td>TBD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P_{tot}$ Total power dissipation</td>
<td>400</td>
<td>mW</td>
<td></td>
</tr>
<tr>
<td>$T_A$ Operating free-air temperature range</td>
<td>−40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

7.2 Handling Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{stg}$ Storage temperature range</td>
<td>−65</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>$V_{(ESD)}$ Electrostatic discharge</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)</td>
<td>0</td>
<td>2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)</td>
<td>0</td>
<td>1000</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$ Supply voltage</td>
<td>2.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$ High-level input voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCL, SDA</td>
<td>0.7 × $V_{CC}$</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>A1, A0, INT3–INT0, RESET</td>
<td>0.7 × $V_{CC}$</td>
<td>$V_{CC}$ + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$ Low-level input voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCL, SDA</td>
<td>−0.5</td>
<td>0.3 × $V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>A1, A0, INT3–INT0, RESET</td>
<td>−0.5</td>
<td>0.3 × $V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>$T_A$ Operating free-air temperature</td>
<td>−40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, Literature number SCBA004.
### 7.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>$V_{POR}$</th>
<th>$I_{O,\text{INT}}$</th>
<th>$I_{OL}$</th>
<th>$I_{CC}$</th>
<th>$\Delta I_{CC}$</th>
<th>$C_{i,\text{ON(OFF)}}$</th>
<th>$R_{ON}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{POR}$</td>
<td>Power-on reset voltage$^{(2)}$</td>
<td>No load, $V_{I} = V_{CC}$ or $GND$</td>
<td>$5 , V$</td>
<td>3.6</td>
<td>$100 \mu A$</td>
<td>$3 , \text{mA}$</td>
<td>$3 , \mu A$</td>
<td>$12 , \mu A$</td>
<td>$6 , \mu F$</td>
<td>$45 , \Omega$</td>
</tr>
<tr>
<td>$V_{\text{pass}}$</td>
<td>Switch output voltage</td>
<td>$V_{SW_{in}} = V_{CC}$, $I_{SW_{out}} = -100 \mu A$</td>
<td>$4.5 , \text{V}$ to $5.5 , \text{V}$</td>
<td>2.6</td>
<td>4.5</td>
<td>$3 , \text{V}$</td>
<td>1.6</td>
<td>2.8</td>
<td>$2.5 , \text{V}$</td>
<td>$1.5 , \text{mA}$</td>
</tr>
</tbody>
</table>

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V $V_{CC}$), $T_{A} = 25^\circ C$.
(2) The power-on reset circuit resets the I$^2$C bus logic with $V_{CC} < V_{POR}$. $V_{CC}$ must be lowered to 0.2 V to reset the device.
(3) $C_{i\,\text{ON(OFF)}}$ depends on the device capacitance and load that is downstream from the device.
## 7.5 \text{i}^{2}\text{C} Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

<table>
<thead>
<tr>
<th></th>
<th>STANDARD MODE</th>
<th>FAST MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>I^{2}C BUS</td>
<td>I^{2}C BUS</td>
</tr>
<tr>
<td><strong>f_{scl}</strong> I^{2}C clock frequency</td>
<td>MIN 100 kHz</td>
<td>MIN 0 kHz</td>
</tr>
<tr>
<td><strong>t_{sch}</strong> I^{2}C clock high time</td>
<td>4 μs</td>
<td>0.6 μs</td>
</tr>
<tr>
<td><strong>t_{scl}</strong> I^{2}C clock low time</td>
<td>4.7 μs</td>
<td>1.3 μs</td>
</tr>
<tr>
<td><strong>t_{sp}</strong> I^{2}C spike time</td>
<td>50 μs</td>
<td>50 μs</td>
</tr>
<tr>
<td><strong>t_{sds}</strong> I^{2}C serial-data setup time</td>
<td>250 ns</td>
<td>100 ns</td>
</tr>
<tr>
<td><strong>t_{sth}</strong> I^{2}C serial-data hold time</td>
<td>0(1) μs</td>
<td>0(1) μs</td>
</tr>
<tr>
<td><strong>t_{ir}</strong> I^{2}C input rise time</td>
<td>1000 ns</td>
<td>20 + 0.1C_{b}(2) 300 ns</td>
</tr>
<tr>
<td><strong>t_{idf}</strong> I^{2}C input fall time</td>
<td>300 ns</td>
<td>20 + 0.1C_{b}(2) 300 ns</td>
</tr>
<tr>
<td><strong>t_{ocf}</strong> I^{2}C output fall time</td>
<td>300 ns 10-pF to 400-pF bus</td>
<td>20 + 0.1C_{b}(2) 300 ns</td>
</tr>
<tr>
<td><strong>t_{buf}</strong> I^{2}C bus free time between stop and start</td>
<td>4.7 μs</td>
<td>1.3 μs</td>
</tr>
<tr>
<td><strong>t_{stb}</strong> I^{2}C start or repeated start condition setup</td>
<td>4.7 μs</td>
<td>0.6 μs</td>
</tr>
<tr>
<td><strong>t_{sth}</strong> I^{2}C start or repeated start condition hold</td>
<td>4 μs</td>
<td>0.6 μs</td>
</tr>
<tr>
<td><strong>t_{eos}</strong> I^{2}C stop condition setup</td>
<td>4 μs</td>
<td>0.6 μs</td>
</tr>
<tr>
<td><strong>t_{vdL(Data)}</strong> Valid-data time (high to low)(3)</td>
<td>SCL low to SDA output low valid</td>
<td>1 μs</td>
</tr>
<tr>
<td><strong>t_{vdH(Data)}</strong> Valid-data time (low to high)(3)</td>
<td>SCL low to SDA output high valid</td>
<td>0.6 μs</td>
</tr>
<tr>
<td><strong>t_{vd(ack)}</strong> Valid-data time of ACK condition</td>
<td>ACK signal from SCL low to SDA output low</td>
<td>1 μs</td>
</tr>
<tr>
<td><strong>C_{b}</strong> I^{2}C bus capacitive load</td>
<td>400 pF</td>
<td>400 pF</td>
</tr>
</tbody>
</table>

(1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the \text{V}_{IH}\text{ min} of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.

(2) \text{C}_{b} = \text{total bus capacitance of one bus line in pF}

(3) Data taken using a 1-kΩ pull-up resistor and 50-pF load (see Figure 1)
## 7.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100 \text{ pF}$ (unless otherwise noted) (see Figure 3)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{pd}$ (1)</td>
<td>Propagation delay time</td>
<td>$R_{ON} = 20 \Omega$, $C_L = 15 \text{ pF}$</td>
<td>SDA or SCL</td>
<td>SDn or SCn</td>
<td>0.3</td>
</tr>
<tr>
<td></td>
<td>$R_{ON} = 20 \Omega$, $C_L = 50 \text{ pF}$</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>$t_{iv}$</td>
<td>Interrupt valid time (2)</td>
<td>INTn</td>
<td>INT</td>
<td>4</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_{ir}$</td>
<td>Interrupt reset delay time (2)</td>
<td>INTn</td>
<td>INT</td>
<td>2</td>
<td>$\mu$s</td>
</tr>
</tbody>
</table>

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).  
(2) Data taken using a 4.7-k$\Omega$ pull-up resistor and 100-pF load (see Figure 3)

## 7.7 Interrupt and Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PWRL}$</td>
<td>Low-level pulse duration rejection of INTn inputs</td>
<td>1</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_{PWRRH}$</td>
<td>High-level pulse duration rejection of INTn inputs</td>
<td>0.5</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_{WL}$</td>
<td>Pulse duration, RESET low</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{rst}$ (1)</td>
<td>RESET time (SDA clear)</td>
<td>500</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{REC(STA)}$</td>
<td>Recovery time from RESET to start</td>
<td>0</td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) $t_{rst}$ is the propagation delay measured from the time the RESET pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of $t_{WL}$.
8 Parameter Measurement Information

VOLTAGE WAVEFORMS

A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10$ MHz, $Z_O = 50$ $\Omega$, $t_{r/f} = 30$ ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 1. $I^2C$ Interface Load Circuit, Byte Descriptions, and Voltage Waveforms
Parameter Measurement Information (continued)

\[
\begin{align*}
\text{SCL} & \quad \text{Start} \quad \text{ACK or Read Cycle} \\
\text{SDA} & \quad \text{VCC} \\
\text{RESET} & \quad t_{\text{REC}} \\
\end{align*}
\]

\[
\begin{align*}
R_L = 4.7 \text{ k}\Omega \\
V_{\text{CC}} \\
C_L = 100 \text{ pF} \\
(\text{See Note A})
\end{align*}
\]

\section*{Interrupt Load Configuration}

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{reset_timing.png}
\caption{Reset Timing}
\end{figure}

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{interrupt_load_circuit.png}
\caption{Interrupt Load Circuit and Voltage Waveforms}
\end{figure}

A. \( C_L \) includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR \( \leq 10 \text{ MHz} \), \( Z_O = 50 \Omega \), \( t_r/t_l = 30 \text{ ns} \).
9 Detailed Description

9.1 Overview

The PCA9545A is a 4-channel, bidirectional translating \( \text{I}^2\text{C} \) switch. The master SCL/SDA signal pair is directed to four channels of slave devices, SC0/SD0-SC3/SD3. Any individual downstream channel can be selected as well as any combination of the four channels. The PCA9545A also supports interrupt signals in order for the master to detect an interrupt on the INT output terminal that can result from any of the slave devices connected to the INT3-INT0 input terminals.

The device offers an active-low RESET input which resets the state machine and allows the PCA9545A to recover should one of the downstream \( \text{I}^2\text{C} \) buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, \( V_{\text{CC}} \), also known as a power-on reset (POR). Both the RESET function and a POR will cause all channels to be deselected.

The connections of the \( \text{I}^2\text{C} \) data path are controlled by the same \( \text{I}^2\text{C} \) master device that is switched to communicate with multiple \( \text{I}^2\text{C} \) slaves. After the successful acknowledgment of the slave address (hardware selectable by A0 and A1 terminals), a single 8-bit control register is written to or read from to determine the selected channels and state of the interrupts.

The PCA9545A may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.
9.2 Functional Block Diagram

Pin numbers shown are for DGV, DW, PW, and RGY packages.
9.3 Feature Description
The PCA9545A is a 4-channel, bidirectional translating switch for I²C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The PCA9545A features I²C control using a single 8-bit control register in which the four least significant bits control the enabling and disabling of the 4 switch channels of I²C data flow. The PCA9545A also supports interrupt signals for each slave channel and this data is held in the four most significant bits of the control register. Depending on the application, voltage translation of the I²C bus can also be achieved using the PCA9545A to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I²C bus enters a fault state, the PCA9545A can be reset to resume normal operation using the RESET pin feature or by a power-on reset which results from cycling power to the device.

9.4 Device Functional Modes

9.4.1 RESET Input
The RESET input can be used to recover the PCA9545A from a bus-fault condition. The registers and the I²C state machine within this device initialize to their default states if this signal is asserted low for a minimum of tWL. All channels also are deselected in this case. RESET must be connected to VCC through a pull-up resistor.

9.4.1.1 RESET Errata
If RESET voltage set higher than VCC, current will flow from RESET pin to VCC pin.

System Impact
VCC will be pulled above its regular voltage level

System Workaround
Design such that RESET voltage is same or lower than VCC

9.4.2 Power-On Reset
When power is applied to VCC, an internal power-on reset holds the PCA9545A in a reset condition until VCC has reached VPORR. At this point, the reset condition is released and the PCA9545A registers and I²C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, VCC must be lowered below at least VPORF to reset the device.

Refer to the Power-On Reset Errata section.

9.5 Programming

9.5.1 I²C Interface
The I²C bus is for two-way two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer can be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse, as changes in the data line at this time are interpreted as control signals (see Figure 4).
Programming (continued)

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 5).

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master, and the devices that are controlled by the master are the slaves (see Figure 6).

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 7). Setup and hold times must be taken into account.
A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

Data is transmitted to the PCA9545A control register using the write mode shown in Figure 8.

Data is read from the PCA9545A control register using the read mode shown in Figure 9.
9.6 Control Register

9.6.1 Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the PCA9545A is shown in Figure 10. To conserve power, no internal pull-up resistors are incorporated on the hardware-selectable address terminals, and they must be pulled high or low.

![Figure 10. PCA9545A Address](image)

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

9.6.2 Control Register Description

Following the successful acknowledgment of the slave address, the bus master sends a byte to the PCA9545A, which is stored in the control register (see Figure 11). If multiple bytes are received by the PCA9545A, it saves the last byte received. This register can be written and read via the I²C bus.

![Figure 11. Control Register](image)

9.6.3 Control Register Definition

One or several SCn/SDn downstream pairs, or channels, are selected by the contents of the control register (see Table 1). After the PCA9545A has been addressed, the control register is written. The four LSBs of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I²C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition must occur always right after the acknowledge cycle.
Control Register (continued)

Table 1. Control Register Write (Channel Selection), Control Register Read (Channel Status)\(^{(1)}\)

<table>
<thead>
<tr>
<th>INT3</th>
<th>INT2</th>
<th>INT1</th>
<th>INT0</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
<th>COMMAND</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>Channel 0 disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Channel 0 enabled</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>Channel 1 disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Channel 1 enabled</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>Channel 2 disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Channel 2 enabled</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>Channel 3 disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Channel 3 enabled</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>No channel selected, (\text{power-up/reset default state})</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Several channels can be enabled at the same time. For example, B3 = 0, B2 = 1, B1 = 1, B0 = 0 means that channels 0 and 3 are disabled, and channels 1 are 2 and enabled. Care should be taken not to exceed the maximum bus capacity.

9.6.4 Interrupt Handling

The PCA9545A provides four interrupt inputs (one for each channel) and one open-drain interrupt output (see Table 2). When an interrupt is generated by any device, it is detected by the PCA9545A and the interrupt output is driven low. The channel does not need to be active for detection of the interrupt. A bit also is set in the control register.

Bits 4–7 of the control register correspond to channels 0–3 of the PCA9545A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master then can address the PCA9545A and read the contents of the control register to determine which channel contains the device generating the interrupt. The master then can reconfigure the PCA9545A to select this channel and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs can be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to \(V_{\text{CC}}\).

Table 2. Control Register Read (Interrupt)\(^{(1)}\)

<table>
<thead>
<tr>
<th>INT3</th>
<th>INT2</th>
<th>INT1</th>
<th>INT0</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
<th>COMMAND</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>No interrupt on channel 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Interrupt on channel 0</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>No interrupt on channel 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Interrupt on channel 1</td>
</tr>
<tr>
<td>X</td>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>No interrupt on channel 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Interrupt on channel 2</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>No interrupt on channel 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Interrupt on channel 3</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Several interrupts can be active at the same time. For example, INT3 = 0, INT2 = 1, INT1 = 1, INT0 = 0 means that there is no interrupt on channels 0 and 3, and there is interrupt on channels 1 and 2.
10 Application and Implementation

10.1 Application Information

Applications of the PCA9545A will contain an \( \text{I}^2\text{C} \) (or SMBus) master device and up to four \( \text{I}^2\text{C} \) slave devices. The downstream channels are ideally used to resolve \( \text{I}^2\text{C} \) slave address conflicts. For example, if four identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0, 1, 2, and 3. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the \( \text{I}^2\text{C} \) master can move on and read the next channel.

In an application where the \( \text{I}^2\text{C} \) bus will contain many additional slave devices that do not result in \( \text{I}^2\text{C} \) slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches will be enabled simultaneously, additional design requirements must be considered (See Design Requirements and Detailed Design Procedure).

10.2 Typical Application

A typical application of the PCA9545A will contain anywhere from 1 to 5 separate data pull-up voltages, \( \text{V}_{\text{DPU}} \), one for the master device (\( \text{V}_{\text{DPUM}} \)) and one for each of the selectable slave channels (\( \text{V}_{\text{DPU0}} \)–\( \text{V}_{\text{DPU3}} \)). In the event where the master device and all slave devices operate at the same voltage, then the pass voltage, \( \text{V}_{\text{PASS}} = \text{V}_{\text{DPU}} \). Once the maximum \( \text{V}_{\text{PASS}} \) is known, \( \text{V}_{\text{CC}} \) can be selected easily using Figure 13. In an application where voltage translation is necessary, additional design requirements must be considered (See Design Requirements).

Figure 12 shows an application in which the PCA9545A can be used.

![Figure 12. Typical Application Schematic](image-url)
Typical Application (continued)

10.2.1 Design Requirements

The pull-up resistors on the INT3-INT0 terminals in the application schematic are not required in all applications. If the device generating the interrupt has an open-drain output structure or can be tri-stated, a pull-up resistor is required. If the device generating the interrupt has a push-pull output structure and cannot be tri-stated, a pull-up resistor is not required. The interrupt inputs should not be left floating in the application.

The A0 and A1 terminals are hardware selectable to control the slave address of the PCA9545A. These terminals may be tied directly to GND or V_{CC} in the application.

If multiple slave channels will be activated simultaneously in the application, then the total $I_{OL}$ from SCL/SDA to GND on the master side will be the sum of the currents through all pull-up resistors, $R_p$.

The pass-gate transistors of the PCA9545A are constructed such that the $V_{CC}$ voltage can be used to limit the maximum voltage that is passed from one I$^2$C bus to another.

Figure 13 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the Electrical Characteristics section of this data sheet). In order for the PCA9545A to act as a voltage translator, the $V_{pass}$ voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V, $V_{pass}$ must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 13, $V_{pass(max)}$ is 2.7 V when the PCA9545A supply voltage is 4 V or lower, so the PCA9545A supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 12).

10.2.2 Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors, $R_p$, for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of $V_{DPUX}$, $V_{OL(max)}$, and $I_{OL}$:

$$R_p^{(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}}$$

(1)

The maximum pull-up resistance is a function of the maximum rise time, $t_r$ (300 ns for fast-mode operation, $f_{SCL} = 400$ kHz) and bus capacitance, $C_b$:

$$R_p^{(max)} = \frac{t_r}{0.8473 \times C_b}$$

(2)

The maximum bus capacitance for an I$^2$C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCA9545A, $C_{io(OFF)}$, the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If multiple channels will be activated simultaneously, each of the slaves on all channels will contribute to total bus capacitance.
Typical Application (continued)

10.2.3 PCA9545A Application Curves

Figure 13. Pass-Gate Voltage ($V_{pass}$) vs Supply Voltage ($V_{CC}$) at Three Temperature Points

Figure 14. Maximum Pull-Up resistance ($R_{p(max)}$) vs Bus Capacitance ($C_{b}$)

Figure 15. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage ($V_{DPUX}$)

$V_{OL} = 0.2 \times V_{DPUX}$, $I_{OL} = 2 \text{ mA}$ when $V_{DPUX} \leq 2 \text{ V}$

$V_{OL} = 0.4 \text{ V}$, $I_{OL} = 3 \text{ mA}$ when $V_{DPUX} > 2 \text{ V}$
11 Power Supply Recommendations

The operating power-supply voltage range of the PCA9545A is 2.3 V to 5.5 V applied at the VCC pin. When the PCA9545A is powered on for the first time or anytime the device needs to be reset by cycling the power supply, the power-on reset requirements must be followed to ensure the I²C bus logic is initialized properly.

11.1 Power-On Reset Errata

A power-on reset condition can be missed if the VCC ramps are outside specification listed below.

**System Impact**

If ramp conditions are outside timing allowances above, POR condition can be missed, causing the device to lock up.

12 Layout

12.1 Layout Guidelines

For PCB layout of the PCA9545A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I²C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and terminals that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC terminal, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all V_{DPUX} voltages and V_{CC} could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V_{DPUM}, V_{DPUD}, V_{DPUL}, V_{DPU2}, and V_{DPU3} may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I²C bus capacitance added by PCB parasitics, data lines (SCn, SDn and INTn) should be as short as possible and the widths of the traces should also be minimized (e.g. 5-10 mils depending on copper weight).
12.2 Layout Example

LEGEND
- Partial Power Plane
- Polygonal Copper Pour
- VIA to Power Plane
- VIA to GND Plane (Inner Layer)

PCA9545A

To Slave Channel 0
To Slave Channel 1
V\textsubscript{DPU1}

To I2C Master
V\textsubscript{DPLUM}

GND

A0
A1
RESET
INT0
SD0
SC0
INT1
SD1
SC1
GND
VCC
SDA
SCL
INT
SC3
SD3
INT3
SC2
SD2
INT2
V\textsubscript{DPU0}

V\textsubscript{DPU3}

By-pass/De-coupling capacitors

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13 Device and Documentation Support

13.1 Trademarks
All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary
SLYZ022 — *TI Glossary.*
This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCA9545ADW</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>25</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>PCA9545A</td>
<td>Samples</td>
</tr>
<tr>
<td>PCA9545ADWR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>PCA9545A</td>
<td>Samples</td>
</tr>
<tr>
<td>PCA9545APW</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>20</td>
<td>70</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>PD545A</td>
<td>Samples</td>
</tr>
<tr>
<td>PCA9545APWR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>20</td>
<td>2000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>PD545A</td>
<td>Samples</td>
</tr>
<tr>
<td>PCA9545APWT</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>20</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>PD545A</td>
<td>Samples</td>
</tr>
<tr>
<td>PCA9545ARGYR</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGY</td>
<td>20</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>PD545A</td>
<td>Samples</td>
</tr>
<tr>
<td>PCA9545ARGYRG4</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGY</td>
<td>20</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>PD545A</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a “~” will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### REEL DIMENSIONS

- Reel Diameter
- Reel Width (W1)

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- Q1: Pocket Quadrants
- Q2: Sprocket Holes
- Q3: User Direction of Feed

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCA9545ADWR</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>330.0</td>
<td>24.4</td>
<td>10.8</td>
<td>13.3</td>
<td>2.7</td>
<td>12.0</td>
<td>24.0</td>
<td>Q1</td>
</tr>
<tr>
<td>PCA9545APWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>20</td>
<td>2000</td>
<td>330.0</td>
<td>16.4</td>
<td>6.95</td>
<td>7.0</td>
<td>1.4</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>PCA9545APWT</td>
<td>TSSOP</td>
<td>PW</td>
<td>20</td>
<td>250</td>
<td>330.0</td>
<td>16.4</td>
<td>6.95</td>
<td>7.0</td>
<td>1.4</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>PCA9545ARGYR</td>
<td>VQFN</td>
<td>RGY</td>
<td>20</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>3.8</td>
<td>4.8</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCA9545ADWR</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>367.0</td>
<td>367.0</td>
<td>45.0</td>
</tr>
<tr>
<td>PCA9545APWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>20</td>
<td>2000</td>
<td>853.0</td>
<td>449.0</td>
<td>35.0</td>
</tr>
<tr>
<td>PCA9545APWT</td>
<td>TSSOP</td>
<td>PW</td>
<td>20</td>
<td>250</td>
<td>853.0</td>
<td>449.0</td>
<td>35.0</td>
</tr>
<tr>
<td>PCA9545ARGYR</td>
<td>VQFN</td>
<td>RGY</td>
<td>20</td>
<td>3000</td>
<td>853.0</td>
<td>449.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
\(\Delta\) Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.
\(\Delta\) Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.
E. Falls within JEDEC MO-153
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application; refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged, or tented.
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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