# PCF8574 Remote 8-Bit I/O Expander for I²C Bus

## 1 Features

- Low standby-current consumption of 10μA max
- I²C to parallel-port expander
- Open-drain interrupt output
- Compatible with most microcontrollers
- Latched outputs with high-current drive capability for directly driving LEDs
- Latch-up performance exceeds 100mA per JESD 78, Class II

## 2 Applications

- Telecom shelters: filter units
- Servers
- Routers (telecom switching equipment)
- Personal computers
- Personal electronics
- Industrial automation
- Products with GPIO-limited processors

## 3 Description

This 8-bit input/output (I/O) expander for the two-line bidirectional bus (I²C) is designed for 2.5V to 6V $V_{CC}$ operation.

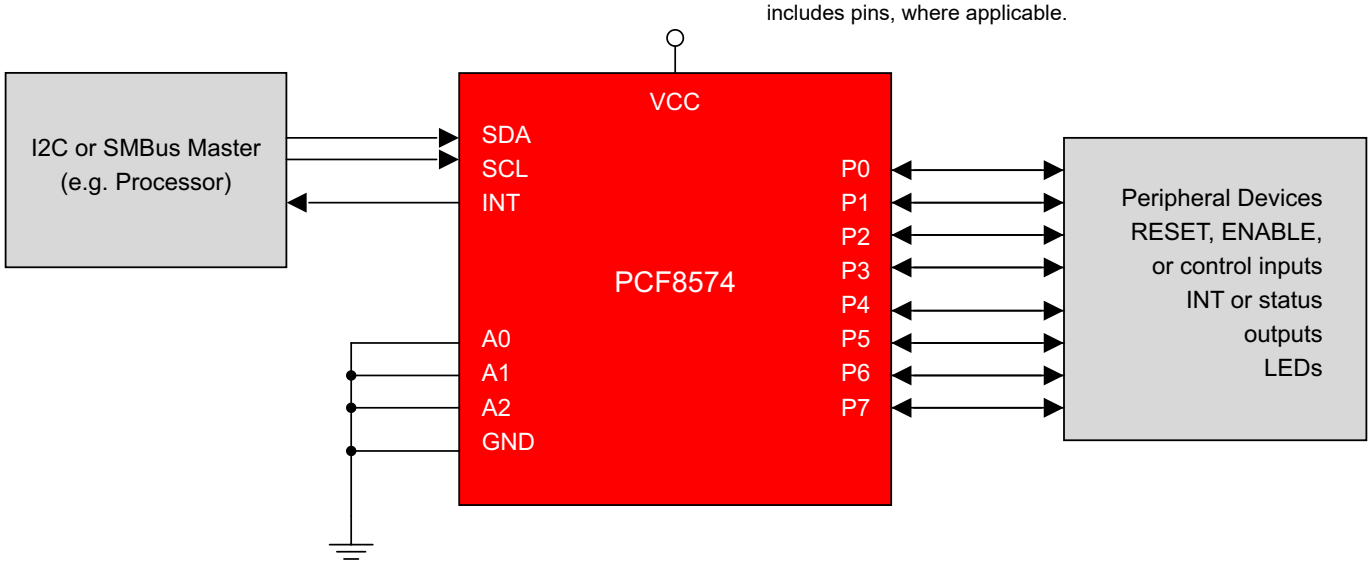
The PCF8574 device provides general-purpose remote I/O expansion for most microcontroller families by way of the I²C interface [serial clock (SCL), serial data (SDA)].

The device features an 8-bit quasi-bidirectional I/O port (P0–P7), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source to $V_{CC}$ is active.

**Package Information**

| PART NUMBER | PACKAGE (1) | PACKAGE SIZE(2) |
|---|---|---|
| PCF8574 | TVSOP (DGV, 20) | 5mm × 6.40mm |
| | SOIC (DW, 16) | 10.3mm × 10.3mm |
| | PDIP (N, 16) | 19.3mm × 9.4mm |
| | TSSOP (PW,20) | 6.5mm × 6.4mm |
| | VQFN (RGT, 16) | 3mm × 3mm |
| | VQFN (RGY, 20) | 4.5mm × 3.5mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Simplified Schematic**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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# 4 Pin Configuration and Functions

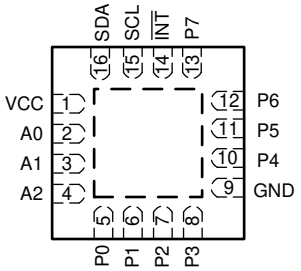


**Figure 4-1. RGT Package, 16 Pins (Top View)**

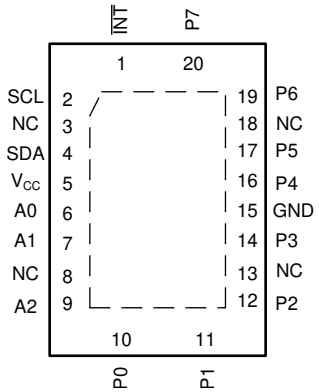


**Figure 4-2. RGY Package, 20 Pins (Top View)**

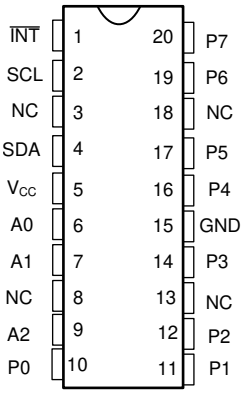


**Figure 4-3. DGV or PW Package, 20 Pins (Top View)**

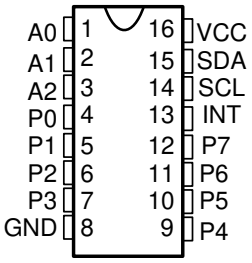


**Figure 4-4. DW or N Package, 20 Pins, Top View**

**Table 4-1. Pin Functions**

| PIN | | | | | TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|
| NAME | RGT | RGY | DGV or PW | DW or N | | |
| A [0..2] | 2, 3, 4 | 6, 7, 9 | 6, 7, 9 | 1, 2, 3 | I | Address inputs 0 through 2. Connect directly to $V_{CC}$ or ground. Pullup resistors are not needed. |
| GND | 9 | 15 | 15 | 8 | — | Ground |
| $\overline{INT}$ | 14 | 1 | 1 | 13 | O | Interrupt output. Connect to $V_{CC}$ through a pullup resistor. |
| NC | - | 3, 8, 13, 18 | 3, 8, 13, 18 | - | — | Do not connect |
| P[0..7] | 5, 6, 7, 8, 10, 11, 12, 13 | 10, 11, 12, 14, 16, 17, 19, 20 | 10, 11, 12, 14, 16, 17, 19, 20 | 4, 5, 6, 7, 9, 10, 11, 12 | I/O | P-port input/output. Push-pull design structure. |
| SCL | 15 | 2 | 2 | 14 | I | Serial clock line. Connect to $V_{CC}$ through a pullup resistor |
| SDA | 16 | 4 | 4 | 15 | I/O | Serial data line. Connect to $V_{CC}$ through a pullup resistor. |
| $V_{CC}$ | 1 | 5 | 5 | 16 | — | Voltage supply |

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage range[2] | | –0.5 | $V_{CC}$ + 0.5 | V |
| $V_O$ | Output voltage range[2] | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ | | –20 | mA |
| $I_{OK}$ | Input/output clamp current | $V_O < 0$ or $V_O > V_{CC}$ | | ±400 | µA |
| $I_{OL}$ | Continuous output low current | $V_O = 0$ to $V_{CC}$ | | 50 | mA |
| $I_{OH}$ | Continuous output high current | $V_O = 0$ to $V_{CC}$ | | –4 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 5.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1] | 1500 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 [2] | 2000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

## 5.3 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 2.5 | 6 | V |
| $V_{IH}$ | High-level input voltage | 0.7 × $V_{CC}$ | $V_{CC}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | –0.5 | 0.3 × $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –1 | mA |
| $I_{OL}$ | Low-level output current | | 25 | mA |
| $T_A$ | Operating free-air temperature | –40 | 85 | °C |

## 5.4 Thermal Information

| THERMAL METRIC [1] | | PCF8574 | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | DGV | DW | N | PW | RGT | RGY | |
| | | 20 PINS | 16 PINS | 16 PINS | 20 PINS | 16 PINS | 20 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 92 | 76.7 | 73.1 | 94.8 | 56.0 | 52.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | - | 45.1 | 51.9 | 40.2 | 67.4 | 50.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | - | 45.8 | 48.3 | 58.5 | 31.2 | 29.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | - | 17.2 | 29.8 | 2.8 | 3.9 | 3.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | - | 45.2 | 47.9 | 58.0 | 31.1 | 29.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | - | n/a | n/a | n/a | 15.1 | 16.0 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.


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## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| | | TEST CONDITIONS | | | VCC | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input diode clamp voltage | $I_I$ = –18 mA | | | 2.5 V to 6 V | –1.2 | | | V |
| $V_{POR}$ | Power-on reset voltage | $V_I = V_{CC}$ or GND, | $I_O$ = 0 | | 6 V | | 1.3 | 2.4 | V |
| $I_{OH}$ | P port | $V_O$ = GND | | | 2.5 V to 6 V | -310 | | -30 | µA |
| $I_{OHT}$ | P port transient pullup current | High during acknowledge, $V_{OH}$ = GND | | | 2.5 V | | –1 | | mA |
| $I_{OL}$ | SDA | $V_O$ = 0.4 V | | | 2.5 V to 6 V | 3 | | | mA |
| | P port | $V_O$ = 1 V | | | 5 V | 10 | 25 | | |
| | $\overline{INT}$ | $V_O$ = 0.4 V | | | 2.5 V to 6 V | 1.6 | | | |
| $I_I$ | SCL, SDA | $V_I = V_{CC}$ or GND | | | 2.5 V to 6 V | | | ±5 | µA |
| | $\overline{INT}$ | | | | | | | ±5 | |
| | A0, A1, A2 | | | | | | | ±5 | |
| $I_{IHL}$ | P port | -250mV < Vi < GND | | | 2.5 V to 6 V | | | ±400 | µA |
| $I_{CC}$ | Operating mode | $V_I = V_{CC}$ or GND, | $I_O$ = 0, | $f_{SCL}$ = 100 kHz | 6 V | | 40 | 100 | µA |
| | Standby mode | $V_I = V_{CC}$ or GND, | $I_O$ = 0 | | | | 2.5 | 10 | |
| $C_i$ | SCL | $V_I = V_{CC}$ or GND | | | 2.5 V to 6 V | | 1.5 | 7 | pF |
| $C_{io}$ | SDA | $V_{IO} = V_{CC}$ or GND | | | 2.5 V to 6 V | | 3 | 7 | pF |
| | P port | | | | | | 4 | 10 | |

(1) All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## 5.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{scl}$ | I²C clock frequency | | | 100 | kHz |
| $t_{sch}$ | I²C clock high time | | 4 | | µs |
| $t_{scl}$ | I²C clock low time | | 4.7 | | µs |
| $t_{sp}$ | I²C spike time | | | 70 | ns |
| $t_{sds}$ | I²C serial data setup time | | 250 | | ns |
| $t_{sdh}$ | I²C serial data hold time | | 0 | | ns |
| $t_{icr}$ | I²C input rise time | | | 1 | µs |
| $t_{icf}$ | I²C input fall time | | | 0.3 | µs |
| $t_{ocf}$ | I²C output fall time (10-pF to 400-pF bus) | | | 300 | ns |
| $t_{buf}$ | I²C bus free time between stop and start | | 4.7 | | µs |
| $t_{sts}$ | I²C start or repeated start condition setup | | 4.7 | | µs |
| $t_{sth}$ | I²C start or repeated start condition hold | | 4 | | µs |
| $t_{sps}$ | I²C stop condition setup | | 4 | | µs |
| $t_{vd}$ | Valid data time | SCL low to SDA output valid | | 3.4 | µs |
| $C_b$ | I²C bus capacitive load | | | 400 | pF |

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## 5.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L$ ≤ 100 pF (unless otherwise noted)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pv}$ | Output data valid | SCL | P port | | 4 | µs |
| $t_{su}$ | Input data setup time | P port | SCL | 0 | | µs |
| $t_h$ | Input data hold time | P port | SCL | 4 | | µs |
| $t_{iv}$ | Interrupt valid time | P port | $\overline{INT}$ | | 4 | µs |
| $t_{ir}$ | Interrupt reset delay time | SCL | $\overline{INT}$ | | 4 | µs |


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## 5.8 Typical Characteristics

$T_A$ = 25°C (unless otherwise noted)

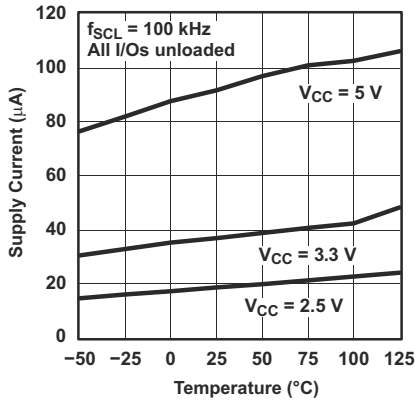


**Figure 5-1. Supply Current vs Temperature**

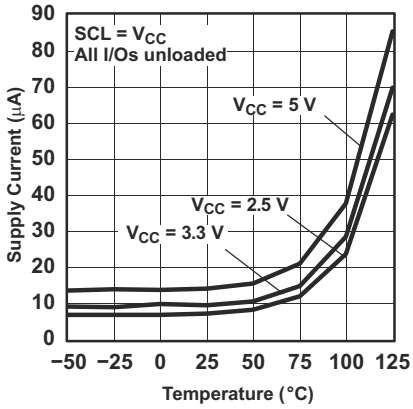


**Figure 5-2. Standby Supply Current vs Temperature**

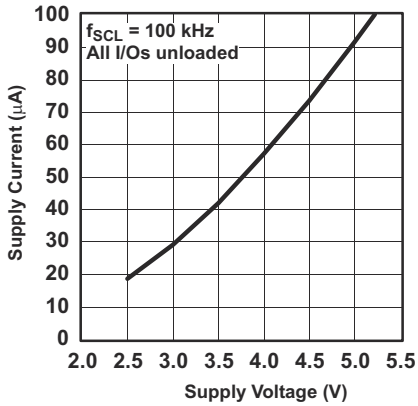


**Figure 5-3. Supply Current vs Supply Voltage**

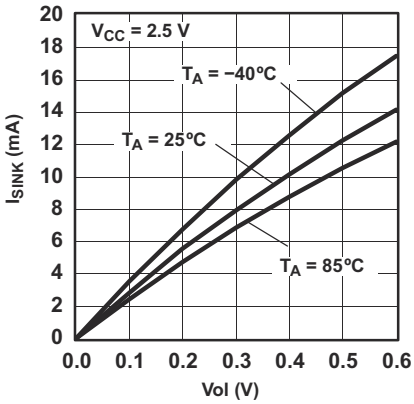


**Figure 5-4. I/O Sink Current vs Output Low Voltage**

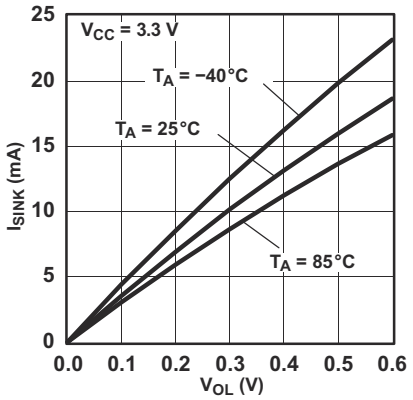


**Figure 5-5. I/O Sink Current vs Output Low Voltage**

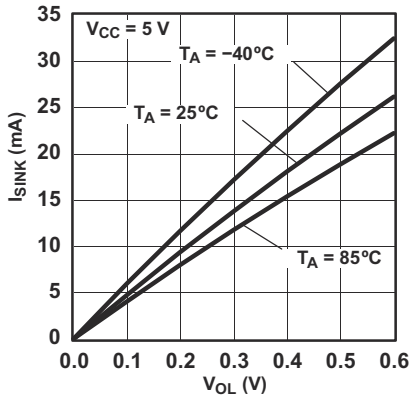


**Figure 5-6. I/O Sink Current vs Output Low Voltage**

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## 5.8 Typical Characteristics (continued)

$T_A$ = 25°C (unless otherwise noted)

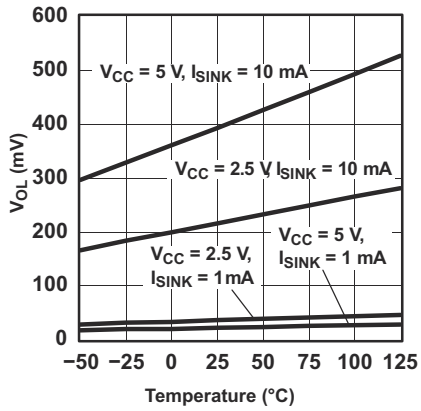


**Figure 5-7. I/O Output Low Voltage vs Temperature**

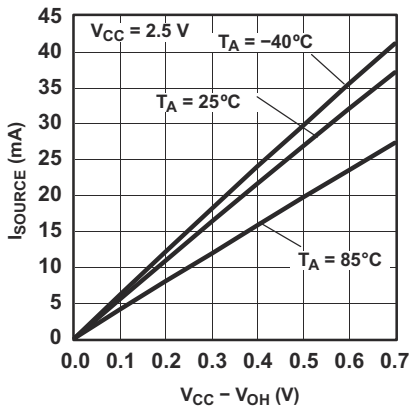


**Figure 5-8. I/O Source Current vs Output High Voltage**

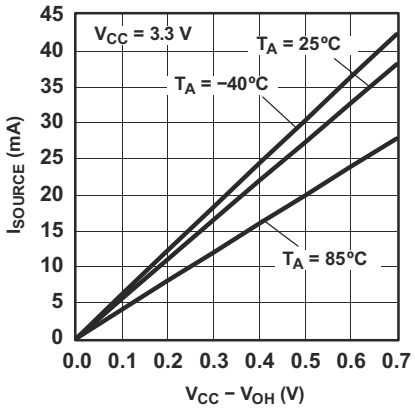


**Figure 5-9. I/O Source Current vs Output High Voltage**

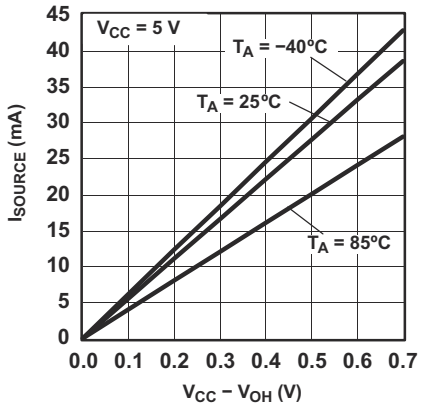


**Figure 5-10. I/O Source Current vs Output High Voltage**

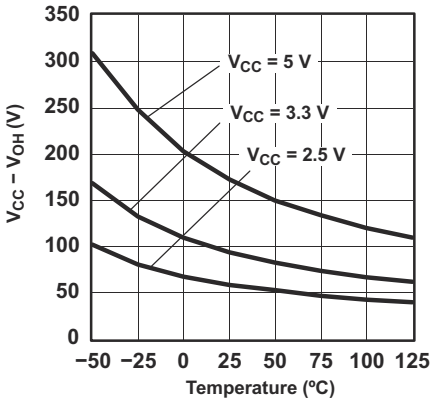


**Figure 5-11. I/O High Voltage vs Temperature**


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## 6 Parameter Measurement Information

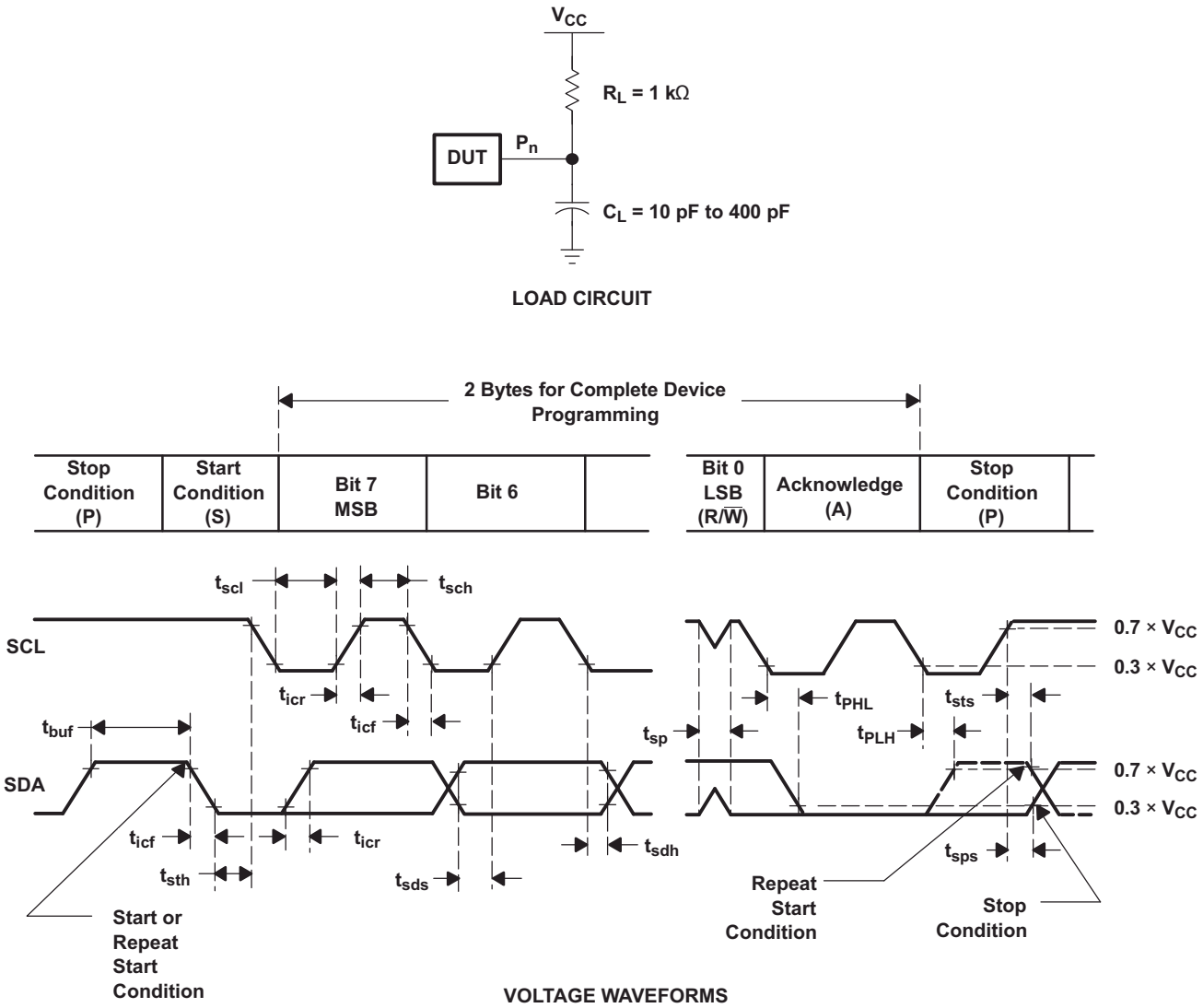


**Figure 6-1. I²C Interface Load Circuit and Voltage Waveforms**

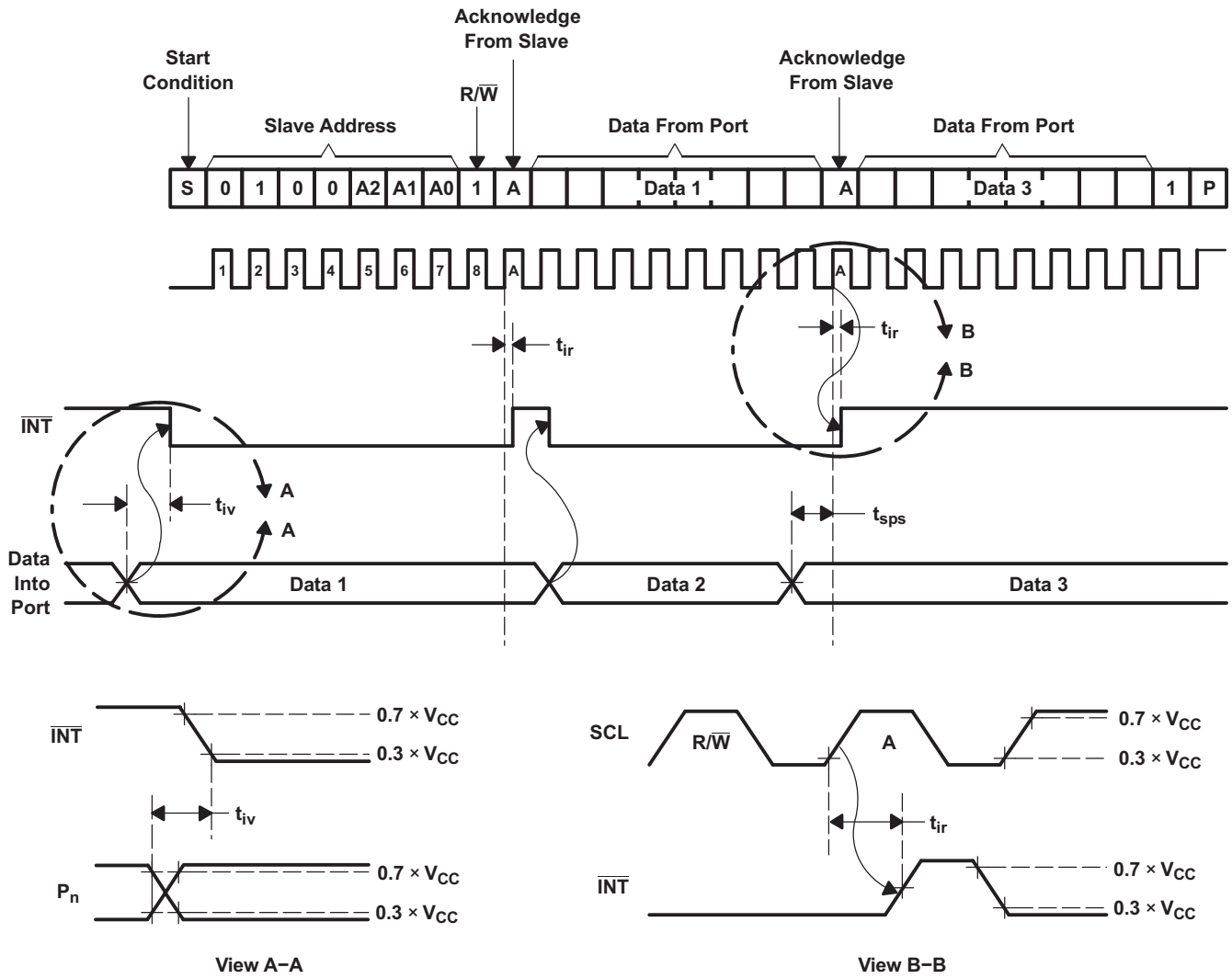


**Figure 6-2. Interrupt Voltage Waveforms**

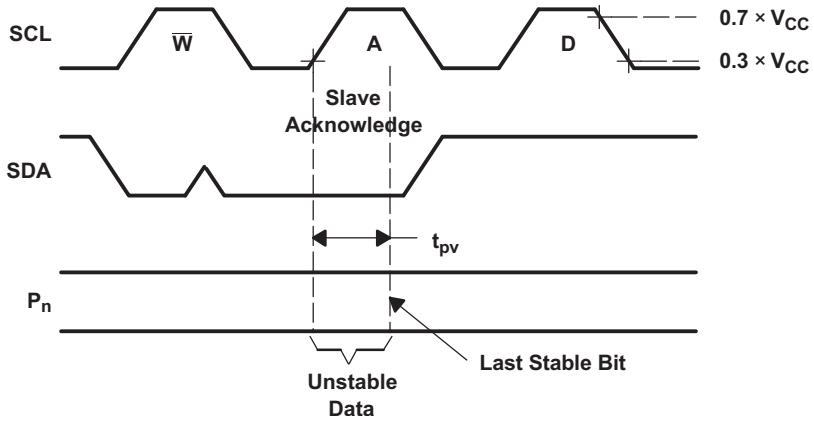


**Figure 6-3. I²C Write Voltage Waveforms**


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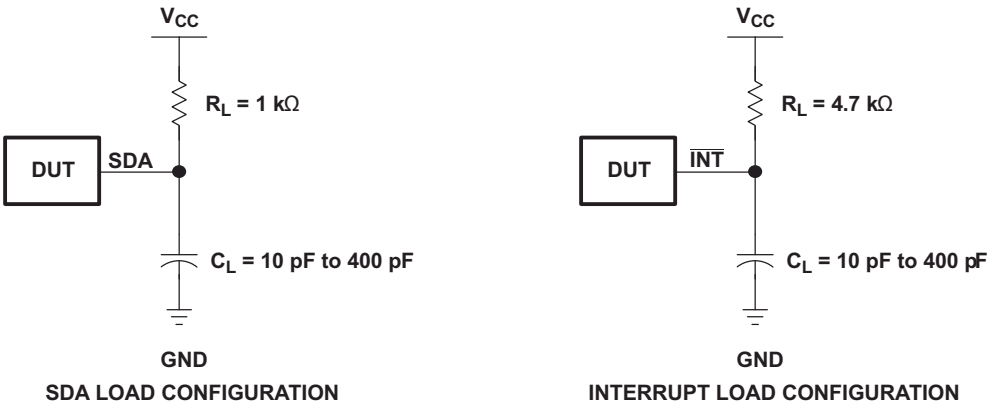



**Figure 6-4. Load Circuits**

# 7 Detailed Description

## 7.1 Overview

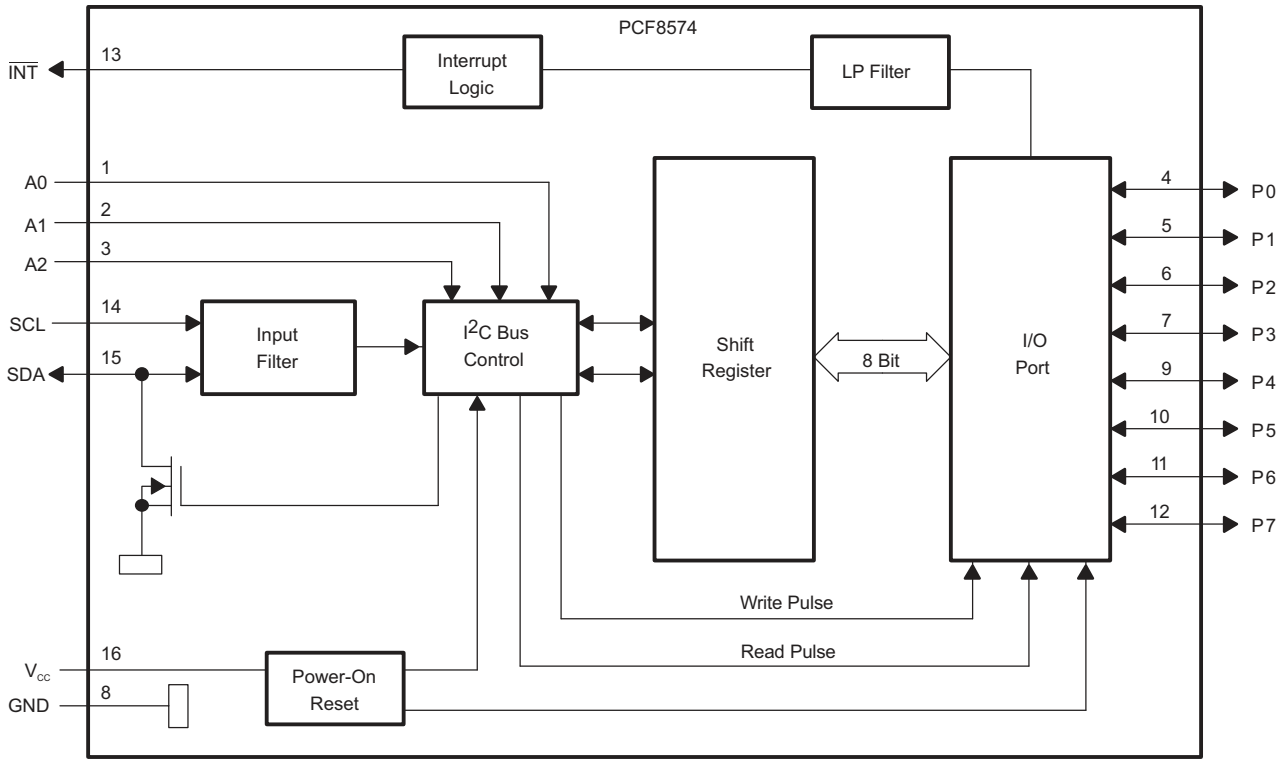
The PCF8574 device is an 8-bit I/O expander for the two-line bidirectional bus (I2C) is designed for 2.5-V to 6-V $V_{CC}$ operation. It provides general-purpose remote I/O expansion for most micro-controller families via the I2C interface (serial clock, SCL, and serial data, SDA, pins).

The PCF8574 device provides an open-drain output ( $\overline{INT}$) that can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, $t_{iv}$, $\overline{INT}$ is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from, or written to, the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge bit after the rising edge of the SCL signal, or in the write mode at the acknowledge bit after the high-to-low transition of the SCL signal. Interrupts that occur during the acknowledge clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and, after the next rising clock edge, is transmitted as $\overline{INT}$. Reading from, or writing to, another device does not affect the interrupt circuit. This device does not have internal configuration or status registers. Instead, read or write to the device I/Os directly after sending the device address (see Figure 7-3 and Figure 7-4).

By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate by way of the $I^2C$ bus. Therefore, PCF8574 can remain a simple target device.

An additional strong pullup to $V_{CC}$ allows fast rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs.

## 7.2 Functional Block Diagram




Pin numbers shown are for the DW and N packages.

**Figure 7-1. Simplified Block Diagram of Device**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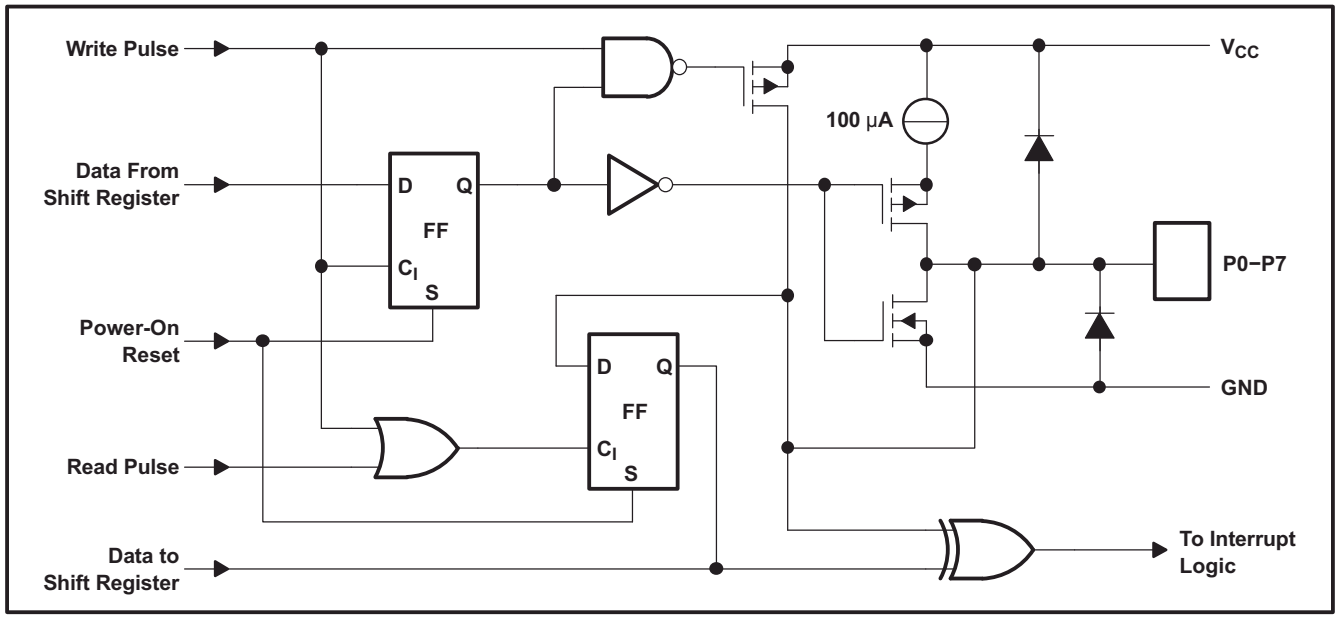


**Figure 7-2. Simplified Schematic Diagram of Each P-Port Input or Output**

## 7.3 Feature Description

### *7.3.1 I²C Interface*

I²C communication with this device is initiated by a controller sending a start condition, a high-to-low transition on the SDA I/O while the SCL input is high. After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/ $\overline{W}$). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an acknowledge, a low on the SDA I/O during the high of the acknowledge-related clock pulse. The address inputs (A0–A2) of the target device must not be changed between the start and the stop conditions.

The data byte follows the address acknowledge. If the R/ $\overline{W}$ bit is high, the data from this device are the values read from the P port. If the R/ $\overline{W}$ bit is low, the data are from the controller, to be output to the P port. The data byte is followed by an acknowledge sent from this device. If other data bytes are sent from the controller, following the acknowledge, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data will be valid at time, $t_{pv}$, after the low-to-high transition of SCL and during the clock cycle for the acknowledge.

A stop condition, which is a low-to-high transition on the SDA I/O while the SCL input is high, is sent by the controller.

### *7.3.2 Interface Definition*

| BYTE | BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 (MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) |
| I²C target address | L | H | L | L | A2 | A1 | A0 | R/ $\overline{W}$ |
| I/O data bus | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

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### 7.3.3 Address Reference

| INPUTS | | | I²C BUS TARGET 8-BIT READ ADDRESS | I²C BUS TARGET 8-BIT WRITE ADDRESS |
|---|---|---|---|---|
| A2 | A1 | A0 | | |
| L | L | L | 65 (decimal), 41 (hexadecimal) | 64 (decimal), 40 (hexadecimal) |
| L | L | H | 67 (decimal), 43 (hexadecimal) | 66 (decimal), 42 (hexadecimal) |
| L | H | L | 69 (decimal), 45 (hexadecimal) | 68 (decimal), 44 (hexadecimal) |
| L | H | H | 71 (decimal), 47 (hexadecimal) | 70 (decimal), 46 (hexadecimal) |
| H | L | L | 73 (decimal), 49 (hexadecimal) | 72 (decimal), 48 (hexadecimal) |
| H | L | H | 75 (decimal), 4B (hexadecimal) | 74 (decimal), 4A (hexadecimal) |
| H | H | L | 77 (decimal), 4D (hexadecimal) | 76 (decimal), 4C (hexadecimal) |
| H | H | H | 79 (decimal), 4F (hexadecimal) | 78 (decimal), 4E (hexadecimal) |

## 7.4 Device Functional Modes

Figure 7-3 and Figure 7-4 show the address and timing diagrams for the write and read modes, respectively.

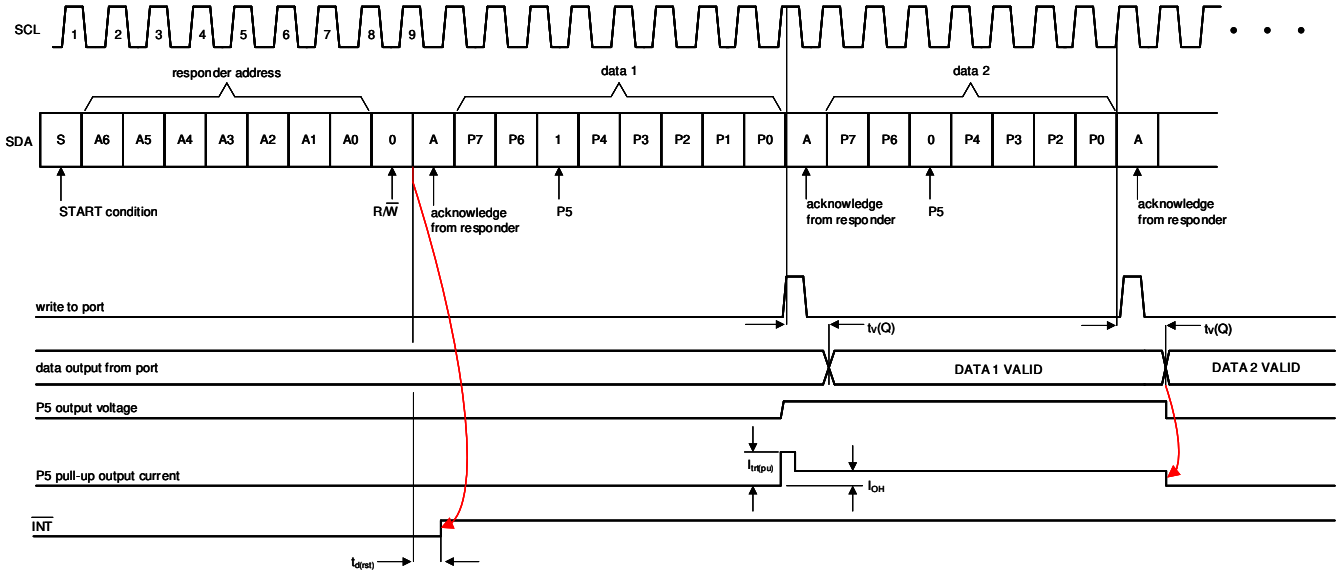


**Figure 7-3. Write Mode (Output)**


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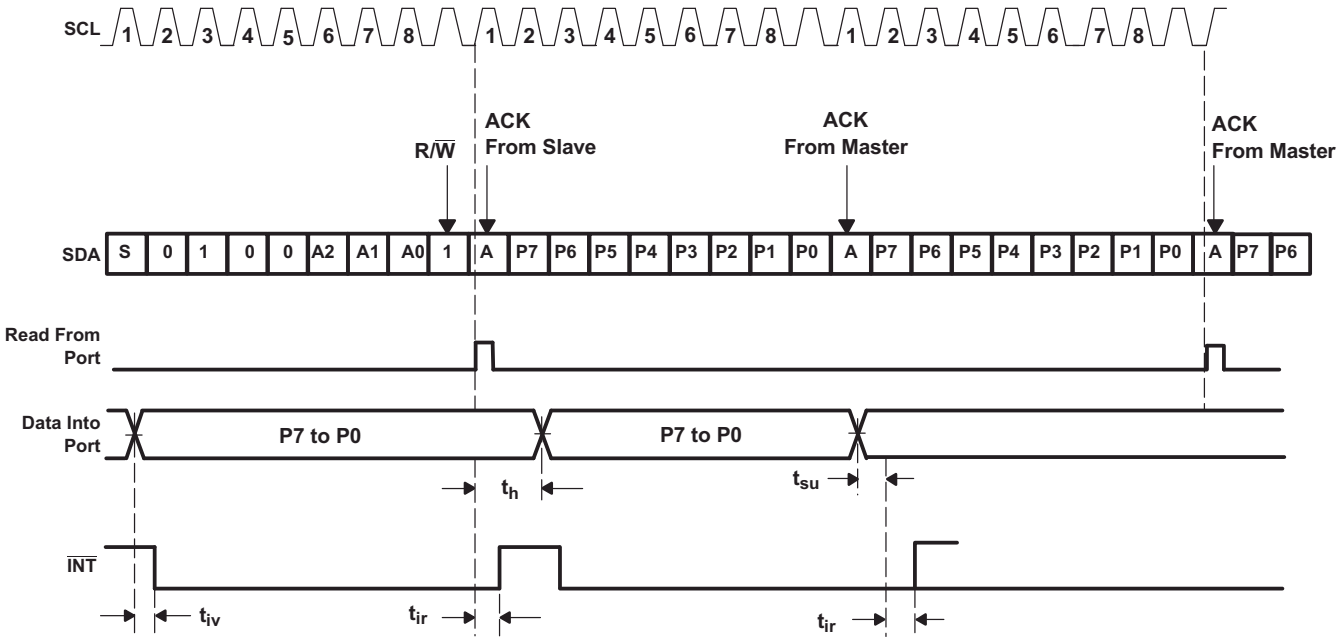



A. A low-to-high transition of SDA while SCL is high is defined as the stop condition (P). The transfer of data can be stopped at any moment bya stop condition. When this occurs, data present at the latest ACK phase is valid (output mode). Input data is lost.

**Figure 7-4. Read Mode (Input)**

# 8 Application and Implementation

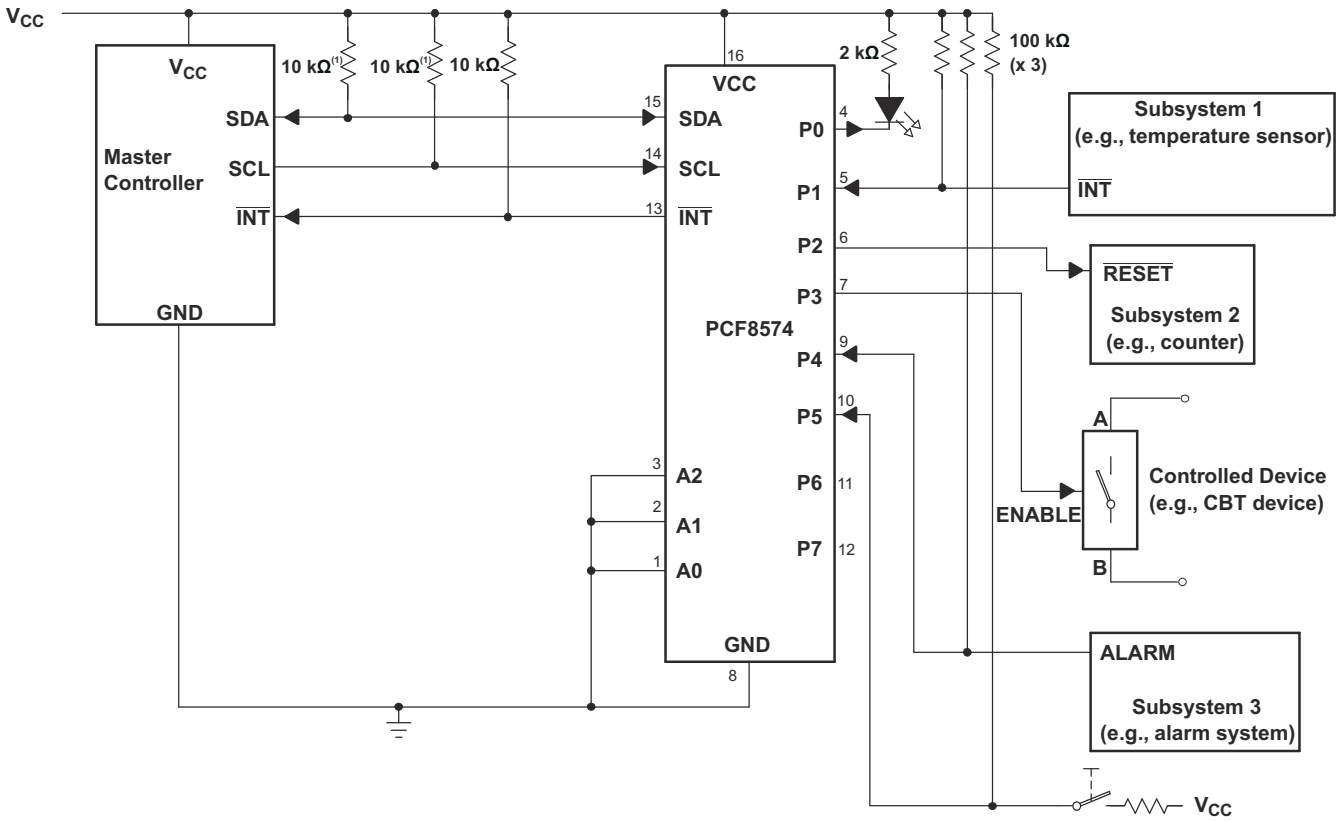
**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

Figure 8-1 shows an application in which the PCF8574 device can be used.

## 8.2 Typical Application




A. The SCL and SDA pins must be tied directly to $V_{CC}$ because if SCL and SDA are tied to an auxiliary power supply that could be powered on while $V_{CC}$ is powered off, then the supply current, ICC, will increase as a result.
B. Device address is configured as 0100000 for this example.
C. P0, P2, and P3 are configured as outputs.
D. P1, P4, and P5 are configured as inputs.
E. P6 and P7 are not used and must be configured as outputs.

**Figure 8-1. Application Schematic**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### *8.2.1 Design Requirements*

#### 8.2.1.1 Minimizing $I_{CC}$ When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to $V_{CC}$ through a resistor as shown in Figure 8-1. For a P-port configured as an input, $I_{CC}$ increases as $V_I$ becomes lower than $V_{CC}$. The LED is a diode, with threshold voltage $V_T$, and when a P-port is configured as an input the LED will be off but $V_I$ is a $V_T$ drop below $V_{CC}$.

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to $V_{CC}$ when the P-ports are configured as input to minimize current consumption. Figure 8-2 shows a high-value resistor in parallel with the LED. Figure 8-3 shows $V_{CC}$ less than the LED supply voltage by at least $V_T$. Both of these methods maintain the I/O $V_I$ at or above $V_{CC}$ and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.

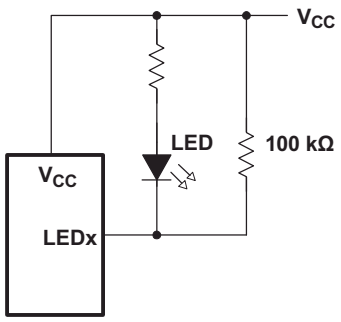



**Figure 8-2. High-Value Resistor in Parallel With LED**

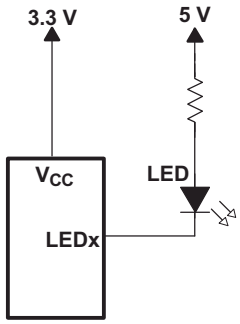



**Figure 8-3. Device Supplied by a Lower Voltage**

### 8.2.2 Detailed Design Procedure

The pull-up resistors, $R_P$, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all targets on the $I^2C$ bus. The minimum pull-up resistance is a function of $V_{CC}$, $V_{OL,(max)}$, and $I_{OL}$:

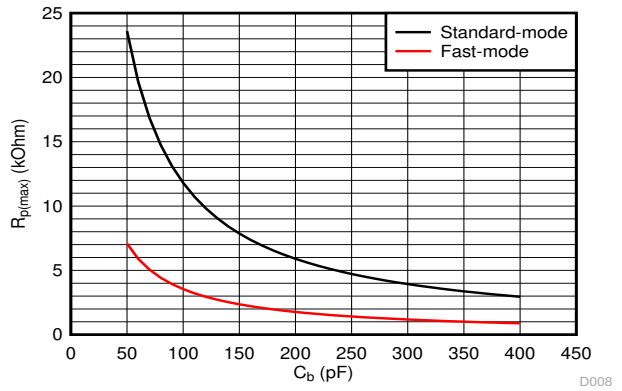
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \tag{1}$$

The maximum pull-up resistance is a function of the maximum rise time, $t_r$ (300 ns for fast-mode operation, $f_{SCL}$ = 400 kHz) and bus capacitance, $C_b$:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \tag{2}$$

The maximum bus capacitance for an $I^2C$ bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCF8574 device, $C_i$ for SCL or $C_{io}$ for SDA, the capacitance of wires/connections/traces, and the capacitance of additional targets on the bus.

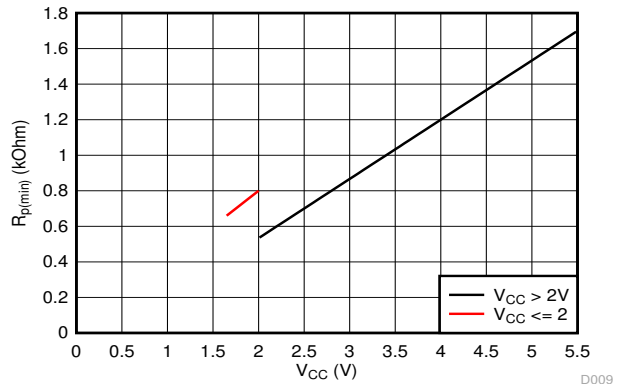
### 8.2.3 Application Curves




Standard-mode ($f_{SCL}$= 100 kHz, $t_r$ = 1 µs)

Fast-mode ($f_{SCL}$= 400 kHz, $t_r$= 300 ns)

**Figure 8-4. Maximum Pull-Up resistance ($R_{p(max)}$) vs Bus Capacitance ($C_b$)**




$V_{OL}$ = 0.2*$V_{CC}$, $I_{OL}$ = 2 mA when $V_{CC}$ ≤ 2 V

$V_{OL}$ = 0.4 V, $I_{OL}$ = 3 mA when $V_{CC}$ > 2 V

**Figure 8-5. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage ($V_{CC}$)**

## 8.3 Power Supply Recommendations

### 8.3.1 Power-On Reset Requirements

In the event of a glitch or data corruption, the PCF8574 device can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 8-6 and Figure 8-7.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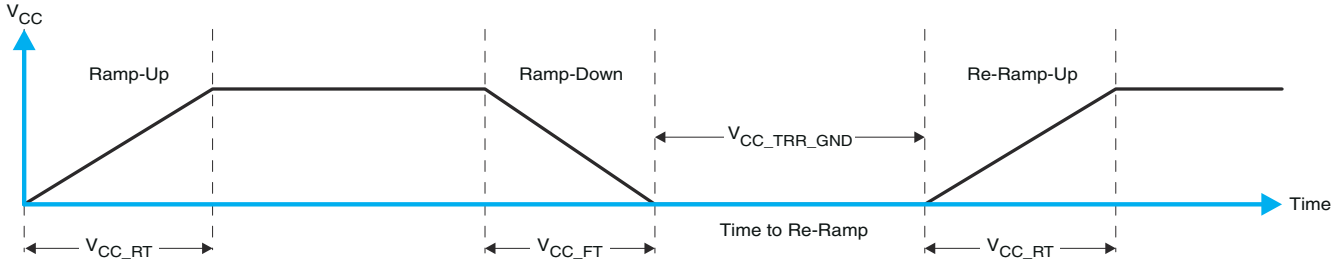


**Figure 8-6. $V_{CC}$ is Lowered Below 0.2 V or 0 V and Then Ramped Up to $V_{CC}$**

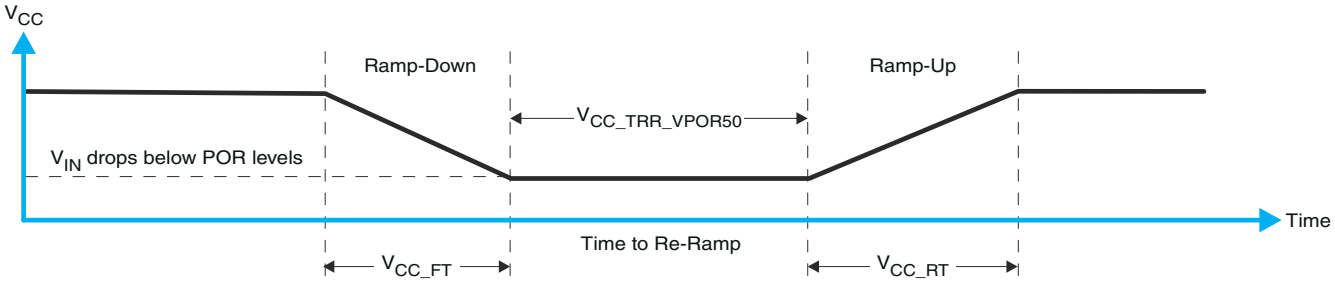


**Figure 8-7. $V_{CC}$ is Lowered Below the POR Threshold, Then Ramped Back Up to $V_{CC}$**

Table 8-1 specifies the performance of the power-on reset feature for PCF8574 for both types of power-on reset.

**Table 8-1. Recommended Supply Sequencing and Ramp Rates (1)**

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC_FT}$ | Fall rate | See Figure 8-6 | 1 | | 100 | ms |
| $V_{CC_RT}$ | Rise rate | See Figure 8-6 | 0.01 | | 100 | ms |
| $V_{CC_TRR_GND}$ | Time to re-ramp (when $V_{CC}$ drops to GND) | See Figure 8-6 | 0.001 | | | ms |
| $V_{CC_TRR_POR50}$ | Time to re-ramp (when $V_{CC}$ drops to $V_{POR_MIN}$ – 50 mV) | See Figure 8-7 | 0.001 | | | ms |
| $V_{CC_GH}$ | Level that $V_{CCP}$ can glitch down to, but not cause a functional disruption when $V_{CCX_GW}$ = 1 µs | See Figure 8-8 | | | 1.2 | V |
| $V_{CC_GW}$ | Glitch width that will not cause a functional disruption when $V_{CCX_GH}$ = 0.5 × $V_{CCx}$ | See Figure 8-8 | | | | µs |
| $V_{PORF}$ | Voltage trip point of POR on falling $V_{CC}$ | | 0.99 | | 1.28 | V |
| $V_{PORR}$ | Voltage trip point of POR on fising $V_{CC}$ | | 1.190 | | 1.410 | V |

(1) $T_A$ = –40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($V_{CC_GW}$) and height ($V_{CC_GH}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 8-8 and Table 8-1 provide more information on how to measure these specifications.

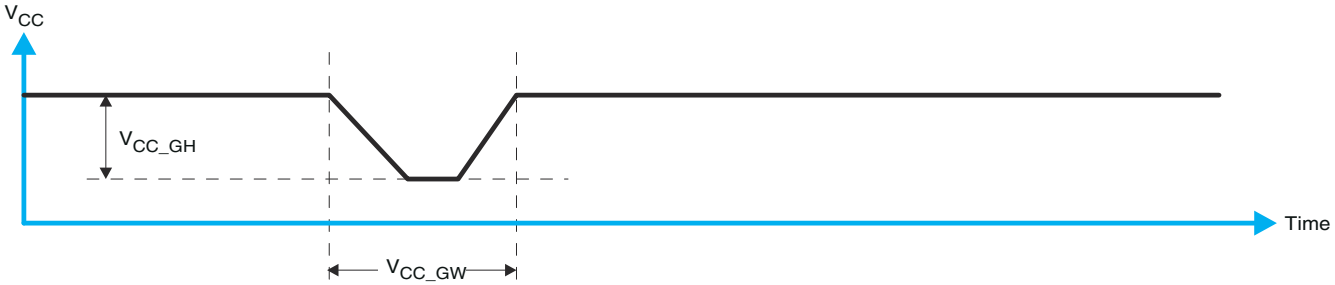


**Figure 8-8. Glitch Width and Glitch Height**

$V_{POR}$ is critical to the power-on reset. $V_{POR}$ is the voltage level at which the reset condition is released and all the registers and the $I^2C$/SMBus state machine are initialized to their default states. The value of $V_{POR}$ differs based on the $V_{CC}$ being lowered to or from 0. Figure 8-9 and Table 8-1 provide more details on this specification.

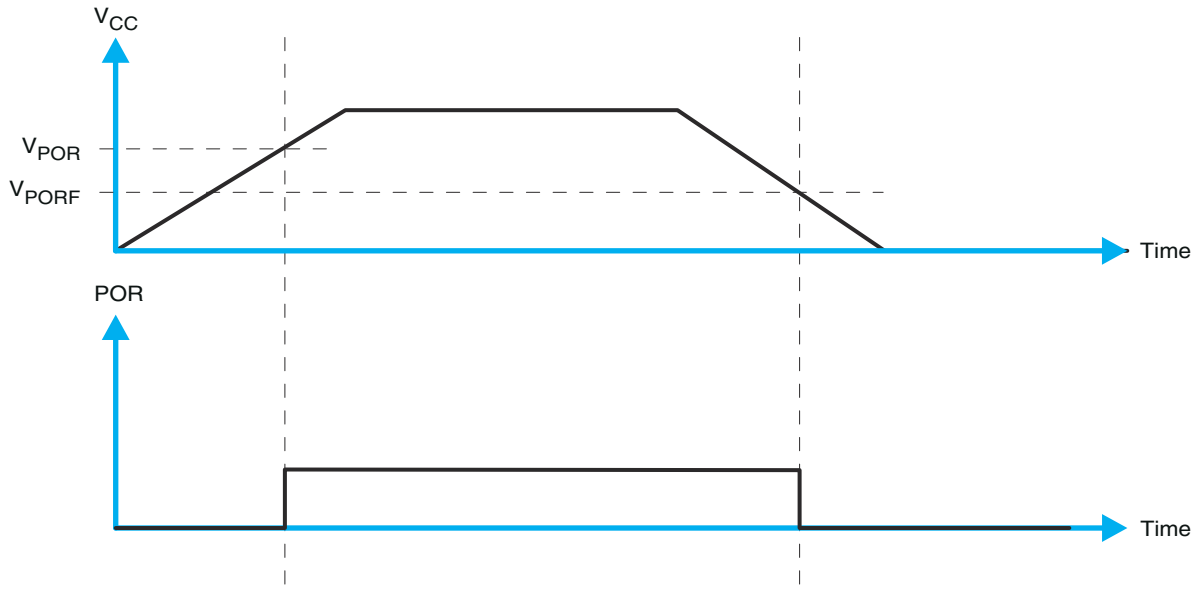


**Figure 8-9. $V_{POR}$**

## 8.4 Layout

### *8.4.1 Layout Guidelines*

For printed circuit board (PCB) layout of the PCF8574 device, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the PCF8574 device as possible. These best practices are shown in Figure 8-10.

For the layout example provided in Figure 8-10, it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (VCC) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to VCC or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 8-10.


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### 8.4.2 Layout Example

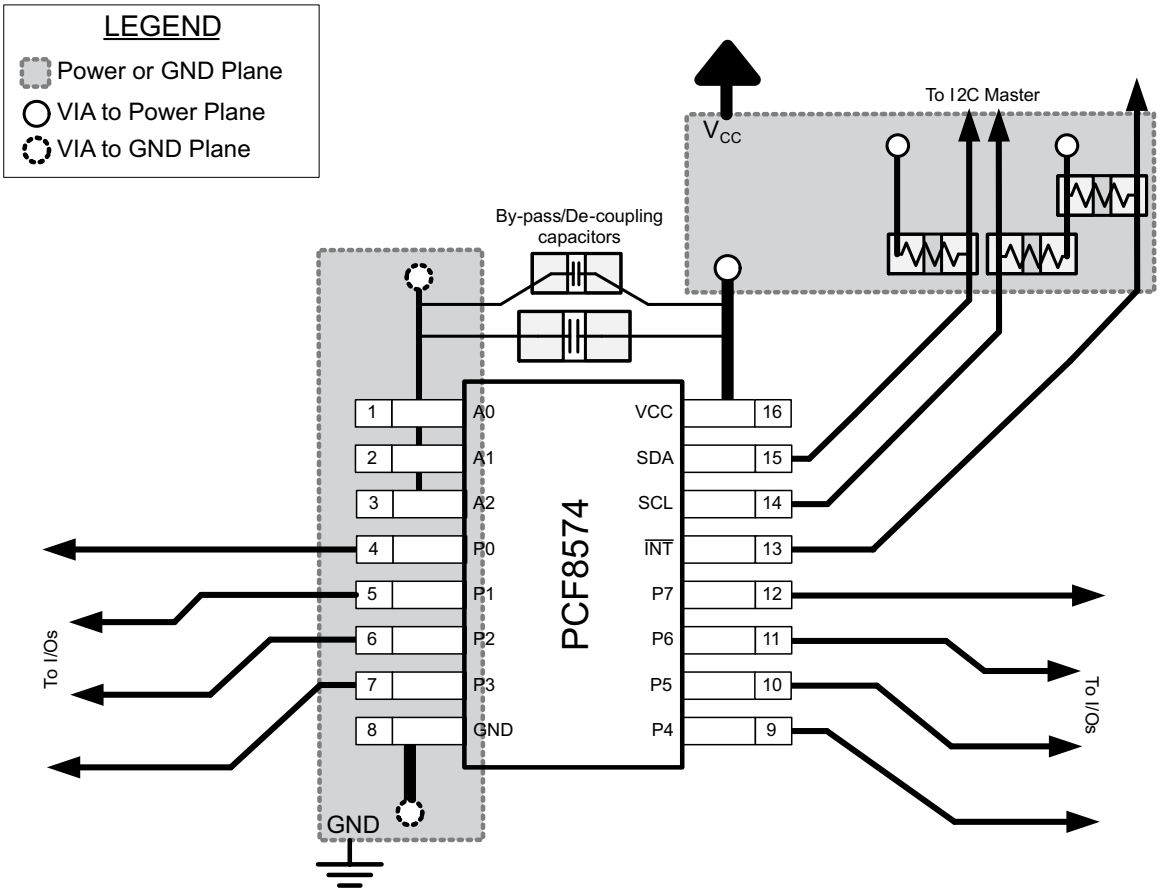


**Figure 8-10. Layout Example for PCF8574**

# 9 Device and Documentation Support

## 9.1 Documentation Support

### *9.1.1 Glossary*

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms and definitions.

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

| Changes from Revision J (March 2016) to Revision K (September 2024) | Page |
|---|---|
| • Changed all instances of legacy terminology to controller and target where $I^2C$ is mentioned | 1 |
| • Changed the Device Information table to the *Package Information* table | 1 |
| • Update *Absolute Max Voltage* from 7V to 6.5V | 4 |
| • Update *Thermal Information* for RGY, PW, RGT, N and DW packages | 4 |
| • Update $I_{OH}$ polarity and increase limit from -300µA to -310µA | 5 |
| • Removed footnote #2 from *Electrical Characteristics* | 5 |
| • Updated $I_{IHL}$ test condition | 5 |
| • Changed Spike filter limit from 100ns to 70ns max | 5 |
| • Changed Figure 7-3 | 14 |
| • Updated VPORF and VPORR values | 18 |

| Changes from Revision I (November 2015) to Revision J (March 2016) | Page |
|---|---|
| • Corrected part number in *Device Information* table | 1 |


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## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCF8574DGVR | ACTIVE | TVSOP | DGV | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PF574 | Samples |
| PCF8574DWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCF8574 | Samples |
| PCF8574N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | PCF8574N | Samples |
| PCF8574NE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | PCF8574N | Samples |
| PCF8574PW | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI | -40 to 85 | PF574 | |
| PCF8574PWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PF574 | Samples |
| PCF8574RGTR | ACTIVE | VQFN | RGT | 16 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ZWJ | Samples |
| PCF8574RGYR | ACTIVE | VQFN | RGY | 20 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PF574 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# GENERIC PACKAGE VIEW

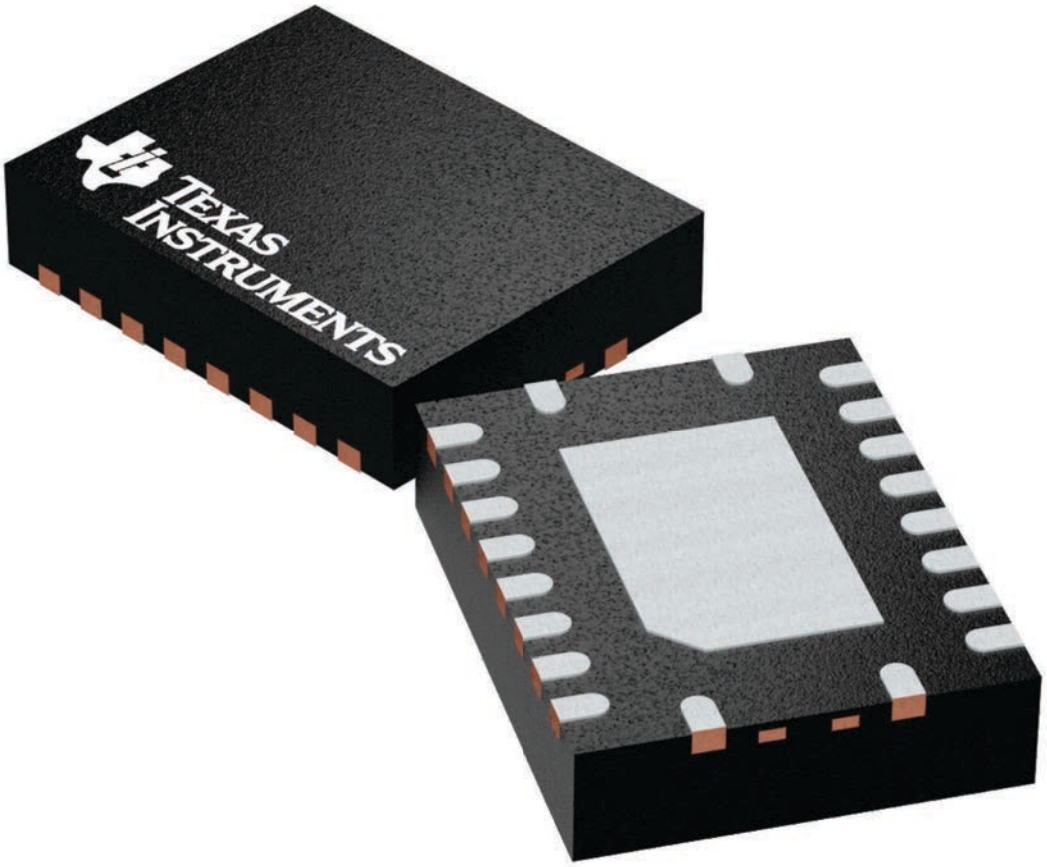
## RGY 20

## VQFN - 1 mm max height

**3.5 x 4.5, 0.5 mm pitch**

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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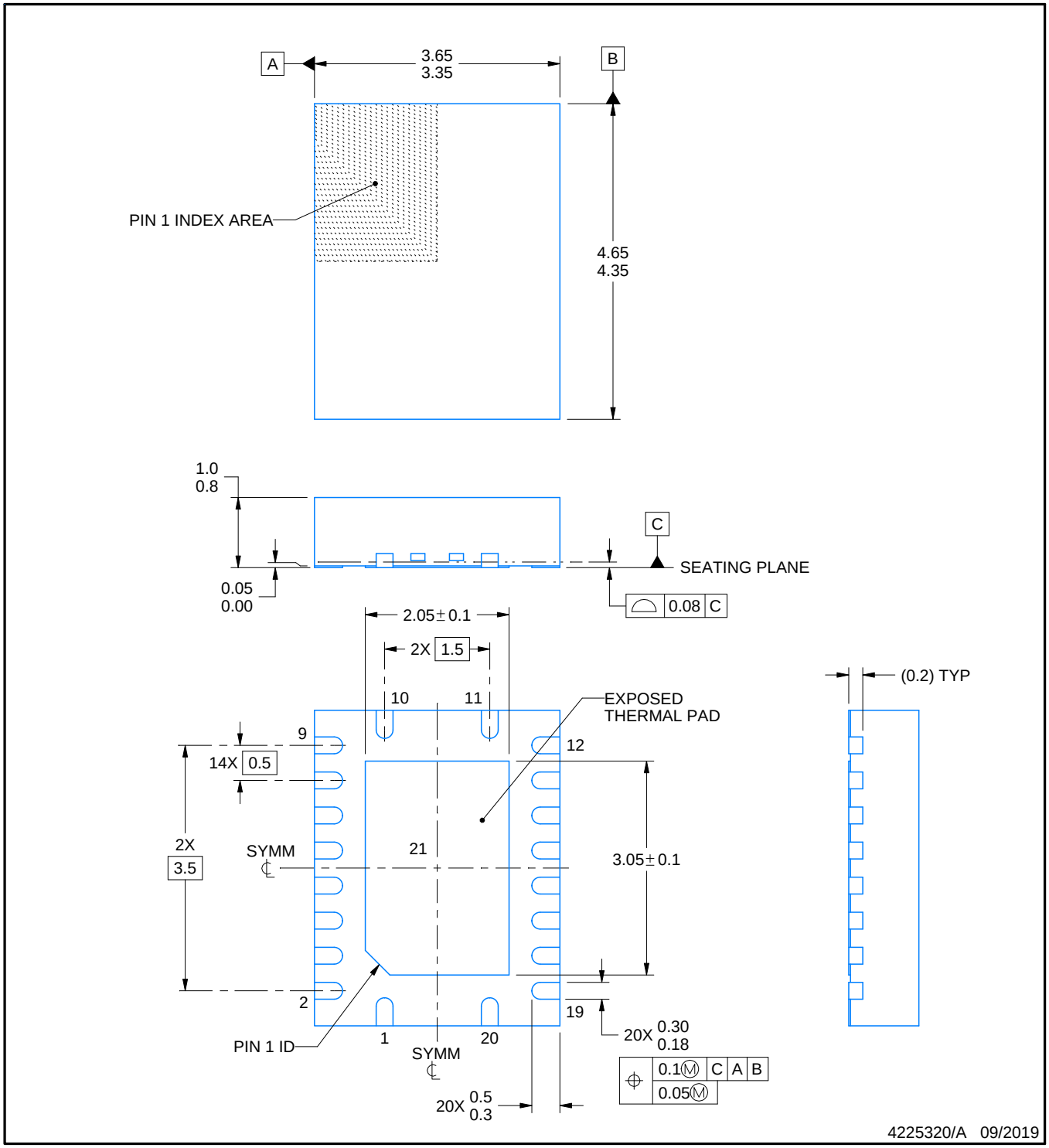
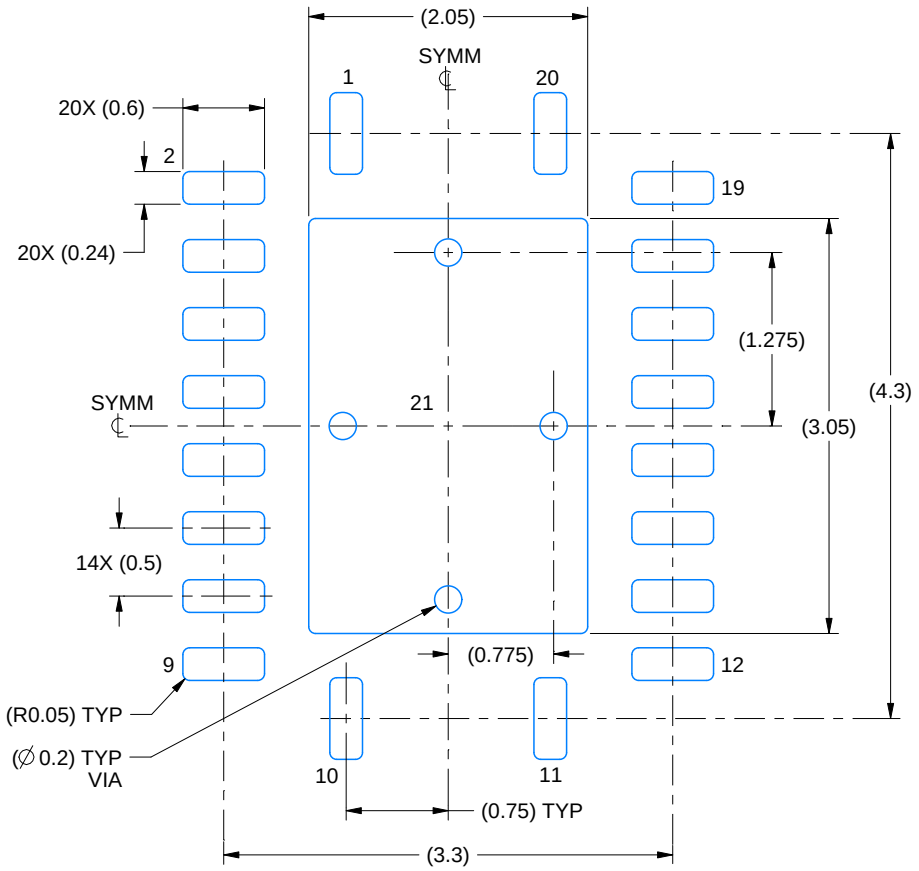
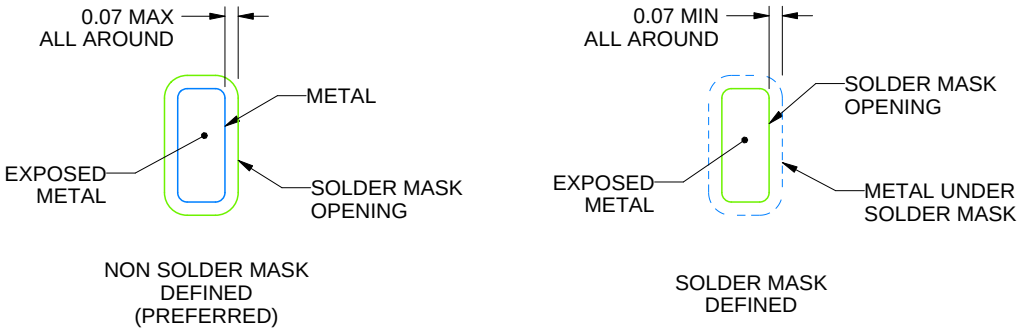



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X




SOLDER MASK DETAILS

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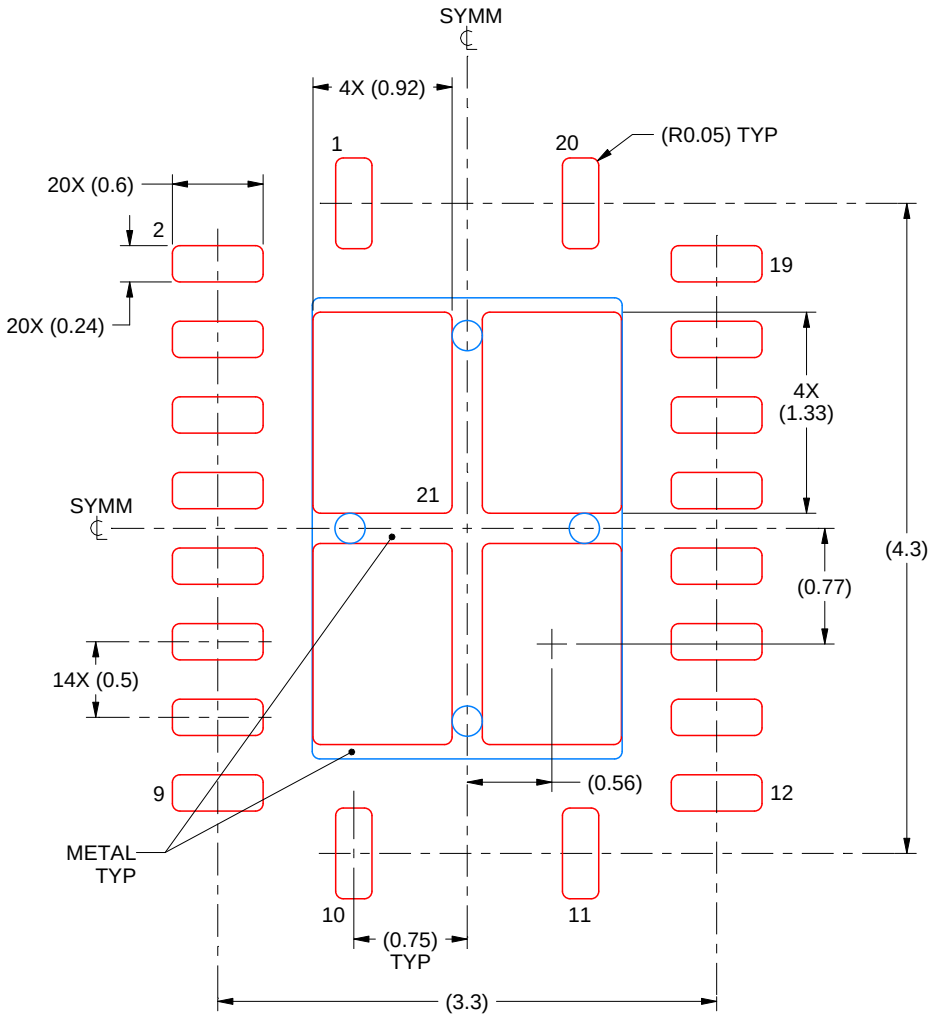
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# GENERIC PACKAGE VIEW

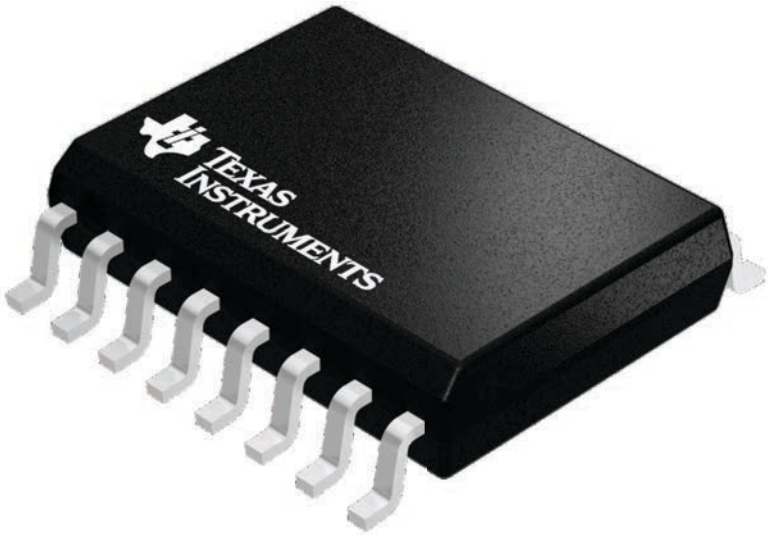
## DW 16

## SOIC - 2.65 mm max height

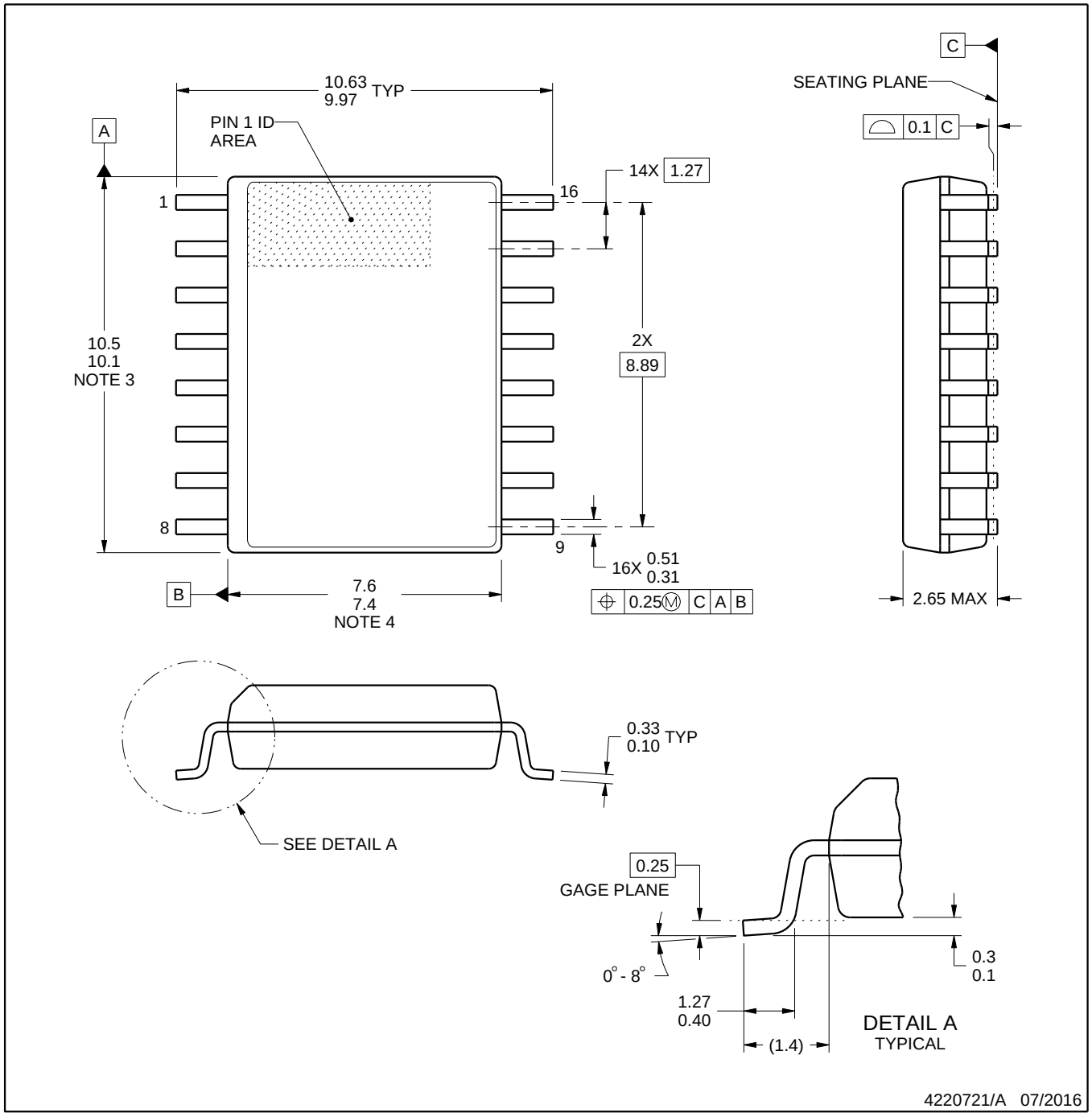
**7.5 x 10.3, 1.27 mm pitch**

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

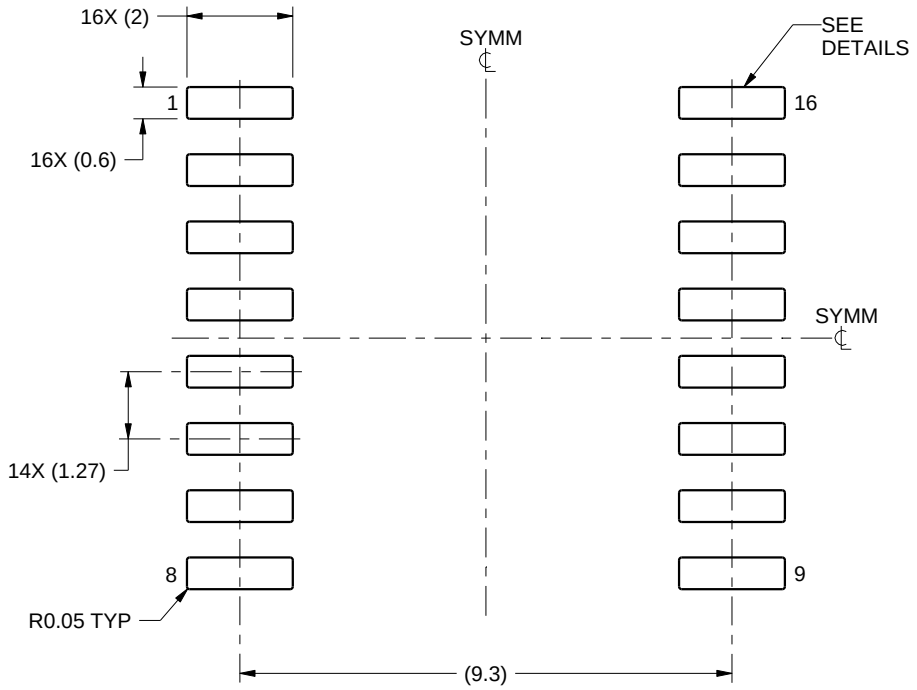



4224780/A

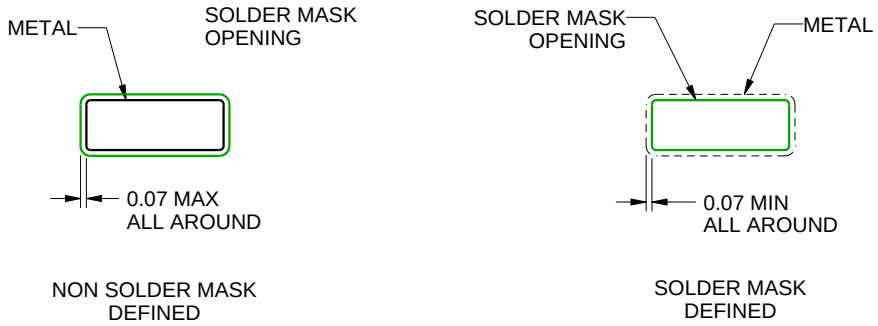



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:7X

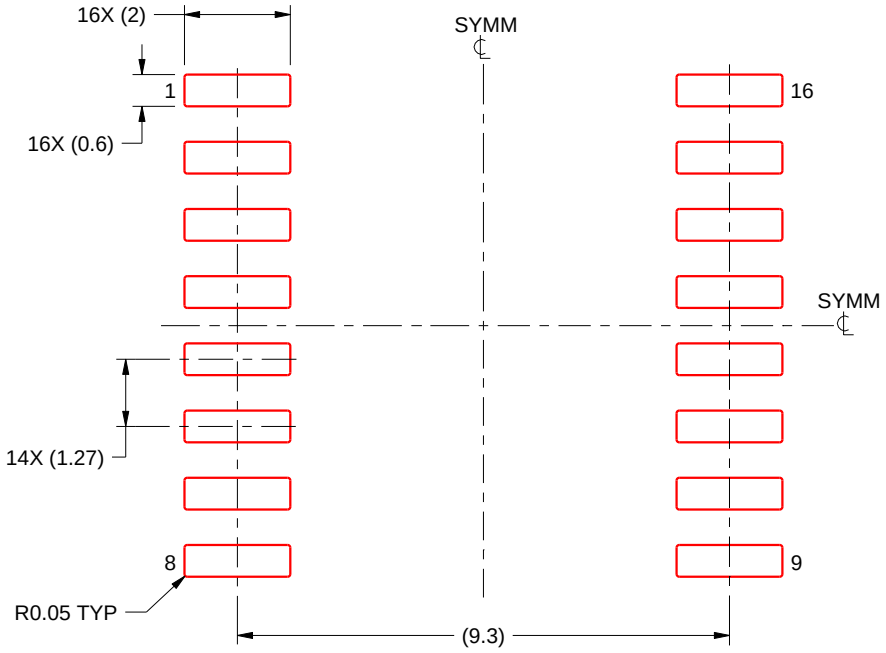



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

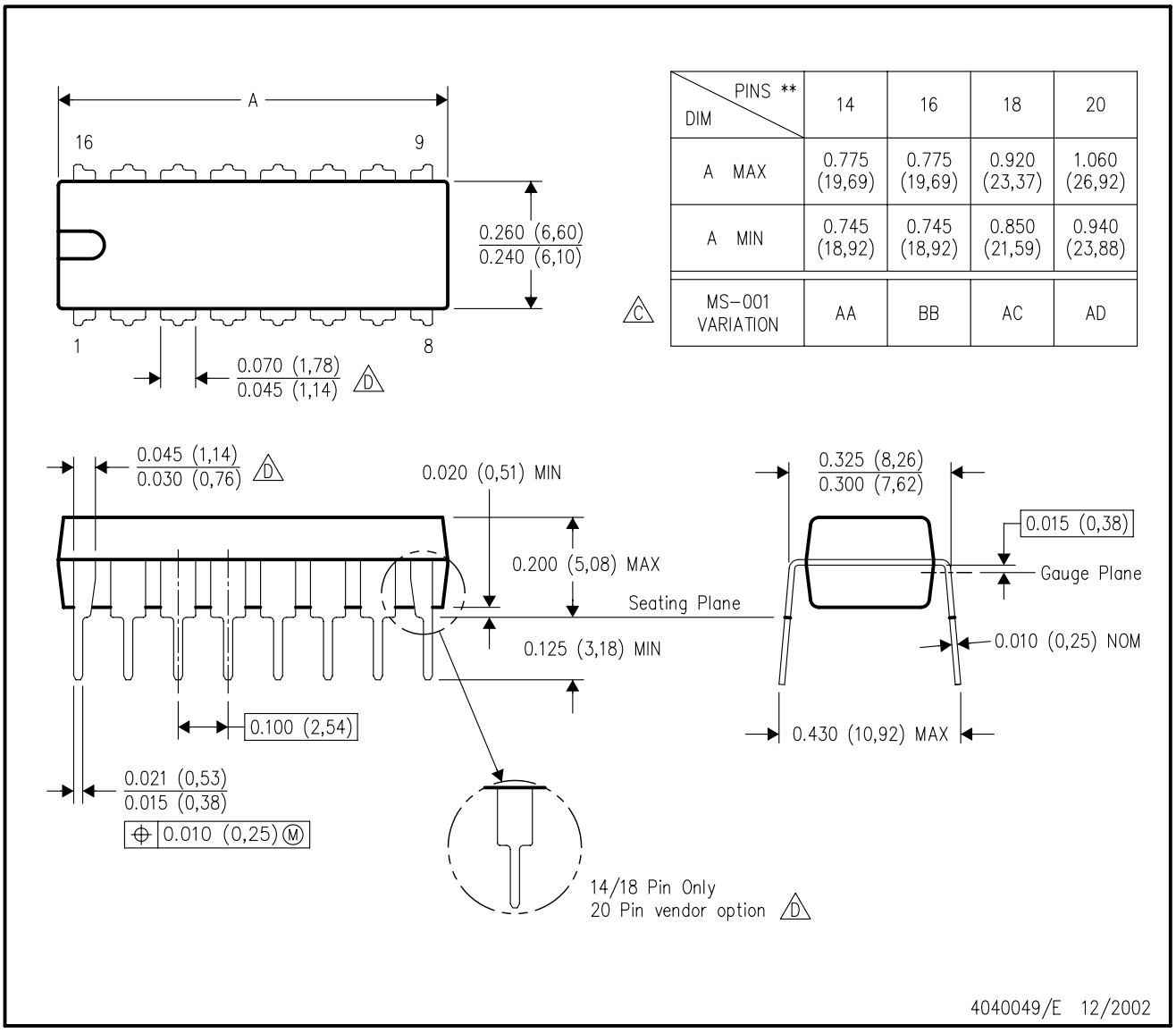
4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

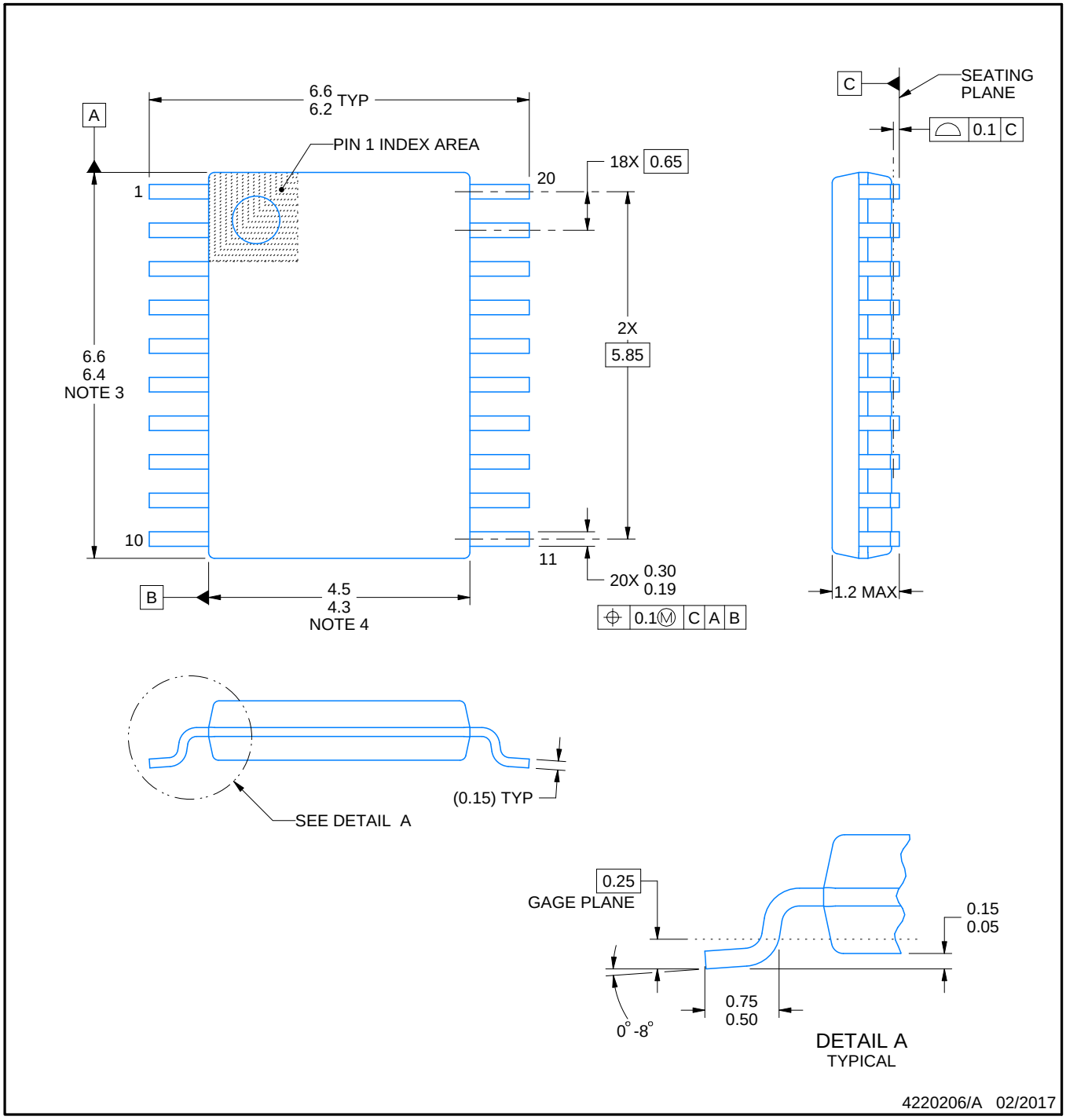
## N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



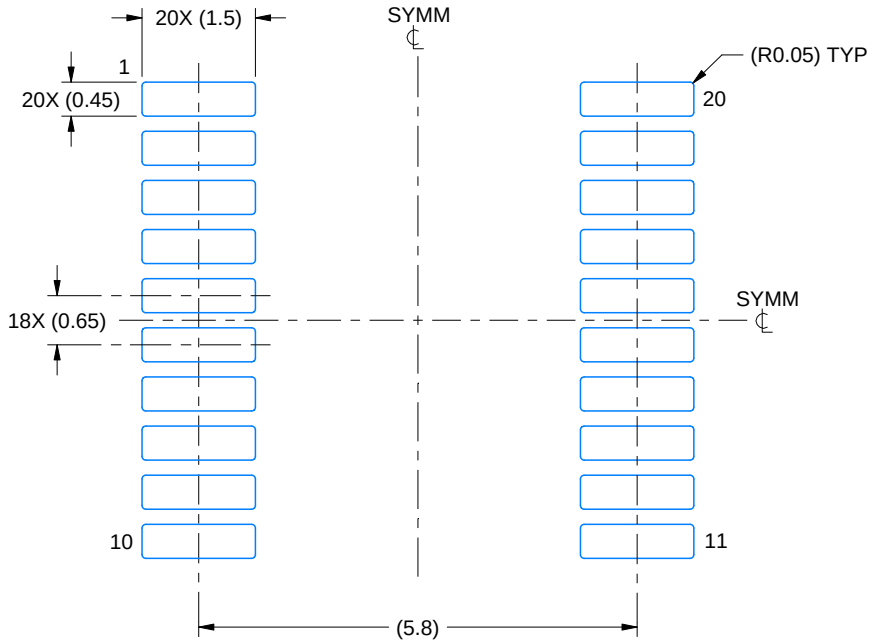

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

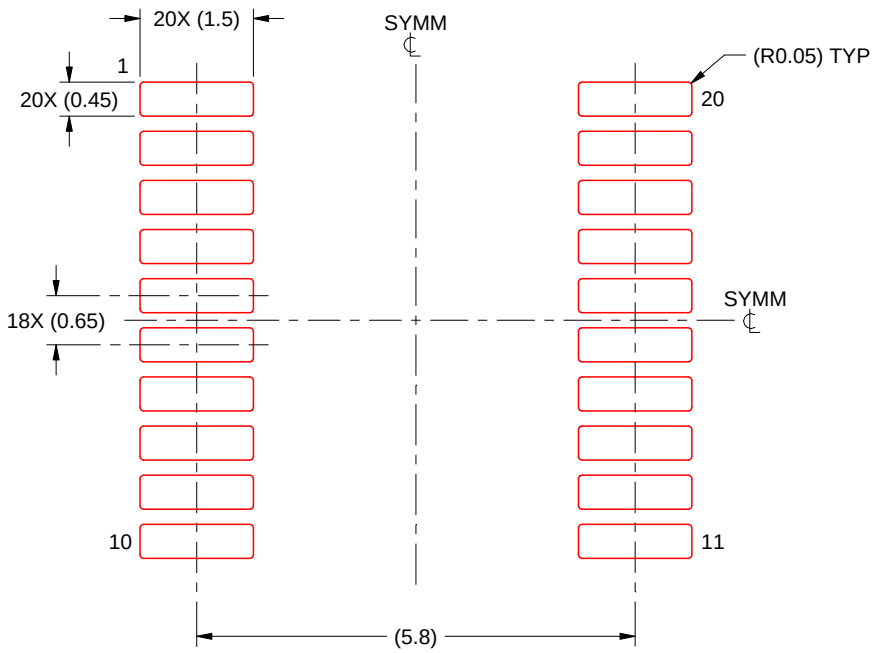
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

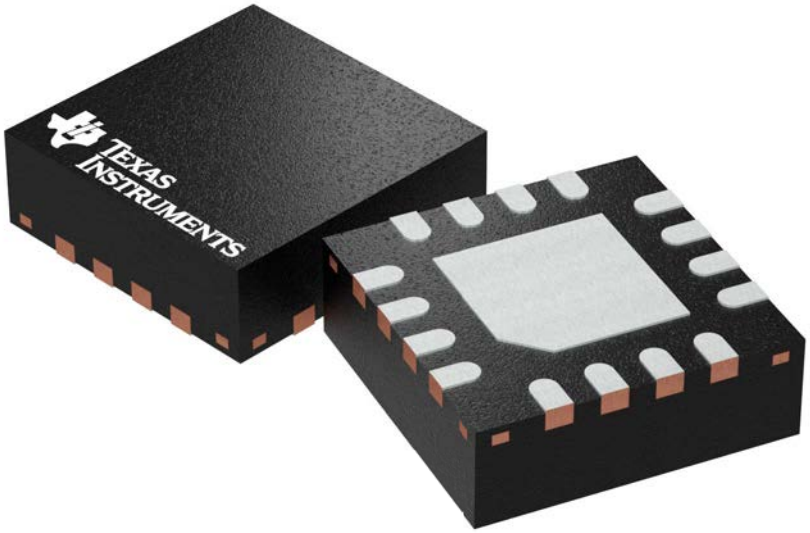
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# RGT 16

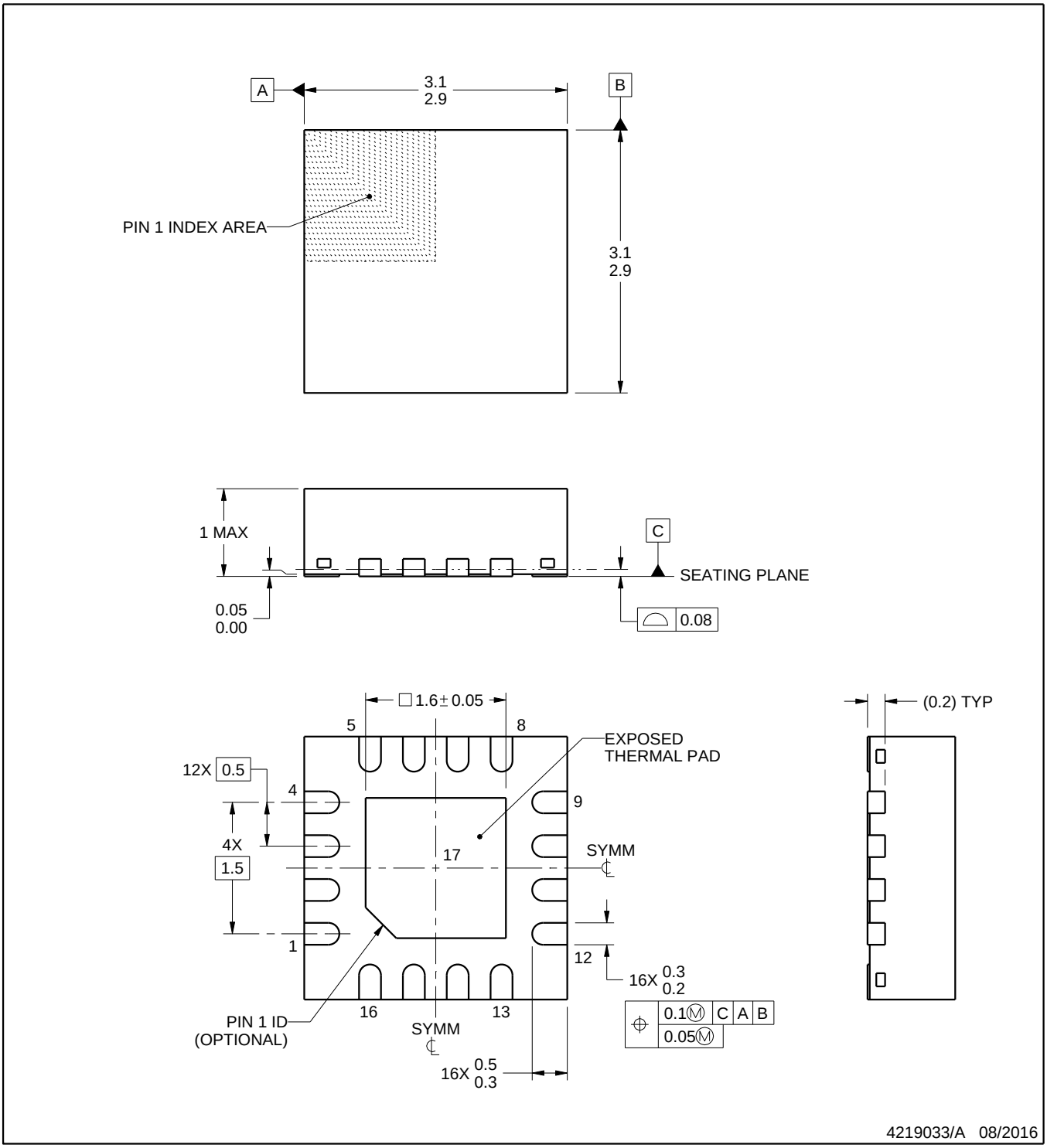
# VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



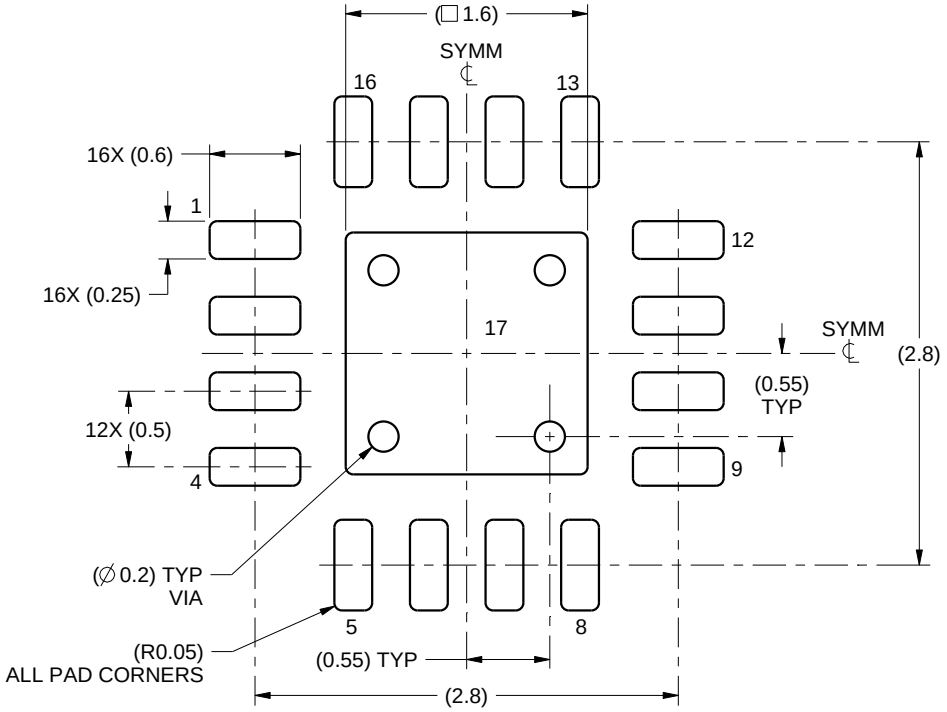

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/I

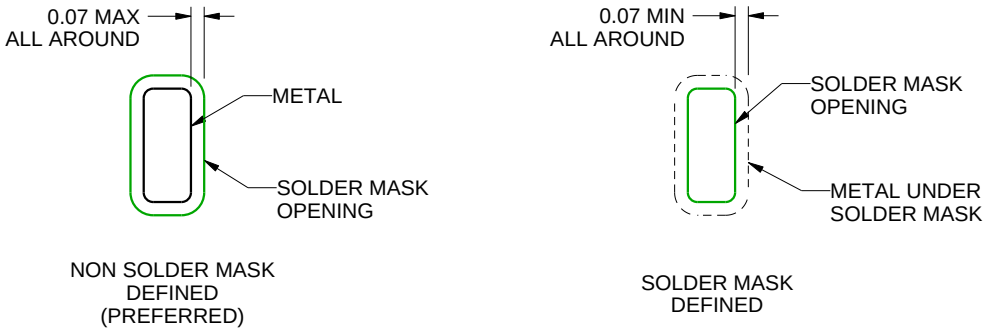



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:20X

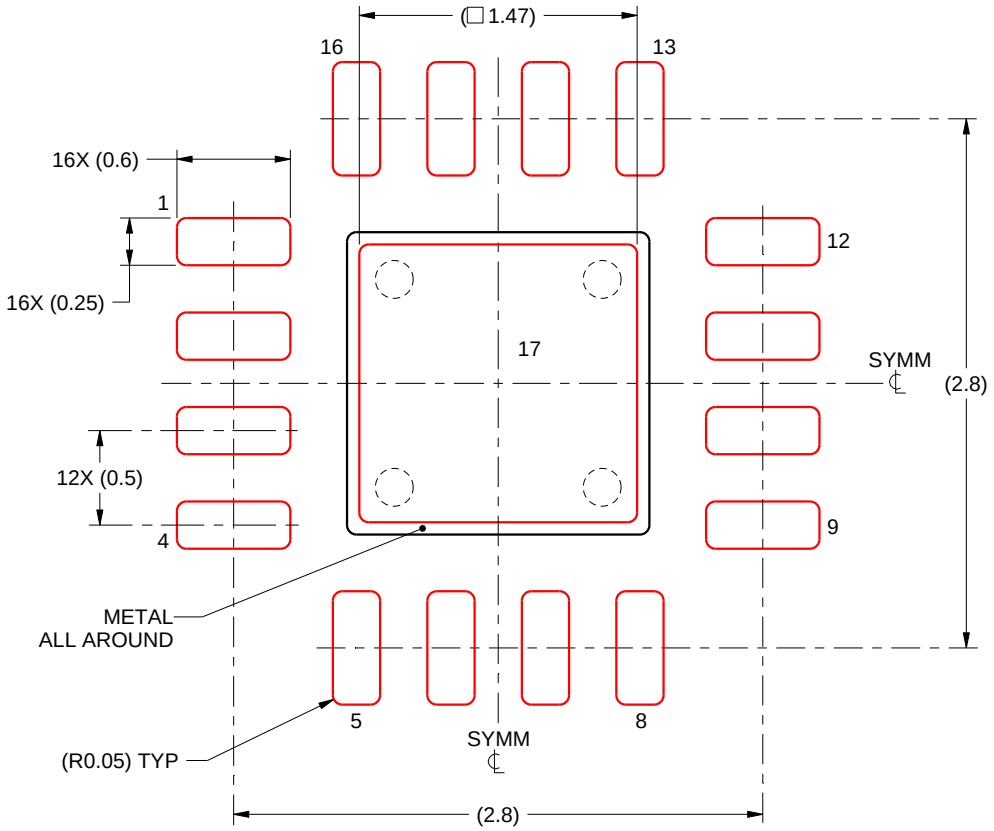



SOLDER MASK DETAILS

4219033/A 08/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219033/A 08/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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