24-BIT, 192-kHz SAMPLING, ADVANCED SEGMENT, AUDIO STEREO DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 24-Bit Resolution
- Analog Performance:
  - Dynamic Range:
    - 132 dB (9 V rms, Mono)
    - 129 dB (4.5 V rms, Stereo)
    - 127 dB (2 V rms, Stereo)
  - THD+N: 0.0004%
- Differential Current Output: 7.8 mA p-p
- 8× Oversampling Digital Filter:
  - Stop-Band Attenuation: –130 dB
  - Pass-Band Ripple: ±0.00001 dB
- Sampling Frequency: 10 kHz to 200 kHz
- System Clock: 128, 192, 256, 384, 512, or 768 fS With Autodetect
- Accepts 16-, 20-, and 24-Bit Audio Data
- PCM Data Formats: Standard, I²S, and Left-Justified
- DSD Format Interface Available
- Optional Interface to External Digital Filter or DSP Available
- TDMCA or Serial Port (SPI/I²C)
- User-Programmable Mode Controls:
  - Digital Attenuation: 0 dB to –120 dB, 0.5 dB/Step
  - Digital De-Emphasis
  - Digital Filter Rolloff: Sharp or Slow
  - Soft Mute
  - Zero Flag for Each Output
- Dual Supply Operation:
  - 5-V Analog, 3.3-V Digital
  - 5-V Tolerant Digital Inputs
  - Small 28-Lead SSOP Package

APPLICATIONS

- A/V Receivers
- SACD Player
- DVD Players
- HDTV Receivers
- Car Audio Systems
- Digital Multitrack Recorders
- Other Applications Requiring 24-Bit Audio

DESCRIPTION

The PCM1792 is a monolithic CMOS integrated circuit that includes stereo digital-to-analog converters and support circuitry in a small 28-lead SSOP package. The data converters use TI’s advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1792 provides balanced current outputs, allowing the user to optimize analog performance externally. The PCM1792 accepts PCM and DSD audio data formats, providing easy interfacing to audio DSP and decoder chips. The PCM1792 also accepts to interface external digital filter devices (DF1704, DF1706, PMD200). Sampling rates up to 200 kHz are supported. A full set of user-programmable functions is accessible through an SPI or I²C serial control port, which supports register write and readback functions. The PCM1792 also supports the time division multiplexed command and audio (TDMCA) data format.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>PACKAGE</th>
<th>PACKAGE CODE</th>
<th>OPERATION TEMPERATURE RANGE</th>
<th>PACKAGE MARKING</th>
<th>ORDERING NUMBER</th>
<th>TRANSPORT MEDIA</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCM1792DB</td>
<td>28-lead SSOP</td>
<td>28DB</td>
<td>-25°C to 85°C</td>
<td>PCM1792</td>
<td>PCM1792DB</td>
<td>Tube</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PCM1792DBR</td>
<td>Tape and reel</td>
</tr>
</tbody>
</table>

**ABSOLUTE MAXIMUM RATINGS**
over operating free-air temperature range unless otherwise noted

- **Supply voltage**: $V_{CC1}, V_{CC2L}, V_{CC2R}$
  - $V_{DD}$: $-0.3 \text{ V to } 6.5 \text{ V}$
  - $V_{DD}$: $-0.3 \text{ V to } 4 \text{ V}$
- **Supply voltage differences**: $V_{CC1}, V_{CC2L}$ and $V_{CC2R}$
  - $\pm 0.1 \text{ V}$
- **Ground voltage differences**: $AGND1, AGND2, AGND3L, AGND3R$, and $DGND$
  - $\pm 0.1 \text{ V}$
- **Digital input voltage**: $LRCK, DATA, BCK, SCK, MSEL, RST, MS(2), MDI, MC, MDO(2), ZEROL(2), ZEROR(2)$
  - $\pm 0.3 \text{ V to } 6.5 \text{ V}$
- **Analog input voltage**: $\pm 0.3 \text{ V to } (V_{DD} + 0.3 \text{ V}) < 4 \text{ V}$
- **Input current (any pins except supplies)**: $\pm 10 \text{ mA}$
- **Ambient temperature under bias**: $-40 \text{ °C to } 125 \text{ °C}$
- **Storage temperature**: $-55 \text{ °C to } 150 \text{ °C}$
- **Junction temperature**: $150 \text{ °C}$
- **Lead temperature (soldering)**: $260 \text{ °C, 5 s}$
- **Package temperature (IR reflow, peak)**: $250 \text{ °C}$

1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. Input mode or I$^2$C mode.
3. Output mode except for I$^2$C mode.

**ELECTRICAL CHARACTERISTICS**

- All specifications at $T_A = 25 \text{ °C}$, $V_{CC1} = V_{CC2L} = V_{CC2R} = 5 \text{ V}$, $f_S = 44.1 \text{ kHz}$, system clock = 256 $f_S$, and 24-bit data unless otherwise noted

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>PCM1792DB</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESOLUTION</td>
<td></td>
<td>24</td>
<td>Bits</td>
</tr>
<tr>
<td><strong>DATA FORMAT (PCM Mode)</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Audio data interface format</td>
<td>Standard, I$^2$S, left justified</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Audio data bit length</td>
<td>16-, 20-, 24-bit selectable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Audio data format</td>
<td>MSB first, 2s complement</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_S$ Sampling frequency</td>
<td>10 to 200 kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>System clock frequency</td>
<td>128, 192, 256, 384, 512, 768 $f_S$</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>DATA FORMAT (DSD Mode)</strong></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Audio data interface format</td>
<td>DSD (direct stream digital)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Audio data bit length</td>
<td>1 Bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_S$ Sampling frequency</td>
<td>2.8224 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>System clock frequency</td>
<td>2.8224 to 11.2896 MHz</td>
<td></td>
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</tr>
<tr>
<td><strong>DIGITAL INPUT/OUTPUT</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic family</td>
<td>TTL compatible</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$ Input logic level</td>
<td></td>
<td>2</td>
<td>VDC</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td></td>
<td>0.8</td>
<td></td>
</tr>
<tr>
<td>$I_{IH}$ Input logic current</td>
<td>$V_{IN} = V_{DD}$</td>
<td>10</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td></td>
<td>-10</td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$ Output logic level</td>
<td>$I_{OH} = -2 \text{ mA}$</td>
<td>2.4</td>
<td>VDC</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td></td>
<td>0.4</td>
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</tbody>
</table>

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input mode or I$^2$C mode.

(3) Output mode except for I$^2$C mode.
ELECTRICAL CHARACTERISTICS (Continued)

all specifications at $T_A = 25^\circ C$, $V_{CC1} = V_{CC2L} = V_{CC2R} = 5 \text{ V}$, $f_S = 44.1 \text{ kHz}$, system clock = 256 $f_S$, and 24-bit data unless otherwise noted

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>PCM1792DB</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td>DYNAMIC PERFORMANCE (PCM MODE, 2-V RMS OUTPUT)</td>
<td>$f_S = 44.1 \text{ kHz}$</td>
<td>0.0004%</td>
<td>0.0008%</td>
</tr>
<tr>
<td></td>
<td>$f_S = 96 \text{ kHz}$</td>
<td>0.0008%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_S = 192 \text{ kHz}$</td>
<td>0.0015%</td>
<td></td>
</tr>
<tr>
<td>THD+N at $V_{OUT} = 0 \text{ dB}$</td>
<td>$EIAJ, \text{ A-weighted, } f_S = 44.1 \text{ kHz}$</td>
<td>123</td>
<td>127</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>$EIAJ, \text{ A-weighted, } f_S = 96 \text{ kHz}$</td>
<td>127</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$EIAJ, \text{ A-weighted, } f_S = 192 \text{ kHz}$</td>
<td>127</td>
<td></td>
</tr>
<tr>
<td>Signal-to-noise ratio</td>
<td>$EIAJ, \text{ A-weighted, } f_S = 44.1 \text{ kHz}$</td>
<td>123</td>
<td>127</td>
</tr>
<tr>
<td></td>
<td>$EIAJ, \text{ A-weighted, } f_S = 96 \text{ kHz}$</td>
<td>127</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$EIAJ, \text{ A-weighted, } f_S = 192 \text{ kHz}$</td>
<td>127</td>
<td></td>
</tr>
<tr>
<td>Channel separation</td>
<td>$f_S = 44.1 \text{ kHz}$</td>
<td>120</td>
<td>123</td>
</tr>
<tr>
<td></td>
<td>$f_S = 96 \text{ kHz}$</td>
<td>122</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_S = 192 \text{ kHz}$</td>
<td>120</td>
<td></td>
</tr>
<tr>
<td>Level Linearity Error</td>
<td>$V_{OUT} = -120 \text{ dB}$</td>
<td>±1</td>
<td></td>
</tr>
<tr>
<td>DYNAMIC PERFORMANCE (PCM Mode, 4.5-V RMS Output)</td>
<td>$f_S = 44.1 \text{ kHz}$</td>
<td>0.0004%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_S = 96 \text{ kHz}$</td>
<td>0.0008%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_S = 192 \text{ kHz}$</td>
<td>0.0015%</td>
<td></td>
</tr>
<tr>
<td>THD+N at $V_{OUT} = 0 \text{ dB}$</td>
<td>$EIAJ, \text{ A-weighted, } f_S = 44.1 \text{ kHz}$</td>
<td>129</td>
<td></td>
</tr>
<tr>
<td>Dynamic range</td>
<td>$EIAJ, \text{ A-weighted, } f_S = 96 \text{ kHz}$</td>
<td>129</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$EIAJ, \text{ A-weighted, } f_S = 192 \text{ kHz}$</td>
<td>129</td>
<td></td>
</tr>
<tr>
<td>Signal-to-noise ratio</td>
<td>$EIAJ, \text{ A-weighted, } f_S = 44.1 \text{ kHz}$</td>
<td>129</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$EIAJ, \text{ A-weighted, } f_S = 96 \text{ kHz}$</td>
<td>129</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$EIAJ, \text{ A-weighted, } f_S = 192 \text{ kHz}$</td>
<td>129</td>
<td></td>
</tr>
<tr>
<td>Channel separation</td>
<td>$f_S = 44.1 \text{ kHz}$</td>
<td>124</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_S = 96 \text{ kHz}$</td>
<td>123</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_S = 192 \text{ kHz}$</td>
<td>121</td>
<td></td>
</tr>
<tr>
<td>DYNAMIC PERFORMANCE (MONO MODE)</td>
<td>$f_S = 44.1 \text{ kHz}$</td>
<td>0.0004%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_S = 96 \text{ kHz}$</td>
<td>0.0008%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_S = 192 \text{ kHz}$</td>
<td>0.0015%</td>
<td></td>
</tr>
<tr>
<td>THD+N at $V_{OUT} = 0 \text{ dB}$</td>
<td>$EIAJ, \text{ A-weighted, } f_S = 44.1 \text{ kHz}$</td>
<td>132</td>
<td></td>
</tr>
<tr>
<td>Dynamic range</td>
<td>$EIAJ, \text{ A-weighted, } f_S = 96 \text{ kHz}$</td>
<td>132</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$EIAJ, \text{ A-weighted, } f_S = 192 \text{ kHz}$</td>
<td>132</td>
<td></td>
</tr>
<tr>
<td>Signal-to-noise ratio</td>
<td>$EIAJ, \text{ A-weighted, } f_S = 44.1 \text{ kHz}$</td>
<td>132</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$EIAJ, \text{ A-weighted, } f_S = 96 \text{ kHz}$</td>
<td>132</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$EIAJ, \text{ A-weighted, } f_S = 192 \text{ kHz}$</td>
<td>132</td>
<td></td>
</tr>
</tbody>
</table>

(1) Filter condition:
- THD+N: 20-Hz HPF, 20-kHz apogee LPF
- Dynamic range: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted
- Signal-to-noise ratio: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted
- Channel separation: 20-Hz HPF, 20-kHz AES17 LPF
- Analog performance specifications are measured using the System Two™ Cascade audio measurement system by Audio Precision® in the averaging mode.

(2) Dynamic performance and dc accuracy are specified at the output of the postamplifier as shown in Figure 36.

(3) Dynamic performance and dc accuracy are specified at the output of the postamplifier as shown in Figure 37.

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Other trademarks are the property of their respective owners.
ELECTRICAL CHARACTERISTICS (Continued)
all specifications at $T_A = 25^\circ C$, $V_{CC1} = V_{CC2L} = V_{CC2R} = 5$ V, $f_S = 44.1$ kHz, system clock = $256 f_S$, and 24-bit data unless otherwise noted

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>PCM1792DB</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DSD MODE DYNAMIC PERFORMANCE</strong> $(1)$ $(2)$ $(44.1$ kHz, $64 f_S)$</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>THD+N at $f_S$</td>
<td>4.5 V rms</td>
<td>0.0005%</td>
<td></td>
</tr>
<tr>
<td>Dynamic range</td>
<td>$-60$ dB, EIAJ, A-weighted</td>
<td>128</td>
<td>dB</td>
</tr>
<tr>
<td>Signal-to-noise ratio</td>
<td>EIAJ, A-weighted</td>
<td>128</td>
<td>dB</td>
</tr>
<tr>
<td><strong>ANALOG OUTPUT</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain error</td>
<td>$-6$ $\pm$ 2 $6$ % of FSR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain mismatch, channel-to-channel</td>
<td>$-3$ $\pm$ 0.5 $3$ % of FSR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bipolar zero error</td>
<td>At BPZ</td>
<td>$-2$ $\pm$ 0.5 $2$ % of FSR</td>
<td></td>
</tr>
<tr>
<td>Output current</td>
<td>Full scale $(0$ dB)</td>
<td>7.8</td>
<td>mA p-p</td>
</tr>
<tr>
<td>Center current</td>
<td>At BPZ</td>
<td>$-6.2$</td>
<td>mA</td>
</tr>
<tr>
<td><strong>DIGITAL FILTER PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>De-emphasis error</td>
<td>$\pm$ 0.004 dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>FILTER CHARACTERISTICS–1: SHARP ROLL OFF</strong></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Pass band</td>
<td>$\pm$ 0.00001 dB</td>
<td>$0.454 f_S$</td>
<td></td>
</tr>
<tr>
<td>Stop band</td>
<td>$-3$ dB</td>
<td>$0.49 f_S$</td>
<td></td>
</tr>
<tr>
<td>Pass-band ripple</td>
<td>$0.546 f_S$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stop-band attenuation</td>
<td>Stop band $= 0.546 f_S$</td>
<td>$-130$ dB</td>
<td></td>
</tr>
<tr>
<td>Delay time</td>
<td>$55/f_S$ s</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>FILTER CHARACTERISTICS–2: SLOW ROLL OFF</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pass band</td>
<td>$\pm$ 0.04 dB</td>
<td>$0.254 f_S$</td>
<td></td>
</tr>
<tr>
<td>Stop band</td>
<td>$-3$ dB</td>
<td>$0.46 f_S$</td>
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<tr>
<td>Pass-band ripple</td>
<td>$0.732 f_S$</td>
<td></td>
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<tr>
<td>Stop-band attenuation</td>
<td>Stop band $= 0.732 f_S$</td>
<td>$-100$ dB</td>
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<tr>
<td>Delay time</td>
<td>$18/f_S$ s</td>
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</table>

$(1)$ Filter condition:
THD+N: 20-Hz HPF, 20-kHz apogee LPF
Dynamic range: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted
Signal-to-noise ratio: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted
Channel separation: 20-Hz HPF, 20-kHz AES17 LPF
Analog performance specifications are measured using the System Two Cascade audio measurement system by Audio Precision in the averaging mode.

$(2)$ Dynamic performance and dc accuracy are specified at the output of the postamplifier as shown in Figure 38.
ELECTRICAL CHARACTERISTICS (Continued)

all specifications at $T_A = 25^\circ C$, $V_{CC1} = V_{CC2L} = V_{CC2R} = 5$ V, $f_S = 44.1$ kHz, system clock $= 256f_S$, and 24-bit data unless otherwise noted

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>PCM1792DB</th>
<th>UNIT</th>
</tr>
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<tbody>
<tr>
<td>$V_{DD}$</td>
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<td>3.3</td>
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<tr>
<td>$V_{CC1}$</td>
<td>Voltage range</td>
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<tr>
<td>$V_{CC2L}$</td>
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<td>4.75</td>
<td>5</td>
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<tr>
<td>$V_{CC2R}$</td>
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</tr>
<tr>
<td>$I_{DD}$</td>
<td>$f_S = 44.1$ kHz</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td>$f_S = 96$ kHz</td>
<td>23</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_S = 192$ kHz</td>
<td>45</td>
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<tr>
<td>$I_{CC}$</td>
<td>$f_S = 44.1$ kHz</td>
<td>33</td>
<td>40</td>
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<td>$f_S = 96$ kHz</td>
<td>35</td>
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<td></td>
<td>$f_S = 192$ kHz</td>
<td>37</td>
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<tr>
<td>Power dissipation</td>
<td>$f_S = 44.1$ kHz</td>
<td>205</td>
<td>250</td>
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<td></td>
<td>$f_S = 96$ kHz</td>
<td>250</td>
<td></td>
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<tr>
<td></td>
<td>$f_S = 192$ kHz</td>
<td>335</td>
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TEMPERATURE RANGE

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>PCM1792DB</th>
<th>UNIT</th>
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</thead>
<tbody>
<tr>
<td>Operation</td>
<td>Temperature</td>
<td></td>
<td>–25</td>
</tr>
<tr>
<td>$\theta JA$</td>
<td>Thermal resistance</td>
<td>28-pin SSOP</td>
<td>100</td>
</tr>
</tbody>
</table>

---

(1) Input is BPZ data.

PIN ASSIGNMENTS

**PCM1792**

(TOP VIEW)

<table>
<thead>
<tr>
<th>ZEROL</th>
<th>1</th>
<th>28</th>
<th>VCC2L</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZEROR</td>
<td>2</td>
<td>27</td>
<td>AGND3L</td>
</tr>
<tr>
<td>MSEL</td>
<td>3</td>
<td>26</td>
<td>IOUTL−</td>
</tr>
<tr>
<td>LRCK</td>
<td>4</td>
<td>25</td>
<td>IOUTL+</td>
</tr>
<tr>
<td>DATA</td>
<td>5</td>
<td>24</td>
<td>AGND2</td>
</tr>
<tr>
<td>BCK</td>
<td>6</td>
<td>23</td>
<td>VCC1</td>
</tr>
<tr>
<td>SCK</td>
<td>7</td>
<td>22</td>
<td>VCOML</td>
</tr>
<tr>
<td>DGN1</td>
<td>8</td>
<td>21</td>
<td>VCOMR</td>
</tr>
<tr>
<td>VDD</td>
<td>9</td>
<td>20</td>
<td>IREF</td>
</tr>
<tr>
<td>MS</td>
<td>10</td>
<td>19</td>
<td>AGND1</td>
</tr>
<tr>
<td>MDI</td>
<td>11</td>
<td>18</td>
<td>IOUTR−</td>
</tr>
<tr>
<td>MC</td>
<td>12</td>
<td>17</td>
<td>IOUTR+</td>
</tr>
<tr>
<td>MDO</td>
<td>13</td>
<td>16</td>
<td>AGND3R</td>
</tr>
<tr>
<td>RST</td>
<td>14</td>
<td>15</td>
<td>VCC2R</td>
</tr>
</tbody>
</table>
## Terminal Functions

<table>
<thead>
<tr>
<th>TERMINAL NAME</th>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>AGND1</td>
<td>19</td>
<td>–</td>
<td>Analog ground (internal bias)</td>
</tr>
<tr>
<td>AGND2</td>
<td>24</td>
<td>–</td>
<td>Analog ground (internal bias)</td>
</tr>
<tr>
<td>AGND3L</td>
<td>27</td>
<td>–</td>
<td>Analog ground (L-channel DACFF)</td>
</tr>
<tr>
<td>AGND3R</td>
<td>16</td>
<td>–</td>
<td>Analog ground (R-channel DACFF)</td>
</tr>
<tr>
<td>BCK</td>
<td>6</td>
<td>I</td>
<td>Bit clock input&lt;sup&gt;(1)&lt;/sup&gt;</td>
</tr>
<tr>
<td>DATA</td>
<td>5</td>
<td>I</td>
<td>Serial audio data input for normal operation&lt;sup&gt;(1)&lt;/sup&gt;</td>
</tr>
<tr>
<td>DGN D</td>
<td>8</td>
<td>–</td>
<td>Digital ground</td>
</tr>
<tr>
<td>I&lt;sub&gt;L&lt;/sub&gt;OUT+</td>
<td>25</td>
<td>O</td>
<td>L-channel analog current output+</td>
</tr>
<tr>
<td>I&lt;sub&gt;L&lt;/sub&gt;OUT–</td>
<td>26</td>
<td>O</td>
<td>L-channel analog current output–</td>
</tr>
<tr>
<td>I&lt;sub&gt;R&lt;/sub&gt;OUT+</td>
<td>17</td>
<td>O</td>
<td>R-channel analog current output+</td>
</tr>
<tr>
<td>I&lt;sub&gt;R&lt;/sub&gt;OUT–</td>
<td>18</td>
<td>O</td>
<td>R-channel analog current output–</td>
</tr>
<tr>
<td>I&lt;sub&gt;REF&lt;/sub&gt;</td>
<td>20</td>
<td>–</td>
<td>Output current reference bias pin</td>
</tr>
<tr>
<td>LRCK</td>
<td>4</td>
<td>I</td>
<td>Left and right clock (f&lt;sub&gt;S&lt;/sub&gt;) input for normal operation&lt;sup&gt;(1)&lt;/sup&gt;</td>
</tr>
<tr>
<td>MC</td>
<td>12</td>
<td>I</td>
<td>Mode control clock input&lt;sup&gt;(1)&lt;/sup&gt;</td>
</tr>
<tr>
<td>MDI</td>
<td>11</td>
<td>I</td>
<td>Mode control data input&lt;sup&gt;(1)&lt;/sup&gt;</td>
</tr>
<tr>
<td>MDO</td>
<td>13</td>
<td>I/O</td>
<td>Mode control readback data output&lt;sup&gt;(3)&lt;/sup&gt;</td>
</tr>
<tr>
<td>MS</td>
<td>10</td>
<td>I/O</td>
<td>Mode control chip-select input&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
<tr>
<td>MSEL</td>
<td>3</td>
<td>I</td>
<td>I&lt;sub&gt;2&lt;/sub&gt;C/SPI select&lt;sup&gt;(1)&lt;/sup&gt;</td>
</tr>
<tr>
<td>RST</td>
<td>14</td>
<td>I</td>
<td>Reset&lt;sup&gt;(1)&lt;/sup&gt;</td>
</tr>
<tr>
<td>SCK</td>
<td>7</td>
<td>I</td>
<td>System clock input&lt;sup&gt;(1)&lt;/sup&gt;</td>
</tr>
<tr>
<td>V&lt;sub&gt;CC&lt;/sub&gt;1</td>
<td>23</td>
<td>–</td>
<td>Analog power supply, 5 V</td>
</tr>
<tr>
<td>V&lt;sub&gt;CC&lt;/sub&gt;2L</td>
<td>28</td>
<td>–</td>
<td>Analog power supply (L-channel DACFF), 5 V</td>
</tr>
<tr>
<td>V&lt;sub&gt;CC&lt;/sub&gt;2R</td>
<td>15</td>
<td>–</td>
<td>Analog power supply (R-channel DACFF), 5 V</td>
</tr>
<tr>
<td>V&lt;sub&gt;COM&lt;/sub&gt;L</td>
<td>22</td>
<td>–</td>
<td>L-channel internal bias decoupling pin</td>
</tr>
<tr>
<td>V&lt;sub&gt;COM&lt;/sub&gt;R</td>
<td>21</td>
<td>–</td>
<td>R-channel internal bias decoupling pin</td>
</tr>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>9</td>
<td>–</td>
<td>Digital power supply, 3.3 V</td>
</tr>
<tr>
<td>ZEROL</td>
<td>1</td>
<td>I/O</td>
<td>Zero flag for L-channel&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
<tr>
<td>ZEROR</td>
<td>2</td>
<td>I/O</td>
<td>Zero flag for R-channel&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
</tbody>
</table>

<sup>(1)</sup> Schmitt-trigger input, 5-V tolerant

<sup>(2)</sup> Schmitt-trigger input and output. 5-V tolerant input and CMOS output

<sup>(3)</sup> Schmitt-trigger input and output. 5-V tolerant input. In I<sub>2</sub>C mode, this pin becomes an open-drain 3-state output; otherwise, this pin is a CMOS output.
FUNCTIONAL BLOCK DIAGRAM
TYPICAL PERFORMANCE CURVES

DIGITAL FILTER

Digital Filter Response

Figure 1. Frequency Response, Sharp Rolloff

Figure 2. Pass-Band Ripple, Sharp Rolloff

Figure 3. Frequency Response, Slow Rolloff

Figure 4. Transition Characteristics, Slow Rolloff
De-Emphasis Filter

**Figure 5**

DE-EMPHASIS LEVEL vs FREQUENCY

![Graph of De-Emphasis Level vs Frequency for f_s = 32 kHz](image)

**Figure 6**

DE-EMPHASIS ERROR vs FREQUENCY

![Graph of De-Emphasis Error vs Frequency for f_s = 32 kHz](image)

**Figure 7**

DE-EMPHASIS LEVEL vs FREQUENCY

![Graph of De-Emphasis Level vs Frequency for f_s = 44.1 kHz](image)

**Figure 8**

DE-EMPHASIS ERROR vs FREQUENCY

![Graph of De-Emphasis Error vs Frequency for f_s = 44.1 kHz](image)
De-Emphasis Filter (Continued)

**Figure 9**

De-Emphasis Level vs Frequency

**Figure 10**

De-Emphasis Error vs Frequency

---

**Notes:**

- **f_S = 48 kHz**
- **De-Emphasis Level in dB**
- **De-Emphasis Error in dB**
ANALOG DYNAMIC PERFORMANCE

Supply Voltage Characteristics

**Figure 11**

TOTAL HARMONIC DISTORTION + NOISE vs SUPPLY VOLTAGE

- THD+N = Total Harmonic Distortion + Noise (%)
- VCC = Supply Voltage (V)
- fS = 48 kHz
- fS = 96 kHz
- fS = 192 kHz

**Figure 12**

DYNAMIC RANGE vs SUPPLY VOLTAGE

- Dynamic Range (dB)
- VCC = Supply Voltage (V)
- fS = 48 kHz
- fS = 96 kHz
- fS = 192 kHz

**Figure 13**

SIGNAL-to-NOISE RATIO vs SUPPLY VOLTAGE

- SNR = Signal-to-Noise Ratio (dB)
- VCC = Supply Voltage (V)
- fS = 48 kHz
- fS = 96 kHz
- fS = 192 kHz

**Figure 14**

CHANNEL SEPARATION vs SUPPLY VOLTAGE

- Channel Separation (dB)
- VCC = Supply Voltage (V)
- fS = 48 kHz
- fS = 96 kHz
- fS = 192 kHz

**NOTE:** PCM mode, $T_A = 25^\circ C$, $V_{DD} = 3.3$ V, measurement circuit is Figure 37 ($V_{OUT} = 4.5$ V rms).
Temperature Characteristics

**Figure 15**

TOTAL HARMONIC DISTORTION + NOISE vs FREE-AIR TEMPERATURE

---

**Figure 16**

DYNAMIC RANGE vs FREE-AIR TEMPERATURE

---

**Figure 17**

SIGNAL-to-NOISE RATIO vs FREE-AIR TEMPERATURE

---

**Figure 18**

CHANNEL SEPARATION vs FREE-AIR TEMPERATURE

---

NOTE: PCM mode, VDD = 3.3 V, VCC = 5 V, measurement circuit is Figure 37 (VOUT = 4.5 V rms).
Figure 19. −60-dB Output Spectrum, BW = 20 kHz

Figure 20. −60-dB Output Spectrum, BW = 100 kHz

NOTE: PCM mode, $f_S = 48$ kHz, 32,768 point 8 average, $T_A = 25^\circ$C, $V_{DD} = 3.3$ V, $V_{CC} = 5$ V, measurement circuit is Figure 37.

Figure 21. THD+N vs Input Level, PCM Mode

NOTE: PCM mode, $f_S = 48$ kHz, $T_A = 25^\circ$C, $V_{DD} = 3.3$ V, $V_{CC} = 5$ V, measurement circuit is Figure 37.
Figure 22. −60-dB Output Spectrum, DSD Mode

NOTE: DSD mode (FIR-4), 32,768 point 8 average, $T_A = 25^\circ C$, $V_{DD} = 3.3$ V, $V_{CC} = 5$ V, measurement circuit is Figure 38.

Figure 23. −150-dB Output Spectrum, DSD Mono Mode

NOTE: DSD mode (FIR-4), 32,768 point 8 average, $T_A = 25^\circ C$, $V_{DD} = 3.3$ V, $V_{CC} = 5$ V, measurement circuit is Figure 38.
SYSTEM CLOCK AND RESET FUNCTIONS

System Clock Input

The PCM1792 requires a system clock for operating the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input (pin 7). The PCM1792 has a system clock detection circuit that automatically senses if the system clock is operating between 128 $f_S$ and 768 $f_S$. Table 1 shows examples of system clock frequencies for common audio sampling rates. If the oversampling rate of the delta-sigma modulator is selected as 128 $f_S$, the system clock frequency is over 256 $f_S$.

Figure 24 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. One of the Texas Instruments’ PLL1700 family of multiclock generators is an excellent choice for providing the PCM1792 system clock.

### Table 1. System Clock Rates for Common Audio Sampling Frequencies

<table>
<thead>
<tr>
<th>SAMPLING FREQUENCY</th>
<th>128 $f_S$</th>
<th>192 $f_S$</th>
<th>256 $f_S$</th>
<th>384 $f_S$</th>
<th>512 $f_S$</th>
<th>768 $f_S$</th>
</tr>
</thead>
<tbody>
<tr>
<td>32 kHz</td>
<td>4.096 (1)</td>
<td>6.144 (1)</td>
<td>8.192</td>
<td>12.288</td>
<td>16.384</td>
<td>24.576</td>
</tr>
<tr>
<td>44.1 kHz</td>
<td>5.6488 (1)</td>
<td>8.4672</td>
<td>11.2896</td>
<td>16.9344</td>
<td>22.5792</td>
<td>33.8688</td>
</tr>
<tr>
<td>96 kHz</td>
<td>12.288</td>
<td>18.432</td>
<td>24.576</td>
<td>36.864</td>
<td>49.152 (1)</td>
<td>73.728 (1)</td>
</tr>
<tr>
<td>192 kHz</td>
<td>24.576</td>
<td>36.864</td>
<td>49.152 (1)</td>
<td>73.728 (1)</td>
<td>(2)</td>
<td>(2)</td>
</tr>
</tbody>
</table>

(1) This system clock rate is not supported in I2C fast mode.
(2) This system clock rate is not supported for the given sampling frequency.

![System Clock Timing Diagram](image)

Figure 24. System Clock Input Timing

Power-On and External Reset Functions

The PCM1792 includes a power-on reset function. Figure 25 shows the operation of this function. With $V_{DD} > 2$ V, the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time $V_{DD} > 2$ V. After the initialization period, the PCM1792 is set to its default reset state, as described in the MODE CONTROL REGISTERS section of this data sheet.

The PCM1792 also includes an external reset capability using the $RST$ input (pin 14). This allows an external controller or master reset circuit to force the PCM1792 to initialize to its default reset state.

Figure 26 shows the external reset operation and timing. The $RST$ pin is set to logic 0 for a minimum of 20 ns. The $RST$ pin is then set to a logic 1 state, thus starting the initialization sequence, which requires 1024 system clock periods. The external reset is especially useful in applications where there is a delay between the PCM1792 power up and system clock activation.
Reset

1024 System Clocks

Figure 25. Power-On Reset Timing

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>t(RST)</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Reset pulse duration, LOW

Figure 26. External Reset Timing
AUDIO DATA INTERFACE

Audio Serial Interface

The audio interface port is a 3-wire serial port. It includes LRCK (pin 4), BCK (pin 6), and DATA (pin 5). BCK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the serial shift register of the audio interface. Serial data is clocked into the PCM1792 on the rising edge of BCK. LRCK is the serial audio left/right word clock.

The PCM1792 requires the synchronization of LRCK and system clock, but does not need a specific phase relation between LRCK and system clock.

If the relationship between LRCK and system clock changes more than ±6 BCK, internal operation is initialized within 1/f_s and analog outputs are forced to the bipolar zero level until resynchronization between LRCK and system clock is completed.

PCM Audio Data Formats and Timing

The PCM1792 supports industry-standard audio data formats, including standard right-justified, I²S, and left-justified. The data formats are shown in Figure 28. Data formats are selected using the format bits, FMT[2:0], in control register 18. The default data format is 24-bit I²S. All formats require binary 2s complement, MSB-first audio data. Figure 27 shows a detailed timing diagram for the serial audio interface.

![Timing of Audio Interface](figure27.png)

---

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>t(BCY)</td>
<td></td>
<td>70</td>
<td>ns</td>
</tr>
<tr>
<td>t(BCL)</td>
<td>30</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t(BCH)</td>
<td>30</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t(BL)</td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t(LB)</td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t(DS)</td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t(DH)</td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>LRCK clock duty</td>
<td>50% ± 2 bit clocks</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 27. Timing of Audio Interface
(1) Standard Data Format (Right Justified); L-Channel = HIGH, R-Channel = LOW

Audio Data Word = 16-Bit

DATA  14 15 16 1 2 15 16

Audio Data Word = 20-Bit

DATA  18 19 20 1 2 19 20

Audio Data Word = 24-Bit

DATA  22 23 24 1 2 23 24

(2) Left Justified Data Format; L-Channel = HIGH, R-Channel = LOW

Audio Data Word = 24-Bit

DATA  1 2 23 24

(3) I²S Data Format; L-Channel = LOW, R-Channel = HIGH

Audio Data Word = 16-Bit

DATA  1 2 15 16

Audio Data Word = 24-Bit

DATA  1 2 23 24

Figure 28. Audio Data Input Formats
External Digital Filter Interface and Timing

The PCM1792 supports an external digital filter interface comprising a 3- or 4-wire synchronous serial port, which allows the use of an external digital filter. External filters include the Texas Instruments’ DF1704 and DF1706, the Pacific Microsonics PMD200, or a programmable digital signal processor.

In the external DF mode, LRCK (pin 4), BCK (pin 6) and DATA (pin 5) are defined as WDCK, the word clock; BCK, the bit clock; and DATA, the monaural data. The external digital filter interface is selected by using the DFTH bit of control register 20, which functions to bypass the internal digital filter of the PCM1792.

When the DFMS bit of control register 19 is set, the PCM1792 can process stereo data. In this case, ZEROL (pin 1) and ZEROR (pin 2) are defined as L-channel data and R-channel data, respectively.

Detailed information for the external digital filter interface mode is provided in the APPLICATION FOR EXTERNAL DIGITAL FILTER INTERFACE section of this data sheet.

Direct Stream Digital (DSD) Format Interface and Timing

The PCM1792 supports the DSD-format interface operation, which includes out-of-band noise filtering using an internal analog FIR filter. For DSD operation, SCK (pin 7) is redefined as BCK, DATA (pin 5) as DATAL (left channel audio data), and LRCK (pin 4) as DATAR (right channel audio data). BCK (pin 6) must be forced low in the DSD mode. The DSD-format interface is activated by setting the DSD bit of control register 20.

Detailed information for the DSD mode is provided in the APPLICATION FOR DSD-FORMAT (DSD MODE) INTERFACE section of this data sheet.

TDMCA Interface

The PCM1792 supports the time-division-multiplexed command and audio (TDMCA) data format to enable control of and communication with a number of external devices over a single serial interface.

Detailed information for the TDMCA format is provided in the TDMCA Format section of this data sheet.
FUNCTION DESCRIPTIONS

Zero Detect
The PCM1792 has a zero-detect function. When the PCM1792 detects the zero conditions as shown in Table 2, the PCM1792 sets ZEROL (pin 1) and ZEROR (pin 2) to HIGH.

Table 2. Zero Conditions

<table>
<thead>
<tr>
<th>MODE</th>
<th>DETECTING CONDITION AND TIME</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCM</td>
<td>DATA is continuously LOW for 1024 LRCKs.</td>
</tr>
<tr>
<td>External DF Mode</td>
<td>DATA is continuously LOW for 1024 WDCKs.</td>
</tr>
<tr>
<td>DSD DZ0</td>
<td>There are an equal number of 1s and 0s in every 8 bits of DSD input data for 200 ms.</td>
</tr>
<tr>
<td>DSD DZ1</td>
<td>The input data is 1001 0110 continuously for 200 ms.</td>
</tr>
</tbody>
</table>

Serial Control Interface
The PCM1792 supports SPI and I2C that sets mode control registers as shown in Table 4. This serial control interface is selected by MSEL (pin 3); SPI is activated when MSEL is set to LOW, and I2C is activated when MSEL is set to HIGH.

SPI Interface
The SPI interface is a 4-wire synchronous serial port which operates asynchronously to the serial audio interface and the system clock (SCK). The serial control interface is used to program and read the on-chip mode registers. The control interface includes MDO (pin 13), MDI (pin 11), MC (pin 12), and MS (pin 10). MDO is the serial data output, used to read back the values of the mode registers; MDI is the serial data input, used to program the mode registers; MC is the serial bit clock, used to shift data in and out of the control port, and MS is the mode control enable, used to enable the internal mode register access.

Register Read/Write Operation
All read/write operations for the serial control port use 16-bit data words. Figure 29 shows the control data word format. The most significant bit is the read/write (R/W) bit. For write operations, the R/W bit must be set to 0. For read operations, the R/W bit must be set to 1. There are seven bits, labeled IDX[6:0], that hold the register index (or address) for the read and write operations. The least significant eight bits, D[7:0], contain the data to be written to, or the data that was read from, the register specified by IDX[6:0].

Figure 30 shows the functional timing diagram for writing or reading the serial control port. MS is held at a logic 1 state until a register needs to be written or read. To start the register write or read cycle, MS is set to logic 0. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MDI and readback data on MDO. After the eighth clock cycle has completed, the data from the indexed-mode control register appears on MDO during the read operation. After the sixteenth clock cycle has completed, the data is latched into the indexed-mode control register during the write operation. To write or read subsequent data, MS must be set to 1 once.
Figure 29. Control Data Word Format for MDI

<table>
<thead>
<tr>
<th>Register Index (or Address)</th>
<th>Register Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W IDX6 IDX5 IDX4 IDX3 IDX2 IDX1 IDX0 D7 D6 D5 D4 D3 D2 D1 D0</td>
<td></td>
</tr>
</tbody>
</table>

Figure 30. Serial Control Format

NOTE: Bit 15 is used for selection of write or read. Setting R/W = 0 indicates a write, while R/W = 1 indicates a read. Bits 14–8 are used for the register address. Bits 7–0 are used for register data.

Figure 31. Control Interface Timing

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{MCY}$ MC pulse cycle time</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{MCL}$ MC low-level time</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{MCH}$ MC high-level time</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{MHH}$ MS high-level time</td>
<td>80</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{MSS}$ MS falling edge to MC rising edge</td>
<td>15</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{MSH}$ MS hold time(1)</td>
<td>15</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{MDH}$ MDI hold time</td>
<td>15</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{MDS}$ MDI setup time</td>
<td>15</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{MOS}$ MC falling edge to MDO stable</td>
<td>30</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

(1) MC rising edge for LSB to MS rising edge
I²C Interface

The PCM1792 supports the I²C serial bus and the data transmission protocol for standard and fast mode as a slave device. This protocol is explained in I²C specification 2.0.

In I²C mode, the control terminals are changed as follows.

<table>
<thead>
<tr>
<th>TERMINAL NAME</th>
<th>TDMCA NAME</th>
<th>PROPERTY</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>MS</td>
<td>ADR0</td>
<td>Input</td>
<td>I²C address 0</td>
</tr>
<tr>
<td>MDI</td>
<td>ADR1</td>
<td>Input</td>
<td>I²C address 1</td>
</tr>
<tr>
<td>MC</td>
<td>SCL</td>
<td>Input</td>
<td>I²C clock</td>
</tr>
<tr>
<td>MDO</td>
<td>SDA</td>
<td>Input/output</td>
<td>I²C data</td>
</tr>
</tbody>
</table>

### Slave Address

The PCM1792 has 7 bits for its own slave address. The first five bits (MSBs) of the slave address are factory preset to 10011. The next two bits of the address byte are the device select bits which can be user-defined by the ADR1 and ADR0 terminals. A maximum of four PCM1792s can be connected on the same bus at one time. Each PCM1792 responds when it receives its own slave address.

### Packet Protocol

A master device must control packet protocol, which consists of start condition, slave address, read/write bit, data if write or acknowledge if read, and stop condition. The PCM1792 supports only slave receivers and slave transmitters.

**Figure 32. Basic I²C Framework**
Write Register

A master can write to any PCM1792 registers using single or multiple accesses. The master sends a PCM1792 slave address with a write bit, a register address, and the data. If multiple access is required, the address is that of the starting register, followed by the data to be transferred. When the data are received properly, the index register is incremented by 1 automatically. When the index register reaches 0x7F, the next value is 0x0. When undefined registers are accessed, the PCM1792 does not send an acknowledgement. The Figure 33 is a diagram of the write operation.

<table>
<thead>
<tr>
<th>Transmitter</th>
<th>Data Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>M</td>
</tr>
<tr>
<td>St</td>
<td>Slave Address</td>
</tr>
</tbody>
</table>


Figure 33. Write Operation

Read Register

A master can read the PCM1792 register. The value of the register address is stored in an indirect index register in advance. The master sends a PCM1792 slave address with a read bit after storing the register address. Then the PCM1792 transfers the data which the index register points to. When the data are transferred during a multiple access, the index register is incremented by 1 automatically. (When first going into read mode immediately following a write, the index register is not incremented. The master can read the register that was previously written.) When the index register reaches 0x7F, the next value is 0x0. The PCM1792 outputs some data when the index register is 0x10 to 0x1F, even if it is not defined in Table 4. Figure 34 is a diagram of the read operation.

<table>
<thead>
<tr>
<th>Transmitter</th>
<th>Data Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>M</td>
</tr>
<tr>
<td>St</td>
<td>Slave Address</td>
</tr>
</tbody>
</table>


Figure 34. Read Operation

Noise Suppression

The PCM1792 incorporates noise suppression using the system clock (SCK). However, there must be no more than two noise spikes in 600 ns. The noise suppression works for SCK frequencies between 8 MHz and 40 MHz in fast mode. However, it works incorrectly in the following conditions.

**Case 1:**

1. \( t_{SCK} > 120\) ns \((t_{SCK}: \text{period of SCK})\)
2. \( t_{HI} + t_{D-HD} < t_{SCK} \times 5\)
3. Spike noise exists on the first half of the SCL HIGH pulse.
4. Spike noise exists on the SDA HIGH pulse just before SDA goes LOW.

When these conditions occur at the same time, the data is recognized as LOW.
Case 2:
1. \( t(\text{SCK}) > 120 \text{ ns} \)
2. \( t(\text{S–HD}) \text{ or } t(\text{RS–HD}) < t(\text{SCK}) \times 5 \)
3. Spike noise exists on both SCL and SDA during the hold time.

When these conditions occur at the same time, the PCM1792 fails to detect a start condition.

Case 3:
1. \( t(\text{SCK}) < 50 \text{ ns} \)
2. \( t(\text{SP}) > t(\text{SCK}) \)
3. Spike noise exists on SCL just after SCL goes LOW.
4. Spike noise exists on SDA just before SCL goes LOW.

When these conditions occur at the same time, the PCM1792 erroneously detects a start or stop condition.
TIMING DIAGRAM

Start

\( t_{(BUF)} \) \( t_{(D-SU)} \) \( t_{(D-HD)} \) \( t_{(SCL-R)} \) \( t_{(SCL-F)} \) \( t_{(LOW)} \) \( t_{(HI)} \) \( t_{(S-HD)} \) \( t_{(SCL-R1)} \) \( t_{(SCL-F)} \) \( t_{(SCL-R)} \) \( t_{(SCL-F)} \) \( t_{(P-SU)} \)

Repeated Start

Stop

\( t_{(BUF)} \) \( t_{(D-SU)} \) \( t_{(D-HD)} \) \( t_{(SCL-R)} \) \( t_{(SCL-F)} \) \( t_{(LOW)} \) \( t_{(HI)} \) \( t_{(S-HD)} \) \( t_{(SCL-R1)} \) \( t_{(SCL-F)} \) \( t_{(SCL-R)} \) \( t_{(SCL-F)} \) \( t_{(P-SU)} \)

TIMING CHARACTERISTICS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{(SCL)} )</td>
<td>SCL clock frequency</td>
<td>Standard</td>
<td>100</td>
<td>( kHz )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>400</td>
<td></td>
</tr>
<tr>
<td>( t_{(BUF)} )</td>
<td>Bus free time between stop and start conditions</td>
<td>Standard</td>
<td>4.7</td>
<td>( \mu s )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>1.3</td>
<td></td>
</tr>
<tr>
<td>( t_{(LOW)} )</td>
<td>Low period of the SCL clock</td>
<td>Standard</td>
<td>4.7</td>
<td>( \mu s )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>1.3</td>
<td></td>
</tr>
<tr>
<td>( t_{(HI)} )</td>
<td>High period of the SCL clock</td>
<td>Standard</td>
<td>4</td>
<td>( \mu s )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>600</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{(RS-SU)} )</td>
<td>Setup time for (repeated) start condition</td>
<td>Standard</td>
<td>4.7</td>
<td>( \mu s )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>600</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{(S-HD)} )</td>
<td>Hold time for (repeated) start condition</td>
<td>Standard</td>
<td>4</td>
<td>( \mu s )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>600</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{(D-SU)} )</td>
<td>Data setup time</td>
<td>Standard</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>( t_{(D-HD)} )</td>
<td>Data hold time</td>
<td>Standard</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{(SCL-R)} )</td>
<td>Rise time of SCL signal</td>
<td>Standard</td>
<td>20 + 0.1 ( C_B )</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>20 + 0.1 ( C_B )</td>
<td></td>
</tr>
<tr>
<td>( t_{(SCL-R1)} )</td>
<td>Rise time of SCL signal after a repeated start condition and after an acknowledge bit</td>
<td>Standard</td>
<td>20 + 0.1 ( C_B )</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>20 + 0.1 ( C_B )</td>
<td></td>
</tr>
<tr>
<td>( t_{(SCL-F)} )</td>
<td>Fall time of SCL signal</td>
<td>Standard</td>
<td>20 + 0.1 ( C_B )</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>20 + 0.1 ( C_B )</td>
<td></td>
</tr>
<tr>
<td>( t_{(SDA-R)} )</td>
<td>Rise time of SDA signal</td>
<td>Standard</td>
<td>20 + 0.1 ( C_B )</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>20 + 0.1 ( C_B )</td>
<td></td>
</tr>
<tr>
<td>( t_{(SDA-F)} )</td>
<td>Fall time of SDA signal</td>
<td>Standard</td>
<td>20 + 0.1 ( C_B )</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>20 + 0.1 ( C_B )</td>
<td></td>
</tr>
<tr>
<td>( t_{(P-SU)} )</td>
<td>Setup time for stop condition</td>
<td>Standard</td>
<td>4</td>
<td>( \mu s )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast</td>
<td>600</td>
<td>ns</td>
</tr>
<tr>
<td>( C_{(B)} )</td>
<td>Capacitive load for SDA and SCL line</td>
<td>Standard</td>
<td>400</td>
<td>pF</td>
</tr>
<tr>
<td>( t_{(SP)} )</td>
<td>Pulse duration of suppressed spike</td>
<td>Standard</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>( V_{NH} )</td>
<td>Noise margin at high level for each connected device (including hysteresis)</td>
<td>Standard</td>
<td>0.2 ( V_{DD} )</td>
<td>V</td>
</tr>
</tbody>
</table>
MODE CONTROL REGISTERS

User-Programmable Mode Controls

The PCM1792 includes a number of user-programmable functions which are accessed via mode control registers. The registers are programmed using the serial control interface, which was previously discussed in this data sheet. Table 3 lists the available mode-control functions, along with their default reset conditions and associated register index.

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>DEFAULT</th>
<th>REGISTER</th>
<th>BIT</th>
<th>PCM</th>
<th>DSD</th>
<th>DF BYPASS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital attenuation control</td>
<td>0 dB to –120 dB and mute, 0.5 dB step</td>
<td>0 dB</td>
<td>Register 16 ATL[7:0] (for L-ch)</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Attenuation load control</td>
<td>Disabled, enabled</td>
<td>Attenuation disabled</td>
<td>Register 18 ATLD</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input audio data format selection</td>
<td>16-, 20-, 24-bit standard (right-justified) format 24-bit MSB-first left-justified format 16-/24-bit I²S format</td>
<td>24-bit I²S format</td>
<td>Register 18 FMT[2:0]</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sampling rate selection for de-emphasis</td>
<td>Disabled, 44.1 kHz, 48 kHz, 32 kHz</td>
<td>De-emphasis disabled</td>
<td>Register 18 DMF[1:0]</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>De-emphasis control</td>
<td>Disabled, enabled</td>
<td>De-emphasis disabled</td>
<td>Register 18 DME</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Soft mute control</td>
<td>Mute disabled, enabled</td>
<td>Mute disabled</td>
<td>Register 18 MUTE</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output phase reversal</td>
<td>Normal, reverse</td>
<td>Normal</td>
<td>Register 19 REV</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Attenuation speed selection</td>
<td>×1 fₛ, ×(1/2)fₛ, ×(1/4)fₛ, ×(1/8)fₛ</td>
<td>×1 fₛ</td>
<td>Register 19 ATS[1:0]</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DAC operation control</td>
<td>Enabled, disabled</td>
<td>DAC operation enabled</td>
<td>Register 19 OPE</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stereo DF bypass mode select</td>
<td>Monaural, stereo</td>
<td>Monaural</td>
<td>Register 19 DFMS</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Digital filter rolloff selection</td>
<td>Sharp rolloff, slow rolloff</td>
<td>Sharp rolloff</td>
<td>Register 19 FLT</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Infinite zero mute control</td>
<td>Disabled, enabled</td>
<td>Disabled</td>
<td>Register 19 INZD</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>System reset control</td>
<td>Reset operation, normal operation</td>
<td>Normal operation</td>
<td>Register 20 SRST</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DSD interface mode control</td>
<td>Disabled, enabled</td>
<td>Disabled</td>
<td>Register 20 DSD</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Digital-filter bypass control</td>
<td>DF enabled, DF bypass</td>
<td>DF enabled</td>
<td>Register 20 DFTH</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Monaural mode selection</td>
<td>Stereo, monaural</td>
<td>Stereo</td>
<td>Register 20 MONO</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Channel selection for monaural mode data</td>
<td>L-channel, R-channel</td>
<td>L-channel</td>
<td>Register 20 CHSL</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Delta-sigma oversampling rate selection</td>
<td>×64 fₛ, ×128 fₛ, ×32 fₛ</td>
<td>×64 fₛ</td>
<td>Register 20 OS[1:0]</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCM zero output enable</td>
<td>Enabled</td>
<td>PCMZ</td>
<td>Register 21</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DSD zero output enable</td>
<td>Disabled</td>
<td>DZ[1:0]</td>
<td>Register 21</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Function available only for read</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Zero detection flag</td>
<td>Not zero = 0, Zero detected = 1</td>
<td></td>
<td>Register 22 ZFGL (for L-ch) ZFGR (for R-ch)</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Device ID (at TDMCA)</td>
<td></td>
<td></td>
<td>Register 23 ID[4:0]</td>
<td>yes</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) When in DSD mode, DMF[1:0] is defined as DSD filter (analog FIR) performance selection.
(2) When in DSD mode, OS[1:0] is defined as DSD filter (analog FIR) operation rate selection.
Register Map

The mode control register map is shown in Table 4. Registers 16–21 include an R/W bit, which determines whether a register read (R/W = 1) or write (R/W = 0) operation is performed. Registers 22 and 23 are read-only.

Table 4. Mode Control Register Map

<table>
<thead>
<tr>
<th>B15</th>
<th>B14</th>
<th>B13</th>
<th>B12</th>
<th>B11</th>
<th>B10</th>
<th>B9</th>
<th>B8</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register 16</td>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ATL7</td>
<td>ATL6</td>
</tr>
<tr>
<td>Register 17</td>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ATR7</td>
<td>ATR6</td>
</tr>
<tr>
<td>Register 18</td>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>REV</td>
<td>ATLD</td>
</tr>
<tr>
<td>Register 19</td>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>RSV</td>
<td>RSV</td>
</tr>
<tr>
<td>Register 20</td>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>RSV</td>
<td>SRST</td>
<td>RSV</td>
</tr>
<tr>
<td>Register 21</td>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>RSV</td>
<td>SLD</td>
<td>RSV</td>
</tr>
<tr>
<td>Register 22</td>
<td>R</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
</tr>
<tr>
<td>Register 23</td>
<td>R</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
</tr>
</tbody>
</table>

Register Definitions

<table>
<thead>
<tr>
<th>B15</th>
<th>B14</th>
<th>B13</th>
<th>B12</th>
<th>B11</th>
<th>B10</th>
<th>B9</th>
<th>B8</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register 16</td>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ATL7</td>
<td>ATL6</td>
</tr>
<tr>
<td>Register 17</td>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ATR7</td>
<td>ATR6</td>
</tr>
<tr>
<td>Register 18</td>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>REV</td>
<td>ATLD</td>
</tr>
<tr>
<td>Register 19</td>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>RSV</td>
<td>RSV</td>
</tr>
<tr>
<td>Register 20</td>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>RSV</td>
<td>SRST</td>
<td>RSV</td>
</tr>
<tr>
<td>Register 21</td>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>RSV</td>
<td>SLD</td>
<td>RSV</td>
</tr>
<tr>
<td>Register 22</td>
<td>R</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
</tr>
<tr>
<td>Register 23</td>
<td>R</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
</tr>
</tbody>
</table>

R/W: Read/Write Mode Select

When R/W = 0, a write operation is performed.
When R/W = 1, a read operation is performed.
Default value: 0

ATx[7:0]: Digital Attenuation Level Setting

These bits are available for read and write.
Default value: 1111 1111b

Each DAC output has a digital attenuator associated with it. The attenuator can be set from 0 dB to –120 dB, in 0.5-dB steps. Alternatively, the attenuator can be set to infinite attenuation (or mute).
The attenuation data for each channel can be set individually. However, the data load control (the ATLD bit of control register 18) is common to both attenuators. ATLD must be set to 1 in order to change an attenuator setting. The attenuation level can be set using the following formula:

\[
\text{Attenuation level (dB)} = 0.5 \text{ dB} \times (\text{ATx}[7:0]_{\text{DEC}} - 255)
\]

where: ATx[7:0]_{DEC} = 0 through 255

For ATx[7:0]_{DEC} = 0 through 14, the attenuator is set to infinite attenuation. The following table shows attenuation levels for various settings:

<table>
<thead>
<tr>
<th>ATx[7:0]</th>
<th>Decimal Value</th>
<th>Attenuation Level Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111 1111b</td>
<td>255</td>
<td>0 dB, no attenuation (default)</td>
</tr>
<tr>
<td>1111 1110b</td>
<td>254</td>
<td>–0.5 dB</td>
</tr>
<tr>
<td>1111 1101b</td>
<td>253</td>
<td>–1.0 dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0001 0000b</td>
<td>16</td>
<td>–119.5 dB</td>
</tr>
<tr>
<td>0000 1111b</td>
<td>15</td>
<td>–120.0 dB</td>
</tr>
<tr>
<td>0000 1110b</td>
<td>14</td>
<td>Mute</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0000 0000b</td>
<td>0</td>
<td>Mute</td>
</tr>
</tbody>
</table>


R/W: Read/Write Mode Select
When R/W = 0, a write operation is performed.
When R/W = 1, a read operation is performed.
Default value: 0

ATLD: Attenuation Load Control
This bit is available for read and write.
Default value: 0

| ATLD = 0 | Attenuation control disabled (default) |
| ATLD = 1 | Attenuation control enabled |

The ATLD bit is used to enable loading of the attenuation data contained in registers 16 and 17. When ATLD = 0, the attenuation settings remain at the previously programmed levels, ignoring new data loaded from registers 16 and 17. When ATLD = 1, attenuation data written to registers 16 and 17 is loaded normally.

FMT[2:0]: Audio Interface Data Format
These bits are available for read and write.
Default value: 101

For the external digital filter interface mode (DFTH mode), this register is operated as shown in the Application for Interfacing With an External Digital Filter section of this data sheet.

<table>
<thead>
<tr>
<th>FMT[2:0]</th>
<th>Audio Data Format Selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>16-bit standard format, right-justified data</td>
</tr>
<tr>
<td>001</td>
<td>20-bit standard format, right-justified data</td>
</tr>
<tr>
<td>010</td>
<td>24-bit standard format, right-justified data</td>
</tr>
<tr>
<td>011</td>
<td>24-bit MSB-first, left-justified format data</td>
</tr>
<tr>
<td>100</td>
<td>16-bit I²S format data</td>
</tr>
<tr>
<td>101</td>
<td>24-bit I²S format data (default)</td>
</tr>
<tr>
<td>110</td>
<td>Reserved</td>
</tr>
<tr>
<td>111</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

The FMT[2:0] bits are used to select the data format for the serial audio interface.

DMF[1:0]: Sampling Frequency Selection for the De-Emphasis Function
These bits are available for read and write.
Default value: 00

<table>
<thead>
<tr>
<th>DMF[1:0]</th>
<th>De-Emphasis Sampling Frequency Selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Disabled (default)</td>
</tr>
<tr>
<td>01</td>
<td>48 kHz</td>
</tr>
<tr>
<td>10</td>
<td>44.1 kHz</td>
</tr>
<tr>
<td>11</td>
<td>32 kHz</td>
</tr>
</tbody>
</table>

The DMF[1:0] bits are used to select the sampling frequency used by the digital de-emphasis function when it is enabled by setting the DME bit. The de-emphasis curves are shown in the TYPICAL PERFORMANCE CURVES section of this data sheet.

For the DSD mode, analog FIR filter performance can be selected using this register. Filter response plots are shown in the TYPICAL PERFORMANCE CURVES section of this data sheet. A register map is shown in the Configuration for the DSD Interface Mode section of this data sheet.
DME: Digital De-Emphasis Control
This bit is available for read and write.
Default value: 0

| DME = 0 | De-emphasis disabled (default) |
| DME = 1 | De-emphasis enabled |

The DME bit is used to enable or disable the de-emphasis function for both channels.

MUTE: Soft Mute Control
This bit is available for read and write.
Default value: 0

| MUTE = 0 | MUTE disabled (default) |
| MUTE = 1 | MUTE enabled |

The MUTE bit is used to enable or disable the soft mute function for both channels.

Soft mute is operated as a 256-step attenuator. The speed for each step to $-\infty$ dB (mute) is determined by the attenuation rate selected in the ATS register.

R/W: Read/Write Mode Select
When R/W = 0, a write operation is performed.
When R/W = 1, a read operation is performed.
Default value: 0

REV: Output Phase Reversal
This bit is available for read and write.
Default value: 0

| REV = 0 | Normal output (default) |
| REV = 1 | Inverted output |

The REV bit is used to invert the output phase for both channels.

ATS[1:0]: Attenuation Rate Select
These bits are available for read and write.
Default value: 00

| ATS[1:0] | Attenuation Rate Selection |
| 00 | LRCK/1 (default) |
| 01 | LRCK/2 |
| 10 | LRCK/4 |
| 11 | LRCK/8 |

The ATS[1:0] bits are used to select the rate at which the attenuator is decremented/incremented during level transitions.
OPE: DAC Operation Control
This bit is available for read and write.
Default value: 0

| OPE = 0 | DAC operation enabled (default) |
| OPE = 1 | DAC operation disabled |

The OPE bit is used to enable or disable the analog output for both channels. Disabling the analog outputs forces them to the bipolar zero level (BPZ) even if digital audio data is present on the input.

DFMS: Stereo DF Bypass Mode Select
This bit is available for read and write.
Default value: 0

| DFMS = 0 | Monaural (default) |
| DFMS = 1 | Stereo input enabled |

The DFMS bit is used to enable stereo operation in DF bypass mode. In the DF bypass mode, when DFMS is set to 0, the pin for the input data is DATA (pin 5) only, therefore the PCM1792 operates as a monaural DAC. When DFMS is set to 1, the PCM1792 can operate as a stereo DAC with inputs of L-channel and R-channel data on ZEROL (pin 1) and ZEROR (pin 2), respectively.

FLT: Digital Filter Rolloff Control
This bit is available for read and write.
Default value: 0

| FLT = 0 | Sharp rolloff (default) |
| FLT = 1 | Slow rolloff |

The FLT bit is used to select the digital filter rolloff characteristic. The filter responses for these selections are shown in the TYPICAL PERFORMANCE CURVES section of this data sheet.

INZD: Infinite Zero Detect Mute Control
This bit is available for read and write.
Default value: 0

| INZD = 0 | Infinite zero detect mute disabled (default) |
| INZD = 1 | Infinite zero detect mute enabled |

The INZD bit is used to enable or disable the zero detect mute function. Setting INZD to 1 forces muted analog outputs to hold a bipolar zero level when the PCM1792 detects a zero condition in both channels. The infinite zero detect mute function is disabled in the DSD mode.

R/W: Read/Write Mode Select
When R/W = 0, a write operation is performed.
When R/W = 1, a read operation is performed.
Default value: 0
SRST: System Reset Control
This bit is available for write only.
Default value: 0

<table>
<thead>
<tr>
<th>SRST</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Normal operation (default)</td>
</tr>
<tr>
<td>1</td>
<td>System reset operation (generate one reset pulse)</td>
</tr>
</tbody>
</table>

The SRST bit is used to reset the PCM1792 to the initial system condition.

DSD: DSD Interface Mode Control
This bit is available for read and write.
Default value: 0

<table>
<thead>
<tr>
<th>DSD</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>DSD interface mode disabled (default)</td>
</tr>
<tr>
<td>1</td>
<td>DSD interface mode enabled</td>
</tr>
</tbody>
</table>

The DSD bit is used to enable or disable the DSD interface mode.

DFTH: Digital Filter Bypass (or Through Mode) Control
This bit is available for read and write.
Default value: 0

<table>
<thead>
<tr>
<th>DFTH</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Digital filter enabled (default)</td>
</tr>
<tr>
<td>1</td>
<td>Digital filter bypassed for external digital filter</td>
</tr>
</tbody>
</table>

The DFTH bit is used to enable or disable the external digital filter interface mode.

MONO: Monaural Mode Selection
This bit is available for read and write.
Default value: 0

<table>
<thead>
<tr>
<th>MONO</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Stereo mode (default)</td>
</tr>
<tr>
<td>1</td>
<td>Monaural mode</td>
</tr>
</tbody>
</table>

The MONO function is used to change operation mode from the normal stereo mode to the monaural mode. When the monaural mode is selected, both DACs operate in a balanced mode for one channel of audio input data. Channel selection is available for L-channel or R-channel data, determined by the CHSL bit as described immediately following.

CHSL: Channel Selection for Monaural Mode
This bit is available for read and write.
Default value: 0

This bit is available when MONO = 1.

<table>
<thead>
<tr>
<th>CHSL</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>L-channel selected (default)</td>
</tr>
<tr>
<td>1</td>
<td>R-channel selected</td>
</tr>
</tbody>
</table>

The CHSL bit selects L-channel or R-channel data to be used in monaural mode.
OS[1:0]: Delta-Sigma Oversampling Rate Selection

These bits are available for read and write.

Default value: 00

<table>
<thead>
<tr>
<th>OS[1:0]</th>
<th>Operation Speed Select</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>64 times $f_S$ (default)</td>
</tr>
<tr>
<td>01</td>
<td>32 times $f_S$</td>
</tr>
<tr>
<td>10</td>
<td>128 times $f_S$</td>
</tr>
<tr>
<td>11</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

The OS bits are used to change the oversampling rate of delta-sigma modulation. Use of this function enables the designer to stabilize the conditions at the post low-pass filter for different sampling rates. As an application example, programming to set 128 times in 44.1-kHz operation, 64 times in 96-kHz operation, and 32 times in 192-kHz operation allows the use of only a single type (cutoff frequency) of post low-pass filter. The 128 $f_S$ oversampling rate is not available at sampling rates above 100 kHz. If the 128-$f_S$ oversampling rate is selected, a system clock of more than 256 $f_S$ is required.

In DSD mode, these bits are used to select the speed of the bit clock for DSD data coming into the analog FIR filter.

R/W: Read/Write Mode Select

When R/W = 0, a write operation is performed.

When R/W = 1, a read operation is performed.

Default value: 0

DZ[1:0]: DSD Zero Output Enable

These bits are available for read and write.

Default value: 00

<table>
<thead>
<tr>
<th>DZ[1:0]</th>
<th>Zero Output Enable</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Disabled (default)</td>
</tr>
<tr>
<td>01</td>
<td>Even pattern detect</td>
</tr>
<tr>
<td>1x</td>
<td>96_H pattern detect</td>
</tr>
</tbody>
</table>

The DZ bits are used to enable or disable the output zero flags, and to select the zero pattern in the DSD mode.

PCMZ: PCM Zero Output Enable

These bits are available for read and write.

Default value: 1

<table>
<thead>
<tr>
<th>PCMZ</th>
<th>PCM zero output enable</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>PCM zero output disabled</td>
</tr>
<tr>
<td>1</td>
<td>PCM zero output enabled (default)</td>
</tr>
</tbody>
</table>

The PCMZ bit is used to enable or disable the output zero flags in the PCM mode and the external DF mode.

R: Read Mode Select

Value is always 1, specifying the readback mode.
ZFGx: Zero-Detection Flag

Where x = L or R, corresponding to the DAC output channel. These bits are available only for readback.

Default value: 00

<table>
<thead>
<tr>
<th>ZFGx</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZFGx = 0</td>
<td>Not zero</td>
</tr>
<tr>
<td>ZFGx = 1</td>
<td>Zero detected</td>
</tr>
</tbody>
</table>

These bits show zero conditions. Their status is the same as that of the zero flags at ZEROL (pin 1) and ZEROR (pin 2). See Zero Detect in the FUNCTION DESCRIPTIONS section.

R: Read Mode Select

Value is always 1, specifying the readback mode.

ID[4:0]: Device ID

The ID[4:0] bits hold a device ID in the TDMCA mode.

TYPICAL CONNECTION DIAGRAM IN PCM MODE

Figure 35. Typical Application Circuit for Standard PCM Audio Operation
APPLICATION INFORMATION

APPLICATION CIRCUIT

The design of the application circuit is very important in order to actually realize the high S/N ratio of which the PCM1792 is capable. This is because noise and distortion that are generated in an application circuit are not negligible.

In the circuit of Figure 36, the output level is 2 V rms and 127 dB S/N is achieved.

The circuit of Figure 37 can realize the highest performance. In this case the output level is set to 4.5 V rms and 129 dB S/N is achieved (stereo mode). In monaural mode, if the output of the L-channel and R-channel is used as a balanced output, 132 dB S/N is achieved (see Figure 39).

Figure 38 shows a circuit for the DSD mode, which is a 4th-order LPF in order to reduce the out-of-band noise.

I/V Section

The current of the PCM1792 on each of the output pins (I_{OUTL+}, I_{OUTL−}, I_{OUTR+}, I_{OUTR−}) is 7.8 mA p-p at 0 dB (full scale). The voltage output level of the I/V converter (Vi) is given by following equation:

\[ V_i = 7.8 \text{ mA p-p} \times R_f \]  

\( R_f \) : feedback resistance of I/V converter

An NE5534 operational amplifier is recommended for the I/V circuit to obtain the specified performance. Dynamic performance such as the gain bandwidth, settling time, and slew rate of the operational amplifier affects the audio dynamic performance of the I/V section.

Differential Section

The PCM1792 voltage outputs are followed by differential amplifier stages, which sum the differential signals for each channel, creating a single-ended I/V op-amp output. In addition, the differential amplifiers provide a low-pass filter function.

The operational amplifier recommended for the IV circuit is the NE5534, and the operational amplifier recommended for the differential circuit is the Linear Technology LT1028, because its input noise is low.
Figure 36. Measurement Circuit for PCM, $V_{OUT} = 2$ V rms
Figure 37. Measurement Circuit for PCM, $V_{OUT} = 4.5$ V rms
Figure 38. Measurement Circuit for DSD
APPLICATION FOR EXTERNAL DIGITAL FILTER INTERFACE

DFMS = 0

External Filter Device

PCM1792

1 ZEROL
2 ZEROR
3 MSEL
4 LRCK

DATA
BCK
SCK

WDCK (Word Clock)

DFMS = 1

External Filter Device

PCM1792

1 ZEROL
2 ZEROR
3 MSEL
4 LRCK

DATA_L
DATA_R

WDCK (Word Clock)

BCK
SCK

Figure 40. Connection Diagram for External Digital Filter (Internal DF Bypass Mode) Application
Application for Interfacing With an External Digital Filter

For some applications, it may be desirable to use an external digital filter to perform the interpolation function, as it can provide improved stop-band attenuation when compared to the internal digital filter of the PCM1792.

The PCM1792 supports several external digital filters, including:

- Texas Instruments DF1704 and DF1706
- Pacific Microsonics PMD200 HDCD filter/decoder IC
- Programmable digital signal processors

The external digital filter application mode is accessed by programming the following bits in the corresponding control register:

- DFTH = 1 (register 20)

The pins used to provide the serial interface for the external digital filter are shown in the connection diagram of Figure 40. The word (WDCK) signal must be operated at $8 \times$ or $4 \times$ the desired sampling frequency, $f_S$.

System Clock (SCK) and Interface Timing

The PCM1792 in an application using an external digital filter requires the synchronization of WDCK and the system clock. The system clock is phase-free with respect to WDCK. Interface timing among WDCK, BCK, DATAL, and DATAR is shown in Figure 42.

Audio Format

The PCM1792 in the external digital filter interface mode supports right-justified audio formats including 16-bit, 20-bit, and 24-bit audio data, as shown in Figure 41. The audio format is selected by the FMT[2:0] bits of control register 18.

![Figure 41. Audio Data Input Format for External Digital Filter (Internal DF Bypass Mode) Application](image-url)
Figure 42. Audio Interface Timing for External Digital Filter (Internal DF Bypass Mode) Application

Functions Available in the External Digital Filter Mode

The external digital filter mode allows access to the majority of the PCM1792 mode control functions.

The following table shows the register mapping available when the external digital filter mode is selected, along with descriptions of functions which are modified when using this mode selection.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>t(BCY)</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(BCL)</td>
<td>7</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(BCH)</td>
<td>7</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(BL)</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(LB)</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(DS)</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t(DH)</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

NOTE: 1: Bit is required for selection of external digital filter mode.

−: Function is disabled. No operation even if data bit is set

FMT[2:0]: Audio Data Format Selection

Default value: 000

<table>
<thead>
<tr>
<th>FMT[2:0]</th>
<th>Audio Data Format Select</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>16-bit right-justified format (default)</td>
</tr>
<tr>
<td>001</td>
<td>20-bit right-justified format</td>
</tr>
<tr>
<td>010</td>
<td>24-bit right-justified format</td>
</tr>
<tr>
<td>Other</td>
<td>N/A</td>
</tr>
</tbody>
</table>
OS[1:0]: Delta-Sigma Modulator Oversampling Rate Selection

Default value: 00

<table>
<thead>
<tr>
<th>OS[1:0]</th>
<th>Operation Speed Select</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>8 times WDCK (default)</td>
</tr>
<tr>
<td>01</td>
<td>4 times WDCK</td>
</tr>
<tr>
<td>10</td>
<td>16 times WDCK</td>
</tr>
<tr>
<td>11</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

The effective oversampling rate is determined by the oversampling performed by both the external digital filter and the delta-sigma modulator. For example, if the external digital filter is $8 \times$ oversampling, and the user selects OS[1:0] = 00, then the delta-sigma modulator oversamples by $8 \times$, resulting in an effective oversampling rate of $64 \times$. The $16 \times$ WDCK oversampling rate is not available above a 100-kHz sampling rate. If the oversampling rate selected is $16 \times$ WDCK, the system clock frequency must be over 256 fs.

APPLICATION FOR DSD FORMAT (DSD MODE) INTERFACE

![Connection Diagram in DSD Mode](image)

Figure 43. Connection Diagram in DSD Mode

Feature

This mode is used for interfacing directly to a DSD decoder, which is found in Super Audio CD (SACD) applications. The DSD mode is accessed by programming the following bit in the corresponding control register.

$$DSD = 1 \text{ (register 20)}$$

The DSD mode provides a low-pass filtering function. The filtering is provided using an analog FIR filter structure. Four FIR responses are available, and are selected by the DMF[1:0] bits of control register 18.

The DSD bit must be set before inputting DSD data; otherwise, the PCM1792 erroneously detects the TDMCA mode, and commands are not accepted through the serial control interface.

Super Audio CD is a trademark of Sony Kabushiki Kaisha TA Sony Corporation, Japan.
Pin Assignment When Using DSD Format Interface

Several pins are redefined for DSD mode operation. These include:

- **DATA** (pin 5): DSDL as L-channel DSD data input
- **LRCK** (pin 4): DSDR as R-channel DSD data input
- **SCK** (pin 7): DBCK as a bit-clock input
- **BCK** (pin 6): Set LOW (N/A)

![Diagram of DSD interface pins](image)

**Table 1:** Timing Parameters for DSD Audio Interface

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{(BCY)} )</td>
<td>85(^1)</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{(BCH)} )</td>
<td>30</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{(BCL)} )</td>
<td>30</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{(DS)} )</td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{(DH)} )</td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

\(^1\) 2.8224 MHz \times 4. (2.8224 MHz = 64 \times 44.1 kHz. This value is specified as a sampling rate of DSD.)

**Figure 44. Normal Data Output Form From DSD Decoder**

**Figure 45. Timing for DSD Audio Interface**
ANALOG FIR FILTER PERFORMANCE IN DSD MODE

Figure 46. DSD Filter-1, Low BW

Figure 47. DSD Filter-1, High BW

Figure 48. DSD Filter-2, Low BW

Figure 49. DSD Filter-2, High BW

(1) This gain is in comparison to PCM 0 dB, when the DSD input signal efficiency is 50%.

All specifications at DBCK = 2.8224 MHz (44.1 kHz × 64 fS), and 50% modulation DSD data input, unless otherwise noted.
Figure 50. DSD Filter-3, Low BW

Figure 51. DSD Filter-3, High BW

Figure 52. DSD Filter-4, Low BW

Figure 53. DSD Filter-4, High BW

(1) This gain is in comparison to PCM 0 dB, when the DSD input signal efficiency is 50%.

All specifications at DBCK = 2.8224 MHz (44.1 kHz \times 64 f_s), and 50% modulation DSD data input, unless otherwise noted.
DSD MODE CONFIGURATION AND FUNCTION CONTROLS

Configuration for the DSD Interface Mode

DSD = 1 (Register 20, B5)

<table>
<thead>
<tr>
<th>Register 16</th>
<th>B15</th>
<th>B14</th>
<th>B13</th>
<th>B12</th>
<th>B11</th>
<th>B10</th>
<th>B9</th>
<th>B8</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register 17</th>
<th>B15</th>
<th>B14</th>
<th>B13</th>
<th>B12</th>
<th>B11</th>
<th>B10</th>
<th>B9</th>
<th>B8</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register 18</th>
<th>B15</th>
<th>B14</th>
<th>B13</th>
<th>B12</th>
<th>B11</th>
<th>B10</th>
<th>B9</th>
<th>B8</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register 19</th>
<th>B15</th>
<th>B14</th>
<th>B13</th>
<th>B12</th>
<th>B11</th>
<th>B10</th>
<th>B9</th>
<th>B8</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register 20</th>
<th>B15</th>
<th>B14</th>
<th>B13</th>
<th>B12</th>
<th>B11</th>
<th>B10</th>
<th>B9</th>
<th>B8</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R/W</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register 21</th>
<th>B15</th>
<th>B14</th>
<th>B13</th>
<th>B12</th>
<th>B11</th>
<th>B10</th>
<th>B9</th>
<th>B8</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register 22</th>
<th>B15</th>
<th>B14</th>
<th>B13</th>
<th>B12</th>
<th>B11</th>
<th>B10</th>
<th>B9</th>
<th>B8</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: −: Function is disabled. No operation even if data bit is set.

DMF[1:0]: Analog FIR Performance Selection

Default value: 00

<table>
<thead>
<tr>
<th>DMF[1:0]</th>
<th>Analog-FIR Performance Select</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>FIR-1 (default)</td>
</tr>
<tr>
<td>01</td>
<td>FIR-2</td>
</tr>
<tr>
<td>10</td>
<td>FIR-3</td>
</tr>
<tr>
<td>11</td>
<td>FIR-4</td>
</tr>
</tbody>
</table>

Plots for the four analog FIR filter responses are shown in the TYPICAL PERFORMANCE CURVES section of this data sheet.

OS[1:0]: Analog-FIR Operation-Speed Selection

Default value: 00

<table>
<thead>
<tr>
<th>OS[1:0]</th>
<th>Operation Speed Select</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>fDBCK (default)</td>
</tr>
<tr>
<td>01</td>
<td>fDBCK/2</td>
</tr>
<tr>
<td>10</td>
<td>Reserved</td>
</tr>
<tr>
<td>11</td>
<td>fDBCK/4</td>
</tr>
</tbody>
</table>

The OS bit in the DSD mode is used to select the operating rate of the analog FIR. The OS bits must be set before setting the DSD bit to 1.

TDMCA Format

The PCM1792 supports the time-division-multiplexed command and audio (TDMCA) data format to simplify the host control serial interface. The TDMCA format is designed not only for the McBSP of TI DSPs but also for any programmable devices. The TDMCA format can transfer not only audio data but also command data, so that it can be used together with any kind of device that supports the TDMCA format. The TDMCA frame consists of command field, extended command field, and some audio data fields. Those audio data are transported to IN devices (such as a DAC) and/or from OUT devices (such as an ADC). The PCM1792 is an IN device. LRCK and BCK are used with both IN and OUT devices so that the sample frequency of all devices in a system must be the same. The TDMCA mode supports a maximum of 30 device IDs. The maximum number of audio channels depends on the BCK frequency.
TDMCA Mode Determination

The PCM1792 recognizes the TDMCA mode automatically when it receives an LRCK signal with a pulse duration of two BCK clocks. If the TDMCA mode operation is not needed, the duty cycle of LRCK must be 50%. Figure 54 shows the LRCK and BCK timing that determines the TDMCA mode. The PCM1792 enters the TDMCA mode after two continuous TDMCA frames. Any TDMCA commands can be issued during the next TDMCA frame after the TDMCA mode is entered.

![Figure 54. LRCK and BCK Timing of Determination TDMCA Mode](image)

TDMCA Terminals

TDMCA requires six signals, of which four signals are for command and audio data interface, and two pairs of signals which are for daisy chaining. Those signals can be shared as in the following table. The DO signal has a 3-state output so that it can be connected directly to other devices.

<table>
<thead>
<tr>
<th>TERMINAL NAME</th>
<th>TDMCA NAME</th>
<th>PROPERTY</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>LRCK</td>
<td>LRCK</td>
<td>input</td>
<td>TDMCA frame start signal. It must be the same as the sampling frequency.</td>
</tr>
<tr>
<td>BCK</td>
<td>BCK</td>
<td>input</td>
<td>TDMCA clock. Its frequency must be high enough to communicate a TDMCA frame within an LRCK cycle.</td>
</tr>
<tr>
<td>DATA</td>
<td>DI</td>
<td>input</td>
<td>TDMCA command and audio data input signal</td>
</tr>
<tr>
<td>MDO</td>
<td>DO</td>
<td>output</td>
<td>TDMCA command data 3-state output signal</td>
</tr>
<tr>
<td>MC</td>
<td>DCl</td>
<td>input</td>
<td>TDMCA daisy-chain input signal</td>
</tr>
<tr>
<td>MS</td>
<td>DCO</td>
<td>output</td>
<td>TDMCA daisy-chain output signal</td>
</tr>
</tbody>
</table>

Device ID Determination

The TDMCA mode also supports a multichip implementation in one system. This means a host controller (DSP) can simultaneously support several TDMCA devices, which can be of the same type or different types, including PCM devices. The PCM devices are categorized as IN device, OUT device, IN/OUT device, and NO device. The IN device has an input port to get audio data, the OUT device has an output port to supply audio data, the IN/OUT device has both input and output ports for audio data, and the NO device has no port for audio data but needs command data from the host. A DAC is an IN device, an ADC is an OUT device, a CODEC is an IN/OUT device, and a PLL is a NO device. The PCM1792 is an IN device. For the host controller to distinguish the devices, each device is assigned its own device ID by the daisy chain. The devices obtain their own device IDs automatically by connecting their DCI to the DCO of the preceding device and their DCO to the DCI of the following device in the daisy chain. The daisy chains are categorized as the IN chain and the OUT chain, which are completely independent and equivalent. Figure 55 shows an example daisy chain connection. If a system needs to chain the PCM1792 and a NO device in the same IN or OUT chain, the NO device should be chained at the back end of the chain because it does not require any audio data. Figure 56 shows an example of TDMCA system including an IN chain and an OUT chain with a TI DSP. For a device to get its own device ID, the DID signal must be set to 1 (see the Command Field section for details), and LRCK and BCK must be driven in the TDMCA mode for all PCM devices which are chained. The device at the top of the chain knows its device ID is 1 because its DCI is fixed HIGH. Other devices count the BCK pulses and observe their own DCI signal to determine their position and ID. Figure 57 shows the initialization of each device ID.
Figure 55. Daisy Chain Connection
Figure 56. IN Daisy Chain and OUT Daisy Chain Connection for a Multichip System
**TDMCA Frame**

In general, the TDMCA frame consists of the command field, extended command (EMD) field, and audio data fields. All of them are 32 bits in length, but the lowest byte has no meaning. The MSB is transferred first for each field. The command field is always transferred as the first packet of the frame. The EMD field is transferred if the EMD flag of the command field is HIGH. If any EMD packets are transferred, no audio data follows the EMD packets. This frame is for quick system initialization. All devices of a daisy chain should respond to the command field and extended command field. The PCM1792 has two audio channels that can be selected by OPE (register 19). If this OPE bit is not set to HIGH, those audio channels are transferred. Figure 58 shows the general TDMCA frame. If some DACs are enabled, but corresponding audio data packets are not transferred, the analog outputs are unpredictable.

---

**Figure 57. Device ID Determination Sequence**

**Figure 58. General TDMCA Frame**
**Command Field**

The normal command field is defined as follows. When the DID bit (MSB) is 1, this frame is used only for device ID determination, and all remaining bits in the field are ignored.

| Bit 31 | Bit 30 | Bit 29 | Bit 28 | Bit 27 | Bit 26 | Bit 25 | Bit 24 | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| DID   | EMD   | DCS   | device ID | R/W | register ID | data | not used |

**Bit 31: Device ID enable flag**

The PCM1792 operates to get its own device ID for TDMCA initialization if this bit is HIGH.

**Bit 30: Extended command enable flag**

The EMD packet will be transferred if this bit is HIGH, otherwise skipped. Once this bit is HIGH, this frame does not contain any audio data. This is for system initialization.

**Bit 29: Daisy chain selection flag**

HIGH designates OUT-chain devices, LOW designates IN-chain devices. The PCM1792 is an IN device, so the DCS bit must be set to LOW.

**Bits[28:24]: Device ID. It is 5 bits length, and it can be defined.**

These bits identify the order of a device in the IN or OUT daisy chain. The top of the daisy chain defines device ID 1 and successive devices are numbered 2, 3, 4, etc. All devices for which the DCI is fixed HIGH are also defined as ID 1. The maximum device ID is 30 each in the IN and OUT chains. If a device ID of 0x1F is used, all devices are selected as broadcast when in the write mode. If a device ID of 0x00 is used, no device is selected.

**Bit 23: Command Read/Write flag**

If this bit is HIGH, the command is a read operation.

**Bits[22:16]: Register ID**

It is 7 bits in length.

**Bits[15:8]: Command data**

It is 8 bits in length. Any valid data can be chosen for each register.

**Bits[7:0]: Not used**

These bits are never transported when a read operation is performed.

**Extended command field**

The extended command field is the same as the command field, except that it does not have a DID flag.
Audio Fields

The audio field is 32 bits in length and the audio data is transferred MSB first, so the other fields must be stuffed with 0s as shown in the following example.

<table>
<thead>
<tr>
<th>audio data</th>
<th>31</th>
<th>16</th>
<th>12</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td></td>
<td>24 bits</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LSB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>All 0s</td>
</tr>
</tbody>
</table>

TDMCA Register Requirements

TDMCA mode requires device ID and audio channel information, previously described. The OPE bit in register 19 indicates audio channel availability and register 23 indicates the device ID. Register 23 is used only in the TDMCA mode. See the mode control register map (Table 4).

Register Write/Read Operation

The command supports register write and read operations. If the command requests to read one register, the read data is transferred on DO during the data phase of the timing cycle. The DI signal can be retrieved at the positive edge of BCK, and the DO signal is driven at the negative edge of BCK. DO is activated one BCK cycle early to compensate for the output delay caused by high impedance. Figure 60 shows the TDMCA write and read timing.

TDMCA-Mode Operation

DCO specifies the owner of the next audio channel in TDMCA-mode operation. When a device retrieves its own audio channel data, DCO goes HIGH during the last audio channel period. Figure 61 shows the DCO output timing in TDMCA-mode operation. The host controller ignores the behavior of DCI and DCO. DCO indicates the last audio channel of each device. Therefore, DCI means the next audio channel is allocated.

If some devices are skipped due to no active audio channel, the skipped devices must notify the next device that the DCO will be passed through the next DCI. Figure 62 and Figure 63 show DCO timing with skip operation. Figure 64 shows the ac timing of the daisy chain signals.
Figure 61. DCO Output Timing of TDMCA Mode Operation

Figure 62. DCO Output Timing With Skip Operation
Figure 63. DCO Output Timing With Skip Operation (for Command Packet 1)
### AC Timing of Daisy Chain Signals

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{(BCY)}$</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{(LB)}$</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{(BL)}$</td>
<td>3</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{(DS)}$</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{(DH)}$</td>
<td>3</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{(DOE)}$</td>
<td>8</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{(COE)}$</td>
<td>6</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) Load capacitance is 10 pF.
THEORY OF OPERATION

The PCM1792 uses TI’s advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1792 provides balanced current outputs.

Digital input data via the digital filter is separated into six upper bits and 18 lower bits. The six upper bits are converted to inverted complementary offset binary (ICOB) code. The lower 18 bits, associated with the MSB, are processed by a five-level third-order delta-sigma modulator operated at 64 fS by default. The 1 level of the modulator is equivalent to the 1 LSB of the ICOB code converter. The data groups processed in the ICOB converter and third-order delta-sigma modulator are summed together to an up to 66-level digital code, and then processed by data-weighted averaging (DWA) to reduce the noise produced by element mismatch. The data of up to 66 levels from the DWA is converted to an analog output in the differential-current segment section.

This architecture has overcome the various drawbacks of conventional multibit processing and also achieves excellent dynamic performance.

Figure 65. Advanced Segments DAC
Analog output

The following table and Figure 66 show the relationship between the digital input code and analog output.

<table>
<thead>
<tr>
<th></th>
<th>800000 (−FS)</th>
<th>000000 (BPZ)</th>
<th>7FFFFFF (+FS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOUTN [mA]</td>
<td>−2.3</td>
<td>−6.2</td>
<td>−10.1</td>
</tr>
<tr>
<td>IOUTP [mA]</td>
<td>−10.1</td>
<td>−6.2</td>
<td>−2.3</td>
</tr>
<tr>
<td>VOUTN [V]</td>
<td>−1.725</td>
<td>−4.650</td>
<td>−7.575</td>
</tr>
<tr>
<td>VOUTP [V]</td>
<td>−7.575</td>
<td>−4.650</td>
<td>−1.725</td>
</tr>
<tr>
<td>VOUT [V]</td>
<td>−2.821</td>
<td>0</td>
<td>2.821</td>
</tr>
</tbody>
</table>

NOTE: VOUTN is the output of U1, VOUTP is the output of U2, and VOUT is the output of U3 in the measurement circuit of Figure 36.

Figure 66. The Relationship Between Digital Input and Analog Output
<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PIns</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCM1792DB</td>
<td>NRND</td>
<td>SSOP</td>
<td>DB</td>
<td>28</td>
<td>47</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-25 to 85</td>
<td>PCM1792</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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