24-BIT, 192-kHz SAMPLING, ADVANCED SEGMENT, AUDIO STEREO DIGITAL-TO-ANALOG CONVERTER

FEATURES
- 24-Bit Resolution
- Analog Performance:
  - Dynamic Range: 113 dB
  - THD+N: 0.001%
  - Full-Scale Output: 2.1 V rms (at Postamplifier)
- Differential Voltage Output: 3.2 V p-p
- 8x Oversampling Digital Filter:
  - Stop-Band Attenuation: –82 dB
  - Pass-Band Ripple: ±0.002 dB
- Sampling Frequency: 10 kHz to 200 kHz
- System Clock: 128, 192, 256, 384, 512, or 768 fS With Autodetect
- Accepts 16-, 20-, and 24-Bit Audio Data
- Data Formats: Standard, I2S, and Left-Justified
- Digital De-Emphasis
- Soft Mute
- Zero Flags for Each Output
- Dual Supply Operation:
  - 5-V Analog, 3.3-V Digital
- 5-V Tolerant Digital Inputs
- Small 28-Lead SSOP Package, Lead-Free Product

APPLICATIONS
- A/V Receivers
- DVD Players
- Musical Instruments
- HDTV Receivers
- Car Audio Systems
- Digital Multitrack Recorders
- Other Applications Requiring 24-Bit Audio

DESCRIPTION
The PCM1793 is a monolithic CMOS integrated circuit that includes stereo digital-to-analog converters and support circuitry in a small 28-lead SSOP package. The data converters use TI’s advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1793 provides balanced voltage outputs, allowing the user to optimize analog performance externally. Sampling rates up to 200 kHz are supported.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
ORDERING INFORMATION

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>PACKAGE</th>
<th>PACKAGE CODE</th>
<th>OPERATION TEMPERATURE RANGE</th>
<th>PACKAGE MARKING</th>
<th>ORDERING NUMBER</th>
<th>TRANSPORT MEDIA</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCM1793DB</td>
<td>28-lead SSOP</td>
<td>28DB</td>
<td>−25°C to 85°C</td>
<td>PCM1793</td>
<td>PCM1793DB</td>
<td>Tube</td>
</tr>
<tr>
<td>PCM1793DB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PCM1793DBR</td>
<td>Tape and reel</td>
</tr>
</tbody>
</table>

ABSOLUTE MAXIMUM RATINGS
over operating free-air temperature range unless otherwise noted(1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>PCM1793</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>$V_{CC,F}, V_{CC,L}, V_{CC,C}, V_{CC,R}$</td>
</tr>
<tr>
<td></td>
<td>$V_{DD}$</td>
</tr>
<tr>
<td></td>
<td>−0.3 V to 6.5 V</td>
</tr>
<tr>
<td></td>
<td>−0.3 V to 4 V</td>
</tr>
<tr>
<td>Supply voltage differences: $V_{CC,F}, V_{CC,L}, V_{CC,C}, V_{CC,R}$</td>
<td>±0.1 V</td>
</tr>
<tr>
<td>Ground voltage differences: $AGND_{F}, AGND_{L}, AGND_{C}, AGND_{R}, DGND$</td>
<td>±0.1 V</td>
</tr>
<tr>
<td>Digital input voltage</td>
<td>$LRCK, DATA, BCK, SCK, DEMP0, DEMP1, FMT0, FMT1, FMT2, RST, MUTE $</td>
</tr>
<tr>
<td></td>
<td>ZEROL, ZEROR</td>
</tr>
<tr>
<td></td>
<td>−0.3 V to 6.5 V</td>
</tr>
<tr>
<td></td>
<td>−0.3 V to $(V_{DD} + 0.3 V) &lt; 4 V$</td>
</tr>
<tr>
<td>Analog input voltage</td>
<td>−0.3 V to $(V_{CC} + 0.3 V) &lt; 6.5 V</td>
</tr>
<tr>
<td>Input current (any pins except supplies)</td>
<td>±10 mA</td>
</tr>
<tr>
<td>Ambient temperature under bias</td>
<td>−40°C to 125°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>−55°C to 150°C</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>150°C</td>
</tr>
<tr>
<td>Lead temperature (soldering)</td>
<td>260°C, 5 s</td>
</tr>
<tr>
<td>Package temperature (IR reflow, peak)</td>
<td>260°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS
all specifications at $T_A = 25°C$, $V_{CC} = 5 V$, $V_{DD} = 3.3 V$, $f_S = 44.1$ kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>PCM1793DB</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESOLUTION</td>
<td></td>
<td>MIN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TYP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MAX</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UNIT</td>
</tr>
<tr>
<td>DATA FORMAT</td>
<td></td>
<td>24</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>Audio data interface format</td>
<td>Standard, $I^2S$, left justified</td>
<td></td>
</tr>
<tr>
<td>Audio data bit length</td>
<td></td>
<td>16-, 20-, 24-bit selectable</td>
</tr>
<tr>
<td>Audio data format</td>
<td></td>
<td>MSB first, 2s complement</td>
</tr>
<tr>
<td>$f_S$</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>200</td>
</tr>
<tr>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>System clock frequency</td>
<td></td>
<td>128, 192, 256, 384, 512, 768 $f_S$</td>
</tr>
</tbody>
</table>

DIGITAL INPUT/OUTPUT

<table>
<thead>
<tr>
<th>Logic family</th>
<th>TTL compatible</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input logic level</td>
<td>2</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input logic current</td>
<td>$V_{IN} = V_{DD}$</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>$V_{IN} = 0 V$</td>
<td>10</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>$V_{OL} = −2 mA$</td>
<td>2.4</td>
</tr>
<tr>
<td>Output logic level</td>
<td>$I_{OH} = 2 mA$</td>
<td>0.4</td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS (Continued)

All specifications at $T_A = 25^\circ C$, $V_{CC} = 5$ V, $V_{DD} = 3.3$ V, $f_S = 44.1$ kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted.

#### DYNAMIC PERFORMANCE (1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>PCM1793DB</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>THD+N at $V_{OUT} = 0$ dB</td>
<td>$f_S = 44.1$ kHz</td>
<td>0.001%</td>
<td>0.002%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_S = 96$ kHz</td>
<td>0.0015%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_S = 192$ kHz</td>
<td>0.003%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dynamic range</td>
<td>EIAJ, A-weighted, $f_S = 44.1$ kHz</td>
<td>110</td>
<td>113</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>EIAJ, A-weighted, $f_S = 96$ kHz</td>
<td>113</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>EIAJ, A-weighted, $f_S = 192$ kHz</td>
<td>113</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Signal-to-noise ratio</td>
<td>EIAJ, A-weighted, $f_S = 44.1$ kHz</td>
<td>110</td>
<td>113</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>EIAJ, A-weighted, $f_S = 96$ kHz</td>
<td>113</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>EIAJ, A-weighted, $f_S = 192$ kHz</td>
<td>113</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Channel separation</td>
<td>$f_S = 44.1$ kHz</td>
<td>106</td>
<td>110</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>$f_S = 96$ kHz</td>
<td>110</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>$f_S = 192$ kHz</td>
<td>109</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Level linearity error</td>
<td>$V_{OUT} = −120$ dB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### ANALOG OUTPUT

- Gain error
  - $−8 \pm 3 \%)$ of $f_S$

- Gain mismatch, channel-to-channel
  - $−3 \pm 0.5 \%)$ of $f_S$

- Bipolar zero error
  - $−2 \pm 0.5 \%)$ of $f_S$

- Differential output voltage (2)
  - Full scale (0 dB)
  - 3.2 V p-p

- Bipolar zero voltage (2)
  - Full scale (0 dB)
  - 1.4 V

- Load impedance (2)
  - $R_1 = R_2$
  - 1.7 kΩ

#### DIGITAL FILTER PERFORMANCE

- De-emphasis error
  - $±0.1$ dB

- Pass band
  - $±0.002$ dB
  - $0.454 f_S$
  - $−3$ dB
  - $0.49 f_S$

- Stop band
  - 0.546 $f_S$

- Pass-band ripple
  - $±0.002$ dB

- Stop-band attenuation
  - $Stop band = 0.546 f_S$
  - $−75$ dB
  - $Stop band = 0.567 f_S$
  - $−82$ dB

- Delay time
  - $29/f_S$
  - s

(1) Dynamic performance and DC accuracy are specified at the output of the postamplifier as shown in Figure 28. Analog performance specifications are measured using the System Two™ Cascade audio measurement system by Audio Precision™ in the averaging mode. At all sampling frequency operations, measurement bandwidth is limited with a 20-kHz AES17 filter.

(2) These parameters are defined at the PCM1793 output pin. Load impedance, $R_1$ and $R_2$, are input resistors of the postamplifier. These are defined as dc loads.

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Other trademarks are the property of their respective owners.
## ELECTRICAL CHARACTERISTICS (Continued)

all specifications at $T_A = 25^\circ C$, $V_{CC} = 5 \text{ V}$, $V_{DD} = 3.3 \text{ V}$, $f_S = 44.1 \text{ kHz}$, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>PCM1793DB</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td>Power supply requirements</td>
<td></td>
<td>3</td>
<td>3.3</td>
</tr>
<tr>
<td>$V_{DD}$ Voltage range</td>
<td></td>
<td>4.5</td>
<td>5</td>
</tr>
<tr>
<td>$I_{DD}$ Supply current (1)</td>
<td>$f_S = 44.1 \text{ kHz}$</td>
<td>6.5</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>$f_S = 96 \text{ kHz}$</td>
<td>13.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_S = 192 \text{ kHz}$</td>
<td>28</td>
<td></td>
</tr>
<tr>
<td>$I_{CC}$ Supply current (1)</td>
<td>$f_S = 44.1 \text{ kHz}$</td>
<td>14</td>
<td>16</td>
</tr>
<tr>
<td></td>
<td>$f_S = 96 \text{ kHz}$</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_S = 192 \text{ kHz}$</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>Power dissipation (1)</td>
<td>$f_S = 44.1 \text{ kHz}$</td>
<td>90</td>
<td>110</td>
</tr>
<tr>
<td></td>
<td>$f_S = 96 \text{ kHz}$</td>
<td>120</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_S = 192 \text{ kHz}$</td>
<td>170</td>
<td></td>
</tr>
</tbody>
</table>

### TEMPERATURE RANGE

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>PCM1793DB</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operation temperature</td>
<td></td>
<td>–25</td>
<td>85</td>
</tr>
<tr>
<td>$\theta_{JA}$ Thermal resistance</td>
<td>28-pin SSOP</td>
<td>100</td>
<td></td>
</tr>
</tbody>
</table>

(1) Input is BPZ data.

## PIN ASSIGNMENTS

![PCM1793 PIN ASSIGNMENTS](image-url)
## Terminal Functions

<table>
<thead>
<tr>
<th>TERMINAL NAME</th>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>AGNDC</td>
<td>16</td>
<td>–</td>
<td>Analog ground (internal bias and current DAC)</td>
</tr>
<tr>
<td>AGNDF</td>
<td>9</td>
<td>–</td>
<td>Analog ground (DACFF)</td>
</tr>
<tr>
<td>AGNDL</td>
<td>19</td>
<td>–</td>
<td>Analog ground (L-channel I/V)</td>
</tr>
<tr>
<td>AGNDR</td>
<td>11</td>
<td>–</td>
<td>Analog ground (R-channel I/V)</td>
</tr>
<tr>
<td>BCK</td>
<td>2</td>
<td>I</td>
<td>Bit clock input (1)</td>
</tr>
<tr>
<td>DATA</td>
<td>3</td>
<td>I</td>
<td>Serial audio data input (1)</td>
</tr>
<tr>
<td>DEMP0</td>
<td>24</td>
<td>I</td>
<td>De-emphasis control 0 (1)</td>
</tr>
<tr>
<td>DEMP1</td>
<td>25</td>
<td>I</td>
<td>De-emphasis control 1 (1)</td>
</tr>
<tr>
<td>DGND</td>
<td>8</td>
<td>–</td>
<td>Digital ground</td>
</tr>
<tr>
<td>FMT0</td>
<td>26</td>
<td>I</td>
<td>Audio data format select 0 (1)</td>
</tr>
<tr>
<td>FMT1</td>
<td>27</td>
<td>I</td>
<td>Audio data format select 1 (1)</td>
</tr>
<tr>
<td>FMT2</td>
<td>28</td>
<td>I</td>
<td>Audio data format select 2 (1)</td>
</tr>
<tr>
<td>LRCK</td>
<td>1</td>
<td>I</td>
<td>Left and right clock (f_s) input (1)</td>
</tr>
<tr>
<td>MUTE</td>
<td>4</td>
<td>I</td>
<td>Analog output mute control (1)</td>
</tr>
<tr>
<td>RST</td>
<td>6</td>
<td>I</td>
<td>Reset (1)</td>
</tr>
<tr>
<td>SCK</td>
<td>5</td>
<td>I</td>
<td>System clock input (1)</td>
</tr>
<tr>
<td>VCC C</td>
<td>15</td>
<td>–</td>
<td>Analog power supply (internal bias and current DAC), 5 V</td>
</tr>
<tr>
<td>VCC F</td>
<td>21</td>
<td>–</td>
<td>Analog power supply (DACFF), 5 V</td>
</tr>
<tr>
<td>VCC L</td>
<td>20</td>
<td>–</td>
<td>Analog power supply (L-channel I/V), 5 V</td>
</tr>
<tr>
<td>VCC R</td>
<td>10</td>
<td>–</td>
<td>Analog power supply (R-channel I/V), 5 V</td>
</tr>
<tr>
<td>V COM</td>
<td>14</td>
<td>–</td>
<td>Internal bias decoupling pin</td>
</tr>
<tr>
<td>VDD</td>
<td>7</td>
<td>–</td>
<td>Digital power supply, 3.3 V</td>
</tr>
<tr>
<td>VOUT L+</td>
<td>17</td>
<td>O</td>
<td>L-channel analog voltage output +</td>
</tr>
<tr>
<td>VOUT L−</td>
<td>18</td>
<td>O</td>
<td>L-channel analog voltage output −</td>
</tr>
<tr>
<td>VOUT R+</td>
<td>13</td>
<td>O</td>
<td>R-channel analog voltage output +</td>
</tr>
<tr>
<td>VOUT R−</td>
<td>12</td>
<td>O</td>
<td>R-channel analog voltage output −</td>
</tr>
<tr>
<td>ZEROL</td>
<td>23</td>
<td>O</td>
<td>Zero flag for L-channel</td>
</tr>
<tr>
<td>ZEROR</td>
<td>22</td>
<td>O</td>
<td>Zero flag for R-channel</td>
</tr>
</tbody>
</table>

(1) Schmitt-trigger input, 5-V tolerant
DIGITAL FILTER

Digital Filter Response

**Figure 1. Frequency Response, Sharp Rolloff**

**Figure 2. Pass-Band Ripple, Sharp Rolloff**

**Figure 3. Frequency Response, Slow Rolloff**

**Figure 4. Transition Characteristics, Slow Rolloff**
De-Emphasis Filter

**De-emphasis Level vs Frequency**

![Graph showing de-emphasis level vs frequency for f_s = 32 kHz.]

**De-emphasis Error vs Frequency**

![Graph showing de-emphasis error vs frequency for f_s = 32 kHz.]

**De-emphasis Level vs Frequency**

![Graph showing de-emphasis level vs frequency for f_s = 44.1 kHz.]

**De-emphasis Error vs Frequency**

![Graph showing de-emphasis error vs frequency for f_s = 44.1 kHz.]

Figure 5

Figure 6

Figure 7

Figure 8
De-Emphasis Filter (Continued)

DE-EMPHASIS LEVEL
vs
FREQUENCY

DE-EMPHASIS ERROR
vs
FREQUENCY

Figure 9

Figure 10
ANALOG DYNAMIC PERFORMANCE

Supply Voltage Characteristics

NOTE: PCM mode, \( T_A = 25^\circ C, V_{DD} = 3.3 V \).
Temperature Characteristics

**Figure 15**

TOTAL HARMONIC DISTORTION + NOISE vs FREE-AIR TEMPERATURE

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>THD+N, %</th>
</tr>
</thead>
<tbody>
<tr>
<td>-50</td>
<td>0.01</td>
</tr>
<tr>
<td>-25</td>
<td>0.01</td>
</tr>
<tr>
<td>0</td>
<td>0.01</td>
</tr>
<tr>
<td>25</td>
<td>0.01</td>
</tr>
<tr>
<td>50</td>
<td>0.01</td>
</tr>
<tr>
<td>75</td>
<td>0.01</td>
</tr>
<tr>
<td>100</td>
<td>0.01</td>
</tr>
</tbody>
</table>

- $f_S = 192$ kHz
- $f_S = 96$ kHz
- $f_S = 44.1$ kHz

**Figure 16**

DYNAMIC RANGE vs FREE-AIR TEMPERATURE

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Dynamic Range, dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>-50</td>
<td>118</td>
</tr>
<tr>
<td>-25</td>
<td>118</td>
</tr>
<tr>
<td>0</td>
<td>118</td>
</tr>
<tr>
<td>25</td>
<td>118</td>
</tr>
<tr>
<td>50</td>
<td>118</td>
</tr>
<tr>
<td>75</td>
<td>118</td>
</tr>
<tr>
<td>100</td>
<td>118</td>
</tr>
</tbody>
</table>

- $f_S = 192$ kHz
- $f_S = 96$ kHz
- $f_S = 44.1$ kHz

**Figure 17**

SIGNAL-to-NOISE RATIO vs FREE-AIR TEMPERATURE

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>SNR, dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>-50</td>
<td>118</td>
</tr>
<tr>
<td>-25</td>
<td>118</td>
</tr>
<tr>
<td>0</td>
<td>118</td>
</tr>
<tr>
<td>25</td>
<td>118</td>
</tr>
<tr>
<td>50</td>
<td>118</td>
</tr>
<tr>
<td>75</td>
<td>118</td>
</tr>
<tr>
<td>100</td>
<td>118</td>
</tr>
</tbody>
</table>

- $f_S = 192$ kHz
- $f_S = 96$ kHz
- $f_S = 44.1$ kHz

**Figure 18**

CHANNEL SEPARATION vs FREE-AIR TEMPERATURE

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Channel Separation, dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>-50</td>
<td>118</td>
</tr>
<tr>
<td>-25</td>
<td>118</td>
</tr>
<tr>
<td>0</td>
<td>118</td>
</tr>
<tr>
<td>25</td>
<td>118</td>
</tr>
<tr>
<td>50</td>
<td>118</td>
</tr>
<tr>
<td>75</td>
<td>118</td>
</tr>
<tr>
<td>100</td>
<td>118</td>
</tr>
</tbody>
</table>

- $f_S = 192$ kHz
- $f_S = 96$ kHz
- $f_S = 44.1$ kHz

**NOTE:** PCM mode, $V_{DD} = 3.3$ V, $V_{CC} = 5$ V.
Figure 19. −60-dB Output Spectrum, BW = 20 kHz  
Figure 20. −60-dB Output Spectrum, BW = 100 kHz

NOTE: PCM mode, f_s = 44.1 kHz, 32768 points, 8 average, T_A = 25°C, V_DD = 3.3 V, V_CC = 5 V.

Figure 21. THD+N vs Input Level, PCM Mode

NOTE: PCM mode, f_s = 44.1 kHz, T_A = 25°C, V_DD = 3.3 V, V_CC = 5 V.
SYSTEM CLOCK AND RESET FUNCTIONS

System Clock Input

The PCM1793 requires a system clock for operating the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input (pin 5). The PCM1793 has a system clock detection circuit that automatically senses which frequency the system clock is operating. Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 22 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. One of the Texas Instruments’ PLL1700 family of multiclock generators is an excellent choice for providing the PCM1793 system clock.

Table 1. System Clock Rates for Common Audio Sampling Frequencies

<table>
<thead>
<tr>
<th>SAMPLING FREQUENCY</th>
<th>SYSTEM CLOCK FREQUENCY (FSCK) (MHZ)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>128 FS</td>
</tr>
<tr>
<td>44.1 kHz</td>
<td>5.6488</td>
</tr>
<tr>
<td>96 kHz</td>
<td>12.288</td>
</tr>
<tr>
<td>192 kHz</td>
<td>24.576</td>
</tr>
</tbody>
</table>

(1) This system clock rate is not supported for the given sampling frequency.

Power-On and External Reset Functions

The PCM1793 includes a power-on reset function. Figure 23 shows the operation of this function. With VDD > 2 V, the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time VDD > 2 V.

The PCM1793 also includes an external reset capability using the RST input (pin 6). This allows an external controller or master reset circuit to force the PCM1793 to initialize to its default reset state.

Figure 24 shows the external reset operation and timing. The RST pin is set to logic 0 for a minimum of 20 ns. The RST pin is then set to a logic 1 state, thus starting the initialization sequence, which requires 1024 system clock periods. The external reset is especially useful in applications where there is a delay between the PCM1793 power up and system clock activation.
Figure 23. Power-On Reset Timing

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>t(RST)</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Figure 24. External Reset Timing
AUDIO DATA INTERFACE

Audio Serial Interface

The audio interface port is a 3-wire serial port. It includes LRCK (pin 1), BCK (pin 2), and DATA (pin 3). BCK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the serial shift register of the audio interface. Serial data is clocked into the PCM1793 on the rising edge of BCK. LRCK is the serial audio left/right word clock.

The PCM1793 requires the synchronization of LRCK and the system clock, but does not need a specific phase relation between LRCK and the system clock.

If the relationship between LRCK and the system clock changes more than ±6 BCK, internal operation is initialized within 1/fs and the analog outputs are forced to the bipolar zero level until resynchronization between LRCK and the system clock is completed.

PCM Audio Data Formats and Timing

The PCM1793 supports industry-standard audio data formats, including standard right-justified, I²S, and left-justified. The data formats are shown in Figure 26. Data formats are selected using the format bits, FMT2 (pin 28), FMT1 (pin 27), and FMT0 (pin 26) as shown in Table 2. All formats require binary 2s complement, MSB-first audio data. Figure 25 shows a detailed timing diagram for the serial audio interface.

<table>
<thead>
<tr>
<th>FMT2 PIN 28</th>
<th>FMT1 PIN 27</th>
<th>FMT0 PIN 26</th>
<th>FORMAT</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOW</td>
<td>LOW</td>
<td>LOW</td>
<td>16-bit standard format, right-justified</td>
</tr>
<tr>
<td>LOW</td>
<td>LOW</td>
<td>HIGH</td>
<td>20-bit standard format, right-justified</td>
</tr>
<tr>
<td>LOW</td>
<td>HIGH</td>
<td>LOW</td>
<td>24-bit standard format, right-justified</td>
</tr>
<tr>
<td>LOW</td>
<td>HIGH</td>
<td>HIGH</td>
<td>24-bit MSB-first, left-justified format</td>
</tr>
<tr>
<td>HIGH</td>
<td>LOW</td>
<td>LOW</td>
<td>16-bit I²S format</td>
</tr>
<tr>
<td>HIGH</td>
<td>LOW</td>
<td>HIGH</td>
<td>24-bit I²S format</td>
</tr>
<tr>
<td>HIGH</td>
<td>HIGH</td>
<td>LOW</td>
<td>Reserved</td>
</tr>
<tr>
<td>HIGH</td>
<td>HIGH</td>
<td>HIGH</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
PARAMETERS | MIN | MAX | UNITS
---|---|---|---
t(BCY) | 70 ns | 70 ns |
t(BCL) | 30 ns | 30 ns |
t(BCH) | 30 ns | 30 ns |
t(BL) | 10 ns | 10 ns |
t(DS) | 10 ns | 10 ns |
t(DH) | 10 ns | 10 ns |
— | 50% ± 2 bit clocks | 50% ± 2 bit clocks |

Figure 25. Timing of Audio Interface
(1) Standard Data Format (Right Justified); L-Channel = HIGH, R-Channel = LOW

(2) Left Justified Data Format; L-Channel = HIGH, R-Channel = LOW

(3) I2S Data Format; L-Channel = LOW, R-Channel = HIGH

Figure 26. Audio Data Input Formats
FUNCTION DESCRIPTIONS

Zero Detect
When the PCM1793 detects that the audio input data in the L-channel or R-channel is continuously zero for 1024 \( f_S \), the PCM1793 sets ZEROL (pin 23) or ZEROR (pin 22) to HIGH.

Soft Mute
The PCM1793 supports mute operation. When MUTE (pin 4) is set to HIGH, both analog outputs are transitioned to the bipolar zero level in −0.5-dB steps with a transition speed of 1/f\(_S\) per step. This system provides pop-free muting of the DAC output.

De-Emphasis
The PCM1793 has de-emphasis filters for sampling frequencies of 32 kHz, 44.1 kHz, and 48 kHz. DEMP1 (pin 25) and DEMP0 (pin 24) select the sampling frequency for which de-emphasis filtering is performed, as shown in Table 3.

<table>
<thead>
<tr>
<th>DEMP1 Pin 25</th>
<th>DEMP0 Pin 24</th>
<th>De-emphasis Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOW</td>
<td>LOW</td>
<td>Disabled</td>
</tr>
<tr>
<td>LOW</td>
<td>HIGH</td>
<td>48 kHz</td>
</tr>
<tr>
<td>HIGH</td>
<td>LOW</td>
<td>44.1 kHz</td>
</tr>
<tr>
<td>HIGH</td>
<td>HIGH</td>
<td>32 kHz</td>
</tr>
</tbody>
</table>
Figure 27. Typical Application Circuit
APPLICATION INFORMATION

ANALOG OUTPUTS

![Analog Output Diagram]

NOTE: Example R and C values for f_C = 77 kHz – R_1, R_2: 1.8 kΩ, R_3, R_4: 3.3 kΩ, R_5, R_6: 680 Ω, C_1: 1800 pF, C_2, C_3: 560 pF.

Figure 28. Typical Application for Analog Output Stage

Analog Output Level and LPF

The signal level of the DAC differential-voltage output ([V_OUTL+−V_OUTL−], [V_OUTR+−V_OUTR−]) is 3.2 Vp-p at 0 dB (full scale). The voltage output of the LPF is given by following equation:

V_OUT = 3.2 Vp-p × (R_f/R_i)

Here, R_f is the feedback resistor in the LPF, and R_3 = R_4 in a typical application circuit. R_i is the input resistor in the LPF, and R_1 = R_2 in a typical application circuit.

Op Amp for LPF

An OPA2134 or 5532 type op amp is recommended for the LPF circuit to obtain the specified audio performance. Dynamic performance such as gain bandwidth, settling time, and slew rate of the op amp largely determines the audio dynamic performance of the LPF section. The input noise specification of the op amp should be considered to obtain a 113-dB S/N ratio.
Analog Gain of Balanced Amplifier

The DAC voltage outputs are followed by balanced amplifier stages, which sum the differential signals for each channel, creating a single-ended voltage output. In addition, the balanced amplifiers provide a third-order low-pass filter function, which band limits the audio output signal. The cutoff frequency and gain are determined by external R and C component values. In this case, the cutoff frequency is 77 kHz with a gain of 1.83. The output voltage for each channel is 5.9 Vp-p, or 2.1 V rms.

THEORY OF OPERATION

The PCM1793 uses TI’s advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1793 provides balanced voltage outputs.

Digital input data via the digital filter is separated into 6 upper bits and 18 lower bits. The 6 upper bits are converted to inverted complementary offset binary (ICOB) code. The lower 18 bits, associated with the MSB, are processed by a five-level third-order delta-sigma modulator operated at 64 fs by default. The 1 level of the modulator is equivalent to the 1 LSB of the ICOB code converter. The data groups processed in the ICOB converter and third-order delta-sigma modulator are summed together to an up-to-66-level digital code, and then processed by data-weighted averaging (DWA) to reduce the noise produced by element mismatch. The data of up to 66 levels from the DWA is converted to an analog output in the differential-current segment section.

This architecture has overcome the various drawbacks of conventional multibit processing and also achieves excellent dynamic performance.
CONSIDERATIONS FOR APPLICATION CIRCUITS

PCB Layout Guidelines

A typical PCB floor plan for the PCM1793 is shown in Figure 30. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1793 must be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board. Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the D/A converters. In cases where a common 5-V supply would be used for the analog and digital sections, an inductance (RF choke, ferrite bead) must be placed between the analog and digital 5-V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 31 shows the recommended approach for single-supply applications.

![Figure 30. Recommended PCB Layout](image-url)
Bypass and Decoupling Capacitor Requirements

Various-sized decoupling capacitors can be used, with no special tolerances being required. All capacitors must be located as close as possible to the appropriate pins of the PCM1793 to reduce noise pickup from surrounding circuitry. Aluminum electrolytic capacitors that are designed for hi-fi audio applications are recommended for larger values, while metal film or monolithic ceramic capacitors are used for smaller values.

Post-LPF Design

By proper choice of the op amp and resistors used in the post-LPF circuit, excellent performance of the PCM1793 should be achieved. To obtain 0.001% THD+N, 113 dB signal-to-noise-ratio audio performance, the THD+N and input noise performance of the op amp must be considered. This is because the input noise of the op amp contributes directly to the output noise level of the application. The V\text{OUT} pins of the PCM1793 and the input resistor of the post-LPF circuit must be connected as closely as possible.

Out-of-band noise level and attenuated sampling spectrum level are much lower than for typical delta-sigma type DACs due to the combination of a high-performance digital filter and advanced segment DAC architecture. The use of a second-order or third-order post-LPF is recommended for the post-LPF of the PCM1793. The cutoff frequency of the post-LPF depends on the application. For example, there are many sampling-rate operations such as \( f_S = 44.1 \text{ kHz on CDDA} \), \( f_S = 96 \text{ kHz on DVD-M} \), \( f_S = 192 \text{ kHz on DVD-A} \), \( f_S = 64 f_S \) on DSD (SACD).
MECHANICAL DATA

DB (R-PDSO-G**) PLASTIC SMALL-OUTLINE

28 PINS SHOWN

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
D. Falls within JEDEC MO-150

DIMENSION TABLE:

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<thead>
<tr>
<th>DIM</th>
<th>PINS **</th>
<th>14</th>
<th>16</th>
<th>20</th>
<th>24</th>
<th>28</th>
<th>30</th>
<th>38</th>
</tr>
</thead>
<tbody>
<tr>
<td>A MAX</td>
<td></td>
<td>6.50</td>
<td>6.50</td>
<td>7.50</td>
<td>8.50</td>
<td>10.50</td>
<td>10.50</td>
<td>12.90</td>
</tr>
<tr>
<td>A MIN</td>
<td></td>
<td>5.90</td>
<td>5.90</td>
<td>6.90</td>
<td>7.90</td>
<td>9.90</td>
<td>9.90</td>
<td>12.30</td>
</tr>
</tbody>
</table>
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCM1793DB</td>
<td>ACTIVE</td>
<td>SSOP</td>
<td>DB</td>
<td>28/47</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
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<td>SSOP</td>
<td>DB</td>
<td>28/47</td>
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<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
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<td>SSOP</td>
<td>DB</td>
<td>28/2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
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<td>PCM1793DBRG4</td>
<td>ACTIVE</td>
<td>SSOP</td>
<td>DB</td>
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<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSCOLETE**: TI has discontinued the production of the device.

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- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

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<th>Reel Diameter</th>
<th>Width (W1)</th>
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### TAPE DIMENSIONS

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<thead>
<tr>
<th>A0</th>
<th>Dimension designed to accommodate the component width</th>
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<tbody>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
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</tbody>
</table>

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

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<thead>
<tr>
<th>Sprocket Holes</th>
<th>User Direction of Feed</th>
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</thead>
<tbody>
<tr>
<td>Pocket Quadrants</td>
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*All dimensions are nominal.*

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<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
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<td>16.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

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TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
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<td>PCM1793DBR</td>
<td>SSOP</td>
<td>DB</td>
<td>28</td>
<td>2000</td>
<td>336.6</td>
<td>336.6</td>
<td>28.6</td>
</tr>
</tbody>
</table>
MECHANICAL DATA

DB (R-PDSO-G**)  
PLASTIC SMALL-OUTLINE

28 PINS SHOWN

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
D. Falls within JEDEC MO-150


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<table>
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<tr>
<th>Products</th>
<th>Applications</th>
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</thead>
<tbody>
<tr>
<td>Amplifiers</td>
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<td>Automotive</td>
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<tr>
<td>DSP</td>
<td>Broadband</td>
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<td>Clocks and Timers</td>
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<td>RF/IF and ZigBee® Solutions</td>
<td>Video &amp; Imaging</td>
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