

16-Bit, Low-Power Stereo Audio CODEC With Microphone Bias, Headphone, and Digital Speaker Amplifier

FEATURES

- **Analog Front End:**
 - Stereo Single-Ended Input With Multiplexer
 - Mono Differential Input
 - Stereo Programmable Gain Amplifier
 - Microphone Boost Amplifier (20 dB) and Bias
- **Analog BackEnd:**
 - Stereo/Mono Line Output With Volume
 - Stereo/Mono Headphone Amplifier With Volume and Capless Mode
 - Stereo/Mono Digital Speaker Amplifier (BTL) With Volume (PCM3793)
- **Analog Performance:**
 - Dynamic Range: 93 dB (DAC)
 - Dynamic Range: 90 dB (ADC)
 - 40-mW + 40-mW Headphone Output at $R_L = 16 \Omega$
 - 700-mW + 700-mW Speaker Output at $R_L = 8 \Omega$
- **Power Supply Voltage**
 - 1.71 V to 3.6 V for Digital I/O Section
 - 1.71 V to 3.6 V for Digital Core Section
 - 2.4 V to 3.6 V for Analog Section
 - 2.4 V to 3.6 V for Power Amplifier Section
- **Low Power Dissipation:**
 - 7 mW in Playback, 1.8 V/2.4 V, 48 kHz
 - 13 mW in Record, 1.8 V/2.4 V, 48 kHz
 - 30 μ W in Power Down
- **Sampling Frequency: 5 kHz to 50 kHz**
- **Automatic Level Control for Recording**
- **Operation From a Single Clock Input Without PLL**
- **System Clock:**
 - Common-Audio Clock (256 $f_S/384 f_S$), 12/24, 13/26, 13.5/27, 19.2/38.4, 19.68/39.36 MHz
- **Headphone Plug Insert Detection**
- **2 (I²C) or 3 (SPI) Wire Serial Control**
- **Programmable Function by Register Control:**
 - Digital Attenuation of DAC: 0 dB to –62 dB
 - Power Up/Down Control for Each Module
 - 6-dB to –70-dB Gain for Analog Outputs
 - 30-dB to –12-dB Gain for Analog Inputs
 - 0/20 dB Boost Selectable for Microphone Input
 - 0-dB to –21-dB Gain for Analog Mixing
 - Parameter Settings for ALC
 - Three-Band Tone Control and 3D Sound
 - High-Pass Filter and Two-Stage Notch Filter
 - Analog Mixing
- **Pop-Noise Reduction Circuit**
- **Short and Thermal Protection Circuit**
- **Package: 5-mm × 5-mm QFN Package**
- **Operation Temperature Range: –40°C to 85°C**

APPLICATIONS

- Portable Audio Player, Cellular Phone
- Video Camcorder, Digital Still Camera
- PMP/DMB

DESCRIPTION

The PCM3793/94 is a low-power stereo CODEC designed for portable digital audio applications. The device integrates stereo digital speaker amplifier, headphone amplifier, line amplifier, line input, boost amplifier, microphone bias, programmable gain control, analog mixing, sound effects, and automatic level control (ALC). It is available in a small-footprint, 5-mm × 5-mm QFN package. The PCM3793/94 accepts right-justified, left-justified, I²S, and DSP formats, providing easy interfacing to audio DSP, decoder, and encoder chips. Sampling rates up to 50 kHz are supported. The user-programmable functions are accessible through a two- or three-wire serial control port.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE CODE | OPERATION TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER ⁽¹⁾ | TRANSPORT MEDIA |
|------------|---------|--------------|-----------------------------|-----------------|--------------------------------|---------------------|
| PCM3793RHB | 32 QFN | RHB | –40°C to 85°C | PCM3793 | PCM3793RHBT | Small tape and reel |
| | | | | | PCM3793RHBR | Large tape and reel |
| PCM3794RHB | 32 QFN | RHB | –40°C to 85°C | PCM3794 | PCM3794RHBT | Small tape and reel |
| | | | | | PCM3794RHBR | Large tape and reel |

(1) For the most current specification and package information, see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | PCM3793/94 | UNIT |
|--|------------|---------|
| Supply voltage $V_{DD}, V_{IO}, V_{CC}, V_{PA}$ | –0.3 to 4 | V |
| Ground voltage differences: DGND, AGND, PGND | ±0.1 | V |
| Input voltage | –0.3 to 4 | V |
| Input current (any pins except supplies and SPK out) | ±10 | mA |
| Ambient temperature under bias | –40 to 110 | °C |
| Storage temperature | –55 to 150 | °C |
| Junction temperature | 150 | °C |
| Lead temperature (soldering) | 260 | °C, 5 s |
| Package temperature (reflow, peak) | 260 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|-------------------------------|-----|--------|-------|
| V_{CC}, V_{PA} Analog supply voltage | 2.4 | 3.3 | 3.6 | V |
| V_{DD}, V_{IO} Digital supply voltage | 1.71 | 3.3 | 3.6 | V |
| Digital input logic family | CMOS | | | |
| Digital input clock frequency | SCKI system clock | | 18.432 | MHz |
| | LRCK sampling clock | | 48 | kHz |
| Analog output load resistance | LOL and LOR | | 10 | kΩ |
| | HPOL and HPOR | | 16 | Ω |
| | SPOLP, SPOLN, SPORP and SPORN | | 8 | Ω |
| Analog output load capacitance | | | | 30 pF |
| Digital output load capacitance | | | | 10 pF |
| T_A Operating free-air temperature | –40 | | | 85 °C |

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = $256 f_S$, and 16-bit data (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | PCM3793RHB, PCM3794RHB | | | UNIT |
|--|-----------------------------------|-------------------------|---|-----|---------------|---------------|
| | | | MIN | TYP | MAX | |
| Audio Data Characteristics | | | | | | |
| DATA FORMAT | | | | | | |
| Resolution | | | 16 | | | Bits |
| Audio data interface format | | | I ² S, left-, right-justified, DSP | | | |
| Audio data bit length | | | 16 | | | Bits |
| Audio data format | | | MSB first, 2s complement | | | |
| Sampling frequency (f_S) | | | 5 | | 50 | kHz |
| System clock | | $V_{DD} < 2\text{ V}$ | | | 27 | MHz |
| | | $V_{DD} > 2\text{ V}$ | | | 40 | |
| Digital Input/Output | | | | | | |
| Logic family | | | CMOS compatible | | | |
| V_{IH} | Input logic level | | $0.7 V_{IO}$ | | | VDC |
| V_{IL} | | | $0.3 V_{IO}$ | | | VDC |
| I_{IH} | Input logic current | $V_{IN} = 3.3\text{ V}$ | | | 10 | μA |
| I_{IL} | | $V_{IN} = 0\text{ V}$ | | | -10 | |
| V_{OH} | Output logic level | $I_{OH} = -2\text{ mA}$ | $0.75 V_{IO}$ | | | VDC |
| V_{OL} | | $I_{OL} = 2\text{ mA}$ | | | $0.25 V_{IO}$ | VDC |
| Digital Input to Line Output Through DAC (LOL, LOR, and MONO) | | | | | | |
| $R_L = 10\text{ k}\Omega$, ALC = OFF, volume = 0 dB, speaker = powered down, analog mixing = disabled | | | | | | |
| DYNAMIC PERFORMANCE | | | | | | |
| Full-scale output voltage | | 0 dB | 2.828 | | Vp-p | |
| | | | 1 | | Vrms | |
| Dynamic range | | EIAJ, A-weighted | 93 | | dB | |
| SNR | Signal-to-noise ratio | EIAJ, A-weighted | 86 | 93 | dB | |
| Channel separation | | | 91 | | dB | |
| THD+N | Total harmonic distortion + noise | 0 dB | 0.008% | | | |
| Load resistance | | | 10 | | k Ω | |
| Line Input to Line Output Through Mixing Path (LOL, LOR, and MONO) | | | | | | |
| $R_L = 10\text{ k}\Omega$, ALC = OFF, volume = 0 dB, speaker = powered down, analog mixing = enabled | | | | | | |
| DYNAMIC PERFORMANCE | | | | | | |
| Full-scale input and output voltage | | 0 dB | 2.828 | | Vp-p | |
| | | | 1 | | Vrms | |
| SNR | Signal-to-noise ratio | EIAJ, A-weighted | 84 | 93 | dB | |

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = 256 f_S , and 16-bit data (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | PCM3793RHB, PCM3794RHB | | | UNIT |
|---|--|------------------------|-----|----------|------|
| | | MIN | TYP | MAX | |
| Digital Input to Headphone Output Through DAC (HPOL and HPOR) | | | | | |
| $R_L = 16\ \Omega$ or $32\ \Omega$, ALC = OFF, volume = 0 dB, speaker = powered down, analog mixing = disabled, not capless mode | | | | | |
| DYNAMIC PERFORMANCE | | | | | |
| Full-scale output voltage | 0 dB | 2.828 | | Vp-p | |
| | | 1 | | Vrms | |
| SNR Signal-to-noise ratio | EIAJ, A-weighted | 84 | 93 | dB | |
| THD+N Total harmonic distortion + noise | 30 mW, $R_L = 32\ \Omega$, volume = 0 dB | 0.1% | | | |
| | 40 mW, $R_L = 16\ \Omega$, volume = -1 dB | 0.03% | | | |
| Load resistance | | 16 | | Ω | |
| PSRR Power-supply rejection ratio | 200 Hz, 140 mVp-p | -40 | | dB | |
| | 1 kHz, 140 mVp-p | -45 | | | |
| | 20 kHz, 140 mVp-p | -32 | | | |
| Line Input to Headphone Output Through Mixing Path (HPOL and HPOR) | | | | | |
| $R_L = 16\ \Omega$ or $32\ \Omega$, ALC = OFF, volume = 0 dB, speaker = powered down, analog mixing = enabled, not capless mode | | | | | |
| DYNAMIC PERFORMANCE | | | | | |
| Full-scale output voltage | 0 dB | 2.828 | | Vp-p | |
| | | 1 | | Vrms | |
| SNR Signal-to-noise ratio | EIAJ, A-weighted | 84 | 93 | dB | |
| Load resistance | | 16 | | Ω | |
| Digital Input to Speaker Output Through DAC (SPOLP, SPOLN, SPORP, and SPORN): PCM3793 | | | | | |
| $R_L = 8\ \Omega$, ALC = OFF, volume = 0 dB, headphone = powered down, analog mixing = disabled | | | | | |
| DYNAMIC PERFORMANCE | | | | | |
| Full-scale output voltage | 0 dB | 2.52 | | Vp-p | |
| | | 0.9 | | Vrms | |
| SNR Signal-to-noise ratio | EIAJ, A-weighted | 84 | 93 | dB | |
| THD+N Total harmonic distortion + noise | 400 mW, $R_L = 8\ \Omega$, volume = 0 dB | 0.3% | | | |
| Load resistance | | 8 | | Ω | |
| PSRR Power-supply rejection ratio | 200 Hz, 140 mVp-p | -50 | | dB | |
| | 1 kHz, 140 mVp-p | -45 | | | |
| | 20 kHz, 140 mVp-p | -25 | | | |
| Line Input to Speaker Output Through Mixing Path (SPOLP, SPOLN, SPORP, and SPORN): PCM3793 | | | | | |
| $R_L = 8\ \Omega$, ALC = OFF, volume = 0 dB, headphone = powered down, analog mixing = enabled | | | | | |
| DYNAMIC PERFORMANCE | | | | | |
| Full-scale output voltage | 0 dB | 2.52 | | Vp-p | |
| | | 0.9 | | Vrms | |
| SNR Signal-to-noise ratio | EIAJ, A-Weighted | 84 | 93 | dB | |

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = $256 f_S$, and 16-bit data (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | PCM3793RHB, PCM3794RHB | | | UNIT | |
|--|-----------------------------------|------------------------|--------|------------|---------------|----|
| | | MIN | TYP | MAX | | |
| Line Input to Digital Output Through ADC (AIN1L/R, AIN2L/R, AIN3L, and AIN3L/R) | | | | | | |
| ALC = OFF, microphone boost = 0 dB, PGA = 0 dB, speaker and headphone = powered down, analog mixing = disabled | | | | | | |
| DYNAMIC PERFORMANCE | | | | | | |
| Full-scale input voltage | 0 dB | 2.828 | | | Vp-p | |
| | | 1 | | | Vrms | |
| Dynamic range | EIAJ, A-weighted | 90 | | | dB | |
| SNR | Signal-to-noise ratio | EIAJ, A-weighted | 83 | 90 | dB | |
| | Channel separation | | 87 | | | dB |
| THD+N | Total harmonic distortion + noise | -1 dB | 0.009% | | | |
| ANALOG INPUT | | | | | | |
| Center voltage | | 0.5 V_{CC} | | | V | |
| Input impedance | | 10 | 20 | k Ω | | |
| Microphone Bias | | | | | | |
| ALC = OFF, microphone boost = 0 dB, PGA = 0 dB, speaker and headphone = powered down, analog mixing = disabled | | | | | | |
| Bias voltage | | 0.75 V_{CC} | | | V | |
| Bias source current | | 2 | | | mA | |
| Output noise | | 14 | | | μV | |
| Filter Characteristics | | | | | | |
| INTERPOLATION FILTER FOR DAC | | | | | | |
| Pass band | | 0.454 f_S | | | | |
| Stop band | | 0.546 f_S | | | | |
| Pass-band ripple | | ± 0.04 | | | dB | |
| Stop-band attenuation | | -50 | | | dB | |
| Group delay | | 19/ f_S | | | s | |
| De-emphasis error | | ± 0.1 | | | dB | |
| ANALOG FILTER FOR DAC | | | | | | |
| Frequency response | $f = 20\text{ kHz}$ | ± 0.2 | | | dB | |
| DECIMATION FILTER FOR ADC | | | | | | |
| Pass band | | 0.408 f_S | | | | |
| Stop band | | 0.591 f_S | | | | |
| Pass-band ripple | | ± 0.02 | | | dB | |
| Stop-band attenuation | $f < 3.268 f_S$ | -60 | | | dB | |
| Group delay | | 17/ f_S | | | s | |
| HIGH-PASS FILTER FOR ADC | | | | | | |
| Frequency response | -3 dB, $f_c = 4\text{ Hz}$ | 3.74 | | | Hz | |
| | -0.5 dB, $f_c = 4\text{ Hz}$ | 10.66 | | | | |
| | -0.1 dB, $f_c = 4\text{ Hz}$ | 24.2 | | | | |
| | -3 dB, $f_c = 240\text{ Hz}$ | 235.68 | | | | |
| | -0.5 dB, $f_c = 240\text{ Hz}$ | 609.95 | | | | |
| | -0.1 dB, $f_c = 240\text{ Hz}$ | 2601.2 | | | | |

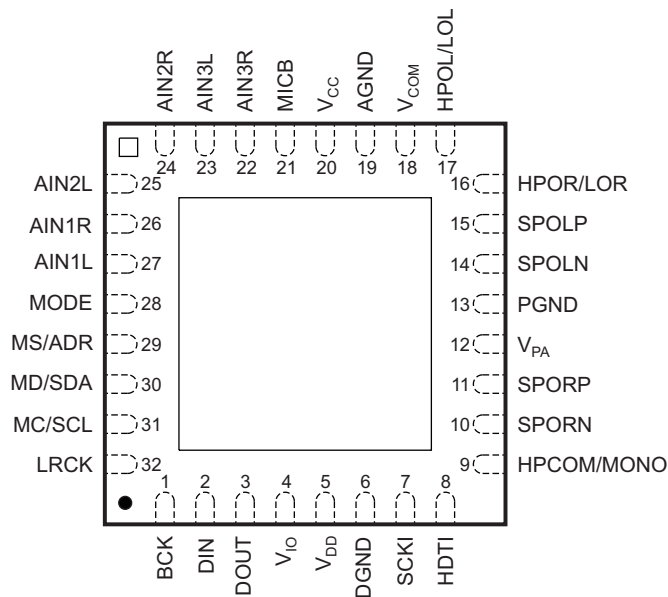
ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = 256 f_S , and 16-bit data (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | PCM3793RHB, PCM3794RHB | | | UNIT |
|--|--------------------|--------------------------------|------------------------|------|-------|---------------------------|
| | | | MIN | TYP | MAX | |
| Power Supply and Supply Current | | | | | | |
| V_{IO} | Voltage range | V_{IO} | 1.71 | 3.3 | 3.6 | VDC |
| V_{DD} | | V_{DD} | 1.71 | 3.3 | 3.6 | |
| V_{CC} | | V_{CC} | 2.4 | 3.3 | 3.6 | |
| V_{PA} | | V_{PA} | 2.4 | 3.3 | 3.6 | |
| Supply current | | BPZ input, all active, no load | | 24.3 | 35 | mA |
| | | All inputs are held static | | 9 | 50 | μA |
| Power dissipation | | BPZ input | | 80.2 | 115.5 | mW |
| | | All inputs are held static | | 30 | 165 | μW |
| Temperature Condition | | | | | | |
| Operation temperature | | | -40 | | 85 | $^\circ\text{C}$ |
| θ_{JA} | Thermal resistance | | | 30 | | $^\circ\text{C}/\text{W}$ |

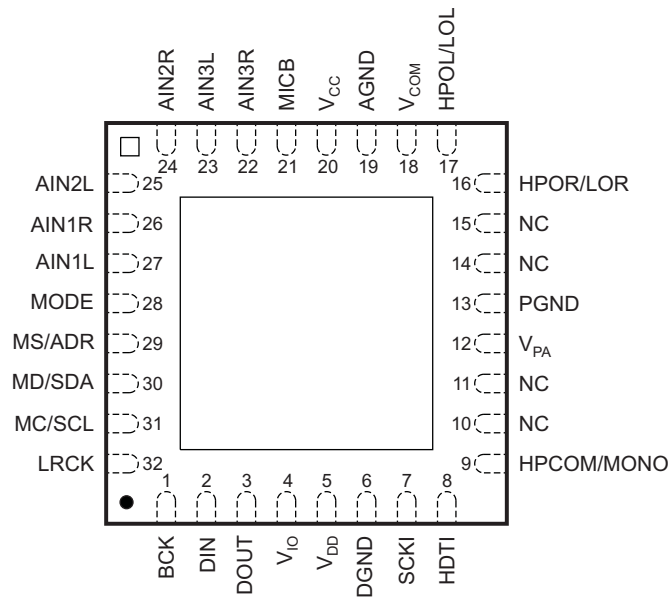
PIN ASSIGNMENTS

PCM3793RHB
(TOP VIEW)



P0048-03

PCM3794RHB
(TOP VIEW)

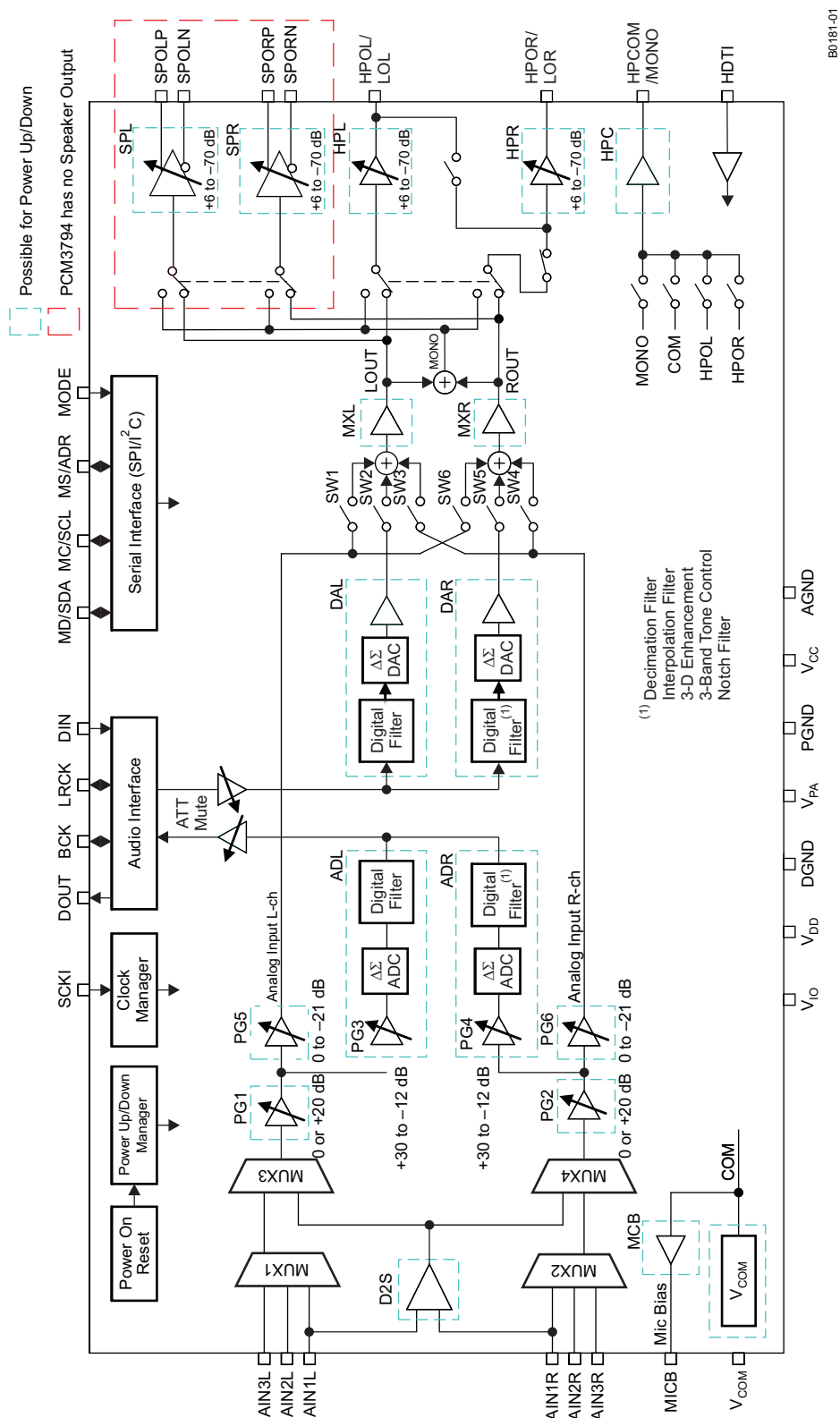


P0048-04

Table 1. TERMINAL FUNCTIONS

| TERMINAL | | | I/O | DESCRIPTION |
|------------------|------------|------------|-----|---|
| NAME | PCM3793RHB | PCM3794RHB | | |
| AGND | 19 | 19 | – | Ground for analog |
| AIN1L | 27 | 27 | I | Analog input 1 for L-channel |
| AIN1R | 26 | 26 | I | Analog input 1 for R-channel |
| AIN2L | 25 | 25 | I | Analog input 2 for L-channel |
| AIN2R | 24 | 24 | I | Analog input 2 for R-channel |
| AIN3L | 23 | 23 | I | Analog input 3 for L-channel |
| AIN3R | 22 | 22 | I | Analog input 3 for R-channel |
| BCK | 1 | 1 | I/O | Serial bit clock |
| DGND | 6 | 6 | – | Digital ground |
| DIN | 2 | 2 | I | Serial audio data input |
| DOUT | 3 | 3 | O | Serial audio data output |
| HDTI | 8 | 8 | I | Headphone plug insertion detection |
| HPCOM/MONO | 9 | 9 | O | Headphone common/mono line output |
| HPOL/LOL | 17 | 17 | O | Headphone/lineout for R-channel |
| HPOR/LOR | 16 | 16 | O | Headphone/lineout for L-channel |
| LRCK | 32 | 32 | I/O | Left and right channel clock |
| MC/SCL | 31 | 31 | I | Mode control clock for three-wire/two-wire interface |
| MD/SDA | 30 | 30 | I/O | Mode control data for three-wire/two-wire interface |
| MICB | 21 | 21 | O | Microphone bias source output |
| MODE | 28 | 28 | I | Two- or three-wire interface selection (LOW: SPI, HIGH: I ² C) |
| MS/ADR | 29 | 29 | I | Mode control select for three-wire/two-wire interface |
| PGND | 13 | 13 | – | Ground for speaker power amplifier |
| SCKI | 7 | 7 | I | System clock |
| SPOLN | 14 | – | O | Speaker output L-channel for negative (PCM3793) |
| SPOLP | 15 | – | O | Speaker output L-channel for positive (PCM3793) |
| SPORN | 10 | – | O | Speaker output R-channel for negative (PCM3793) |
| SPORP | 11 | – | O | Speaker output R-channel for positive (PCM3793) |
| V _{CC} | 20 | 20 | – | Analog power supply |
| V _{COM} | 18 | 18 | – | Analog common voltage |
| V _{DD} | 5 | 5 | – | Power supply for digital core |
| V _{IO} | 4 | 4 | – | Power supply for digital I/O |
| V _{PA} | 12 | 12 | – | Power supply for power amplifier |

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE CURVES

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$, $f_s = 8\text{ to }48\text{ kHz}$, system clock = $256 f_s$, and 16-bit data, unless otherwise noted.

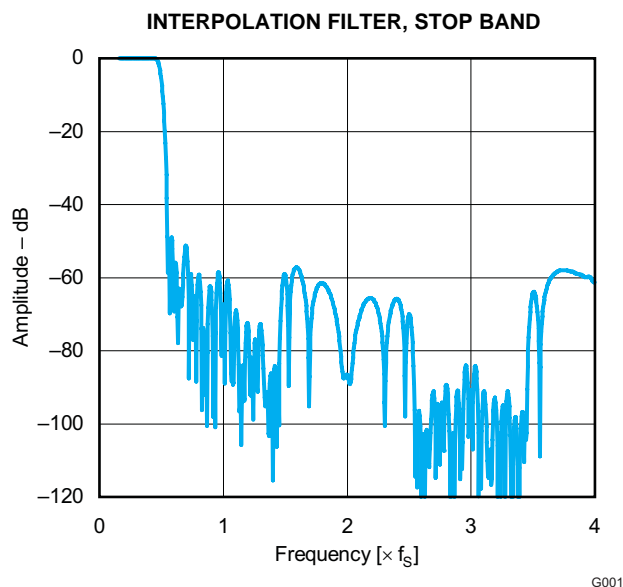


Figure 1.

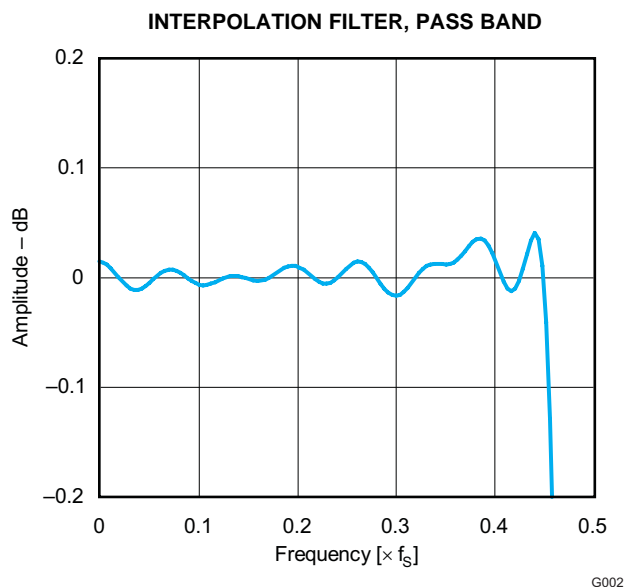


Figure 2.

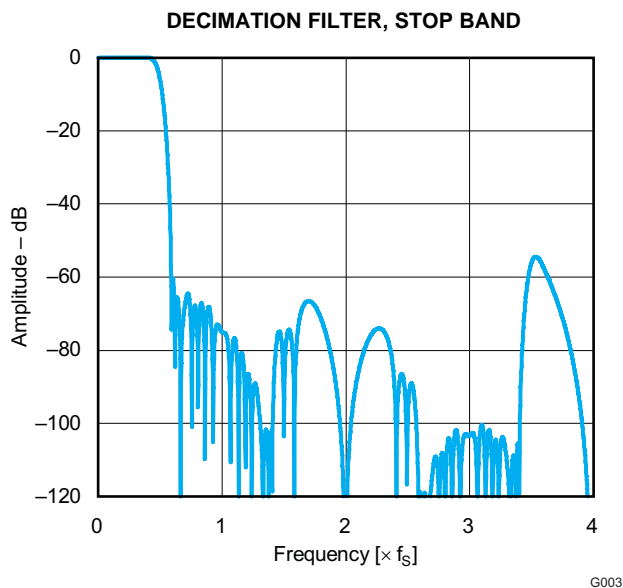


Figure 3.

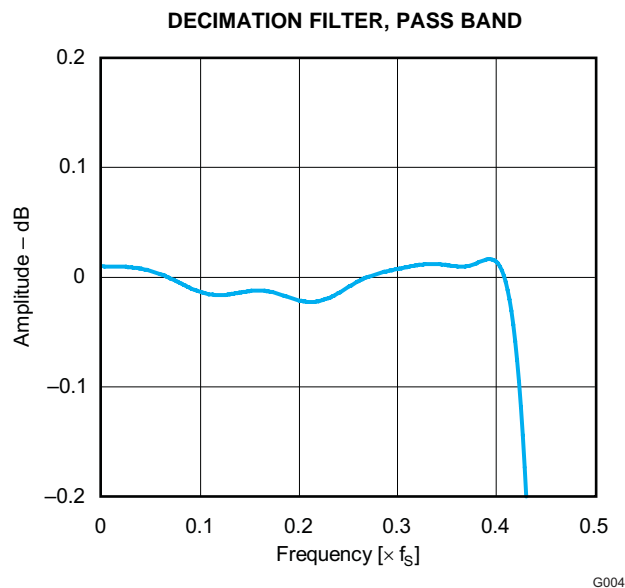


Figure 4.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$, $f_S = 8\text{ to }48\text{ kHz}$, system clock = $256 f_S$, and 16-bit data, unless otherwise noted.

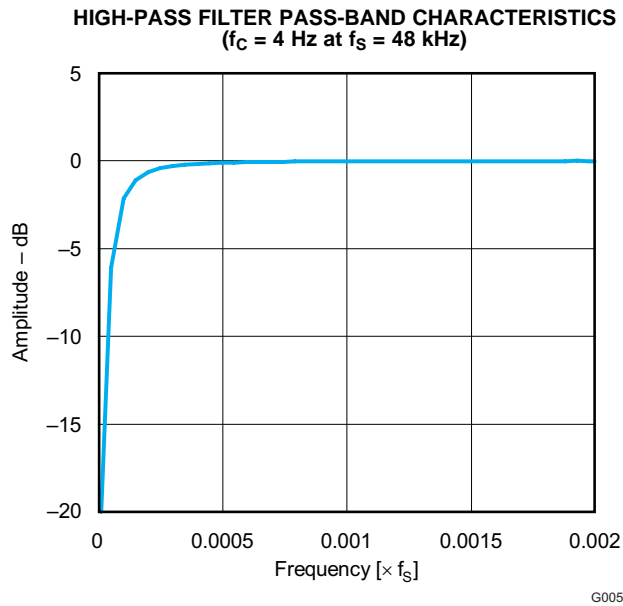


Figure 5.

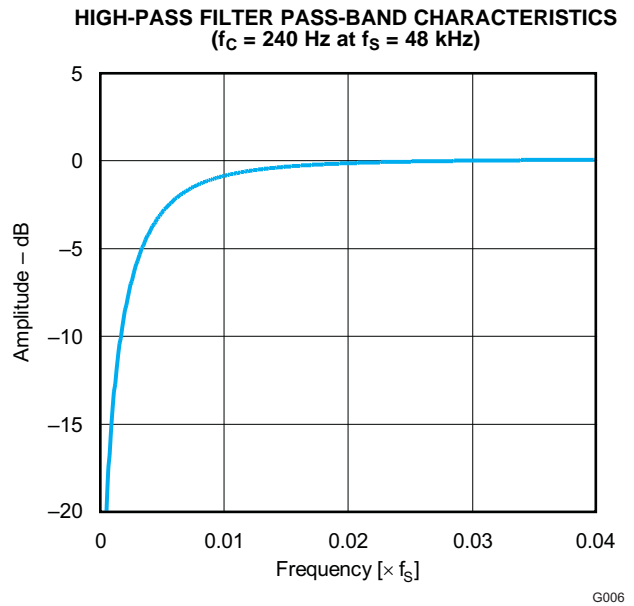


Figure 6.

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$, and 16-bit data, unless otherwise noted.

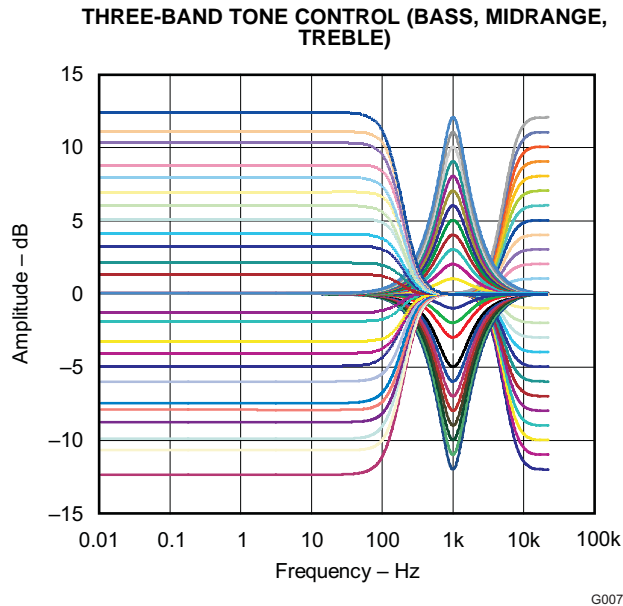


Figure 7.

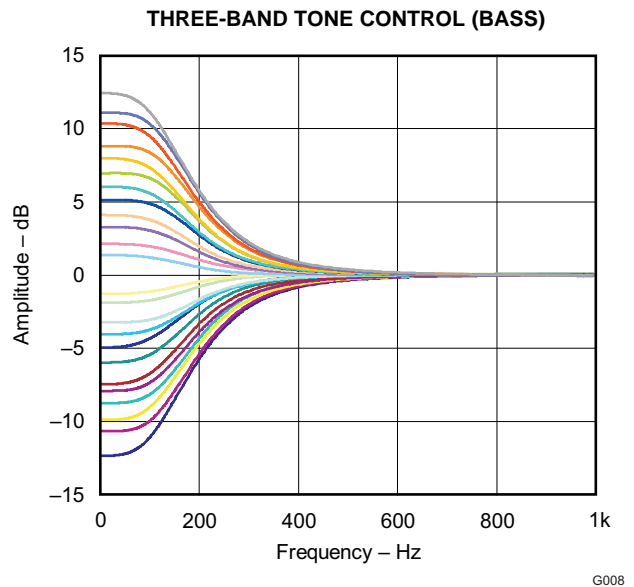
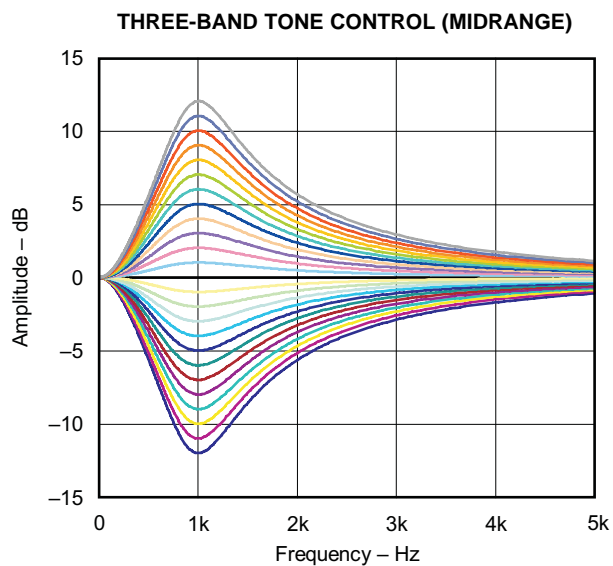


Figure 8.

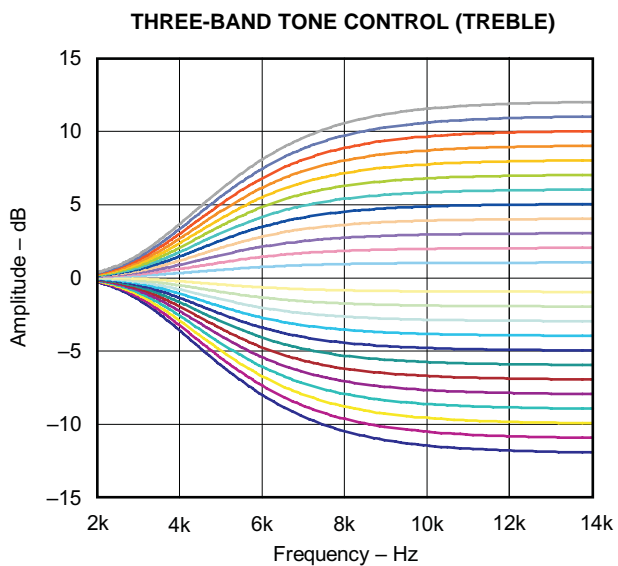
TYPICAL PERFORMANCE CURVES (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$, and 16-bit data, unless otherwise noted.



G009

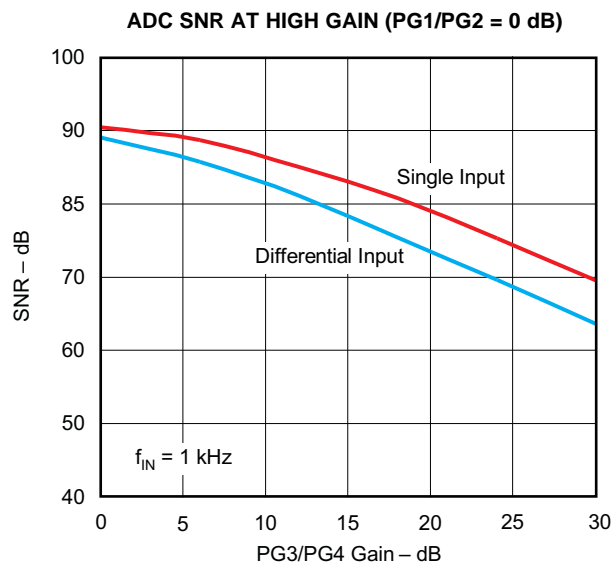
Figure 9.



G010

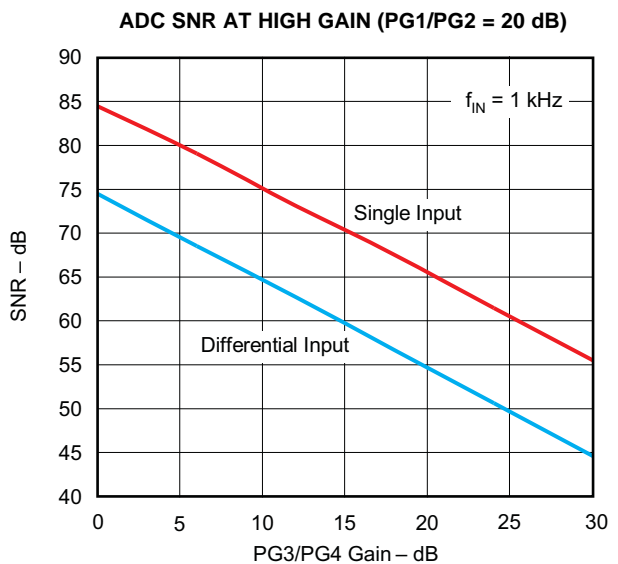
Figure 10.

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = $256 f_S$, and 16-bit data, unless otherwise noted.



G011

Figure 11.



G012

Figure 12.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = $256 f_S$, and 16-bit data, unless otherwise noted.

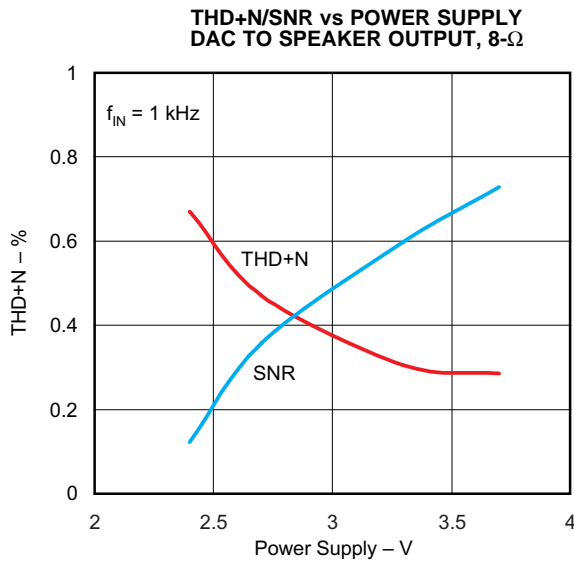


Figure 13.

G013

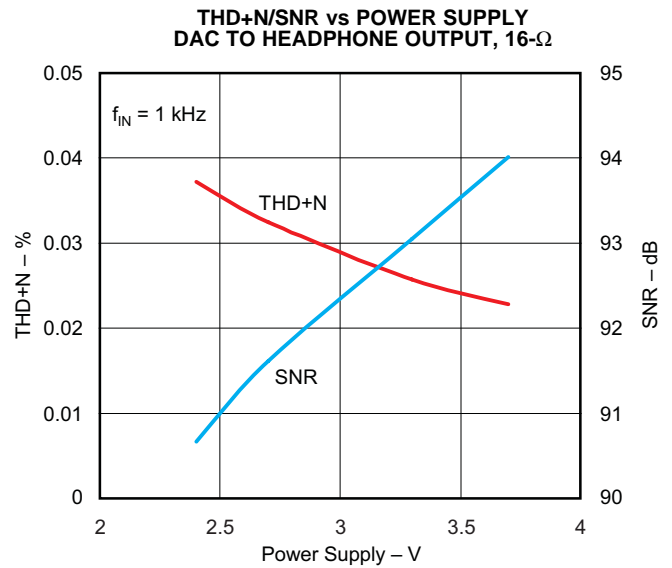


Figure 14.

G014

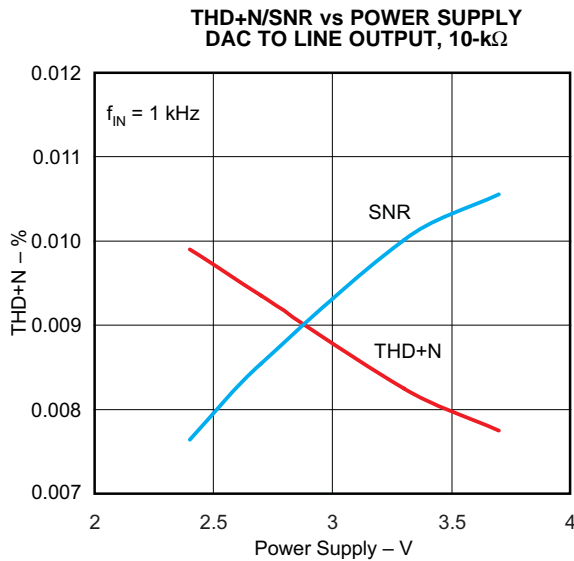


Figure 15.

G015

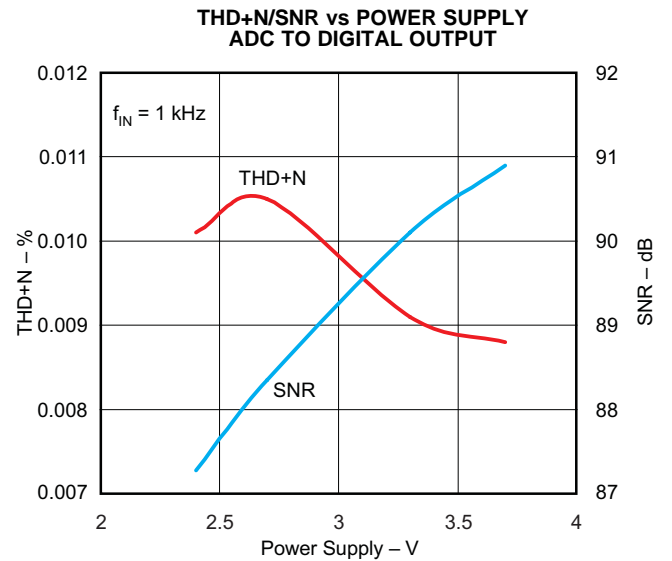


Figure 16.

G016

TYPICAL PERFORMANCE CURVES (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = $256 f_S$, and 16-bit data, unless otherwise noted.

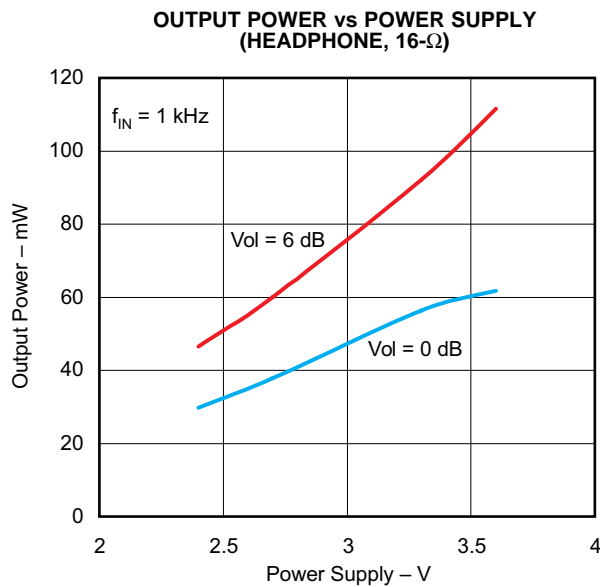


Figure 17.

G017

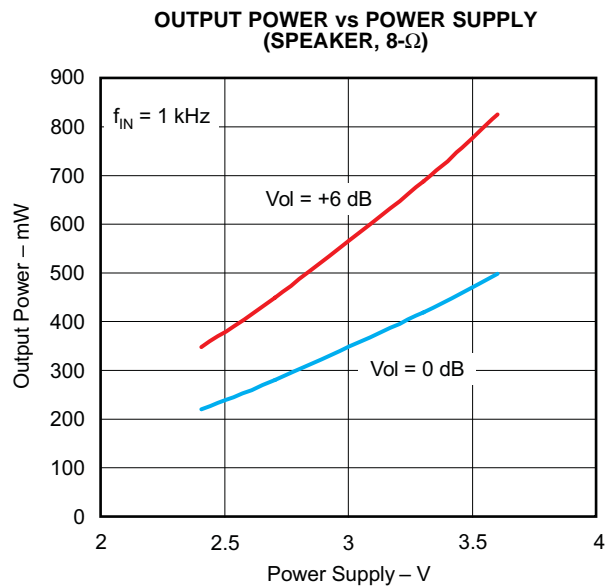


Figure 18.

G018

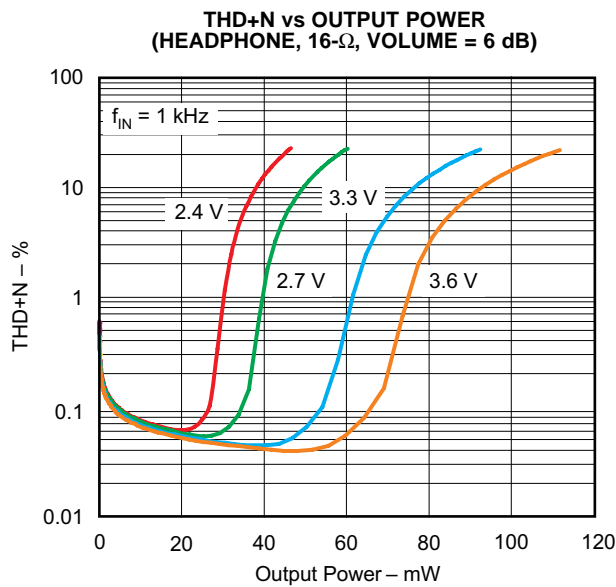


Figure 19.

G019

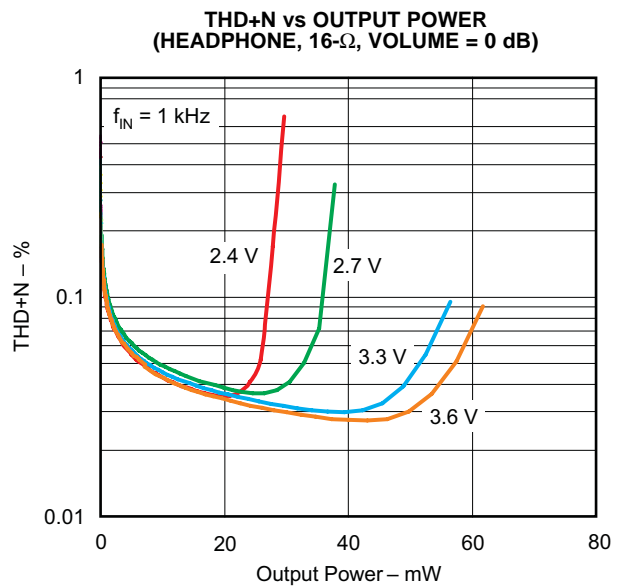


Figure 20.

G020

TYPICAL PERFORMANCE CURVES (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{IO} = V_{CC} = V_{PA} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = $256 f_S$, and 16-bit data, unless otherwise noted.

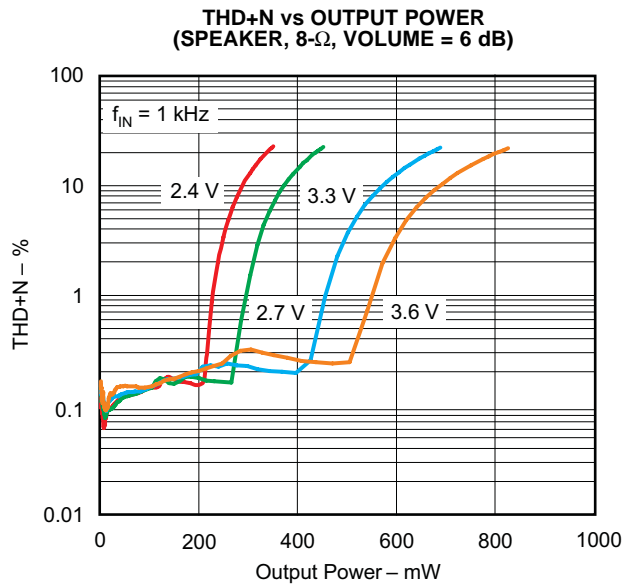


Figure 21.

G021

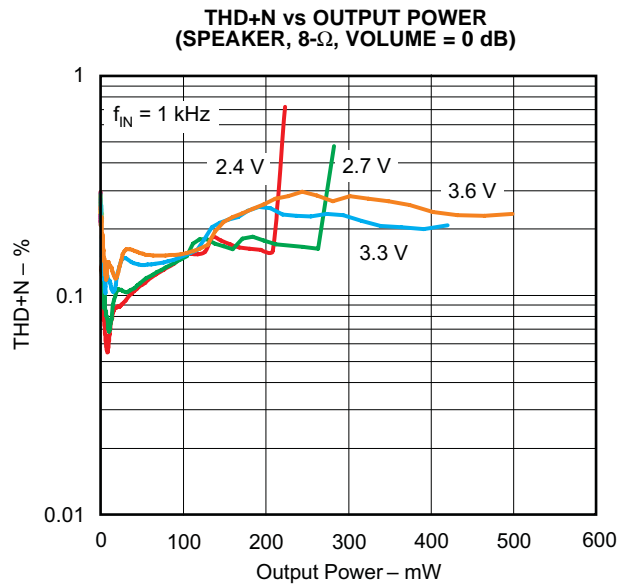


Figure 22.

G022

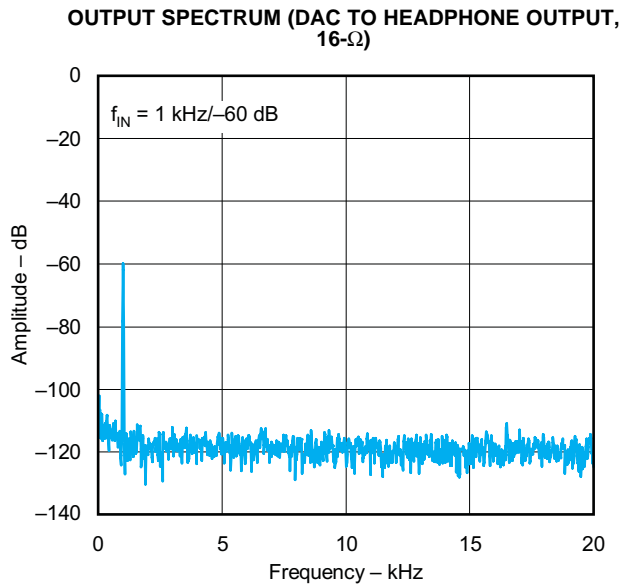


Figure 23.

G023

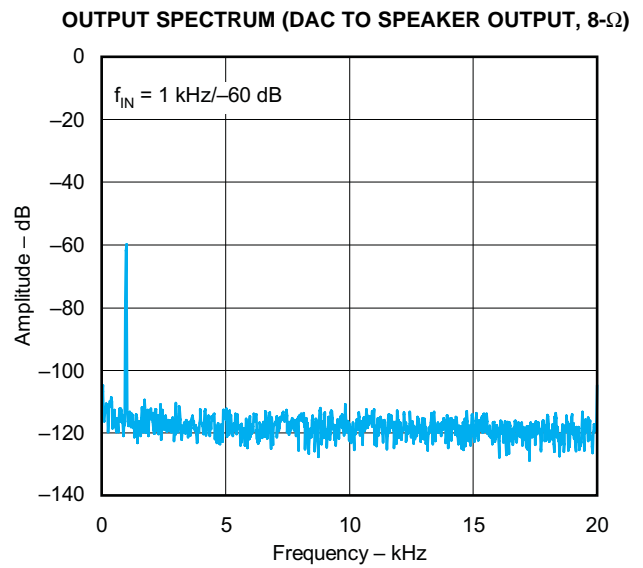


Figure 24.

G024

PCM3793/94 DESCRIPTION

Analog Input

The AIN1L, AIN1R, AIN2L, AIN2R, AIN3L, and AIN3R pins can be used as microphone or line inputs with selectable 0- or 20-dB boost and 1-V_{rms} input. All analog inputs have high input impedance (20 k Ω), which is not changed by gain settings. One pair of inputs is selected by register 87 (AIL[1:0], AIR[1:0]). AIN1L and AIN1R can be used as monaural differential inputs.

Gain Settings for Analog Input

Analog signals can be adjusted from 30 dB to –12 dB in 1-dB steps following the 0- or 20-dB boost amplifier. The gain level can be set for each channel by registers 79 and 80 (ALV[5:0], ARV[5:0]).

A/D Converter

The ADC includes a multilevel delta-sigma modulator, aliasing filter, decimation filter, high-pass filter, and notch filter and can accept a 1-V_{rms} full-scale voltage input. The decimation filter has a digital soft mute controlled by register 81 (RMUL, RMUR). The high-pass filter can be disabled by register 81 (HPF[1:0]) and the notch filter can be disabled by registers 96 to 104 if it is not necessary to cancel a dc offset or compensate for wind noise.

D/A Converter

The DAC includes a multilevel delta-sigma modulator and interpolation filter. These can be used to obtain high PSRR, low jitter sensitivity, and low out-of-band noise quickly and easily. The interpolation filter includes digital attenuator, digital soft mute, three-band tone control (bass, midrange and treble), and 3-D sound controlled by registers 92 to 95. The de-emphasis filter (32, 44.1 and 48 kHz) is controlled by registers 68 to 70 (ATL[5:0], ATR[5:0], PMUL, PMUR, DEM[1:0]). Oversampling rate control can reduce out-of-band noise when operating at low sampling rate by using register 70 (OVER).

Common Voltage

The V_{COM} pin is normally biased to 0.5 V_{CC}, and it provides the common voltage to internal circuitry. It is recommended that a 10- μ F capacitor be connected between this pin and ground to provide clean voltage and avoid pop noise. The PCM3793/94 may have a little pop noise on each analog output if a capacitor smaller than 10 μ F is used.

Line Output

The HPOL/LOL and HPOR/LOR and HPCOM/MONO pins can be used as a monaural single-ended, monaural differential, or stereo single-line output with 1-V_{rms} output by register 74 (HPS[1:0]). The line outputs can drive a 10-k Ω load. These outputs include an analog volume amplifier, except for the HPCOM/MONO pin that can be set from 6 dB to –70 dB and mute with 0.5-, 1-, 2- or 4-dB steps for each output, as controlled by registers 64 and 65 (HLV[5:0], HRV[5:0], HMUL, HMUR). A dc blocking capacitor is not required when connecting to an external speaker amplifier with monaural differential input. The center voltage is 0.5 V_{CC} with zero data input.

Headphone Output

The HPOL/LOL, HPOR/LOR, and HPCOM/MONO pins are stereo, monaural, or monaural differential headphone outputs with more than 30 or 40 mW_{rms} output power into a 32- or 16- Ω load, either through a dc blocking capacitor or without a capacitor, as selected by register 74 (HPS[2:0]). These outputs include analog volume amplifiers, except for the HPCOM/MONO pin, which can be set from 6 dB to –70 dB with 0.5-, 1-, 2- or 4-dB steps for each output using registers 64 and 65 (HLV[5:0], HRV[5:0], HMUL, HMUR). The center voltage is 0.5 V_{CC} with zero data input.

Headphone Plug Insertion Detection

The HDTI pin detects the insertion status of headphone plug and writes the status to register 77 (HPDS), which can be read by the I²C interface. The polarity of the status indication can be inverted by register 75 (HPDP). The headphone and speaker amplifiers are disabled or enabled automatically by headphone plug insertion/extraction if register 75, HPDE = 1. They are controlled by register settings if register 75, HPDE = 0. HPCOM/MONO is not affected by the status when register 74, CMS[0] = 1.

Speaker Output (Class-D, PCM3793)

The SPOLP, SPOLN and SPORP, SPORN pins are stereo or mono speaker differential outputs (BTL) with a maximum of 700 mWrms ($V_{PA} = 3.6$ V, volume = 6 dB) into an 8- Ω load. The digital speaker amplifier offers maximum battery life and minimum heat, eliminates the LC low-pass filter, and includes analog volume amplification for each output from 6 dB to –70 dB with 0.5-, 1-, 2- or 4-dB steps, which can be set by register 66, 67 (SLV[5:0], SLR[5:0]). Spectrum spreading technology and selectable switching frequency to reduce EMI noise is controlled by register 71 (DFQ[2:0], SPS[1:0] and SPSE). The speaker amplifiers have a thermal shutdown circuit which detects when the device temperature reaches approximately 150°C; then the speaker amplifier is powered down.

Analog Mixing and Bypass

Mixing amplifiers (MXL, MXR) mix gain-controlled analog inputs from the AIN pins which have bypassed ADC and DAC and direct the mixed signal to the headphone or speaker outputs. Analog mixing is controlled by register 87 (AD2S, AIR[1:0], AIL[1:0]), register 88 (MXR[2:0], MXL[2:0]), and register 89 (GMR[2:0], GML[2:0]). The analog mixing functions are suitable for FM radio, headset, and another analog sources without an ADC.

Microphone Bias

The MICB pin is the microphone bias source for an external microphone and can provide 2 mA (typical) bias current.

Automatic Level Control (ALC) for Recording

The sound for microphone recording should be expanded to a suitable level without saturation. The digitally controlled automatic level control (ALC) provides automatic expansion for small input signals and compression for large input signals while recording. The expansion level, compression level, attack time, and recovery time can be selected by register 83. The register 83 description explains the details of these settings.

3-D Sound

A 3-D sound effect is provided by mixing L-channel and R-channel data with band pass filter that can be controlled two parameters, mixing ratio and band pass filter characteristic by register 95 (3DP[3:0], 3FLO). The 3-D sound effect can be applied to the DAC digital input or ADC digital output, as selected by register 95 (SDAS).

Three-Band Tone Control

Tone control has bass, midrange, and treble controls that can be adjusted from 12 dB to –12 dB in 1-dB steps by registers 92 to 94 (LGA[4:0], MGA[4:0] and HGA[4:0]). Register 92 (LPAE) attenuates the digital input signal automatically to prevent clipping of the output signal at settings above 0 dB for bass control. LPAE has no effect on midrange and treble controls.

High-Pass Filter and Notch Filter

The high-pass filter eliminates the dc offset of the ADC analog signal and can be set for a cutoff frequency of 4 Hz or 240 Hz at of 48-kHz sampling frequency by register 81 (HPF[1:0]). A register 95 (SDAS) selection applies the filter to either the DAC digital input or the ADC digital output.

Notch filters are provided to remove noise of a particular frequency, such as CCD noise, motor noise, or other mechanical noise in a particular application. The PCM3793/94 has two notch filters for which the center frequency and frequency bandwidth can be programmed by registers 96 to 104. A register 95 (SDAS) selection applies the filter to either the DAC digital input or the ADC digital output.

Digital Monaural Mixing

Register 96 (MXEN) enables or disables the internal mixing of stereo digital data to monaural digital data.

Zero-Cross Detection

Zero-cross detection minimizes audible zipper noise while changing analog volume and digital attenuation. This function can be applied to digital input or digital output by register 86 (ZCRS).

Short Protection

The short-circuit protection on each headphone output prevents damage to the device while an output is shorted to V_{PA} , an output is shorted to PGND, or any two outputs are shorted together. When the short circuit is detected on the outputs, the PCM3793/94 powers down the shorted amplifier at once. The short-protection status can be monitored by reading register 77 (STHC, STHL, SCHR) through the I²C interface. Short-circuit protection operates in any enabled headphone amplifier.

Thermal Protection

The thermal protection on the speaker amplifier prevents damage to the device when the internal die temperature exceeds approximately 150°C. Once the die temperature exceeds the thermal set point, all analog outputs are powered down. This status can be reset by setting register 76 (RLSR, RLSL) and can be watched by reading register 77 (STSR, STSL) on the two-wire (I²C) interface. Thermal protection operates in any enabled speaker amplifier.

Pop-Noise Reduction Circuit

The pop-noise reduction circuit prevents audible noise when turning the power supply on/off and powering the device up/down in portable applications. It is recommended to establish the register settings in the sequence that is shown in [Table 3](#) and [Table 4](#). No particular external parts are required, and power-supply sequencing is not necessary.

Power Up/Down for Each Module

Using register 72 (PMXL, PMXR), register 73 (PBIS, PDAR, PDAL, PHPC, PHPR, PHPL, PSPR, PSPL), register 82 (PAIR, PAIL, PADS, PMCB, PADR, PADL), and register 90 (PCOM), unused modules can be powered down to minimize power consumption (7 mW during playback only and 13 mW when recording only).

Digital Interface

All digital I/O pins can interface at various power supply voltages. The V_{IO} pin can be connected to a 1.71-V to 3.6-V power supply.

Power Supply

The V_{CC} pin and the V_{PA} pin can be connected to 2.4 V to 3.6 V. The same voltage must be applied to both pins. The V_{DD} pin and the V_{IO} pin can be connected to 1.71 V to 3.6 V. A different voltage can be applied to each of these pins (for example, $V_{DD} = 1.8$ V, $V_{IO} = 3.3$ V).

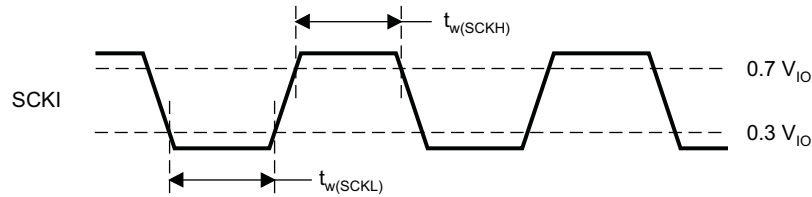
DESCRIPTION OF OPERATION

System Clock Input

The PCM3793/94 can accept clocks of various frequencies without a PLL. They are used for clocking the digital filters and automatic level control and delta-sigma modulators and are classified as common-audio and application-specific clocks. [Table 2](#) shows frequencies of the common-audio clock and application-specific clock. [Figure 25](#) shows the timing requirements for system clock inputs. The sampling rate and frequency of the system clocks are determined by the settings of register 86 (MSR[2:0]) and register 85 (NPR[5:0]). Note that the sampling rate of the application-specific clock has a little sampling error.

Table 2. System Clock Frequencies

| CLOCK | FREQUENCIES |
|----------------------------|--|
| Common-audio clock | 11.2896, 12.288, 16.9344, 18.432 MHz |
| Application-specific clock | 12, 13, 13.5, 24, 26, 27, 19.2, 19.68, 38.4, 39.36 MHz |



T0005-12

| PARAMETERS | SYMBOL | MIN | UNITS |
|-----------------------------------|-----------------------|-----|-------|
| System-clock pulse duration, high | t _w (SCKH) | 7 | ns |
| System-clock pulse duration, low | t _w (SCKL) | 7 | ns |

Figure 25. System Clock Timing

Power-On Reset and System Reset

The power-on-reset circuit outputs a reset signal, typically at V_{DD} = 1.2 V, and this circuit does not depend on the voltage of other power supplies (V_{CC}, V_{PA} and V_{IO}). Internal circuits are cleared to default status, then signals are removed from all analog and digital outputs. The PCM3793/94 does not require any power supply sequencing. Register data must be written after turning all power supplies on.

System reset is enabled by setting register 85 (SRST), and all register are cleared automatically. All circuits are reset to their default status at once. Note that the PCM3793/94 has audible pop noise on the analog outputs when enabling SRST.

Power On/Off Sequence

To reduce audible pop noise, a sequence of register settings is required after turning all power supplies on when powering up, or before turning the power supplies off when powering down. If some modules are not required for a particular application or operation, they should be placed in the power-down state after performing the power-on sequence. The recommended power-on and power-off sequences are shown in Table 3 and Table 4, respectively.

Table 3. Recommended Power-On Sequence

| STEP | REGISTER SETTINGS | NOTE |
|------|-------------------|---|
| 1 | – | Turn on all power supplies ⁽¹⁾ |
| 2 | 4027h | Headphone amplifier L-ch volume (–6 dB) ⁽²⁾ |
| 3 | 4127h | Headphone amplifier R-ch volume (–6 dB) ⁽²⁾ |
| 4 | 4227h | Speaker amplifier L-ch volume (–6 dB) ⁽²⁾ |
| 5 | 4327h | Speaker amplifier R-ch volume (–6 dB) ⁽²⁾ |
| 6 | 4427h | Digital attenuator L-ch (–24 dB) ⁽²⁾ |
| 7 | 4527h | Digital attenuator R-ch (–24 dB) ⁽²⁾ |
| 8 | 4620h | DAC audio interface format (left-justified) ⁽³⁾ |
| 9 | 4BC0h | Headphone detection enable and inverting polarity. Short and thermal detection enable |
| 10 | 5102h | ADC audio interface format (left-justified) ⁽³⁾ |
| 11 | 5A10h | V _{COM} ramp up/down time control. PG1, PG2 gain control (0 dB) |
| 12 | 49E0h | DAC (DAL, DAR) and analog bias power up |
| 13 | 5601h | Zero-cross detection enable |
| 14 | 4803h | Analog mixer (MXL, MXR) power up |
| 15 | 5811h | Analog mixer input (SW2, SW5) select |
| 16 | 49FCh | Headphone amplifier (HPL, HPR, HPC) power up |

- (1) Power supply sequencing is not required. It is recommended to set register data with system clock input after turning all power supplies on.
- (2) Any level is acceptable for volume or attenuation. Level should be resumed by register data recorded when system power off.
- (3) Audio interface format should be set to match the DSP or decoder being used.

Table 3. Recommended Power-On Sequence (continued)

| STEP | REGISTER SETTINGS | NOTE |
|------|-------------------|--|
| 17 | 4C03h | Speaker amplifier shut down release |
| 18 | 4A01h | V _{COM} power up |
| 19 | 523Fh | Analog front end (ADL, ADR, D2S, MCB, PG1, 2, 5, 6) power up |
| 20 | 5711h | Analog input (MUX3, MUX4) select. Analog input (MUX1, MUX2) select |
| 21 | 4F0Ch | Analog input L-ch (PG3) volume (0 dB) ⁽²⁾ |
| 22 | 500Ch | Analog input R-ch (PG4) volume (0 dB) ⁽²⁾ |
| 23 | – | Any settings for other devices or wait time ⁽⁴⁾⁽⁵⁾ |
| 24 | 49FFh | Speaker amplifier (SPL, SPR) power up ⁽⁵⁾ |

(4) The PCM3793 requires time for V_{COM} to reach the common level from GND level. The delay depends on the capacitor value for V_{COM} and the setting of register 90 CMT[1:0]. Wait time [s] = 4 × C_{VCOM} × R_{CMT}

(5) The PCM3794 does not require this setting because it has no speaker output.

Table 4. Recommended Power-Off Sequence

| STEP | REGISTER SETTINGS | NOTE |
|------|-------------------|---|
| 1 | 447Fh | DAC L-ch digital soft-mute enable ⁽¹⁾ |
| 2 | 457Fh | DAC R-ch digital soft-mute enable ⁽¹⁾ |
| 3 | 5132h | ADC L-ch/R-ch digital soft-mute enable, ADC audio interface format (left-justified) ⁽²⁾ |
| 4 | 5811h | Analog mixer input (SW2, SW5) Select |
| 5 | 49FFh | Headphone amplifier (HPL, HPR, HPC) power up ⁽⁴⁾ , speaker amplifier (SPL, SPR) power up ⁽³⁾⁽⁴⁾ |
| 6 | 5200h | Analog front end (ADL, ADR, D2S, MCB, PG1, 2, 5, 6) power down |
| 7 | 5A10h | V _{COM} ramp up/down time control, PG1, PG2 gain control (0 dB) |
| 8 | 4A00h | V _{COM} power down |
| 9 | – | Wait time (100 ms) |
| 10 | 5A00h | V _{COM} ramp up/down time control |
| 11 | – | Wait time (100 ms) |
| 12 | 5A20h | V _{COM} ramp up/down time control |
| 13 | – | Wait time (4000 ms) |
| 14 | 5A30h | V _{COM} ramp up/down time control |
| 15 | 49E0h | Headphone amplifier (HPL, HPR, HPC) power down, speaker amplifier (SPL, SPR) power down |
| 16 | 4800h | Analog mixer (MXL, MXR) power down |
| 17 | 4900h | DAC (DAL, DAR) and analog bias power down |
| 18 | – | Turn off all power supplies ⁽⁵⁾ |

(1) Any level is acceptable for volume or attenuation.

(2) Audio interface format should be set according to DSP or decoder.

(3) PCM3794 has no speaker amplifier.

(4) These modules must be powered up during the power-down sequence.

(5) Power supply sequencing is not required. It is recommended to turn off all power supply after register settings with system clock input.

Power-Supply Current

The current consumption of the PCM3793/94 depends on power up/down status of each circuit module. In order to reduce the power consumption, disabling each module is recommended when it is not used in an application or operation. [Table 5](#) shows the current consumption in some states.

Table 5. Power Consumption Table

| OPERATION MODE | POWER SUPPLY CURRENT [mA] | | | | | PD [mW] | PD [mW] |
|--|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|---------------------------------------|------------------------------------|
| | V _{DD} (1.8 V) | V _{DD} (3.3 V) | V _{CC} (3.3 V) | V _{PA} (3.3 V) | V _{IO} (3.3 V) | TOTAL (V _{DD} = 1.8 V) | TOTAL (V _{DD} = 3.3 V) |
| All Power Down | 0 | 0 | 0.007 | 0.002 | 0 | 0.03 | 0.03 |
| All Active | 2.5 | 5.1 | 7.5 | 11.6 | 0.1 | 67.7 | 80.2 |
| PLAYBACK WITH DIGITAL INPUT | | | | | | | |
| Line output and headphone output | 1.18 | 2.51 | 1.79 | 0.54 | 0.09 | 10.1 | 16.3 |
| Headphone output with sound effect | 1.81 | 3.84 | 1.79 | 0.54 | 0.09 | 11.2 | 20.7 |
| Capless headphone output | 1.18 | 2.51 | 1.8 | 0.75 | 0.09 | 10.8 | 17.0 |
| Headphone output with line input (AIN2L/AIN2R) | 1.18 | 2.52 | 2.09 | 0.54 | 0.09 | 11.1 | 17.3 |
| Headphone output with mono microphone input (AIN1L, 20 dB) | 1.18 | 2.52 | 2.5 | 0.54 | 0.09 | 12.5 | 18.6 |
| Headphone output with mono differential microphone input (AIN1L/AIN1R, 20 dB) | 1.18 | 2.52 | 2.8 | 0.54 | 0.09 | 13.4 | 19.6 |
| Stereo speaker output | 1.21 | 2.58 | 2.18 | 10.94 | 0.09 | 45.8 | 52.1 |
| Mono speaker output | 1.20 | 2.57 | 2.01 | 5.61 | 0.09 | 27.6 | 33.9 |
| Speaker output with line input (AIN2L/AIN2R) | 1.21 | 2.57 | 2.48 | 10.95 | 0.09 | 46.8 | 53.1 |
| Speaker output with mono microphone input (AIN1L, 20 dB) | 1.21 | 2.58 | 2.89 | 10.96 | 0.09 | 48.2 | 54.5 |
| Speaker output with mono differential microphone input (AIN1L/AIN1R, 20 dB) | 1.2 | 2.58 | 3.2 | 10.98 | 0.09 | 49.3 | 55.6 |
| PLAYBACK WITHOUT DIGITAL INPUT | | | | | | | |
| Line input (AIN2L/AIN2R) to headphone output | 0 | 0 | 0.76 | 0.53 | 0 | 4.3 | 4.3 |
| Mono line input (AIN2L) to headphone output | 0 | 0 | 0.61 | 0.53 | 0 | 3.8 | 3.8 |
| Mono microphone Input (AIN1L, 20 dB) to headphone output | 0 | 0 | 1.18 | 0.53 | 0 | 5.6 | 5.6 |
| Mono differential microphone input (AIN1L/AIN1R, 20 dB) to headphone output | 0 | 0 | 1.48 | 0.53 | 0 | 6.6 | 6.6 |
| Mono microphone input (AIN1L, 20 dB) to speaker output | 0 | 0 | 1.57 | 10.92 | 0 | 41.2 | 41.2 |
| RECORDING | | | | | | | |
| Line input (AIN3L/AIN3R) | 1.86 | 3.89 | 4.58 | 0.13 | 0.1 | 19.2 | 28.7 |
| Microphone input (AIN1L/AIN1R, 20 dB) | 1.86 | 3.91 | 5.14 | 0.13 | 0.1 | 21.1 | 30.6 |
| Microphone input (AIN1L/AIN1R, 20 dB) with ALC | 2.78 | 5.77 | 5.14 | 0.13 | 0.1 | 22.7 | 36.8 |
| Mono microphone input (AIN1L, 20 dB) | 1.4 | 2.93 | 3.6 | 0.13 | 0.1 | 15.2 | 22.3 |
| Mono microphone input (AIN1L, 20 dB) with ALC | 2.2 | 4.74 | 3.6 | 0.13 | 0.1 | 16.6 | 28.3 |
| Mono differential microphone input (AIN1L/AIN1R, 20 dB) | 1.4 | 2.94 | 3.96 | 0.13 | 0.1 | 16.3 | 23.5 |
| Mono differential microphone input (AIN1L/AIN1R, 20 dB) with ALC | 2.2 | 4.74 | 3.96 | 0.13 | 0.1 | 17.8 | 29.5 |
| Conditions: 48 kHz/256 f _s , 16 bits, slave mode, zero data input, no load | | | | | | | |

Audio Serial Interface

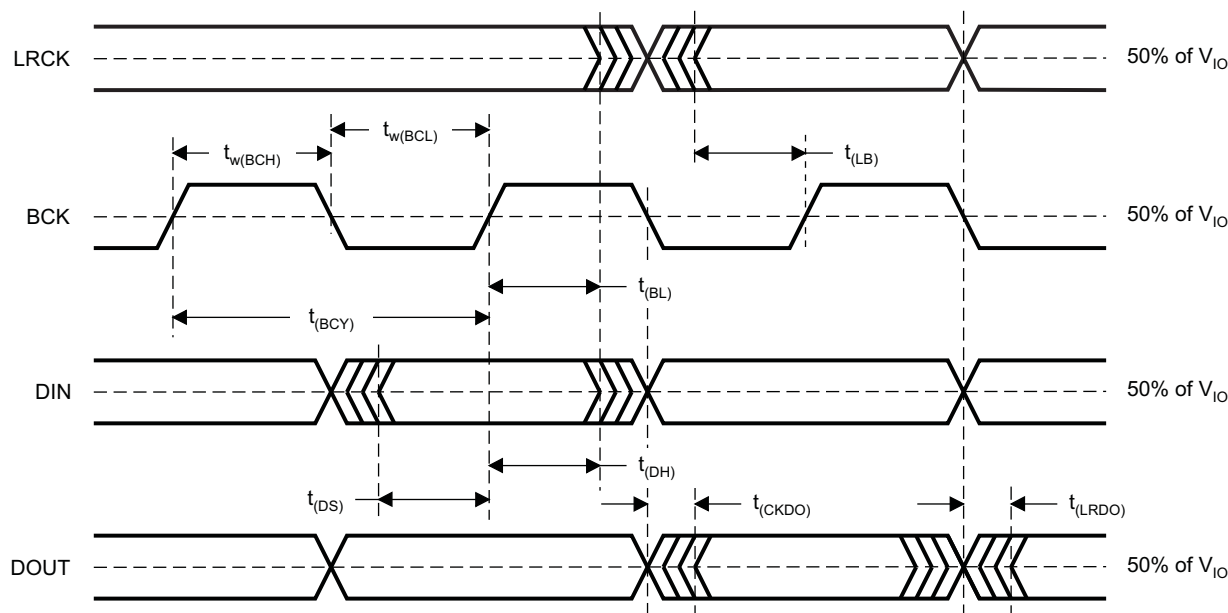
The audio serial interface for the PCM3793/94 comprises LRCK, BCK, DIN, and DOUT. Sampling rate (f_s), left and right channel are present on LRCK. DIN receives the serial data for the DAC interpolation filter, and DOUT transmits the serial data from the ADC decimation filter. BCK clocks the transfer of serial audio data on DIN and DOUT in its high-to-low transition. BCK and LRCK should be synchronized with audio system clock. Ideally, it is recommended that they be derived from it.

The PCM3793/94 requires LRCK to be synchronized with the system clock. The PCM3793/94 does not require a specific phase relationship between LRCK and the system clock.

The PCM3793/94 has both master mode and slave mode interface formats, which can be selected by register 84, MSTR. In master mode, the PCM3793/94 generates LRCK and BCK from the system clock.

Audio Data Formats and Timing

The PCM3793/94 supports I²S, right-justified, left-justified and DSP formats. The data formats are shown in [Figure 28](#) and are selected using register 70 (RFM[1:0], PFM[1:0]). All formats require binary 2s-complement, MSB-first audio data. The default format is I²S. [Figure 26](#) shows a detailed timing diagram.

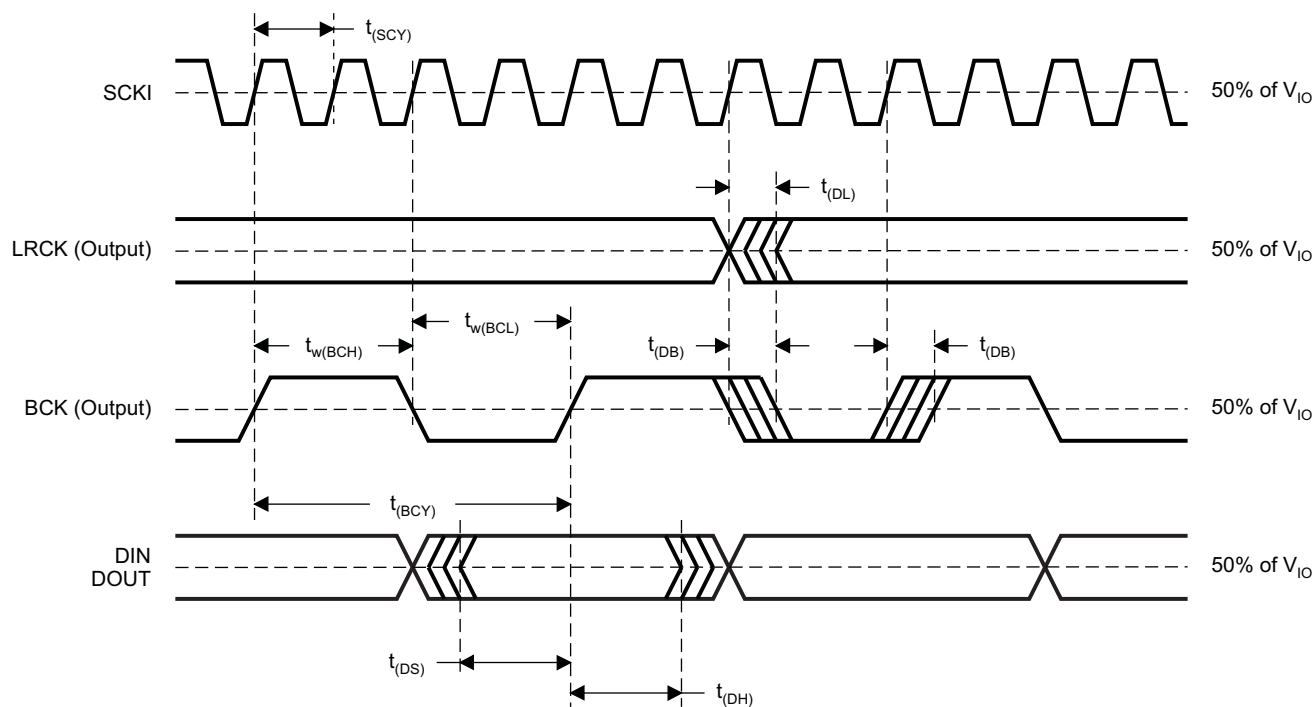


T0010-09

| PARAMETERS | | MIN | MAX | UNITS |
|--------------|--|---------------------|-----|-------|
| $t_{(BCY)}$ | BCK pulse cycle time (I ² S, left- and right-justified formats) | $1/(64 f_s)^{(1)}$ | | |
| | BCK pulse cycle time (DSP format) | $1/(256 f_s)^{(1)}$ | | |
| $t_{w(BCH)}$ | BCK high-level time | 35 | | ns |
| $t_{w(BCL)}$ | BCK low-level time | 35 | | ns |
| $t_{(BL)}$ | BCK rising edge to LRCK edge | 10 | | ns |
| $t_{(LB)}$ | LRCK edge to BCK rising edge | 10 | | ns |
| $t_{(DS)}$ | DIN set up time | 10 | | ns |
| $t_{(DH)}$ | DIN hold time | 10 | | ns |
| $t_{(CKDO)}$ | DOUT delay time from BCK falling edge | | 15 | ns |
| $t_{(LRDO)}$ | DOUT delay time from LRCK falling edge | | 15 | ns |
| t_r | Rising time of all signals | | 10 | ns |
| t_f | Falling time of all signals | | 10 | ns |

(1) f_s is the sampling frequency.

Figure 26. Audio Interface Timing (Slave Mode)



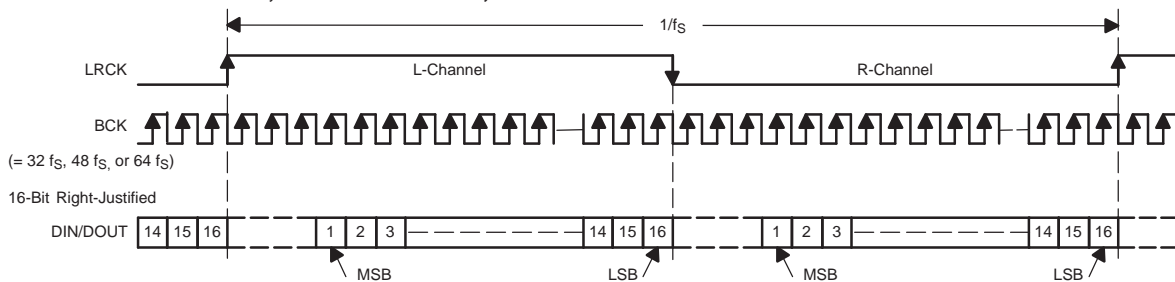
T0011-04

| PARAMETERS | | MIN | MAX | UNIT |
|--------------|---------------------------------|---------------------|-----|------|
| $t_{(SCY)}$ | SCKI pulse cycle time | $1/(256 f_s)^{(1)}$ | | |
| $t_{(DL)}$ | LRCK edge from SCKI rising edge | 0 | 40 | ns |
| $t_{(DB)}$ | BCK edge from SCKI rising edge | 0 | 40 | ns |
| $t_{(BCY)}$ | BCK pulse cycle time | $1/(64 f_s)^{(1)}$ | | |
| $t_{w(BCH)}$ | BCK high level time | 146 | | ns |
| $t_{w(BCL)}$ | BCK low level time | 146 | | ns |
| $t_{(DS)}$ | DATA setup time | 10 | | ns |
| $t_{(DH)}$ | DATA hold time | 10 | | ns |

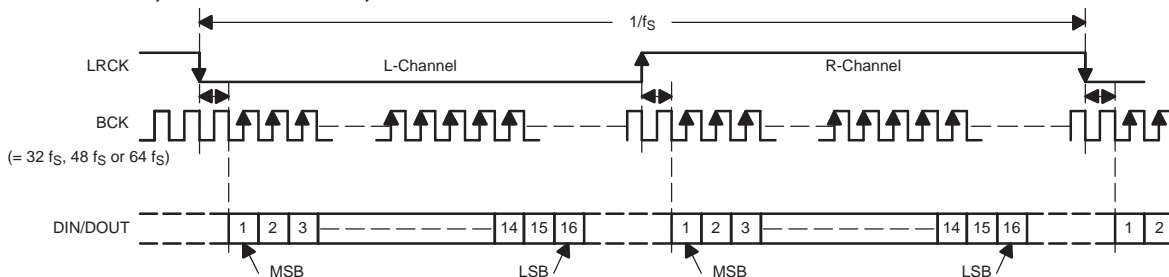
(1) f_s is up to 48 kHz. f_s is the sampling frequency.

Figure 27. Audio Interface Timing (Master Mode)

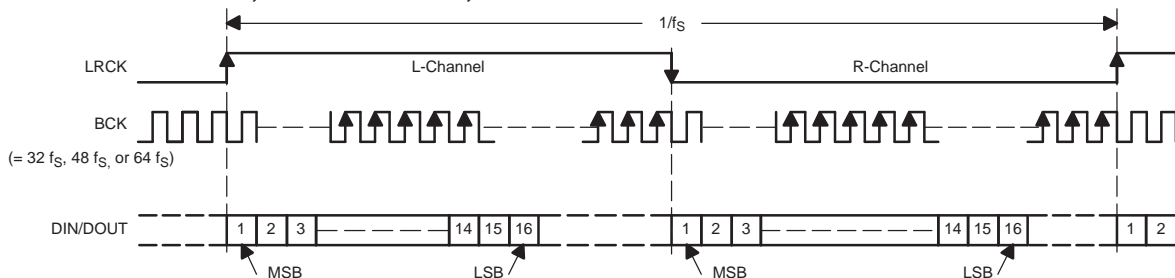
(a) Right-Justified Data Format; L-Channel = HIGH, R-Channel = LOW



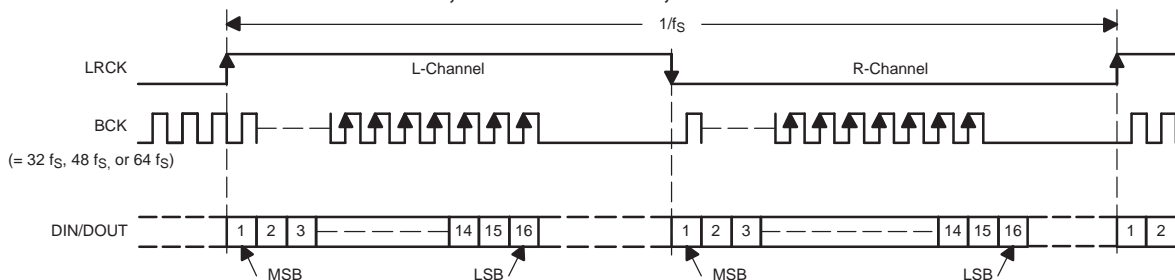
(b) I²S Data Format; L-Channel = LOW, R-Channel = HIGH



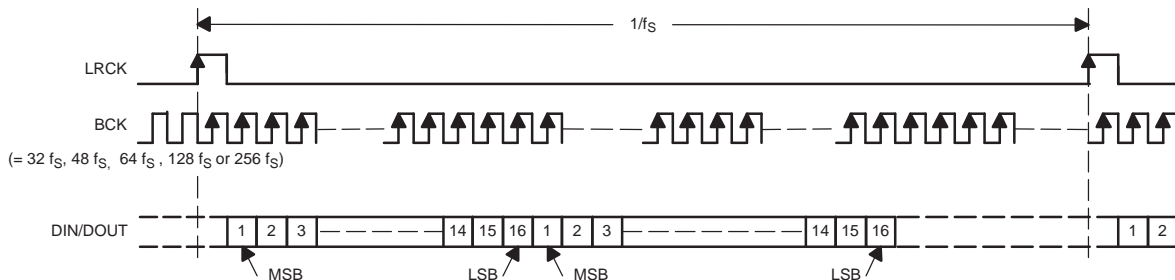
(c) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW



(d) Burst BCK Interface Format at Master Mode; L-Channel = HIGH, R-Channel = LOW



(e) DSP Format



T0009-07

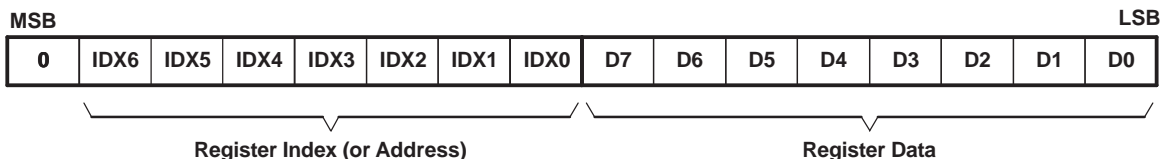
NOTE: All audio interface formats support BCK = $64 f_s$ in master mode (register 69, MSTR = 1). When setting the multisampling rate, the f_s of BCK is set to half the rate of the DSM operation frequency.

Figure 28. Audio Data Input and Output Formats

THREE-WIRE INTERFACE (SPI, MODE (PIN 28) = LOW)

All write operations for the serial control port use 16-bit data words. Figure 29 shows the control data word format. The most significant bit must be 0. There are seven bits, labeled IDX[6:0], that set the register address for the write operation. The least significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

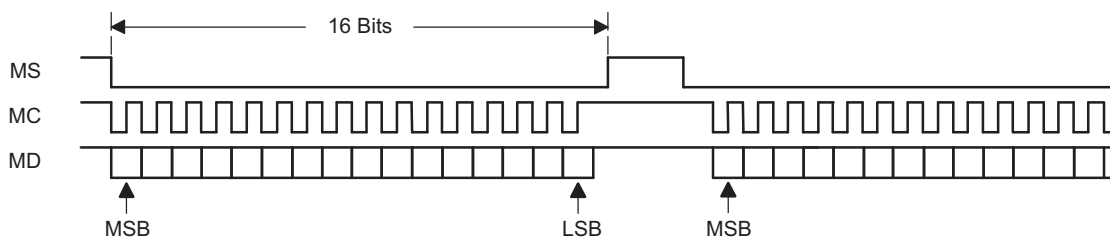
Figure 30 shows the functional timing diagram for writing to the serial control port. To write the data into the mode register, the data is clocked into an internal shift register on the rising edge of the MC clock. The serial data should change on the falling edge of MC clock and should be LOW during write mode. The rising edge of MS should be aligned with the falling edge of the last MC clock pulse in the 16-bit frame. MC can run continuously between transactions while MS is in the LOW state.



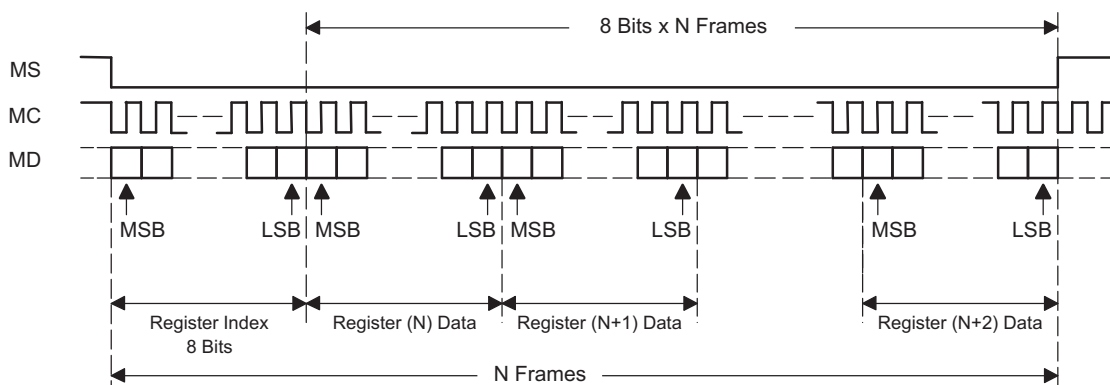
R0001-01

Figure 29. Control Data Word Format for MD

(1) Single Write Operation



(2) Continuous Write Operation

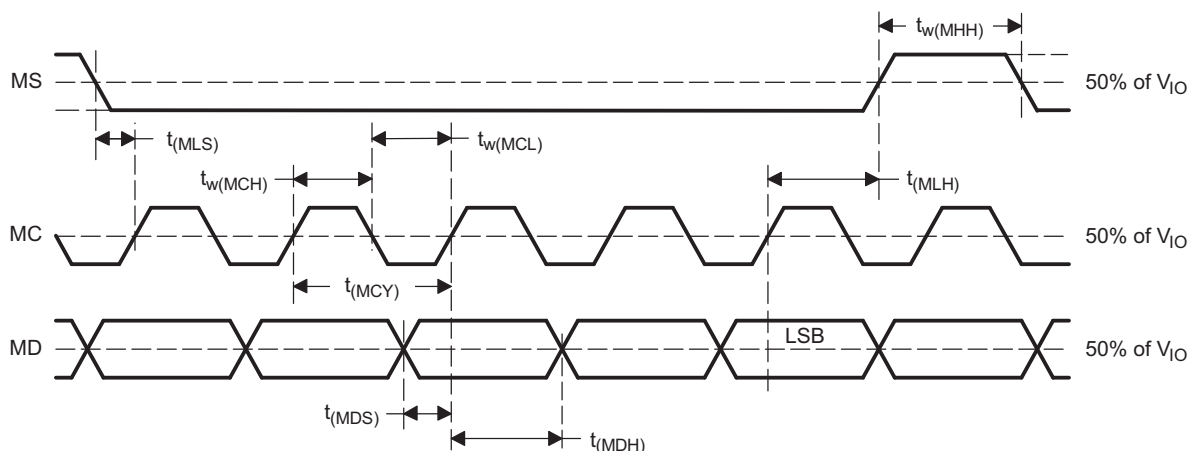


T0012-03

Figure 30. Register Write Operation

Three-Wire Interface (SPI) Timing Requirements

Figure 31 shows a detailed timing diagram for the serial control interface. These timing parameters are critical for proper control port operation.



T0013-08

| PARAMETERS | | MIN | TYP | MAX | UNIT |
|---------------------|-----------------------------------|--------------------|-----|-----|------|
| t _(MCY) | MC pulse cycle time | 500 ⁽¹⁾ | | | ns |
| t _{w(MCL)} | MC low level time | 50 | | | ns |
| t _{w(MCH)} | MC high level time | 50 | | | ns |
| t _{w(MHH)} | MS high level time | (1) | | | ns |
| t _(MLS) | MS falling edge to MC rising edge | 20 | | | ns |
| t _(MLH) | MS hold time | 20 | | | ns |
| t _(MDH) | MD hold time | 15 | | | ns |
| t _(MDS) | MD setup time | 20 | | | ns |

(1) 3/(128 f_s) s (min), where f_s is sampling rate.

Figure 31. SPI Interface Timing

TWO-WIRE INTERFACE [I²C, MODE (PIN 28) = HIGH]

The PCM3793/94 supports the I²C serial bus and the data transmission protocol for the I²C standard as a slave device. This protocol is explained in I²C specification 2.0.

In I²C mode, the control terminals are changed as follows.

| TERMINAL NAME | PROPERTY | DESCRIPTION |
|---------------|--------------|--------------------------|
| MS/ADR | Input | I ² C address |
| MD/SDA | Input/output | I ² C data |
| MC/SCL | Input | I ² C clock |

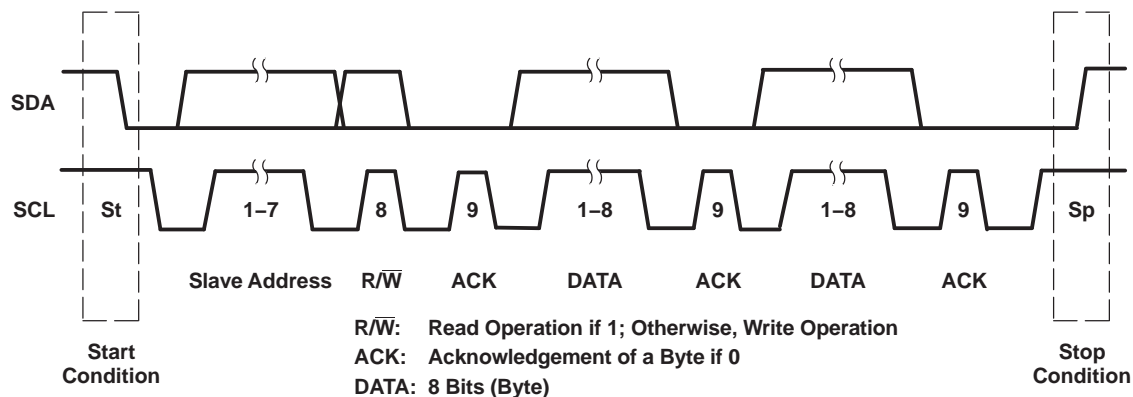
SLAVE ADDRESS

| | | | | | | | |
|-----|---|---|---|---|---|-----|-----|
| MSB | | | | | | LSB | |
| 1 | 0 | 0 | 0 | 1 | 1 | ADR | R/W |

The PCM3793/94 has its own 7-bit slave address. The first six bits (MSBs) of the slave address are factory preset to 100011. The last bit of the address byte is the device select bit, which can be user-defined by the ADR terminal. A maximum of two PCM3793/94s can be connected on the same bus at one time. Each PCM3793/94 responds when it receives its own slave address.

Packet Protocol

The master device must control packet protocol, which consists of start condition, slave address with read/write bit, data if write or acknowledgement if read, and stop condition. The PCM3793/94 supports only slave receiver and slave transmitter.



Write Operation

| | | | | | | | | | |
|-------------|----|---------------|-----|-----|------|-----|------|-----|----|
| Transmitter | M | M | M | S | M | S | M | S | M |
| Data Type | St | Slave Address | R/W | ACK | DATA | ACK | DATA | ACK | Sp |

Read Operation

| | | | | | | | | | |
|-------------|----|---------------|-----|-----|------|-----|------|------|----|
| Transmitter | M | M | M | S | S | M | S | M | M |
| Data Type | St | Slave Address | R/W | ACK | DATA | ACK | DATA | NACK | Sp |

M: Master Device S: Slave Device
St: Start Condition Sp: Stop Condition

T0049-03

Figure 32. Basic I²C Framework

WRITE OPERATION

A master can write any PCM3793/94 registers using single access. The master sends a PCM3793/94 slave address with a write bit, a register address, and the data. When undefined registers are accessed, the PCM3793/94 does not send an acknowledgement. Figure 33 shows a diagram of the write operation.

| | | | | | | | | | |
|-------------|----|---------------|---|-----|-------------|-----|------------|-----|----|
| Transmitter | M | M | M | S | M | S | M | S | M |
| Data Type | St | Slave Address | W | ACK | Reg Address | ACK | Write Data | ACK | Sp |

M: Master Device S: Slave Device
St: Start Condition W: Write ACK: Acknowledge Sp: Stop Condition

R0002-01

Figure 33. Framework for Write Operation

READ OPERATION

A master can read the PCM3793/94 register. The value of the register address is stored in an indirect index register in advance. The master sends a PCM3793/94 slave address with a read bit after storing the register address. Then the PCM3793/94 transfers the data which the index register points to. Figure 34 shows a diagram of the write operation.

| | | | | | | | | | | | | | |
|-------------|----|---------------|-----------|-----|-------------|-----|----|---------------|---|-----|-----------|------|----|
| Transmitter | M | M | M | S | M | S | M | M | M | S | S | M | M |
| Data Type | St | Slave Address | \bar{W} | ACK | Reg Address | ACK | Sr | Slave Address | R | ACK | Read Data | NACK | Sp |

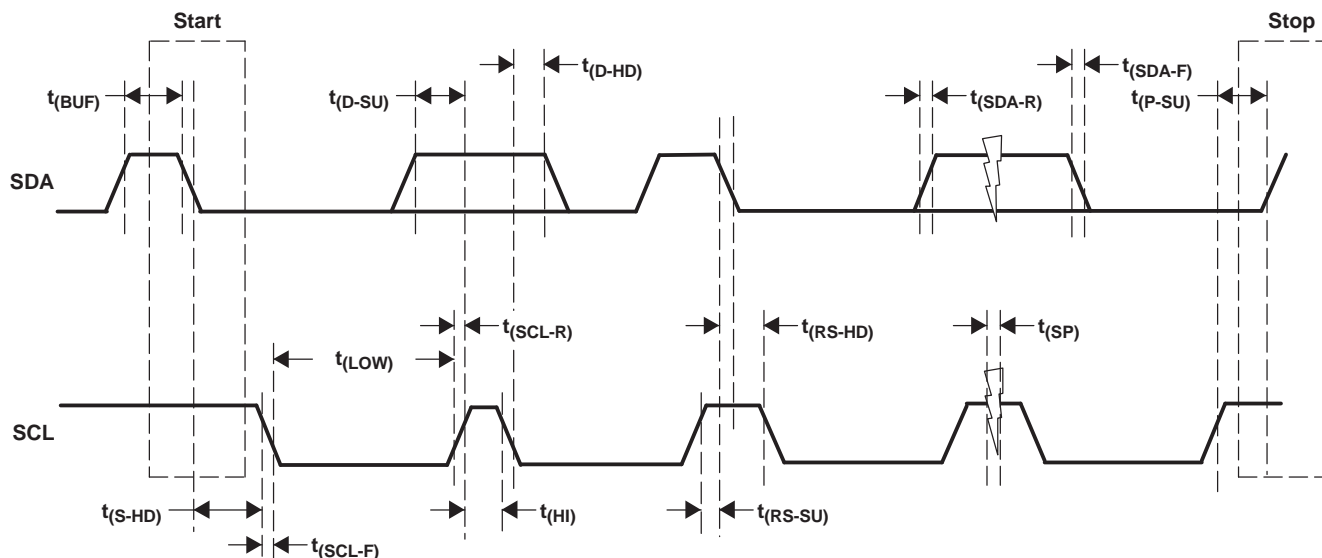
M: Master Device S: Slave Device St: Start Condition
Sr: Repeated Start Condition ACK: Acknowledge Sp: Stop Condition NACK: Not Acknowledge
W: Write R: Read

R0002-02

NOTE: The slave address after the repeated start condition must be the same as the previous slave address.

Figure 34. Read Operation

Timing Diagram



T0050-03

| PARAMETERS | | CONDITIONS | MIN | MAX | UNIT |
|----------------|---|------------|----------------|------|---------|
| f_{SCL} | SCL clock frequency | Standard | | 100 | kHz |
| $t_{(BUF)}$ | Bus free time between a STOP and START condition | Standard | 4.7 | | μ s |
| $t_{(LOW)}$ | Low period of the SCL clock | Standard | 4.7 | | μ s |
| $t_{(HI)}$ | High period of the SCL clock | Standard | 4 | | μ s |
| $t_{(RS-SU)}$ | Setup time for START condition | Standard | 4.7 | | μ s |
| $t_{(S-HD)}$ | Hold time for START condition | Standard | 4 | | μ s |
| $t_{(D-SU)}$ | Data setup time | Standard | 250 | | ns |
| $t_{(D-HD)}$ | Data hold time | Standard | 0 | 900 | ns |
| $t_{(SCL-R)}$ | Rise time of SCL signal | Standard | $20 + 0.1 C_B$ | 1000 | ns |
| $t_{(SCL-R1)}$ | Rise time of SCL signal after a repeated START condition and after an acknowledge bit | Standard | $20 + 0.1 C_B$ | 1000 | ns |
| $t_{(SCL-F)}$ | Fall time of SCL signal | Standard | $20 + 0.1 C_B$ | 1000 | ns |
| $t_{(SDA-R)}$ | Rise time of SDA signal | Standard | $20 + 0.1 C_B$ | 1000 | ns |
| $t_{(SDA-F)}$ | Fall time of SDA signal | Standard | $20 + 0.1 C_B$ | 1000 | ns |
| $t_{(P-SU)}$ | Setup time for STOP condition | Standard | 4 | | μ s |
| C_B | Capacitive load for SDA and SCL line | | | 400 | pF |
| $t_{(SP)}$ | Pulse duration of suppressed spike | | | 25 | ns |

Figure 35. I²C Interface Timing

USER-PROGRAMMABLE MODE CONTROLS

Register Map

The mode control register map is shown in Table 6. Each register includes an index (or address) indicated by the IDX[6:0] bits.

Table 6. Mode Control Register Map

| REGISTER | IDX[6:0] (B14–B8) | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--------------|----------------------|--|------|------|------|------|------|------|------|------|
| Register 64 | 40h | Volume for HPA (L-ch) | RSV | HMUL | HLV5 | HLV4 | HLV3 | HLV2 | HLV1 | HLV0 |
| Register 65 | 41h | Volume for HPA (R-ch) | RSV | HMUR | HRV5 | HRV4 | HRV3 | HRV2 | HRV1 | HRV0 |
| Register 66 | 42h | Volume for SPA (L-ch) | RSV | SMUL | SLV5 | SLV4 | SLV3 | SLV2 | SLV1 | SLV0 |
| Register 67 | 43h | Volume for SPA (R-ch) | RSV | SMUR | SRV5 | SRV4 | SRV3 | SRV2 | SRV1 | SRV0 |
| Register 68 | 44h | DAC digital attenuation and soft mute (L-ch) | RSV | PMUL | ATL5 | ATL4 | ATL3 | ATL2 | ATL1 | ATL0 |
| Register 69 | 45h | DAC digital attenuation and soft mute (R-ch) | RSV | PMUR | ATR5 | ATR4 | ATR3 | ATR2 | ATR1 | ATR0 |
| Register 70 | 46h | DAC over sampling, de-emphasis, audio interface | DEM1 | DEM0 | PFM1 | PFM0 | RSV | RSV | RSV | OVER |
| Register 71 | 47h | SPA (class-D) switching frequency | RSV | RSV | RSV | SPSE | SPS1 | SPS0 | DFQ1 | DFQ0 |
| Register 72 | 48h | Analog mixer power up/down | RSV | RSV | RSV | RSV | RSV | RSV | PMXR | PMXL |
| Register 73 | 49h | DAC, SPA and HPA power up/down | PBIS | PDAR | PDAL | PHPC | PHPR | PHPL | PSPR | PSPL |
| Register 74 | 4Ah | Analog output configuration select | RSV | CMS2 | CMS1 | CMS0 | HPS1 | HPS0 | SPKS | PCOM |
| Register 75 | 4Bh | HPA insertion detection, short/thermal protection | HPDP | HPDE | RSV | SDHC | SDHR | SDHL | SDSR | SDSL |
| Register 76 | 4Ch | SPA shutdown release | RSV | RSV | RSV | RSV | RSV | RSV | RLSR | RLSL |
| Register 77 | 4Dh | Shut down status read back | HPDS | RSV | RSV | STHC | STHR | STHL | STSR | STSL |
| Register 79 | 4Fh | Volume for ADC input (L-ch) | RSV | RSV | ALV5 | ALV4 | ALV3 | ALV2 | ALV1 | ALV0 |
| Register 80 | 50h | Volume for ADC input (R-ch) | RSV | RSV | ARV5 | ARV4 | ARV3 | ARV2 | ARV1 | ARV0 |
| Register 81 | 51h | ADC high-pass filter, soft mute, audio interface | HPF1 | HPF0 | RMUL | RMUR | RSV | DSMC | RFM1 | RFM0 |
| Register 82 | 52h | ADC, MCB, PG1, 2, 5, 6, D2S power up/down | RSV | RSV | PAIR | PAIL | PADS | PMCB | PADR | PADL |
| Register 83 | 53h | Automatic level control for recording | RALC | RSV | RRTC | RATC | RCP1 | RCP0 | RLV1 | RLV0 |
| Register 84 | 54h | Master mode | RSV | RSV | RSV | RSV | RSV | MSTR | RSV | BIT0 |
| Register 85 | 55h | System reset, sampling rate control | SRST | RSV | NPR5 | NPR4 | NPR3 | NPR2 | NPR1 | NPR0 |
| Register 86 | 56h | BCK configuration, sampling rate control, zero-cross | MBST | MSR2 | MSR1 | MSR0 | ATOD | RSV | RSV | ZCRS |
| Register 87 | 57h | Analog input select (MUX1, 2, 3, 4) | AD2S | RSV | AIR1 | AIR0 | RSV | RSV | AIL1 | AIL0 |
| Register 88 | 58h | Analog mixing switch (SW1, 2, 3, 4, 5, 6) | RSV | MXR2 | MXR1 | MXR0 | RSV | MXL2 | MXL1 | MXL0 |
| Register 89 | 59h | Analog to analog path (PG5, 6) gain | RSV | GMR2 | GMR1 | GMR0 | RSV | GML2 | GML1 | GML0 |
| Register 90 | 5Ah | V _{COM} power up/down, ramp up/down time, boost | RSV | RSV | CMT1 | CMT0 | RSV | RSV | G20R | G20L |
| Register 92 | 5Ch | Bass boost gain level | LPAE | RSV | RSV | LGA4 | LGA3 | LGA2 | LGA1 | LGA0 |
| Register 93 | 5Dh | Middle boost gain level | RSV | RSV | RSV | MGA4 | MGA3 | MGA2 | MGA1 | MGA0 |
| Register 94 | 5Eh | Treble boost gain level | RSV | RSV | RSV | HGA4 | HGA3 | HGA2 | HGA1 | HGA0 |
| Register 95 | 5Fh | Sound effect source select, 3D sound | SDAS | 3DEN | RSV | 3FL0 | 3DP3 | 3DP2 | 3DP1 | 3DP0 |
| Register 96 | 60h | 2-stage notch filter, digital monaural mixing | NEN2 | NEN1 | NUP2 | NUP1 | RSV | RSV | RSV | MXEN |
| Register 97 | 61h | 1st stage notch filter lower coefficient (a1) | F107 | F106 | F105 | F104 | F103 | F102 | F101 | F100 |
| Register 98 | 62h | 1st stage notch filter upper coefficient (a1) | F115 | F114 | F113 | F112 | F111 | F110 | F109 | F108 |
| Register 99 | 63h | 1st stage notch filter lower coefficient (a2) | F207 | F206 | F205 | F204 | F203 | F202 | F201 | F200 |
| Register 100 | 64h | 1st stage notch filter upper coefficient (a2) | F215 | F214 | F213 | F212 | F211 | F210 | F209 | F208 |
| Register 101 | 65h | 2nd stage notch filter lower coefficient (a1) | S107 | S106 | S105 | S104 | S103 | S102 | S101 | S100 |
| Register 102 | 66h | 2nd stage notch filter upper coefficient (a1) | S115 | S114 | S113 | S112 | S111 | S110 | S109 | S108 |
| Register 103 | 67h | 2nd stage notch filter lower coefficient (a2) | S207 | S206 | S205 | S204 | S203 | S202 | S201 | S200 |
| Register 104 | 68h | 2nd stage notch filter upper coefficient (a2) | S215 | S214 | S213 | S212 | S211 | S210 | S209 | S208 |

HPA: Headphone amplifier single-ended amplifier SPA: Speaker amplifier DAC: D/A converter ADC: A/D converter MCB: Microphone bias PGx: Analog input buffer D2S: Differential to

Register Definitions

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|-----|------|------|------|------|------|------|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 64 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | HMUL | HLV5 | HLV4 | HLV3 | HLV2 | HLV1 | HLV0 |
| Register 65 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | HMUR | HRV5 | HRV4 | HRV3 | HRV2 | HRV1 | HRV0 |

IDX[6:0]: 100 0000b (40h): Register 64

IDX[6:0]: 100 0001b (41h): Register 65

HMUL: Analog Mute Control for HPL (Line or Headphone L-Channel)

HMUR: Analog Mute Control for HPR (Line or Headphone R-Channel)

Default value: 1

HPOL/LOL and HPOR/LOR can be independently muted to zero level when HMUL and HMUR = 1. The HMuX mute takes precedence over analog volume level settings.

| | |
|----------------|------------------------|
| HMUL, HMUR = 0 | Mute disabled |
| HMUL, HMUR = 1 | Mute enabled (default) |

HLV[5:0]: Analog Volume for HPL (Headphone L-Channel)

HRV[5:0]: Analog Volume for HPR (Headphone R-Channel)

Default value: 00 0000.

HPOL/LOL and HPOR/LOR can be independently controlled from 6 dB to –70 dB, with step size depending on the gain level. Outputs may have zipper noise while changing levels. In the PCM3793/94, the noise can be reduced when making the change by using zero-cross detection (register 85, ZCRS).

Table 7. Headphone Gain Level Setting

| HLV[5:0], HRV[5:0] | STEP | GAIN LEVEL SETTING | HLV[5:0], HRV[5:0] | STEP | GAIN LEVEL SETTING | HLV[5:0], HRV[5:0] | STEP | GAIN LEVEL SETTING |
|-----------------------|------|-----------------------|-----------------------|------|-----------------------|-----------------------|------|-----------------------|
| 11 1111 | 3F | 6 dB | 10 1001 | 29 | –5 dB | 01 0011 | 13 | –21 dB |
| 11 1110 | 3E | 5.5 dB | 10 1000 | 28 | –5.5 dB | 01 0010 | 12 | –22 dB |
| 11 1101 | 3D | 5 dB | 10 0111 | 27 | –6 dB | 01 0001 | 11 | –23 dB |
| 11 1100 | 3C | 4.5 dB | 10 0110 | 26 | –6.5 dB | 01 0000 | 10 | –24 dB |
| 11 1011 | 3B | 4 dB | 10 0101 | 25 | –7 dB | 00 1111 | 0F | –26 dB |
| 11 1010 | 3A | 3.5 dB | 10 0100 | 24 | –7.5 dB | 00 1110 | 0E | –28 dB |
| 11 1001 | 39 | 3 dB | 10 0011 | 23 | –8 dB | 00 1101 | 0D | –30 dB |
| 11 1000 | 38 | 2.5 dB | 10 0010 | 22 | –8.5 dB | 00 1100 | 0C | –32 dB |
| 11 0111 | 37 | 2 dB | 10 0001 | 21 | –9 dB | 00 1011 | 0B | –34 dB |
| 11 0110 | 36 | 1.5 dB | 10 0000 | 20 | –9.5 dB | 00 1010 | 0A | –36 dB |
| 11 0101 | 35 | 1 dB | 01 1111 | 1F | –10 dB | 00 1001 | 09 | –38 dB |
| 11 0100 | 34 | 0.5 dB | 01 1110 | 1E | –10.5 dB | 00 1000 | 08 | –40 dB |
| 11 0011 | 33 | 0 dB | 01 1101 | 1D | –11 dB | 00 0111 | 07 | –42 dB |
| 11 0010 | 32 | –0.5 dB | 01 1100 | 1C | –12 dB | 00 0110 | 06 | –46 dB |
| 11 0001 | 31 | –1 dB | 01 1011 | 1B | –13 dB | 00 0101 | 05 | –50 dB |
| 11 0000 | 30 | –1.5 dB | 01 1010 | 1A | –14 dB | 00 0100 | 04 | –54 dB |
| 10 1111 | 2F | –2 dB | 01 1001 | 19 | –15 dB | 00 0011 | 03 | –58 dB |
| 10 1110 | 2E | –2.5 dB | 01 1000 | 18 | –16 dB | 00 0010 | 02 | –62 dB |
| 10 1101 | 2D | –3 dB | 01 0111 | 17 | –17 dB | 00 0001 | 01 | –66 dB |
| 10 1100 | 2C | –3.5 dB | 01 0110 | 16 | –18 dB | 00 0000 | 00 | –70 dB |
| 10 1011 | 2B | –4 dB | 01 0101 | 15 | –19 dB | | | |
| 10 1010 | 2A | –4.5 dB | 01 0100 | 14 | –20 dB | | | |

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|-----|------|------|------|------|------|------|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 66 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | SMUL | SLV5 | SLV4 | SLV3 | SLV2 | SLV1 | SLV0 |
| Register 67 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | SMUR | SRV5 | SRV4 | SRV3 | SRV2 | SRV1 | SRV0 |

IDX[6:0]: 100 0010b (42h): Register 66

IDX[6:0]: 100 0011b (43h): Register 67

SMUL: Digital Soft Mute Control for SPL (Speaker Output, L-Channel)

SMUR: Digital Soft Mute Control for SPR (Speaker Output R-Channel)

Default value: 1

SPOLP/SPOLN and SPORP/SPORN can be independently muted to the zero level when HMUL and HMUR = 1. The SMUx mute takes precedence over analog volume level settings.

| | |
|----------------|------------------------|
| SMUL, SMUR = 0 | Mute disabled |
| SMUL, SMUR = 1 | Mute enabled (default) |

SLV[5:0]: Gain Setting for SPL (Speaker Output L-Channel)

SRV[5:0]: Gain Setting for SPR (Speaker Output R-Channel)

Default value: 00 0000.

SPOLP/SPOLN and SPORP/SPORN can be independently controlled from 6 dB to –70 dB, with step size depending on the gain level. Outputs may have zipper noise while changing levels. In the PCM3793, the noise can be reduced when making the change by using zero-cross detection (register 85, ZCRS).

Table 8. Speaker Gain Level Setting

| SLV[5:0], SRV[5:0] | STEP | GAIN LEVEL SETTING | SLV[5:0], SRV[5:0] | STEP | GAIN LEVEL SETTING | SLV[5:0], SRV[5:0] | STEP | GAIN LEVEL SETTING |
|-----------------------|------|-----------------------|-----------------------|------|-----------------------|-----------------------|------|-----------------------|
| 11 1111 | 3F | 6 dB | 10 1001 | 29 | –5 dB | 01 0011 | 13 | –21 dB |
| 11 1110 | 3E | 5.5 dB | 10 1000 | 28 | –5.5 dB | 01 0010 | 12 | –22 dB |
| 11 1101 | 3D | 5 dB | 10 0111 | 27 | –6 dB | 01 0001 | 11 | –23 dB |
| 11 1100 | 3C | 4.5 dB | 10 0110 | 26 | –6.5 dB | 01 0000 | 10 | –24 dB |
| 11 1011 | 3B | 4 dB | 10 0101 | 25 | –7 dB | 00 1111 | 0F | –26 dB |
| 11 1010 | 3A | 3.5 dB | 10 0100 | 24 | –7.5 dB | 00 1110 | 0E | –28 dB |
| 11 1001 | 39 | 3 dB | 10 0011 | 23 | –8 dB | 00 1101 | 0D | –30 dB |
| 11 1000 | 38 | 2.5 dB | 10 0010 | 22 | –8.5 dB | 00 1100 | 0C | –32 dB |
| 11 0111 | 37 | 2 dB | 10 0001 | 21 | –9 dB | 00 1011 | 0B | –34 dB |
| 11 0110 | 36 | 1.5 dB | 10 0000 | 20 | –9.5 dB | 00 1010 | 0A | –36 dB |
| 11 0101 | 35 | 1 dB | 01 1111 | 1F | –10 dB | 00 1001 | 09 | –38 dB |
| 11 0100 | 34 | 0.5 dB | 01 1110 | 1E | –10.5 dB | 00 1000 | 08 | –40 dB |
| 11 0011 | 33 | 0 dB | 01 1101 | 1D | –11 dB | 00 0111 | 07 | –42 dB |
| 11 0010 | 32 | –0.5 dB | 01 1100 | 1C | –12 dB | 00 0110 | 06 | –46 dB |
| 11 0001 | 31 | –1 dB | 01 1011 | 1B | –13 dB | 00 0101 | 05 | –50 dB |
| 11 0000 | 30 | –1.5 dB | 01 1010 | 1A | –14 dB | 00 0100 | 04 | –54 dB |
| 10 1111 | 2F | –2 dB | 01 1001 | 19 | –15 dB | 00 0011 | 03 | –58 dB |
| 10 1110 | 2E | –2.5 dB | 01 1000 | 18 | –16 dB | 00 0010 | 02 | –62 dB |
| 10 1101 | 2D | –3 dB | 01 0111 | 17 | –17 dB | 00 0001 | 01 | –66 dB |
| 10 1100 | 2C | –3.5 dB | 01 0110 | 16 | –18 dB | 00 0000 | 00 | –70 dB |
| 10 1011 | 2B | –4 dB | 01 0101 | 15 | –19 dB | | | |
| 10 1010 | 2A | –4.5 dB | 01 0100 | 14 | –20 dB | | | |

**PCM3793
PCM3794**

SLES193C–AUGUST 2006–REVISED FEBRUARY 2007

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|-----|------|------|------|------|------|------|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 68 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | PMUL | ATL5 | ATL4 | ATL3 | ATL2 | ATL1 | ATL0 |
| Register 69 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | PMUR | ATR5 | ATR4 | ATR3 | ATR2 | ATR1 | ATR0 |

IDX[6:0]: 100 0100b (44h): Register 68

IDX[6:0]: 100 0101b (45h): Register 69

PMUL: Digital Soft Mute Control for DAL (DAC, L-Channel)

PMUR: Digital Soft Mute Control for DAR (DAC R-Channel)

Default value: 0

The digital input to the DAC can be independently muted or unmuted. The transition from the current volume level to mute, or the return to the previous volume setting from mute, occurs at the rate of one 1-dB step for each $8/f_s$ time period. When PMUL and PMUR = 0, the digital data is increased from mute to the previous attenuation level, and when PMUL and PMUR = 1, the digital data is decreased from the current attenuation level to mute. In the PCM3793/94, audible zipper noise can be reduced by using zero-cross detection (register 85, ZCRS).

| | |
|----------------|-------------------------|
| PMUL, PMUR = 0 | Mute disabled (default) |
| PMUL, PMUR = 1 | Mute enabled |

ATL[5:0]: Digital Attenuation Setting for DAL (L-Channel DAC)

ATR[5:0]: Digital Attenuation Setting for DAR (R-Channel DAC)

Default value: 11 1111b

The digital inputs to the DAC can be independently attenuated. The attenuation of each digital input is controlled in 1-dB step for every $8/f_s$ time period. Audible zipper noise in the PCM3793/94 can be reduced by changing the attenuation with zero-cross detection (register 85, ZCRS).

Table 9. Digital Attenuation Setting

| ATL[5:0], ATR[5:0] | ATTENUATION LEVEL SETTING | ATL[5:0], ATR[5:0] | ATTENUATION LEVEL SETTING | ATL[5:0], ATR[5:0] | ATTENUATION LEVEL SETTING |
|-----------------------|------------------------------|-----------------------|------------------------------|-----------------------|------------------------------|
| 11 1111 | 3F | 0 dB (default) | 10 1001 | 29 | –22 dB |
| 11 1110 | 3E | –1 dB | 10 1000 | 28 | –23 dB |
| 11 1101 | 3D | –2 dB | 10 0111 | 27 | –24 dB |
| 11 1100 | 3C | –3 dB | 10 0110 | 26 | –25 dB |
| 11 1011 | 3B | –4 dB | 10 0101 | 25 | –26 dB |
| 11 1010 | 3A | –5 dB | 10 0100 | 24 | –27 dB |
| 11 1001 | 39 | –6 dB | 10 0011 | 23 | –28 dB |
| 11 1000 | 38 | –7 dB | 10 0010 | 22 | –29 dB |
| 11 0111 | 37 | –8 dB | 10 0001 | 21 | –30 dB |
| 11 0110 | 36 | –9 dB | 10 0000 | 20 | –31 dB |
| 11 0101 | 35 | –10 dB | 01 1111 | 1F | –32 dB |
| 11 0100 | 34 | –11 dB | 01 1110 | 1E | –33 dB |
| 11 0011 | 33 | –12 dB | 01 1101 | 1D | –34 dB |
| 11 0010 | 32 | –13 dB | 01 1100 | 1C | –35 dB |
| 11 0001 | 31 | –14 dB | 01 1011 | 1B | –36 dB |
| 11 0000 | 30 | –15 dB | 01 1010 | 1A | –37 dB |
| 10 1111 | 2F | –16 dB | 01 1001 | 19 | –38 dB |
| 10 1110 | 2E | –17 dB | 01 1000 | 18 | –39 dB |
| 10 1101 | 2D | –18 dB | 01 0111 | 17 | –40 dB |
| 10 1100 | 2C | –19 dB | 01 0110 | 16 | –41 dB |
| 10 1011 | 2B | –20 dB | 01 0101 | 15 | –42 dB |
| 10 1010 | 2A | –21 dB | 01 0100 | 14 | –43 dB |
| | | | | | |

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|------|------|------|------|-----|-----|-----|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 70 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | DEM1 | DEM0 | PFM1 | PFM0 | RSV | RSV | RSV | OVER |

IDX[6:0]: 100 0110b (46h): Register 70

DEM[1:0]: De-Emphasis Filter Selection

Default value: 00

The digital de-emphasis filter is in front of the interpolation filter. One of three de-emphasis filters can be selected, corresponding to sampling rate, 32 kHz, 44.1 kHz, or 48 kHz.

| DEM[1:0] | De-Emphasis Filter Selection |
|----------|------------------------------|
| 00 | OFF (default) |
| 01 | 32 kHz |
| 10 | 44.1 kHz |
| 11 | 48 kHz |

PFM[1:0]: Audio Interface Selection for DAC (Digital Input)

Default value: 00

The audio interface for the DAC digital input has I²S, right-justified, left-justified, and DSP formats.

| PFM[1:0] | Audio Interface Selection for DAC Digital Input |
|----------|---|
| 00 | I ² S format (default) |
| 01 | Right-justified format |
| 10 | Left-justified format |
| 11 | DSP format |

OVER: Oversampling Control for Delta-Sigma DAC

Default value: 0

This bit is used to control the oversampling rate of delta-sigma DAC. When the PCM3793/94 operates at low sampling rates, less than 24 kHz with SCK1 frequency less than 12.5 MHz, using this function with OVER = 1 is recommended.

| | |
|----------|--|
| OVER = 0 | 128 f _S (default) |
| OVER = 1 | 192 f _S , 256 f _S , 384 f _S |

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|-----|-----|-----|------|------|------|------|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 71 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | RSV | RSV | SPSE | SPS1 | SPS0 | DFQ1 | DFQ0 |

IDX[6:0]: 100 0111b (47h): Register 71

SPSE: Enable of Spectrum Spreading

Default value: 0

The class-D speaker amplifier output can cause RF interference due to switching noise. The PCM3793 can reduce peak noise by the use of spectrum spreading technology when SPSE = 1.

| | |
|----------|-------------------|
| SPSE = 0 | Disable (default) |
| SPSE = 1 | Enable |

SPS[1:0]: Spectrum Spreading Efficiency

Default value: 00

The efficiency of spectrum spreading technology can be changed to low, medium, or high.

| SPS[1:0] | Spectrum Spreading Efficiency |
|----------|-------------------------------|
| 00 | Low (default) |
| 01 | Medium |
| 10 | High |
| 11 | Reserved |

DFQ[1:0]: Switching Frequency for Speaker Amplifier (Class-D)

Default value: 00

Switching frequency for the class-D speaker amplifier can be selected to avoid interference with other equipment.

| DFQ[1:0] | Class D Amplifier Switching Frequency |
|----------|---------------------------------------|
| 00 | 1.5 MHz (default) |
| 01 | 2.25 MHz |
| 10 | 2.65 MHz |
| 11 | 3 MHz |

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|------|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 72 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | RSV | RSV | RSV | RSV | RSV | PMXR | PMXL |

IDX[6:0]: 100 1000b (48h) Register 72

PMXR: Power Up/Down for MXR (Mixer R-Channel)

PMXL: Power Up/Down for MXL (Mixer L-Channel)

Default value: 0

These bits are used to control power up and down for the analog mixer.

| | |
|----------------|----------------------|
| PMXL, PMXR = 0 | Power down (default) |
| PMXL, PMXR = 1 | Power up |

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-------------|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| Register 73 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | PBIS | PDAR | PDAL | PHPC | PHPR | PHPL | PSPR | PSPL |

IDX[6:0]: 100 1001b (49h): Register 73

PBIS: Power Up/Down Control for Bias

Default value: 0

This bit is used to control power up/down for the analog bias circuit.

| | |
|----------|----------------------|
| PBIS = 0 | Power down (default) |
| PBIS = 1 | Power up |

PDAR: Power Up/Down Control for DAR (DAC and R-Channel Digital Filter)

PDAL: Power Up/Down Control for DAL (DAC and L-Channel Digital Filter)

Default value: 0

This bit is used to control power up/down for the DAC and interpolation filter.

| | |
|----------------|----------------------|
| PDAR, PDAL = 0 | Power down (default) |
| PDAR, PDAL = 1 | Power up |

PHPC: Power Up/Down Control for HPC (Headphone COM/Monaural Output)

Default value: 0

This bit is used to control power up/down for the headphone COM or monaural line amplifier.

| | |
|----------|----------------------|
| PHPC = 0 | Power down (default) |
| PHPC = 1 | Power up |

PHPR: Power Up/Down Control for HPR (Line or R-Channel Headphone Output)

PHPL: Power Up/Down Control for HPL (Line or L-Channel Headphone Output)

Default value: 0

This bit is used to control power up/down for the headphone amplifier.

| | |
|----------------|----------------------|
| PHPR, PHPL = 0 | Power down (default) |
| PHPR, PHPL = 1 | Power up |

PSPR: Power Up/Down Control for SPR (R-Channel Speaker Output, PCM3793)

PSPL: Power Up/Down Control for SPL (L-Channel Speaker Output, PCM3793)

Default value: 0

This bit is used to control power up/down for the PCM3793 speaker amplifier. This bit is should be set to 0 for the PCM3794, because it has no speaker outputs.

| | |
|----------------|----------------------|
| PSPR, PSPL = 0 | Power down (default) |
| PSPR, PSPL = 1 | Power up |

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|-----|------|------|------|------|------|------|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 74 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | CMS2 | CMS1 | CMS0 | HPS1 | HPS0 | SPKS | PCOM |

IDX[6:0]: 100 1010b (4Ah): Register 74

CMS[2:0]: Output Selection for HPC (Headphone COM/Monaural Output)

Default value: 000

HPCOM/MONO output can be selected from several input analog sources, including inverted HPOR output, inverted HPOL output, and monaural output.

| CMS[2:0] | HPCOM/MONO Output Selection |
|----------|---|
| 0 0 0 | Common voltage (0.5 V _{CC}) output for capless mode (default) |
| 0 0 1 | Monaural output |
| 0 1 0 | Inverted HPOL output |
| 1 0 0 | Inverted HPOR output |
| Others | Reserved |

HPS[1:0]: Line or Headphone Output Configuration

Default value: 00

The HPOL/LOL and HPOR/LOR output configuration can be selected as follows.

| HPS[1:0] | Line or Headphone Output Configuration |
|----------|--|
| 0 0 | Stereo output (default) |
| 0 1 | Single monaural output |
| 1 0 | Differential monaural output |
| 1 1 | Reserved |

SPKS: Speaker Output Configuration

Default value: 00

The SPOLP/SPOLN and SPORP/SPORN output configuration can be selected as follows.

| | |
|----------|-------------------------|
| SPKS = 0 | Stereo output (default) |
| SPKS = 1 | Monaural output |

PCOM: Power Up/Down Control for V_{COM}

Default value: 0

This bit is used to control power up/down for V_{COM}.

| | |
|----------|----------------------|
| PCOM = 0 | Power down (default) |
| PCOM = 1 | Power up |

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|------|------|-----|------|------|------|------|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 75 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | HPDP | HPDE | RSV | SDHC | SDHR | SDHL | SDSR | SDSL |

IDX[6:0]: 1001011b (4Bh): Register 75

HPDP: Headphone Insertion Detection Polarity

HPDE: Enable for Headphone Insertion Detection

Default value: 0

Table 10. Headphone Insertion Detection

| HPDE | HPDP | HDTI (PIN 8) | HP OUTPUT | SP OUTPUT |
|------|------|--------------|--|-----------|
| 1 | 0 | 0 | Down | Up |
| 1 | 0 | 1 | Up | Down |
| 1 | 1 | 0 | Up | Down |
| 1 | 1 | 1 | Down | Up |
| 0 | X | X | Headphone insertion detection disabled | |

SDHC: Short Protection Disable for HPC (Headphone COM/Monaural Output)

SDHR: Short Protection Disable for HPR (R-Channel Headphone)

SDHL: Short Protection Disable for HPL (L-Channel Headphone)

Default value: 0

Short-circuit protection can be disabled if this function is not needed in an application.

| | |
|----------------------|-------------------|
| SDHC, SDHR, SDHL = 0 | Enabled (default) |
| SDHC, SDHR, SDHL = 1 | Disabled |

SDSR: Thermal Protection Disable for SPR (Speaker Amplifier R-Channel)

SDSL: Thermal Protection Disable for SPL (Speaker Amplifier L-Channel)

Default value: 0

The thermal protection circuit can be disabled if this function is not needed in an application.

| | |
|----------------|-------------------|
| SDSR, SDSL = 0 | Enabled (default) |
| SDSR, SDSL = 1 | Disabled |

SLES193C–AUGUST 2006–REVISED FEBRUARY 2007

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-------------|-----|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|------|------|
| Register 76 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | RSV | RSV | RSV | RSV | RSV | RLSR | RLSL |

IDX[6:0]: 100 1100b (4Ch): Register 76

RLSR: Reset Thermal Protection Circuit for SPR (R-Channel Speaker Amplifier)

RLSL: Reset Thermal Protection Circuit for SPL (L-Channel Speaker Amplifier)

Default value: 0

Short-circuit protection puts the device in power-down status after it detects a temperature of approximately 150°C on the die. These bits must be set to 1 to restore power to the speaker amplifier.

| | |
|----------------|---|
| RLSR, RLSL = 0 | Operation (default) |
| RLSR, RLSL = 1 | Reset (set to 0 automatically after being set to 1) |

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-------------|-----|------|------|------|------|------|------|------|------|-----|-----|------|------|------|------|------|
| Register 77 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | HPDS | RSV | RSV | STHC | STHR | STHL | STSR | STSL |

IDX[6:0]: 100 1101b (4Dh): Register 77

HPDS: Headphone Detection Status

Default value: 0

The HPDS bit shows the status of insert detection for the headphone. This is a read-only bit. The polarity depends on register 75 HPDP setting.

| | |
|----------|--------------------------------------|
| HPDS = 0 | HDTI input (when HPDP = 0) (default) |
| HPDS = 1 | Inverted HDTI input (When HPDP = 1) |

STHC: Short Protection Status for HPC (Headphone COM/Monaural Output)

STHR: Short Protection Status for HPR (R-Channel Headphone)

STHL: Short Protection Status for HPL (L-Channel Headphone)

These bits can be read through the I²C interface to determine short protection status.

| | |
|----------------------|--------------------------|
| STHC, STHR, STHL = 0 | Detect short circuit |
| STHC, STHR, STHL = 1 | Not detect short circuit |

STSR: Thermal Protection Status for SPR (R-Channel Speaker)

STSL: Thermal Protection Status for SPL (L-Channel Speaker)

These bits can be read through the I²C interface to determine thermal protection status.

| | |
|----------------|-------------------------------|
| STSR, STSL = 0 | Detect thermal protection |
| STSR, STSL = 1 | Not detect thermal protection |

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|-----|-----|------|------|------|------|------|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 79 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | RSV | ALV5 | ALV4 | ALV3 | ALV2 | ALV1 | ALV0 |
| Register 80 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | RSV | ARV5 | ARV4 | ARV3 | ARV2 | ARV1 | ARV0 |

IDX[6:0]: 100 1111b (4Fh): Register 79

IDX[6:0]: 101 0000b (50h): Register 80

ALV[5:0]: Gain Control for PG3 (R-Channel ADC Analog Input)

ARV[5:0]: Gain Control for PG4 (L-Channel ADC Analog Input)

Default value: 00

PG3 and PG4 can be independently controlled for ADC input from 30 dB to –12 dB in 1-dB steps. The ADC output may have zipper noise while changing the level. In the PCM3793/94, the noise can be reduced when making the change by using zero-cross detection (register 85, ZCRS).

Table 11. Gain Level Setting

| ALV[5:0], ARV[5:0] | | GAIN LEVEL SETTING | ALV[5:0], ARV[5:0] | | GAIN LEVEL SETTING |
|-----------------------|----|-----------------------|-----------------------|----|-----------------------|
| 10 1010 | 2A | 30 dB | 01 0100 | 14 | 8 dB |
| 10 1001 | 29 | 29 dB | 01 0011 | 13 | 7 dB |
| 10 1000 | 28 | 28 dB | 01 0010 | 12 | 6 dB |
| 10 0111 | 27 | 27 dB | 01 0001 | 11 | 5 dB |
| 10 0110 | 26 | 26 dB | 01 0000 | 10 | 4 dB |
| 10 0101 | 25 | 25 dB | 00 1111 | 0F | 3 dB |
| 10 0100 | 24 | 24 dB | 00 1110 | 0E | 2 dB |
| 10 0011 | 23 | 23 dB | 00 1101 | 0D | 1 dB |
| 10 0010 | 22 | 22 dB | 00 1100 | 0C | 0 dB |
| 10 0001 | 21 | 21 dB | 00 1011 | 0B | –1 dB |
| 10 0000 | 20 | 20 dB | 00 1010 | 0A | –2 dB |
| 01 1111 | 1F | 19 dB | 00 1001 | 09 | –3 dB |
| 01 1110 | 1E | 18 dB | 00 1000 | 08 | –4 dB |
| 01 1101 | 1D | 17 dB | 00 0111 | 07 | –5 dB |
| 01 1100 | 1C | 16 dB | 00 0110 | 06 | –6 dB |
| 01 1011 | 1B | 15 dB | 00 0101 | 05 | –7 dB |
| 01 1010 | 1A | 14 dB | 00 0100 | 04 | –8 dB |
| 01 1001 | 19 | 13 dB | 00 0011 | 03 | –9 dB |
| 01 1000 | 18 | 12 dB | 00 0010 | 02 | –10 dB |
| 01 0111 | 17 | 11 dB | 00 0001 | 01 | –11 dB |
| 01 0110 | 16 | 10 dB | 00 0000 | 00 | –12 dB (default) |
| 01 0101 | 15 | 9 dB | | | |

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|------|------|------|------|-----|------|------|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 81 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | HPF1 | HPF0 | RMUL | RMUR | RSV | DSMC | RFM1 | RFM0 |

IDX[6:0]: 101 0001b (51h): Register 81

HPF[1:0]: High-Pass Filter Selection

Default value: 00

PCM3793/94 has digital high-pass filter to remove dc voltage at the input of the ADC. The cutoff frequency of the high-pass filter can be selected.

| HPF [1:0] | High-Pass Filter Selection |
|-----------|----------------------------------|
| 0 0 | $f_C = 4$ Hz at 48 kHz (default) |
| 0 1 | $f_C = 240$ Hz at 48 kHz |
| 1 0 | Reserved |
| 1 1 | High-pass filter disabled |

RMUL: Digital Soft Mute Control for L-Channel ADC

RMUR: Digital Soft Mute Control for R-Channel ADC

Default value: 1

The digital output of the ADC can be independently muted or unmuted. The transition from the current volume level to mute, or the return to the previous volume setting from mute, occurs at the rate of one 1-dB step for each $8/f_S$ time period. When PMUL and PMUR = 0, the digital data is increased from mute to the previous attenuation level, and when PMUL and PMUR = 1, the digital data is decreased from the current attenuation level to mute. In the PCM3793/94, audible zipper noise can be reduced by using zero-cross detection (register 85, ZCRS).

| | |
|----------------|------------------------|
| RMUL, RMUR = 0 | Mute disabled |
| RMUL, RMUR = 1 | Mute enabled (default) |

DSMC: Waiting Time for ADC Mute Off at Power Up

Default value: 0

The ADC digital output has an optional delay after power up when DSMC = 0. It is recommended to set DSMC = 0.

| | |
|----------|---------------------------|
| DSMC = 0 | 10 ms at 48 kHz (default) |
| DSMC = 1 | No delay |

RFM[1:0]: Audio Interface Selection for ADC (Digital Output)

Default value: 00

The audio interface for the ADC digital input supports I²S, right-justified, left-justified, and DSP formats.

| RFM [1:0] | Audio Interface Selection for ADC Digital Output |
|-----------|--|
| 0 0 | I ² S format (default) |
| 0 1 | Right-justified format |
| 1 0 | Left-justified format |
| 1 1 | DSP format |

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-------------|-----|------|------|------|------|------|------|------|-----|-----|------|------|------|------|------|------|
| Register 82 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | RSV | PAIR | PAIL | PADS | PMCB | PADR | PADL |

IDX[6:0]: 101 0010b (52h): Register 82

PAIR: Power Up/Down for PG2 and PG6 (Gain Amplifier for R-Channel Analog Input)

PAIL: Power Up/Down for PG1 and PG5 (Gain Amplifier for L-Channel Analog Input)

Default value: 0

This bit is used to control power up/down for PG2 and PG6 (gain amplifier for analog input).

| | |
|----------------|----------------------|
| PAIR, PAIL = 0 | Power down (default) |
| PAIR, PAIL = 1 | Power up |

PADS: Power Up/Down for D2S (Differential Amplifier) of AIN1L and AIN1R

Default value: 0

This bit is used to control power up/down for D2S (differential-to-single amplifier).

| | |
|----------|----------------------|
| PADS = 0 | Power down (default) |
| PADS = 1 | Power up |

PMCB: Power Up/Down Control for Microphone Bias Source

Default value: 0

This bit is used to control power up/down for the microphone bias source.

| | |
|----------|----------------------|
| PMCB = 0 | Power down (default) |
| PMCB = 1 | Power up |

PADR: Power Up/Down Control for ADR (ADC and R-Channel Digital Filter)

PADL: Power Up/Down Control for ADL (ADC and L-Channel Digital Filter)

Default value: 0

This bit is used to control power up/down for the ADC and decimation filter.

| | |
|----------------|----------------------|
| PADR, PADL = 0 | Power down (default) |
| PADR, PADL = 1 | Power up |

| Register 83 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-------------|-----|------|------|------|------|------|------|------|------|-----|------|------|------|------|------|------|
| | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RALC | RSV | RRTC | RATC | RCP1 | RCP0 | RLV1 | RLV0 |

IDX[6:0]: 101 0011b (53h): Register 83

RALC: Automatic Level Control (ALC) Enable for Recording

Default value: 0

Automatic level control can be enabled with some parameters for microphone input or lower analog source level.

| | |
|----------|-------------------|
| RALC = 0 | Disable (default) |
| RALC = 1 | Enable |

RRTC: ALC Recovery Time Control for Recording

Default value: 0

This bit is used to select the recovery time for the ALC. The response is shown in [Figure 36](#).

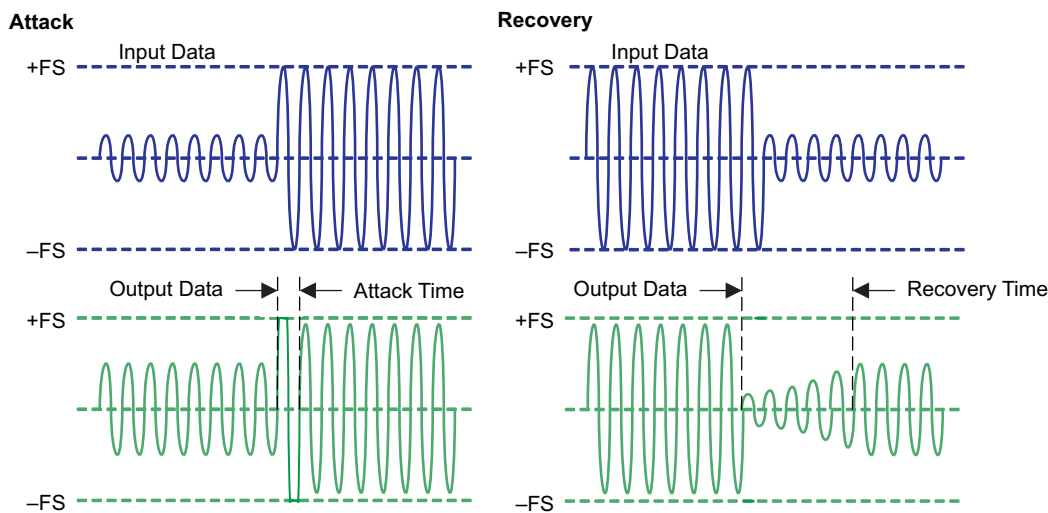
| | |
|----------|-----------------|
| RRTC = 0 | 3.4 s (default) |
| RRTC = 1 | 13.6 s |

RATC: ALC Attack Time Control for Recording

Default value: 0

This bit is used to select the attack time for the ALC. The response is shown in [Figure 36](#).

| | |
|----------|----------------|
| RATC = 0 | 1 ms (default) |
| RATC = 1 | 2 ms |



T0166-01

Figure 36. Attack and Recovery Time Response

RCP[1:0]: ALC Compression Level Control for Recording

Default value: 00

These bits are used to set the compression level for the ALC. The characteristic is shown in [Figure 37](#).

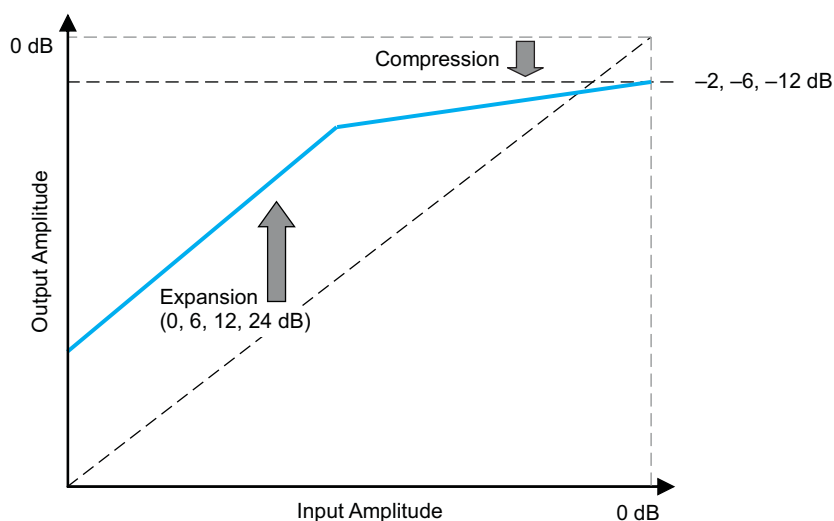
| RCP[1:0] | ALC Compression Level Control for Recording |
|----------|---|
| 0 0 | -2 dB (default) |
| 0 1 | -6 dB |
| 1 0 | -12 dB |
| 1 1 | Reserved |

RLV[1:0]: ALC Expansion Level Control for Recording

Default value: 00

These bits are used to set the expansion level for the ALC. The characteristic is shown in [Figure 37](#).

| RLV[1:0] | ALC Gain Level Control for Recording |
|----------|--------------------------------------|
| 0 0 | 0 dB (default) |
| 0 1 | 6 dB |
| 1 0 | 14 dB |
| 1 1 | 24 dB |



M0057-01

Figure 37. Compression and Expansion Characteristics

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-------------|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| Register 84 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | RSV | RSV | RSV | RSV | MSTR | RSV | BIT0 |
| Register 85 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | SRST | RSV | NPR5 | NPR4 | NPR3 | NPR2 | NPR1 | NPR0 |
| Register 86 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | MBST | MSR2 | MSR1 | MSR0 | ATOD | RSV | RSV | ZCRS |

IDX[6:0]: 101 0100b (54h): Register 84

IDX[6:0]: 101 0101b (55h): Register 85

IDX[6:0]: 101 0110b (56h): Register 86

MSTR: Master or Slave Selection for Audio Interface

Default value: 0

This bit is used to select either master or slave mode for the audio interface. In master mode, the PCM3793/94 generates LRCK and BCK from the system clock. In slave mode, it receives LRCK and BCK from another device.

| | |
|----------|---------------------------|
| MSTR = 0 | Slave interface (default) |
| MSTR = 1 | Master interface |

BIT0: Bit Length Selection for Audio Interface

Default value: 1

This bit is used to select the data bit length for DAC input.

| | |
|----------|-------------------|
| BIT0 = 0 | Reserved |
| BIT0 = 1 | 16 bits (default) |

SRST: System Reset

Default value: 0

This bit is used to enable system reset. All circuits are reset by setting SRST = 1. After completing the reset sequence, SRST is set to 0 automatically.

| | |
|----------|--------------------------|
| SRST = 0 | Reset disabled (default) |
| SRST = 1 | Reset enabled |

NPR[5:0]: System Clock Rate Selection

Default value: 000000

MSR[2:0]: System Clock Dividing Rate Selection in Master Mode (Register 70)

Default value: 000

These bits are used to select the system clock rate and the dividing rate of the input system clock. See [Table 12](#) for the details.

Table 12. System Clock Frequency for Common-Audio Clock

| SYSTEM CLOCK SCK (MHz) | ADC SAMPLING RATE ADC f_s (kHz) | DAC SAMPLING RATE DAC f_s (kHz) | REGISTER SETTINGS ⁽¹⁾ | | BIT CLOCK BCK (f_s) |
|---------------------------|--------------------------------------|--------------------------------------|----------------------------------|----------|----------------------------|
| | | | MSR[2:0] | NPR[5:0] | |
| 6.144 | 24 (SCK/256) | | 010 | 00 0000 | 64 |
| | 16 (SCK/384) | | 011 | 00 0000 | 64 |
| | 12 (SCK/512) | | 100 | 00 0000 | 64 |
| | 8 (SCK/768) | | 101 | 00 0000 | 64 |
| | 6 (SCK/1024) | | 110 | 00 0000 | 64 |
| | 4 (SCK/1536) | | 111 | 00 0000 | 64 |
| 8.192 | 32 (SCK/256) | | 010 | 00 0000 | 64 |
| | 16 (SCK/512) | | 100 | 00 0000 | 64 |
| | 8 (SCK/1024) | | 110 | 00 0000 | 64 |
| 12.288 | 48 (SCK/256) | | 010 | 00 0000 | 64 |
| | 32 (SCK/384) | | 011 | 00 0000 | 64 |
| | 24 (SCK/512) | | 100 | 00 0000 | 64 |
| | 16 (SCK/768) | | 101 | 00 0000 | 64 |
| | 12 (SCK/1024) | | 110 | 00 0000 | 64 |
| | 8 (SCK/1536) | | 111 | 00 0000 | 64 |
| 18.432 | 48 (SCK/384) | | 011 | 00 0000 | 64 |
| | 24 (SCK/768) | | 101 | 00 0000 | 64 |
| | 12 (SCK/1536) | | 111 | 00 0000 | 64 |
| 5.6448 | 22.05 (SCK/256) | | 010 | 00 0000 | 64 |
| | 14.7 (SCK/384) | | 011 | 00 0000 | 64 |
| | 11.025 (SCK/512) | | 100 | 00 0000 | 64 |
| | 7.35 (SCK/768) | | 101 | 00 0000 | 64 |
| | 5.5125 (SCK/1024) | | 110 | 00 0000 | 64 |
| | 3.675 (SCK/1536) | | 111 | 00 0000 | 64 |
| 11.2896 | 44.1 (SCK/256) | | 010 | 00 0000 | 64 |
| | 29.4 (SCK/384) | | 011 | 00 0000 | 64 |
| | 22.05 (SCK/512) | | 100 | 00 0000 | 64 |
| | 14.7 (SCK/768) | | 101 | 00 0000 | 64 |
| | 11.025 (SCK/1024) | | 110 | 00 0000 | 64 |
| | 7.35 (SCK/1536) | | 111 | 00 0000 | 64 |

(1) Other settings are reserved.

Table 13. System Clock Frequency for Application-Specific Clock

| SYSTEM CLOCK SCK (MHz) | ADC SAMPLING RATE ADC f_s (kHz) | DAC SAMPLING RATE DAC f_s (kHz) | REGISTER SETTINGS | | BIT CLOCK BCK (f_s) |
|---------------------------|--------------------------------------|--------------------------------------|-------------------|----------|----------------------------|
| | | | MSR[2:0] | NPR[5:0] | |
| 13.5 | 48.214 (SCK/280) | | 010 | 00 0010 | 70 |
| | 44.407 (SCK/304) | | 010 | 00 0001 | 76 |
| | 32.142 (SCK/420) | | 010 | 10 0010 | 70 |
| | 24.107 (SCK/560) | | 100 | 00 0010 | 70 |
| | 22.203 (SCK/608) | | 100 | 00 0001 | 76 |
| | 16.071 (SCK/840) | | 100 | 10 0010 | 70 |
| | 12.053 (SCK/1120) | | 110 | 00 0010 | 70 |
| | 8.035 (SCK/1680) | | 110 | 10 0010 | 70 |
| 27 | 48.214 (SCK/560) | | 010 | 01 0010 | 70 |
| | 44.407 (SCK/608) | | 010 | 01 0001 | 76 |
| | 32.142 (SCK/840) | | 010 | 11 0010 | 70 |
| | 24.107 (SCK/1120) | | 100 | 01 0010 | 70 |
| | 22.203 (SCK/1216) | | 100 | 01 0001 | 76 |
| | 16.071 (SCK/1680) | | 100 | 11 0010 | 70 |
| | 12.053 (SCK/2240) | | 110 | 01 0010 | 70 |
| | 8.035 (SCK/3360) | | 110 | 11 0010 | 70 |
| 12 | 48.387 (SCK/248) | | 010 | 00 0100 | 62 |
| | 44.117 (SCK/272) | | 010 | 00 0011 | 68 |
| | 32.258 (SCK/372) | | 010 | 10 0100 | 62 |
| | 24.193 (SCK/496) | | 100 | 00 0100 | 62 |
| | 22.058 (SCK/544) | | 100 | 00 0011 | 68 |
| | 16.129 (SCK/744) | | 100 | 10 0100 | 62 |
| | 12.096 (SCK/992) | | 110 | 00 0100 | 62 |
| | 8.064 (SCK/1488) | | 110 | 10 0100 | 62 |
| 24 | 48.387 (SCK/496) | | 010 | 01 0100 | 62 |
| | 44.117 (SCK/544) | | 010 | 01 0011 | 68 |
| | 32.258 (SCK/744) | | 010 | 11 0100 | 62 |
| | 24.193 (SCK/992) | | 100 | 01 0100 | 62 |
| | 22.058 (SCK/1088) | | 100 | 01 0011 | 68 |
| | 16.129 (SCK/1488) | | 100 | 11 0100 | 62 |
| | 12.096 (SCK/1984) | | 110 | 01 0100 | 62 |
| | 8.064 (SCK/2976) | | 110 | 11 0100 | 62 |
| 19.2 | 48.484 (SCK/396) | | 011 | 00 0110 | 66 |
| | 44.444 (SCK/432) | | 011 | 00 0101 | 72 |
| | 32.323 (SCK/594) | | 011 | 10 0110 | 66 |
| | 24.242 (SCK/792) | | 101 | 00 0110 | 66 |
| | 22.222 (SCK/864) | | 101 | 00 0101 | 72 |
| | 16.161 (SCK/1188) | | 101 | 10 0110 | 66 |
| | 12.121 (SCK/1584) | | 111 | 00 0110 | 66 |
| | 8.080 (SCK/2376) | | 111 | 10 0110 | 66 |

Table 13. System Clock Frequency for Application-Specific Clock (continued)

| SYSTEM CLOCK SCK (MHz) | ADC SAMPLING RATE ADC f_s (kHz) | DAC SAMPLING RATE DAC f_s (kHz) | REGISTER SETTINGS | | BIT CLOCK BCK (f_s) |
|---------------------------|--------------------------------------|--------------------------------------|-------------------|----------|----------------------------|
| | | | MSR[2:0] | NPR[5:0] | |
| 38.4 | 48.484 (SCK/792) | | 011 | 01 0110 | 66 |
| | 44.444 (SCK/864) | | 011 | 01 0101 | 72 |
| | 32.323 (SCK/1188) | | 011 | 11 0110 | 66 |
| | 24.242 (SCK/1584) | | 101 | 01 0110 | 66 |
| | 22.222 (SCK/1728) | | 101 | 01 0101 | 72 |
| | 16.161 (SCK/2376) | | 101 | 11 0110 | 66 |
| | 12.121 (SCK/3168) | | 111 | 01 0110 | 66 |
| | 8.080 (SCK/4752) | | 111 | 11 0110 | 66 |
| 13 | 47.794 (SCK/272) | | 010 | 00 1000 | 68 |
| | 43.918 (SCK/296) | | 010 | 00 0111 | 74 |
| | 31.862 (SCK/408) | | 010 | 10 1000 | 68 |
| | 23.897 (SCK/544) | | 100 | 00 1000 | 68 |
| | 21.959 (SCK/592) | | 100 | 00 0111 | 74 |
| | 15.931 (SCK/816) | | 100 | 10 1000 | 68 |
| | 11.948 (SCK/1088) | | 110 | 00 1000 | 68 |
| | 7.965 (SCK/1632) | | 110 | 10 1000 | 68 |
| 26 | 47.794 (SCK/544) | | 010 | 01 1000 | 68 |
| | 43.918 (SCK/592) | | 010 | 01 0111 | 74 |
| | 31.862 (SCK/816) | | 010 | 11 1000 | 68 |
| | 23.897 (SCK/1088) | | 100 | 01 1000 | 68 |
| | 21.959 (SCK/1184) | | 100 | 01 0111 | 74 |
| | 15.931 (SCK/1632) | | 100 | 11 1000 | 68 |
| | 11.948 (SCK/2176) | | 110 | 01 1000 | 68 |
| | 7.965 (SCK/3264) | | 110 | 11 1000 | 68 |
| 19.68 | 48.235 (SCK/408) | | 011 | 00 1010 | 68 |
| | 44.324 (SCK/444) | | 011 | 00 1001 | 74 |
| | 32.156 (SCK/612) | | 011 | 10 1010 | 68 |
| | 24.117 (SCK/816) | | 101 | 00 1010 | 68 |
| | 22.162 (SCK/888) | | 101 | 00 1001 | 74 |
| | 16.078 (SCK/1224) | | 101 | 10 1010 | 68 |
| | 12.058 (SCK/1632) | | 111 | 00 1010 | 68 |
| | 8.039 (SCK/2448) | | 111 | 10 1010 | 68 |
| 39.36 | 48.235 (SCK/816) | | 011 | 01 1010 | 68 |
| | 44.324 (SCK/888) | | 011 | 01 1001 | 74 |
| | 32.156 (SCK/1224) | | 011 | 11 1010 | 68 |
| | 24.117 (SCK/1632) | | 101 | 01 1010 | 68 |
| | 22.162 (SCK/1776) | | 101 | 01 1001 | 74 |
| | 16.078 (SCK/2448) | | 101 | 11 1010 | 68 |
| | 12.058 (SCK/3264) | | 111 | 01 1010 | 68 |
| | 8.039 (SCK/4896) | | 111 | 11 1010 | 68 |

MBST: BCK Output Configuration in Master Mode

Default value: 0

This bit is used to control the BCK output configuration in master mode. In master mode, this bit sets the BCK output configuration to normal mode or burst mode. In normal mode (MBST = 0), the BCK clock runs continuously. In burst mode (MBST = 1), the BCK clock runs intermittently, and the number of clock cycles per LRCK period is reduced to equal the number of bits of audio data being transmitted. Operating in burst mode reduces the power consumption of V_{IO} (I/O cell power supply). This is effective in master mode (register 69 MSTR = 1).

| | |
|----------|-------------------------|
| MBST = 0 | Normal output (default) |
| MBST = 1 | Burst output |

ATOD: ADC Digital Output to DAC Digital Input (Loopback)

Default value: 0

The ADC digital output is internally connected to the DAC digital input by setting ATOD = 1. This setting can be used to debug ADC functions or to monitor a recording.

| | |
|---------|--------------------|
| ATOD= 0 | Disabled (default) |
| ATOD= 1 | Enabled |

ZCRS: Zero-Cross for Digital Attenuation/Mute and Analog Gain Setting

Default value: 0

This bit is used to enable the zero-cross detector, which reduces zipper noise while the digital soft mute, digital attenuation analog gain setting, or analog volume setting is being changed. If no zero-cross data is input for a $512/f_s$ period (10.6 ms at a 48-kHz sampling rate), then a time-out occurs and the PCM3793/94 starts changing the attenuation, gain, or volume level. The zero-cross detector cannot be used with continuous-zero and dc data.

| | |
|----------|-------------------------------|
| ZCRS = 0 | Zero cross disabled (default) |
| ZCRS = 1 | Zero cross enabled |

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|------|-----|------|------|-----|-----|------|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 87 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | AD2S | RSV | AIR1 | AIR0 | RSV | RSV | AIL1 | AILO |

IDX[6:0]: 101 0111b (57h): Register 87

AD2S: Differential Amplifier Selector (MUX3 and MUX4)

Default value: 0

The PCM3793/94 has stereo single-input amplifiers (PG1, PG2) and a monaural differential-input amplifier (D2S) which can be used as ADC inputs. MUX3 and MUX4 can be selected as the monaural differential input by setting AD2S = 1.

| | |
|----------|-----------------------------------|
| AD2S = 0 | Single-input amplifiers (default) |
| AD2S = 1 | Differential-input amplifier |

AIL[1:0]: AIN1L, AIN2L, and AIN3L Selector (MUX1)

Default value: 00

This bit is used to select one of the three analog inputs, AIN1L, AIN2L, or AIN3L.

| AIL[1:0] | AIN L-channel Select |
|----------|----------------------|
| 0 0 | Disconnect (default) |
| 0 1 | AIN1L |
| 1 0 | AIN2L |
| 1 1 | AIN3L |

AIR[1:0]: AIN1R, AIN2R, and AIN3R Selector (MUX2)

Default value: 00

This bit is used to select one of the three stereo analog inputs, AIN1R, AIN2R, or AIN3R.

| AIR[1:0] | AIN R-channel Select |
|----------|----------------------|
| 0 0 | Disconnect (default) |
| 0 1 | AIN1R |
| 1 0 | AIN2R |
| 1 1 | AIN3R |

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-------------|-----|------|------|------|------|------|------|------|-----|------|------|------|-----|------|------|------|
| Register 88 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | MXR2 | MXR1 | MXR0 | RSV | MXL2 | MXL1 | MXL0 |

IDX[6:0]: 101 1000b (58h): Register 88

MXR2: Mixing SW6 to MXR (R-Channel Mixing Amplifier) From L-Channel Analog Input

Default value: 0

This bit is used to connect an analog source to MXR (R-ch mixing amplifier) from the L-ch analog input.

| | |
|----------|-------------------|
| MXR2 = 0 | Disable (default) |
| MXR2 = 1 | Enable |

MXR1: Mixing SW4 to MXR (R-Channel Mixing Amplifier) From R-Channel Analog Input

Default value: 0

This bit is used to connect an analog source to MXR (R-ch mixing amplifier) from the R-ch analog input.

| | |
|----------|-------------------|
| MXR1 = 0 | Disable (default) |
| MXR1 = 1 | Enable |

MXR0: Mixing SW5 to MXR (R-Channel Mixing Amplifier) From R-Channel DAC

Default value: 0

This bit is used to connect an analog source to MXR (R-ch mixing amplifier) from the R-ch DAC.

| | |
|----------|-------------------|
| MXR0 = 0 | Disable (default) |
| MXR0 = 1 | Enable |

MXL2: Mixing SW3 to MXL (L-Channel Mixing Amplifier) From R-Channel Analog Input

Default value: 0

This bit is used to connect an analog source to MXL (L-ch mixing amplifier) from the R-ch analog input.

| | |
|----------|-------------------|
| MXL2 = 0 | Disable (default) |
| MXL2 = 1 | Enable |

MXL1: Mixing SW1 to MXL (L-Channel Mixing Amplifier) From L-Channel Analog Input

Default value: 0

This bit is used to connect an analog source to MXR (L-ch mixing amplifier) from the L-ch analog input.

| | |
|----------|-------------------|
| MXL1 = 0 | Disable (default) |
| MXL1 = 1 | Enable |

MXL0: Mixing SW2 to MXL (L-Channel Mixing Amplifier) From L-Channel DAC

Default value: 0

This bit is used to connect an analog source to MXR (L-ch mixing amplifier) from the L-ch DAC.

| | |
|----------|-------------------|
| MXL0 = 0 | Disable (default) |
| MXL0 = 1 | Enable |

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-------------|-----|------|------|------|------|------|------|------|-----|------|------|------|-----|------|------|------|
| Register 89 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | GMR2 | GMR1 | GMR0 | RSV | GML2 | GML1 | GML0 |

IDX[6:0]: 101 1001b (59h): Register 89

GMR[2:0]: Gain Level Control for PG6 (Gain Amplifier for Analog Input or R-Channel Bypass)

GML[2:0]: Gain Level Control for PG5 (Gain Amplifier for Analog Input or L-Channel Bypass)

Default value: 111

These bits are used for setting the gain level of the analog source to the mixing amplifier. It is recommended to set the gain level to avoid saturation in the analog mixer.

| GMR[2:0] GML[2:0] | Gain Level Control for PG6 Gain Level Control for PG5 |
|------------------------------------|--|
| 0 0 0 | –21 dB |
| 0 0 1 | –18 dB |
| 0 1 0 | –15 dB |
| 0 1 1 | –12 dB |
| 1 0 0 | –9 dB |
| 1 0 1 | –6 dB |
| 1 1 0 | –3 dB |
| 1 1 1 | 0 dB (default) |

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|-----|-----|------|------|-----|-----|------|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 90 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | RSV | CMT1 | CMT0 | RSV | RSV | G20R | G20L |

IDX[6:0]: 1011010b (5Ah): Register 90

CMT[1:0]: V_{COM} Ramp Up/Down Time Control

Default value: 00

These bits are used for selecting ramp up/down time from ground level to the common-voltage level or from the common-voltage to ground level during the power up/down sequence, in order to reduce audible pop noise.

| CMT[1:0] | V_{COM} Ramp Up/Down Time Control |
|----------|---|
| 0 0 | Nominal; $R_{CMT} = 60 \text{ k}\Omega$ (default) |
| 0 1 | Slow; $R_{CMT} = 120 \text{ k}\Omega$ |
| 1 0 | Fast; $R_{CMT} = 30 \text{ k}\Omega$ |
| 1 1 | Fastest; $R_{CMT} = 2.73 \text{ k}\Omega$ |

G20R: 20-dB Boost for PG2 (Gain Amplifier for AIN1R, AIN2R, and AIN3R)

Default value: 0

This bit is used to boost the microphone signal when the analog input is small.

| | |
|----------|----------------|
| G20R = 0 | 0 dB (default) |
| G20R = 1 | 20-dB boost |

G20L: 20-dB Boost for PG1 (Gain Amplifier for AIN1L, AIN2L, and AIN3L)

Default value: 0

This bit is used to boost the microphone signal when the analog input is small.

| | |
|----------|----------------|
| G20L = 0 | 0 dB (default) |
| G20L = 1 | 20-dB boost |

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|------|-----|-----|------|------|------|------|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 92 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | LPAE | RSV | RSV | LGA4 | LGA3 | LGA2 | LGA1 | LGA0 |

IDX[6:0]: 101 1100b (5Ch): Register 92

LPAE: Gain Adjustment for Bass Boost Gain Control

Default value: 0

A gain setting for bass boost may cause digital data may saturation, depending on the input data level. Where this could occur, LPAE can be used to set the same attenuation level as the bass boost gain level for the digital input data.

| | |
|----------|-------------------|
| LPAE = 0 | Disable (default) |
| LPAE = 1 | Enable |

LGA[4:0]: Bass Boost Gain Control

Default value: 0 0000

These bits are used to set the bass boost gain level for digital data. The detailed characteristic is shown in the *Typical Performance Curves*.

| LGA[4:0] | TONE CONTROL GAIN (BASS) | LGA[4:0] | TONE CONTROL GAIN (BASS) |
|----------|--------------------------|----------|--------------------------|
| 0 0000 | 0 dB (default) | 0 1111 | 0 dB |
| 0 0011 | 12 dB | 1 0000 | -1 dB |
| 0 0100 | 11 dB | 1 0001 | -2 dB |
| 0 0101 | 10 dB | 1 0010 | -3 dB |
| 0 0110 | 9 dB | 1 0011 | -4 dB |
| 0 0111 | 8 dB | 1 0100 | -5 dB |
| 0 1000 | 7 dB | 1 0101 | -6 dB |
| 0 1001 | 6 dB | 1 0110 | -7 dB |
| 0 1010 | 5 dB | 1 0111 | -8 dB |
| 0 1011 | 4 dB | 1 1000 | -9 dB |
| 0 1100 | 3 dB | 1 1001 | -10 dB |
| 0 1101 | 2 dB | 1 1010 | -11 dB |
| 0 1110 | 1 dB | 1 1011 | -12 dB |

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|-----|-----|-----|------|------|------|------|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 93 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | RSV | RSV | MGA4 | MGA3 | MGA2 | MGA1 | MGA0 |

IDX[6:0]: 101 1101b (5Dh): Register 93

MGA[4:0]: Middle Boost Gain Control

Default value: 00000

These bits are used to set middle boost gain level to digital data. The detailed characteristic is shown in the *Typical Performance Curves*.

| MGA[4:0] | TONE CONTROL GAIN (MIDRANGE) | MGA[4:0] | TONE CONTROL GAIN (MIDRANGE) |
|----------|------------------------------|----------|------------------------------|
| 0 0000 | 0 dB (default) | 0 1111 | 0 dB |
| 0 0011 | 12 dB | 1 0000 | -1 dB |
| 0 0100 | 11 dB | 1 0001 | -2 dB |
| 0 0101 | 10 dB | 1 0010 | -3 dB |
| 0 0110 | 9 dB | 1 0011 | -4 dB |
| 0 0111 | 8 dB | 1 0100 | -5 dB |
| 0 1000 | 7 dB | 1 0101 | -6 dB |
| 0 1001 | 6 dB | 1 0110 | -7 dB |
| 0 1010 | 5 dB | 1 0111 | -8 dB |
| 0 1011 | 4 dB | 1 1000 | -9 dB |
| 0 1100 | 3 dB | 1 1001 | -10 dB |
| 0 1101 | 2 dB | 1 1010 | -11 dB |
| 0 1110 | 1 dB | 1 1011 | -12 dB |

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|-----|-----|-----|------|------|------|------|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 94 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | RSV | RSV | HGA4 | HGA3 | HGA2 | HGA1 | HGA0 |

IDX[6:0]: 101 1110b (5Eh): Register 94

HGA[4:0]: Treble Boost Gain Control ($f_c = 5$ kHz)

Default value: 00000

These bits are used to set middle boost gain level to digital data. The detailed characteristic is shown in the *Typical Performance Curves*.

| HGA[4:0] | TONE CONTROL GAIN (TREBLE) | HGA[4:0] | TONE CONTROL GAIN (TREBLE) |
|----------|----------------------------|----------|----------------------------|
| 0 0000 | 0 dB (default) | 0 1111 | 0 dB |
| 0 0011 | 12 dB | 1 0000 | -1 dB |
| 0 0100 | 11 dB | 1 0001 | -2 dB |
| 0 0101 | 10 dB | 1 0010 | -3 dB |
| 0 0110 | 9 dB | 1 0011 | -4 dB |
| 0 0111 | 8 dB | 1 0100 | -5 dB |
| 0 1000 | 7 dB | 1 0101 | -6 dB |
| 0 1001 | 6 dB | 1 0110 | -7 dB |
| 0 1010 | 5 dB | 1 0111 | -8 dB |
| 0 1011 | 4 dB | 1 1000 | -9 dB |
| 0 1100 | 3 dB | 1 1001 | -10 dB |
| 0 1101 | 2 dB | 1 1010 | -11 dB |
| 0 1110 | 1 dB | 1 1011 | -12 dB |

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|------|------|-----|------|------|------|------|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 95 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | SDAS | 3DEN | RSV | 3FL0 | 3DP3 | 3DP2 | 3DP1 | 3DP0 |

IDX[6:0]: 101 1111b (5Fh): Register 95

SDAS: Source Select for Sound Effect (Tone Control, 3-D Sound, Notch Filter, Mono Mix)

Default value: 0

The PCM3793/94 includes sound effect circuits (tone control, 3-D sound, notch filter, mono mix) which can be used to filter either the digital input to the DAC or the digital output from the ADC. This bit selects the signal source of the sound effect circuit.

| | |
|----------|-----------------------------|
| SDAS = 0 | DAC digital input (default) |
| SDAS = 1 | ADC digital output |

3DEN: 3-D Sound Effect Enable

Default value: 0

This bit is used for enabling the 3-D sound effect filter. This filter has two independently controlled parameters.

| | |
|----------|-------------------|
| 3DEN = 0 | Disable (default) |
| 3DEN = 1 | Enable |

3FL0: Filter Selection for 3-D Sound

Default value: 0

This bit is used for selecting from two kinds of filter type, narrow and wide. These filters have a different 3-D effect performance.

| | |
|----------|------------------|
| 3FL0 = 0 | Narrow (default) |
| 3FL0 = 1 | Wide |

3DP[3:0]: Efficiency for 3-D Sound Effects

Default value: 0000

These bits are used for adjusting the 3-D sound efficiency. Higher percentages have greater efficiency.

| 3DP[3:0] | 3D Sound Effect Efficiency |
|-----------------|-----------------------------------|
| 0 0 0 0 | 0% (default) |
| 0 0 0 1 | 10% |
| 0 0 1 0 | 20% |
| 0 0 1 1 | 30% |
| 0 1 0 0 | 40% |
| 0 1 0 1 | 50% |
| 0 1 1 0 | 60% |
| 0 1 1 1 | 70% |
| 1 0 0 0 | 80% |
| 1 0 0 1 | 90% |
| 1 0 1 0 | 100% |
| 1 0 1 1 | Reserved |
| : | : |
| 1 1 1 1 | Reserved |

| | | | | | | | | | | | | | | | | |
|-------------|-----|------|------|------|------|------|------|------|------|------|------|------|-----|-----|-----|------|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Register 96 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | NEN2 | NEN1 | NUP2 | NUP1 | RSV | RSV | RSV | MXEN |

IDX[6:0]: 110 0000b (60h): Register 96

NEN2: Second-Stage Notch Filter Enable

Default value: 0

PCM3793/94 has two notch filters with characteristics that can be set separately. This bit is used to enable the second stage.

| | |
|----------|-------------------|
| NEN2 = 0 | Disable (default) |
| NEN2 = 1 | Enable |

NEN1: First-Stage Notch Filter Enable

Default value: 0

PCM3793/94 has two notch filters with characteristics that can be set separately. This bit is used to enable the first stage.

| | |
|----------|-------------------|
| NEN1 = 0 | Disable (default) |
| NEN1 = 1 | Enable |

NUP2: Second-Stage Notch Filter Coefficients Update

Default value: 0

This bit is used to update the coefficients for 2nd stage notch filter. The coefficients written to registers 101, 102, 103, and 104 are updated when NUP2 = 1.

| | |
|----------|--|
| NUP2 = 0 | No Update (default) |
| NUP2 = 1 | Update (set to 0 automatically after set to 1) |

NUP1: First-Stage Notch Filter Coefficients Update

Default value: 0

This bit is used to update the coefficients for the second-stage notch filter. The coefficients written to registers 97, 98, 99, and 100 are updated when NUP1 = 1.

| | |
|----------|--|
| NUP1 = 0 | No Update (default) |
| NUP1 = 1 | Update (set to 0 automatically after set to 1) |

MXEN: Digital Monaural Mixing

Default value: 0

This bit is used to enable or disable monaural mixing in the section that combines L-ch data and R-ch data.

| | |
|----------|------------------|
| MXEN = 0 | Stereo (default) |
| MXEN = 1 | Monaural Mixing |

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--------------|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| Register 97 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | F107 | F106 | F105 | F104 | F103 | F102 | F101 | F100 |
| Register 98 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | F115 | F114 | F113 | F112 | F111 | F110 | F109 | F108 |
| Register 99 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | F207 | F206 | F205 | F204 | F203 | F202 | F201 | F200 |
| Register 100 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | F215 | F214 | F213 | F212 | F211 | F210 | F209 | F208 |

IDX[6:0]: 110 0001b (61h): Register 97

IDX[6:0]: 110 0010b (62h): Register 98

IDX[6:0]: 110 0011b (63h): Register 99

IDX[6:0]: 110 0100b (64h): Register 100

F[107:100]: Lower 8 Bits of Coefficient a_1 for First-Stage Notch Filter

F[115:108]: Upper 8 Bits of Coefficient a_1 for First-Stage Notch Filter

F[207:200]: Lower 8 Bits of Coefficient a_2 for First-Stage Notch Filter

F[215:208]: Upper 8 Bits of Coefficient a_2 for First-Stage Notch Filter

Default value: 0000 0000

These bits are used to change the characteristics of the first-stage notch filter. See [Figure 38](#) for details.

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--------------|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| Register 101 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | S107 | S106 | S105 | S104 | S103 | S102 | S101 | S100 |
| Register 102 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | S115 | S114 | S113 | S112 | S111 | S110 | S109 | S108 |
| Register 103 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | S207 | S206 | S205 | S204 | S203 | S202 | S201 | S200 |
| Register 104 | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | S215 | S214 | S213 | S212 | S211 | S210 | S209 | S208 |

IDX[6:0]: 110 0101b (65h): Register 101

IDX[6:0]: 110 0110b (66h): Register 102

IDX[6:0]: 110 0111b (67h): Register 103

IDX[6:0]: 110 1000b (68h): Register 104

S[107:100]: Lower 8 bits of Coefficient a_1 for Second-Stage Notch Filter

S[115:108]: Upper 8 bits of Coefficient a_1 for Second-Stage Notch Filter

S[207:200]: Lower 8 bits of Coefficient a_2 for Second-Stage Notch Filter

S[215:208]: Upper 8 bits of Coefficient a_2 for Second-Stage Notch Filter

Default value: 00000000

These bits are used to change the characteristics of the second-stage notch filter. See [Figure 38](#) for details.

The PCM3793/94 provides two notch filters for the digital input to the DAC or the digital output from the ADC. The optional filter characteristics of each filter are programmable. The characteristics are given by calculating the coefficients for three parameters, sampling frequency, center frequency, and bandwidth, as shown in [Figure 38](#). All coefficients must be written as 2s-complement binary data into registers 97, 98, 99, 100, 101, 102, 103, and 104.

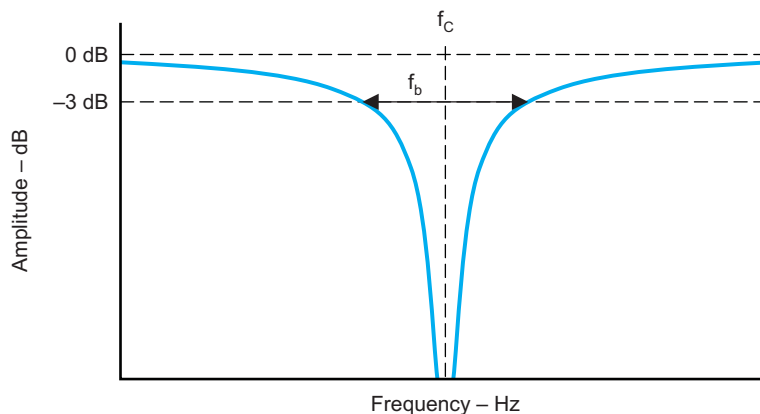
f_s : Sampling Frequency [Hz]

f_c : Center Frequency [Hz]

f_b : Band Width [Hz]

$$a_1 = -(1 + a_2) \cos\left(\frac{2\pi f_c}{f_s}\right) \quad (\text{Equation 1})$$

$$a_2 = \frac{1 - \tan\left(\frac{2\pi f_b / f_s}{2}\right)}{1 + \tan\left(\frac{2\pi f_b / f_s}{2}\right)} \quad (\text{Equation 2})$$



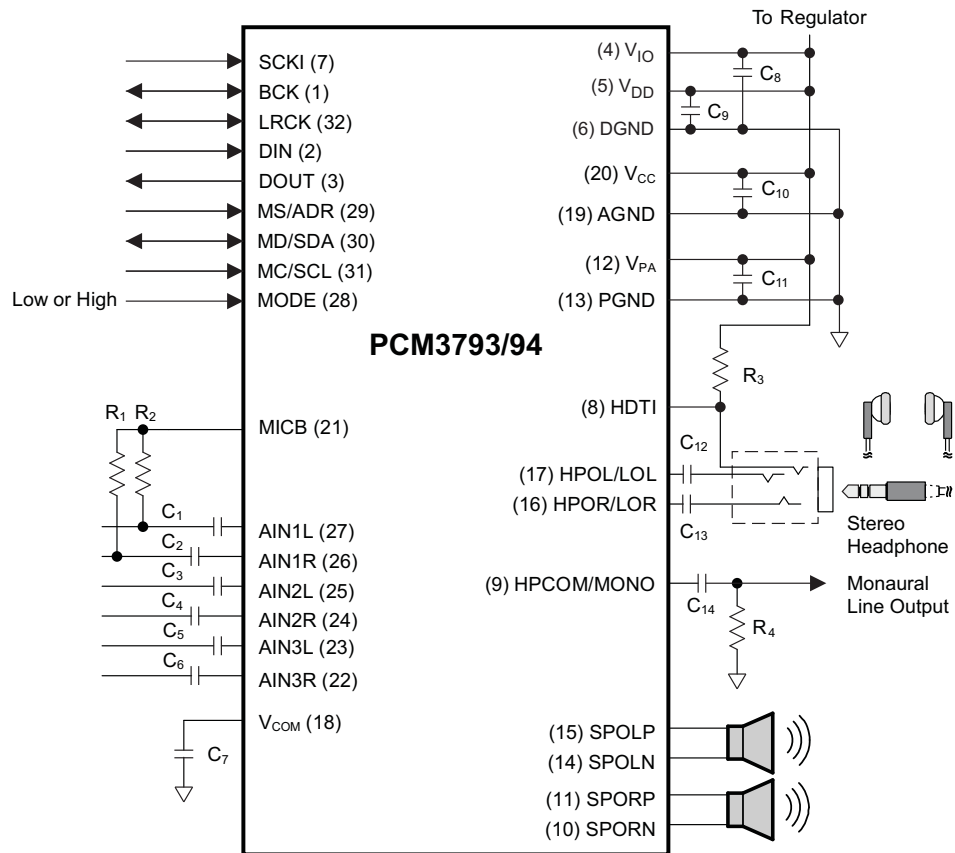
M0058-01

Figure 38. Parameter Settings for Notch Filter

The coefficients are calculated using Equation 1 and Equation 2 in [Figure 38](#). An example follows:

$f_s = 16 \text{ kHz}$, $f_c = 0.5 \text{ kHz}$, $f_b = 0.2 \text{ kHz}$
 $a_2 = 0.924390492 \rightarrow$ Decimal to Hex $\rightarrow 3B29h$
 $a_1 = -1.887413868 \rightarrow$ Decimal to Hex $\rightarrow 8735h$
 a_2 : F[215:208] = 3Bh, F[207:200] = 29h
 a_1 : F[115:108] = 87h, F[107:100] = 35h

CONNECTION DIAGRAM



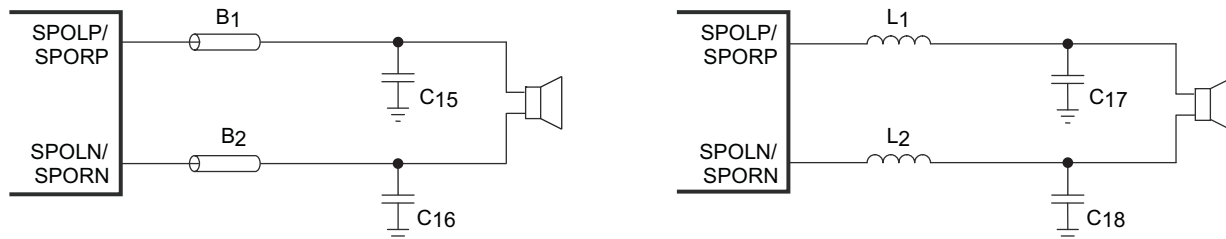
S0220-01

Figure 39. Connection Diagram

Table 14. Recommended External Parts

| | | | |
|----------------------------------|---------------------------|-----------------------------------|--------------|
| C ₁ –C ₆ | 1 μF | C ₁₂ , C ₁₃ | 10 μF–220 μF |
| C ₇ | 1 μF–10 μF ⁽¹⁾ | C ₁₄ | 1 μF–10 μF |
| C ₈ | 0.1 μF | R ₁ , R ₂ | 2.2 kΩ |
| C ₉ , C ₁₀ | 1 μF–4.7 μF | R ₃ | 33 kΩ |
| C ₁₁ | 4.7 μF–10 μF | R ₄ | 10 kΩ |

(1) 10 μF is recommended to reduce audible pop noise.

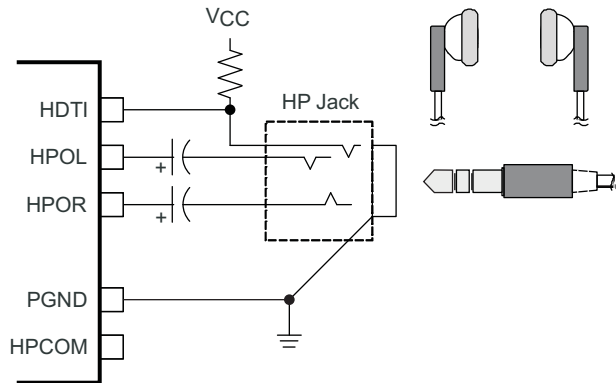


S0221-01

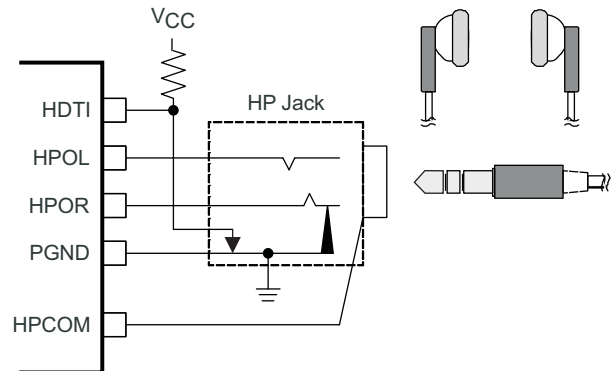
NOTE: C₁₅, C₁₆ = 1 nF C₁₇, C₁₈: 1 μF B₁, B₂: NEC/Tokin N2012ZPS121 L₁, L₂: 22 to 33 μH

Figure 40. Filter Consideration for Speaker Output

Conventional Mode

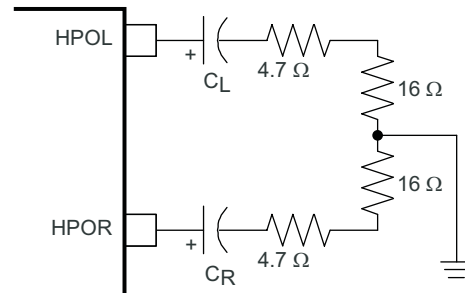
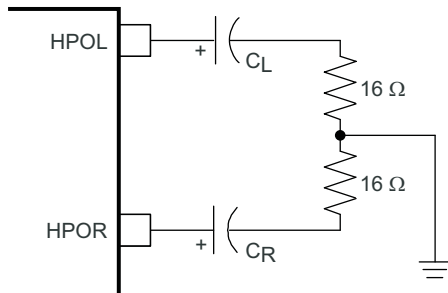


Capless Mode



S0222-01

Figure 41. Connection for Headphone Output and Insertion Detection



| $C_L, C_R - \mu F$ | $f_C - Hz$ |
|--------------------|------------|
| 10 | 995 |
| 47 | 212 |
| 100 | 100 |
| 220 | 45 |

| $C_L, C_R - \mu F$ | $f_C - Hz$ |
|--------------------|------------|
| 10 | 770 |
| 47 | 163 |
| 100 | 77 |
| 220 | 35 |

S0223-01

Figure 42. High-Pass Filter for Headphone Output

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| PCM3793RHBR | NRND | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | | 3793 | |
| PCM3793RHBT | NRND | VQFN | RHB | 32 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | | 3793 | |
| PCM3794RHBT | ACTIVE | VQFN | RHB | 32 | 250 | RoHS & Green | Call TI NIPDAU | Level-2-260C-1 YEAR | | 3794 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| PCM3793RHBR | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| PCM3793RHBT | VQFN | RHB | 32 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PCM3793RHBR | VQFN | RHB | 32 | 3000 | 356.0 | 356.0 | 35.0 |
| PCM3793RHBT | VQFN | RHB | 32 | 250 | 210.0 | 185.0 | 35.0 |

GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A



4223442/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

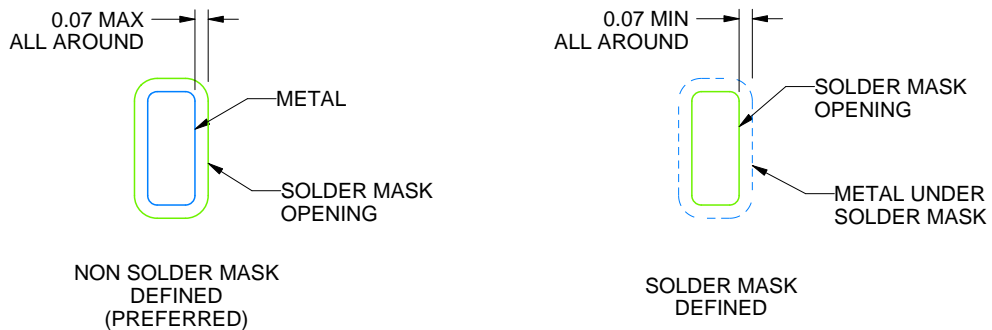
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

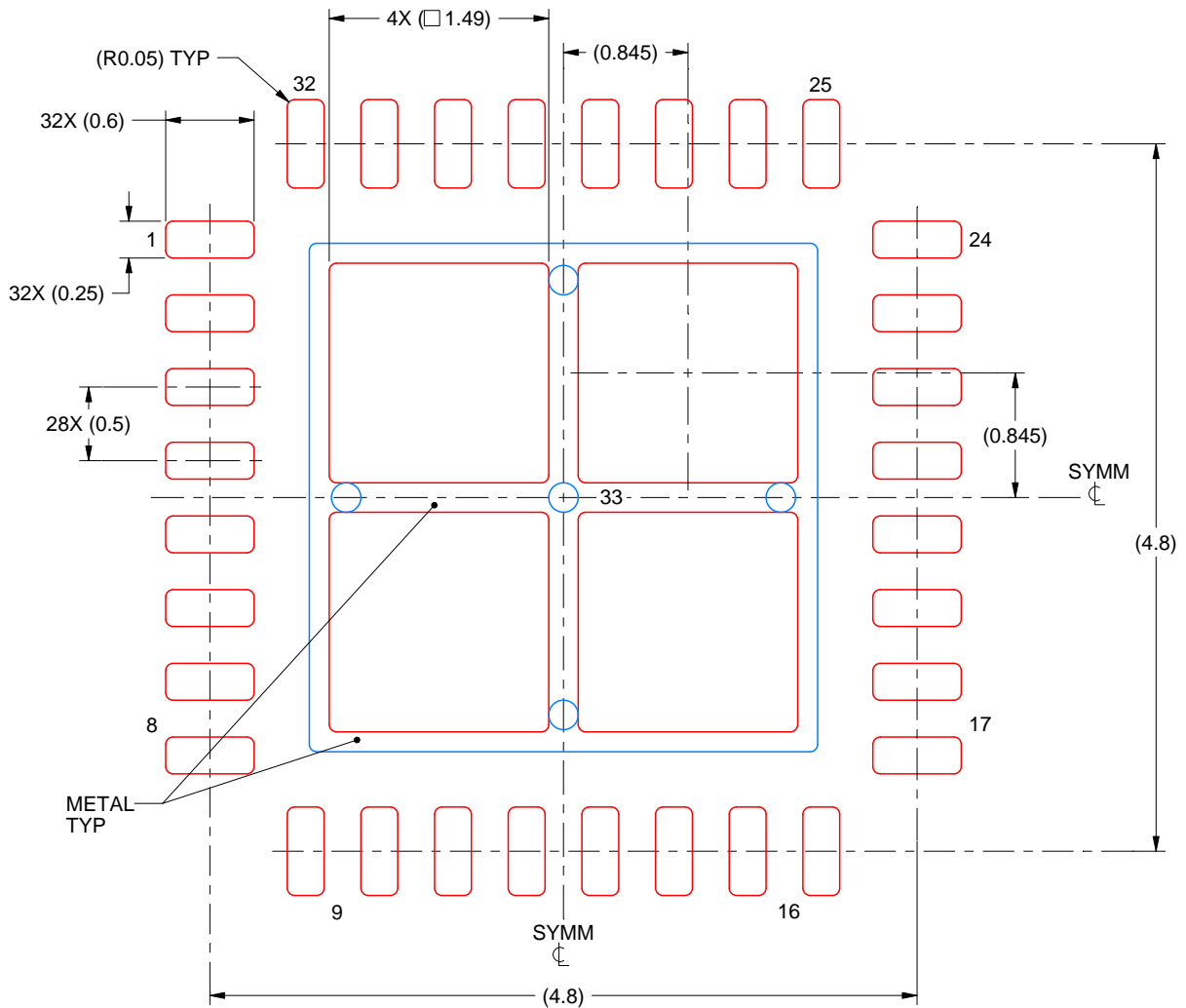
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated