PGA849 Low-Noise, Wide-Bandwidth, Precision Programmable Gain Instrumentation Amplifier

1 Features

- Differential to single-ended conversion
- Eight pin-programmable binary gains
  - G (V/V) = ⅛, ¼, ½, 1, 2, 4, 8, and 16
- Low gain error drift: ±2ppm/°C (maximum)
- Faster signal processing:
  - Wide bandwidth: 10MHz at all gains
  - High slew rate: 35V/µs at G ≥ ½ V/V
  - Settling time: 700ns to 0.01%, 950ns to 0.0015%
  - Input stage noise: 8.6nV/$\sqrt{\text{Hz}}$ at G = 16V/V
  - Filter option to achieve better SNR
- Input overvoltage protection to ±40V beyond supplies
- Input-stage supply range:
  - Single supply: 8V to 36V
  - Dual supply: ±4V to ±18V
- Independent output power-supply pins
- Output-stage supply range:
  - Single supply: 4.5V to 36V
  - Dual supply: ±2.25V to ±18V
- Specified temperature range: –40°C to +125°C
- Small package: 3mm × 3mm QFN

2 Applications

- Factory automation and control
- Analog input module
- Data acquisition (DAQ)
- Test and measurement
- Parametric measurement unit (PMU)

3 Description

The PGA849 is a wide-bandwidth, low-noise programmable gain instrumentation amplifier for differential-to-single-ended conversion. The PGA849 is equipped with eight binary gain settings, from an attenuating gain of 0.125V/V to a maximum of 16V/V, using three digital gain selection pins.

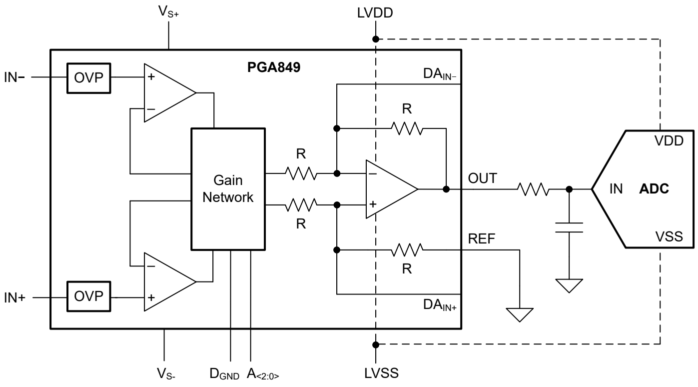
The PGA849 architecture is optimized to drive inputs of high-resolution, precision analog-to-digital converters (ADCs) with sampling rates up to 1MSPS without the need for an additional ADC driver. The output-stage power supplies are decoupled from the input stage to protect the ADC or downstream devices against overdrive damage.

The super-beta input transistors offer an impressively low input bias current, which in turn provides a very low input current noise density of 0.3pA/$\sqrt{\text{Hz}}$, making the PGA849 a versatile choice for virtually any sensor type. The low-noise current-feedback front-end architecture offers exceptional gain flatness even at high frequencies, making the PGA849 an excellent high-impedance sensor readout device. Integrated protection circuitry on the input pins handles overvoltages of up to ±40V beyond the power-supply voltages.

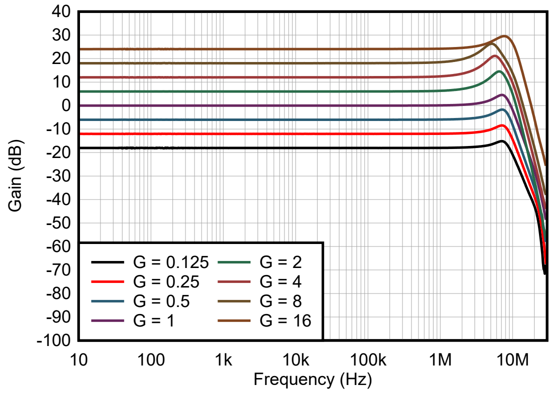
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
PGA849	RGT (VQFN, 16)	3mm × 3mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



PGA849 Simplified Application



Gain vs Frequency

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4 Device Comparison Table

DEVICE	OUTPUT TYPE	GAIN (V/V)	BANDWIDTH (MHz)	SLEW RATE (V/µS)	NOISE (nV/rtHz)
PGA849	Single-ended	⅛, ¼, ½, 1, 2, 4, 8, 16	10	35	8.6
INA849	Single-ended	G = 1 + 6kΩ / RG	28	35	1
PGA855	Differential	⅛, ¼, ½, 1, 2, 4, 8, 16	10	35	7.8
INA851	Differential	G = 1 + 6kΩ / RG	22	37	3.2
INA821	Single-ended	G = 1 + 49.4kΩ / RG	4.7	2	7
INA819	Single-ended	G = 1 + 50kΩ / RG	2	0.9	8

5 Pin Configuration and Functions

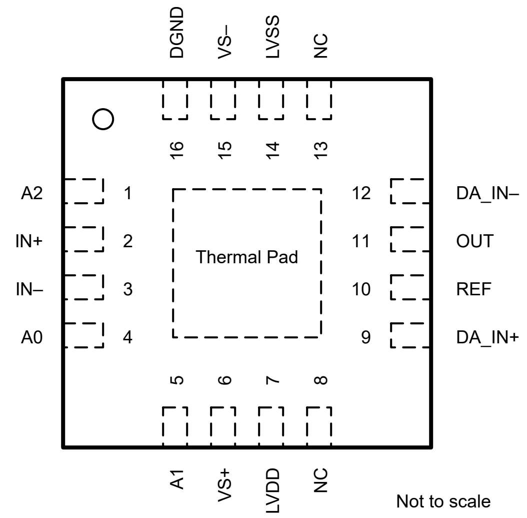


Figure 5-1. RGT Package, 16-Pin VQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	**NO.**		
A0	4	Input	Gain option pin 0
A1	5	Input	Gain option pin 1
A2	1	Input	Gain option pin 2
DA_IN+	9	Input	Connection to output difference amplifier summing node
DA_IN–	12	Input	Connection to output difference amplifier summing node
DGND	16	Power	Ground reference for digital-logic and gain-setting pins
IN–	3	Input	Negative (inverting) input
IN+	2	Input	Positive (noninverting) input
LVDD	7	Power	Output-driver positive supply
LVSS	14	Power	Output-driver negative supply
NC	8	—	Do not connect
NC	13	—	Do not connect
OUT	11	Output	Output
REF	10	Input	Reference input. This pin must be driven by a low-impedance source
VS+	6	Power	Input-stage positive supply
VS–	15	Power	Input-stage negative supply
Thermal Pad	Thermal pad	—	The thermal pad must be soldered to the printed-circuit board (PCB). Connect thermal pad to a plane or large copper pour that is either floating or electrically connected to VS–, even for applications that have low power dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage on V_{S+}, V_{S-} pins; $V_S = (V_{S+}) - (V_{S-})$	0	40	V
V_{SOUT}	Supply voltage on LVDD, LVSS pins; $V_{SOUT} = V_{LVDD} - V_{LVSS}$	0	40	V
	Voltage on power pins LVDD, LVSS	$(V_{S-}) - 0.5$	$(V_{S+}) + 0.5$	V
V_{IN}	Voltage on signal-input pins IN+, IN–	$(V_{S-}) - 40$	$(V_{S+}) + 40$	V
	DGND, DA_IN+, DA_IN– pin voltage	$(V_{S-}) - 0.5$	$(V_{S+}) + 0.5$	V
	Voltage on gain-select pins A2, A1, A0	$V_{DGND} - 0.5$	$(V_{S+}) + 0.5$	V
V_O	Signal output pin maximum voltage	$V_{LVSS} - 0.5$	$V_{LVDD} + 0.5$	V
V_{REF}	Reference input voltage	$V_{LVSS} - 0.5$	$V_{LVDD} + 0.5$	V
I_O	Signal-output pins current	–100	100	mA
I_{SC}	Output short-circuit current(2)	Continuous		
T_A	Operating temperature	–50	150	°C
T_J	Junction Temperature		175	°C
T_{stg}	Storage Temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Short-circuit to V_{SOUT} / 2.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_S	Input stage supply voltage	Single supply	8	36	V
		Dual supply	±4	±18	
V_{SOUT}	Output stage supply voltage	Single supply	4.5	36	V
		Dual supply	±2.25	±18	
T_A	Specified temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		PGA849	UNIT
		RGT (VQFN)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	22.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.8	°C/W

(1) For information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

at T_A = 25 °C, V_S = V_{SOUT} = ±15V, V_{ICM} = 0V, V_{REF} = 0V, R_L = 10kΩ connected to ground, and G = 1V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage (RTI)	G = 1 to 16			±50	±350	µV
		G < 1			±50/G	±350/G	
	Offset voltage drift (RTI)	G = 1 to 16, T_A = –40°C to +125°C			±0.2	±1.0	µV/°C
		G < 1, T_A = –40°C to +125°C			±0.2/G	±1.0/G	
PSRR	Power-supply rejection ratio	±4V ≤ V_S ≤ ±18V, RTI	G = 0.125	95	110		dB
			G = 0.25	98	114		dB
			G = 0.5	100	118		
			G = 1	120	134		
			G = 2	120	126		
			G = 4	120	132		
			G = 8	120	136		
			G = 16	120	140		
z_{id}	Differential input impedance				1 || 1		GΩ || pF
z_{ic}	Common-mode input impedance				1 || 7		GΩ || pF
V_{ICM}	Common-mode input voltage	V_S = ±4V to ±18V		$(V_{S–}) + 2.5$		$(V_{S+}) – 2$	V
		V_S = ±4V to ±18V, T_A = –40°C to +125°C		$(V_{S–}) + 3$		$(V_{S+}) – 2.5$	
CMRR	Common-mode rejection ratio	At DC to 60Hz, V_{ICM} = ±10V, T_A = –40°C to +125°C, RTI	G = 0.125	64	82		dB
			G = 0.25	70	88		
			G = 0.5	76	94		
			G = 1	82	100		
			G = 2	88	106		
			G = 4	94	112		
			G = 8	100	118		
			G = 16	106	124		
BIAS CURRENT							
I_B	Input bias current				±0.5	±1.8	nA
		T_A = –40°C to +125°C			±1		
	Input bias current drift	T_A = –40°C to +125°C				±10	pA/°C
I_{OS}	Input offset current				±0.5	±1	nA
		T_A = –40°C to +125°C			±1		
	Input offset current drift	T_A = –40°C to +125°C				±10	pA/°C

6.5 Electrical Characteristics (continued)

at T_A = 25 °C, V_S = V_{SOUT} = ±15V, V_{ICM} = 0V, V_{REF} = 0V, R_L = 10kΩ connected to ground, and G = 1V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE VOLTAGE							
e_{NI}	Voltage noise density (RTI)	f = 1kHz	G = 16		8.6		nV/√Hz
			G = 8		8.8		
			G = 4		9.6		
			G = 2		13.5		
			G = 1		23.8		
			G = 0.5		47.4		
			G = 0.25		94.9		
			G = 0.125		186.3		
E_{NI}	Voltage noise (RTI)	f_B = 0.1Hz to 10Hz	G = 16		0.28		μV_{PP}
			G = 8		0.29		
			G = 4		0.33		
			G = 2		0.49		
			G = 1		0.91		
			G = 0.5		1.82		
			G = 0.25		3.59		
			G = 0.125		7.28		
i_N	Input current noise density	f = 1kHz			0.3		pA/√Hz
I_N	Input current noise	f_B = 0.1Hz to 10Hz			13		pA_{PP}
GAIN							
	Gain range			0.125		16	V/V
GE	Gain error	G = 0.125			±0.010	±0.045	%
		G = 0.25			±0.005	±0.030	%
		G = 0.5			±0.005	±0.030	%
		G = 1			±0.005	±0.015	%
		G = 2			±0.010	±0.030	%
		G = 4			±0.015	±0.040	%
		G = 8			±0.015	±0.040	%
		G = 16			±0.030	±0.070	%
	Gain nonlinearity	G = 0.125 to 16, V_{OUT} > ±5V			2	5	ppm
	Gain drift	G = 0.125 to 16, T_A = –40°C to +125°C			±1	±2	ppm/°C
OUTPUT							
V_{OUT}	Output voltage	No load	V_{SOUT} = ±2.25V	V_{LVSS} + 0.1		V_{LVDD} – 0.1	V
		R_L = 10kΩ	V_{SOUT} = ±2.25V	V_{LVSS} + 0.2		V_{LVDD} – 0.2	
			V_{SOUT} = ±18V	V_{LVSS} + 0.4		V_{LVDD} – 0.4	
C_L	Load capacitance	Stable operation for capacitive load			100		pF
I_{SC}	Short-circuit current	Continuous to V_{SOUT} / 2			±45		mA
			T_A = –40°C to +125°C	±20		±60	
FREQUENCY RESPONSE							
BW	Bandwidth, –3dB	G = 0.125 to 16			10		MHz
SR	Slew rate	G ≥ 0.5, V_{OUT} = 10			35		V/μs
		G = 0.25, V_{OUT} = 5			23		V/μs
		G = 0.125, V_{OUT} = 2.5			10		V/μs
t_S	Settling time	G = 0.125 to 16 V_{INDIFF} = 10V step or V_{OUT} = 10V step	To 0.01%		0.7		μs
			To 0.0015%		0.95		
	Gain switching time				2		μs

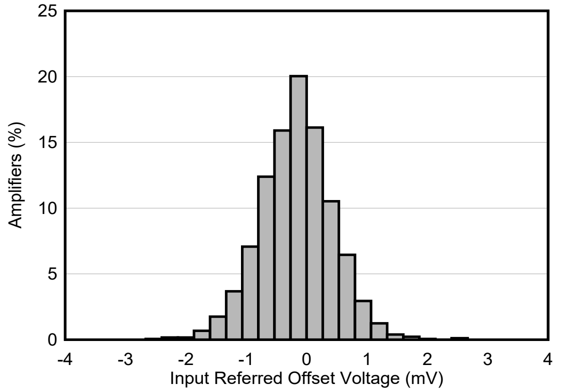
6.5 Electrical Characteristics (continued)

at T_A = 25 °C, $V_S = V_{SOUT}$ = ±15V, V_{ICM} = 0V, V_{REF} = 0V, R_L = 10kΩ connected to ground, and G = 1V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD+N	Total harmonic distortion and Noise	Differential input, f = 10kHz, V_{OUT} = 10V_{PP}		–110		dB
		Single-ended input, f = 10kHz, V_{OUT} = 10V_{PP}		–105		
HD2	Second-order harmonic distortion	Differential input, f = 10kHz, V_{OUT} = 10V_{PP}		–120		
		Single-ended input, f = 10kHz, V_{OUT} = 10V_{PP}		–110		
HD3	Third-order harmonic distortion	Differential input, f = 10kHz, V_{OUT} = 10V_{PP}		–120		
		Single-ended input, f = 10kHz, V_{OUT} = 10V_{PP}		–110		
REFERENCE INPUT						
R_{IN}	Reference input impedance			10		kΩ
	Reference input current	V_{IN} = 0V		140		µA
	Reference input voltage		V_{LVSS}		V_{LVDD}	V
	Reference gain to output			1		V/V
	Reference gain error	V_{OUT} = ±10V, inside the voltage swing range		0.01	0.05	%
INPUT STAGE POWER SUPPLY						
I_{Q_input}	Input stage quiescent current V_{S+}, $V_{S–}$	V_{IN} = 0V		3	3.7	mA
		T_A = –40°C to +125°C			4.6	
OUTPUT STAGE POWER SUPPLY						
I_{Q_output}	Output stage quiescent current LVDD, LVSS	V_{IN} = 0V, V_{REF} = 0V		2.3	2.8	mA
		T_A = –40°C to 125°C			3.5	
DIGITAL LOGIC						
V_{IL}	Digital input logic low	A0, A1, A2 pins, referred to DGND	V_{DGND}		V_{DGND} + 0.8	V
V_{IH}	Digital input logic high	A0, A1, A2 pins, referred to DGND	V_{DGND} + 1.8		V_{S+}	V
	Digital input pin current	A0, A1, A2 pins		1.5	3	µA
V_{DGND}	DGND voltage		$V_{S–}$		(V_{S+}) – 4	V
	DGND reference current			4	10	µA

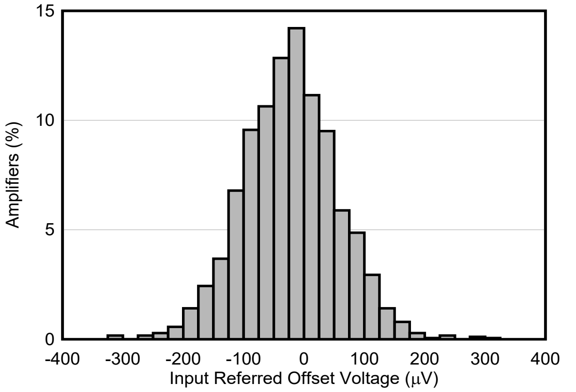
6.6 Typical Characteristics

at T_A = 25°C, $V_S = V_{SOUT}$ = ±15V, $V_{ICM} = V_{REF}$ = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



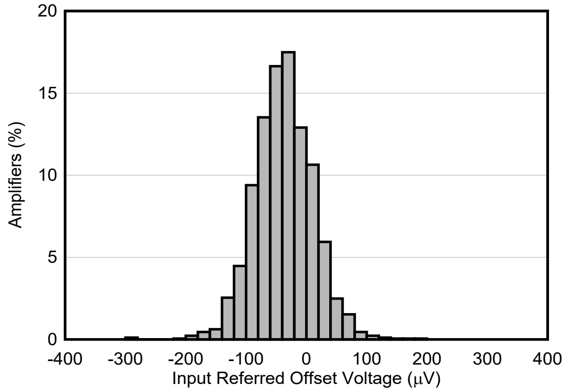
N = 1767 Mean = –165.34µV Std. dev. = 600.90µV
G = 0.125V/V

Figure 6-1. Distribution of Offset Voltage (RTI)



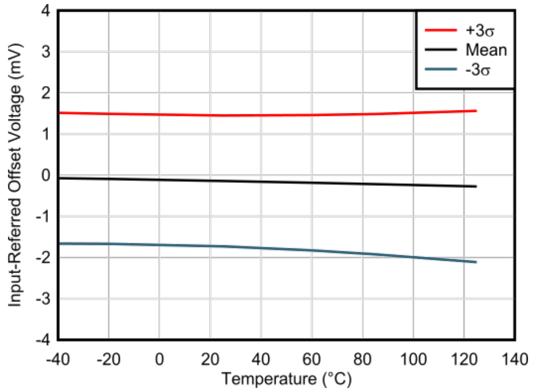
N = 1767 Mean = –22.56µV Std. dev. = 78.45µV
G = 1V/V

Figure 6-2. Distribution of Offset Voltage (RTI)



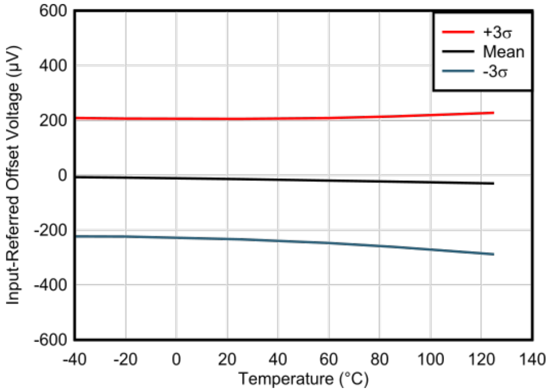
N = 1767 Mean = –37.55µV Std. dev. = 48.69µV
G = 16V/V

Figure 6-3. Distribution of Offset Voltage (RTI)



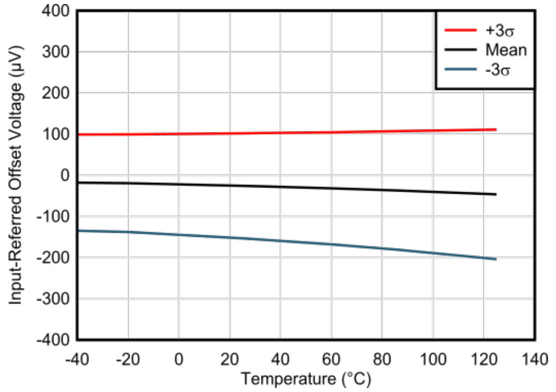
N = 58 1 wafer lot
G = 0.125V/V

Figure 6-4. Offset Voltage (RTI) vs Temperature



N = 58 1 wafer lot
G = 1V/V

Figure 6-5. Offset Voltage (RTI) vs Temperature

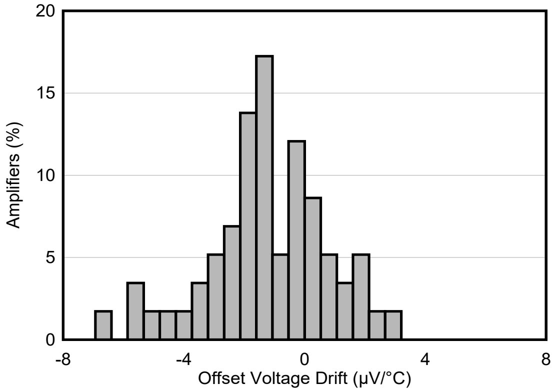


N = 58 1 wafer lot
G = 16V/V

Figure 6-6. Offset Voltage (RTI) vs Temperature

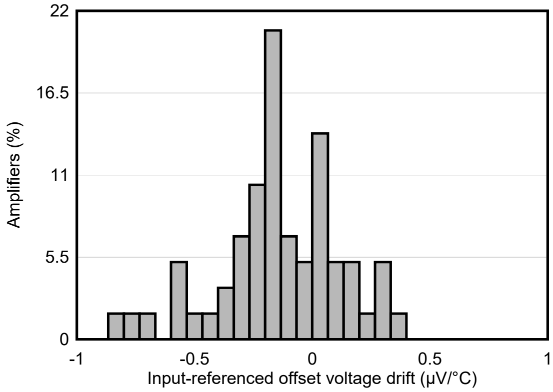
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



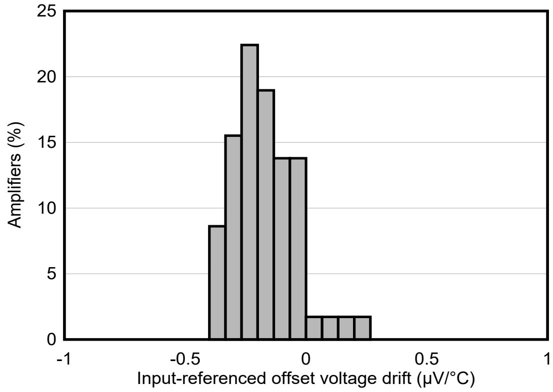
N = 58 Mean = –1.23µV/°C Std. dev. = 2µV/°C
G = 0.125V/V

Figure 6-7. Distribution of Offset Voltage Drift (RTI)



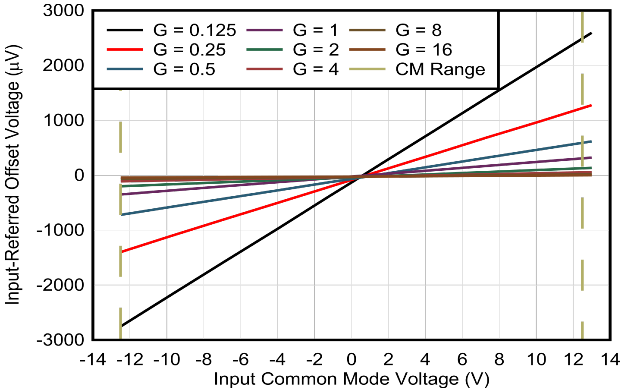
N = 58 Mean = –0.14µV/°C Std. dev. = 0.26µV/°C
G = 1V/V

Figure 6-8. Distribution of Offset Voltage Drift (RTI)



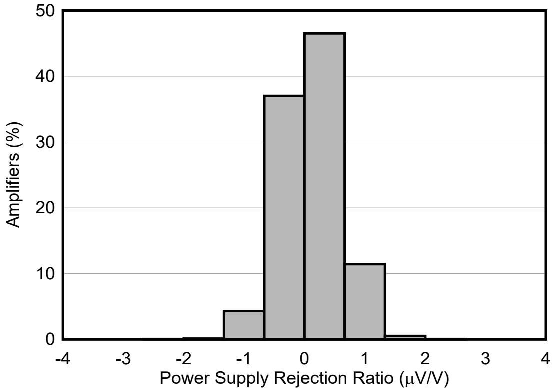
N = 58 Mean = –0.17µV/°C Std. dev. = 0.13µV/°C
G = 16V/V

Figure 6-9. Distribution of Offset Voltage Drift (RTI)



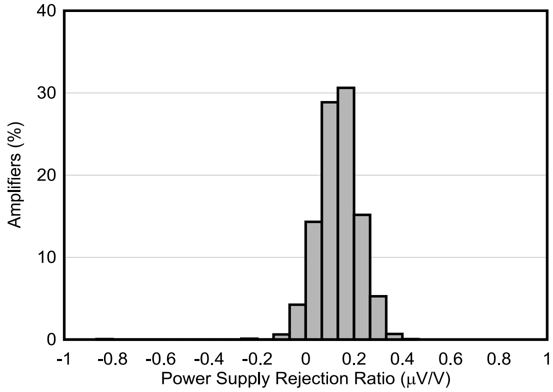
Typical unit shown

Figure 6-10. Offset Voltage (RTI) vs V_{ICM}



N = 1767 Mean = 0.11µV/V Std. dev. = 0.47µV/V
G = 0.125V/V

Figure 6-11. PSRR Distribution

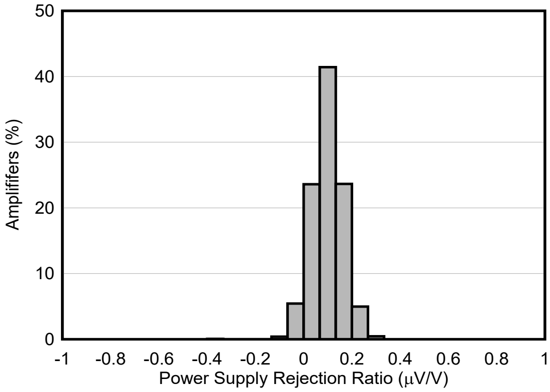


N = 1767 Mean = 0.14µV/V Std. dev. = 0.09µV/V
G = 1V/V

Figure 6-12. PSRR Distribution

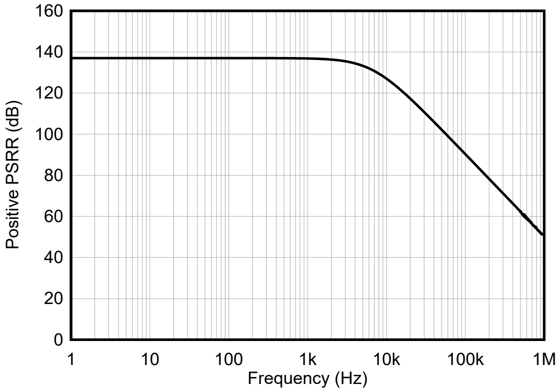
6.6 Typical Characteristics (continued)

at T_A = 25°C, $V_S = V_{SOUT}$ = ±15V, $V_{ICM} = V_{REF}$ = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



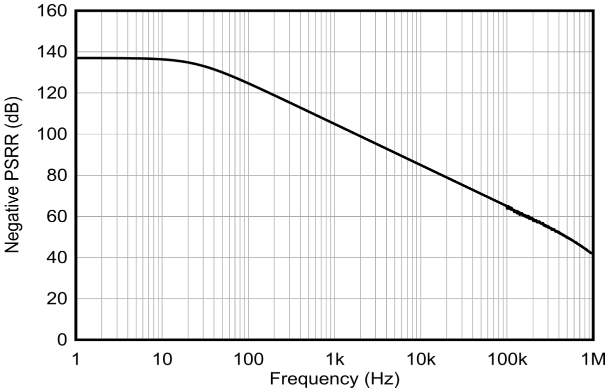
N = 1767 Mean = 0.10µV/V Std. dev. = 0.06µV/V
G = 16V/V

Figure 6-13. PSRR Distribution



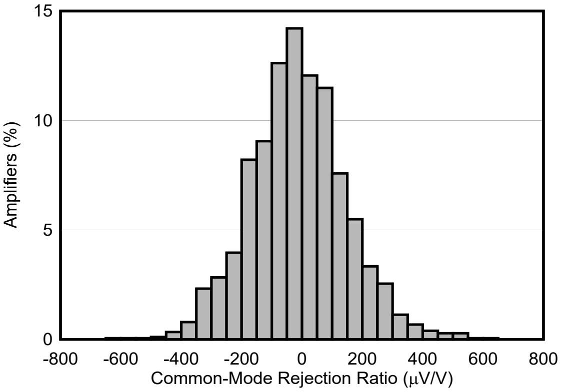
Typical unit shown
G = 1V/V

Figure 6-14. Positive PSRR vs Frequency



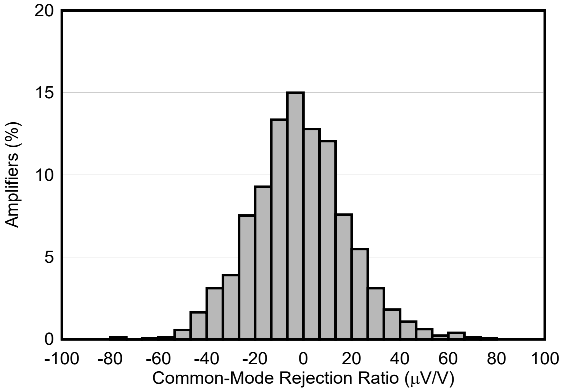
Typical unit shown
G = 1V/V

Figure 6-15. Negative PSRR vs Frequency



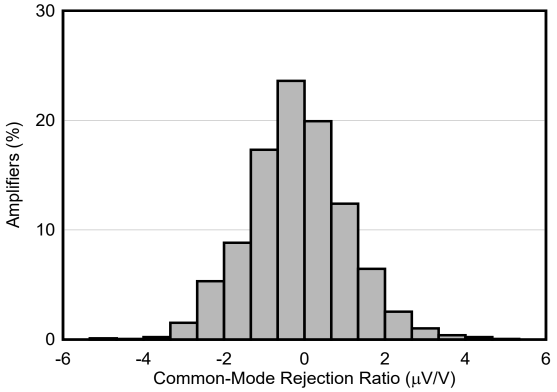
N = 1767 Mean = –12.21µV/V Std. dev. = 159.35µV/V
G = 0.125V/V

Figure 6-16. CMRR Distribution



N = 1767 Mean = –1.55µV/V Std. dev = 19.92µV/V
G = 1V/V

Figure 6-17. CMRR Distribution

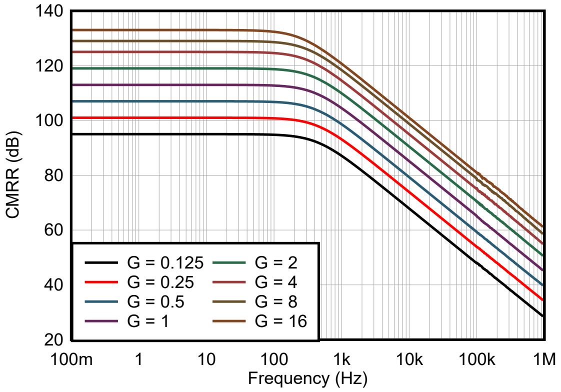


N = 1767 Mean = –0.17µV/V Std. dev = 1.25µV/V
G = 16V/V

Figure 6-18. CMRR Distribution

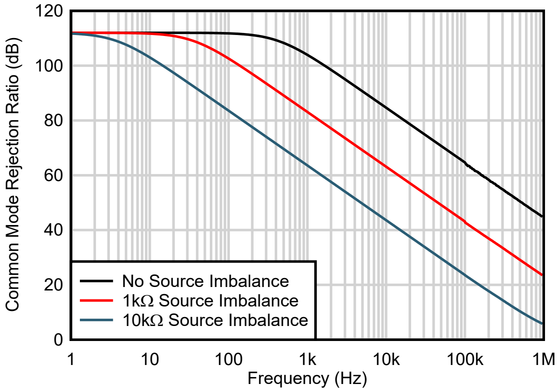
6.6 Typical Characteristics (continued)

at T_A = 25°C, $V_S = V_{SOUT}$ = ±15V, $V_{ICM} = V_{REF}$ = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



Typical unit shown

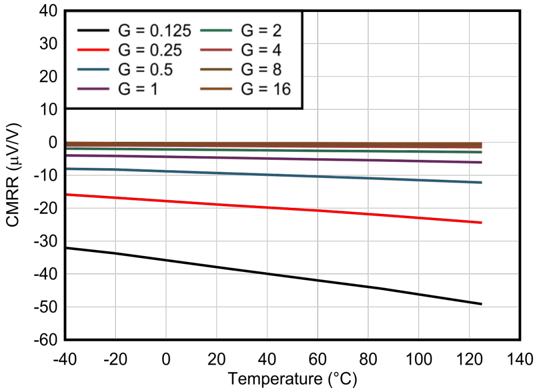
Figure 6-19. CMRR vs Frequency (RTI)



Typical unit shown

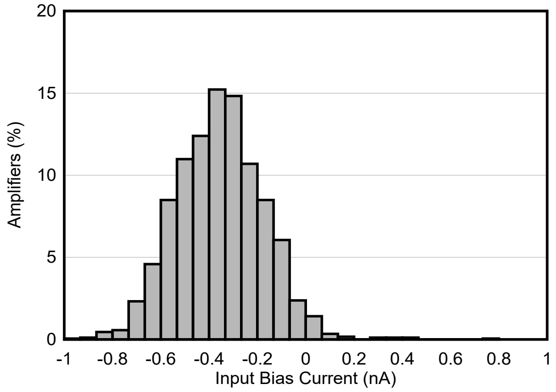
G = 1V/V

Figure 6-20. CMRR vs Frequency (Unbalanced)



Typical unit shown

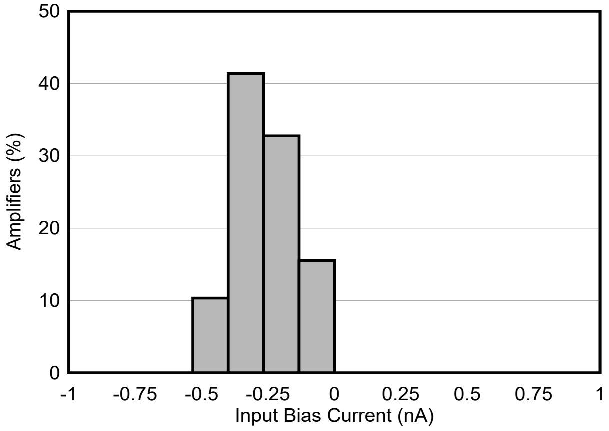
Figure 6-21. CMRR vs Temperature



N = 1767 Mean = –0.35nA Std. dev. = 0.181nA

G = 1V/V

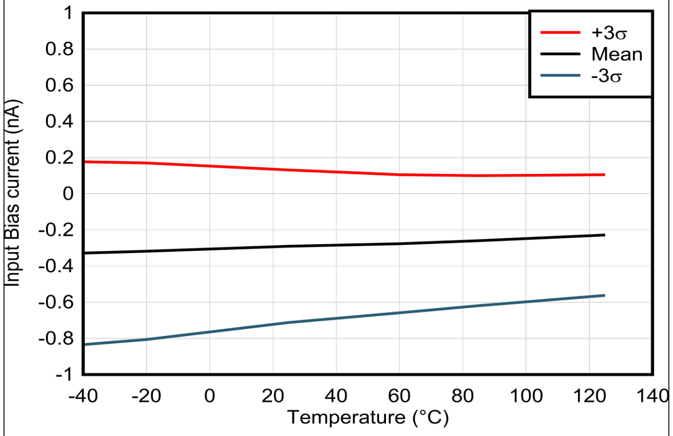
Figure 6-22. Distribution of Input Bias Current



N = 58 Mean = –0.265nA Std. dev. = 0.11nA

T_A = 85°C G = 1V/V

Figure 6-23. Distribution of Input Bias Current



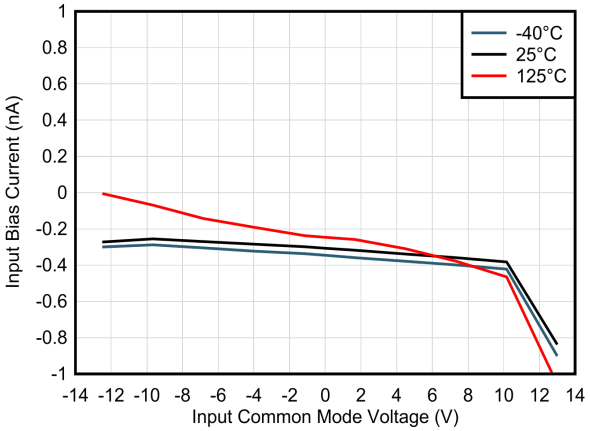
N = 58 1 wafer lot

G = 1V/V

Figure 6-24. Input Bias Current vs Temperature

6.6 Typical Characteristics (continued)

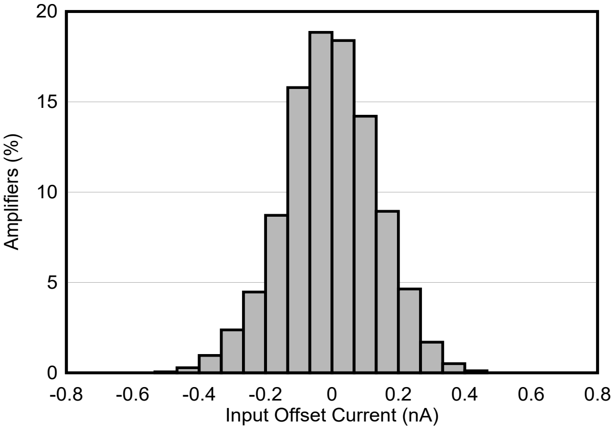
at T_A = 25°C, $V_S = V_{SOUT}$ = ±15V, $V_{ICM} = V_{REF}$ = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



Typical unit shown

G = 1V/V

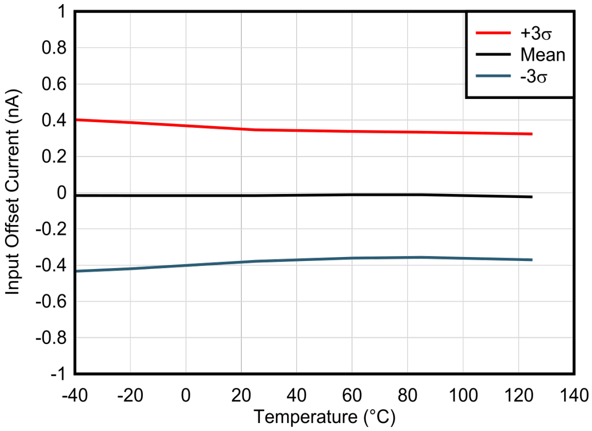
Figure 6-25. Input Bias Current vs V_{ICM}



N = 1767 Mean = –0.006nA Std. dev = 0.139nA

G = 1V/V

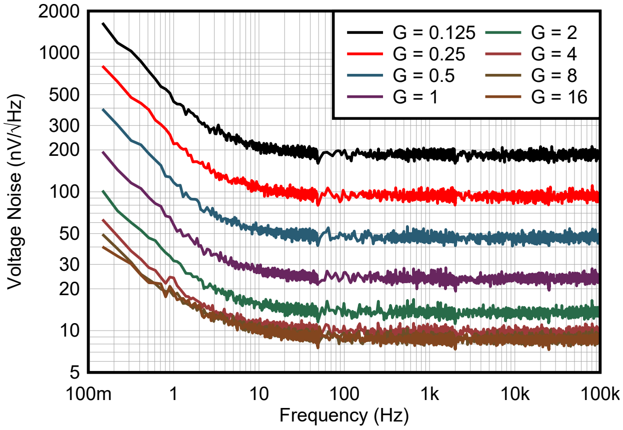
Figure 6-26. Distribution of Input Offset Current



N = 58 1 wafer lot

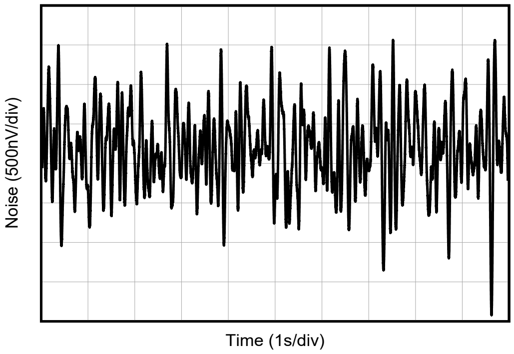
G = 1V/V

Figure 6-27. Input Offset Current vs Temperature



Typical unit shown

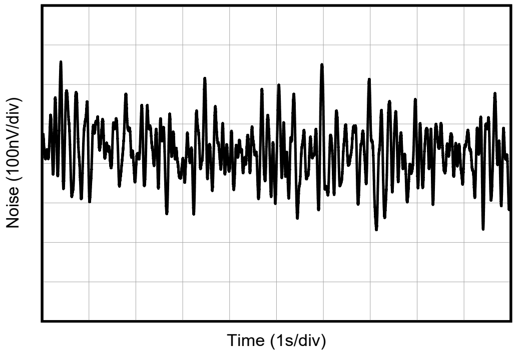
Figure 6-28. Voltage Noise Spectral Density (RTI) vs Frequency



Typical unit shown

G = 0.125V/V

Figure 6-29. 0.1Hz to 10Hz Voltage Noise (RTI)



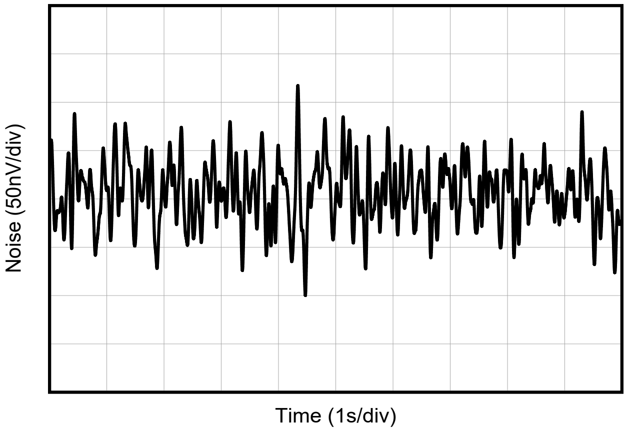
Typical unit shown

G = 1V/V

Figure 6-30. 0.1Hz to 10Hz Voltage Noise (RTI)

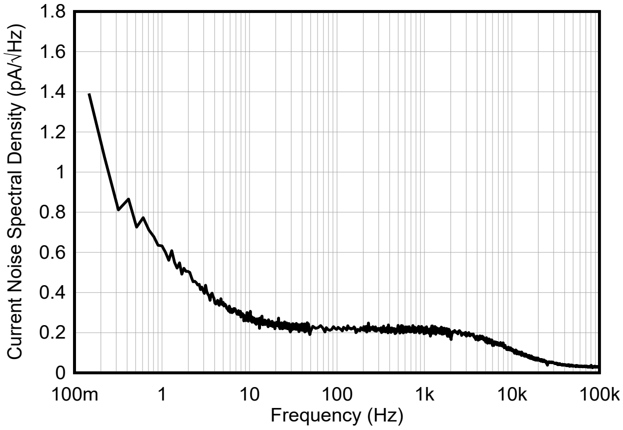
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



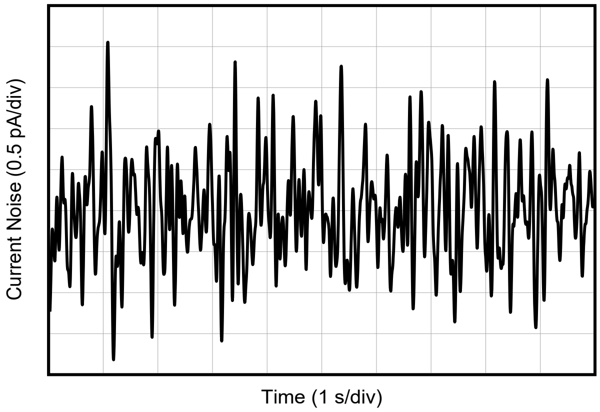
Typical unit shown
G = 16V/V

Figure 6-31. 0.1Hz to 10Hz Voltage Noise (RTI)



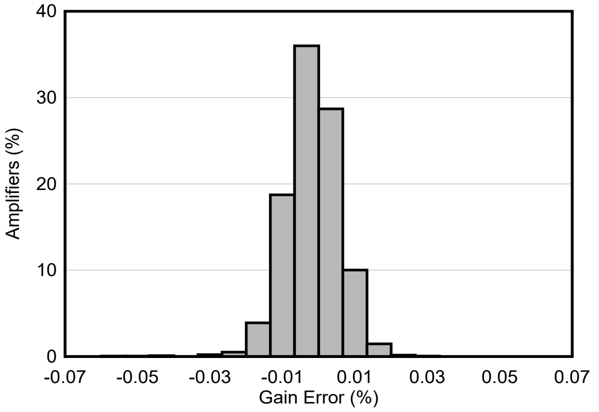
G = 1V/V

Figure 6-32. Current Noise Spectral Density vs Frequency



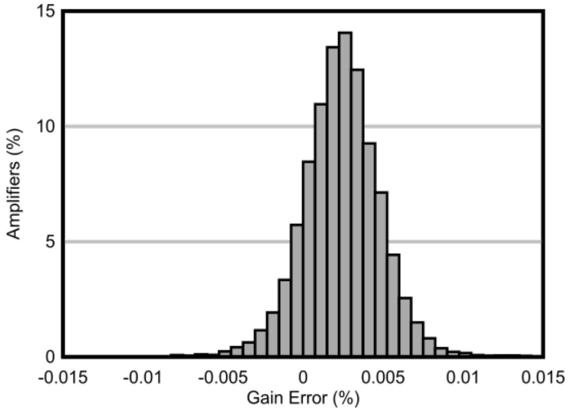
Typical unit shown
G = 1V/V

Figure 6-33. 0.1Hz to 10Hz Current Noise



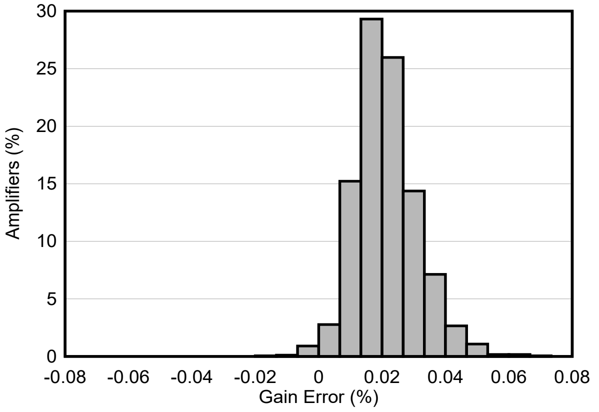
N = 1767 Mean = –0.0017% Std. dev. = 0.0074%
G = 0.125V/V

Figure 6-34. Distribution of Gain Error



N = 10032 Mean = –0.0016% Std. dev. = 0.0025%
G = 1V/V

Figure 6-35. Distribution of Gain Error

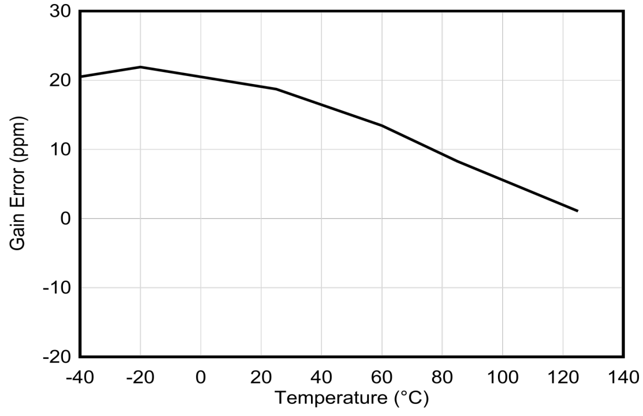


N = 1767 Mean = 0.0124% Std. dev. = 0.0098%
G = 16V/V

Figure 6-36. Distribution of Gain Error

6.6 Typical Characteristics (continued)

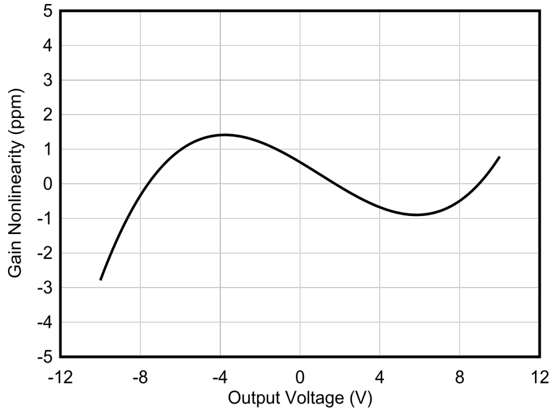
at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



Typical unit shown

G = 1V/V

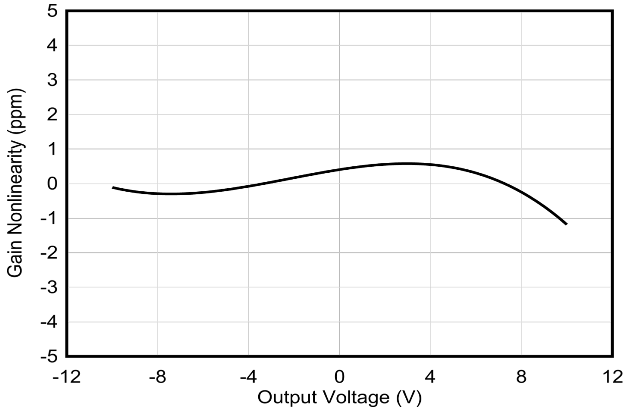
Figure 6-37. Gain Error vs Temperature



V_{OUT} = ±10V G = 1V/V

Typical unit shown

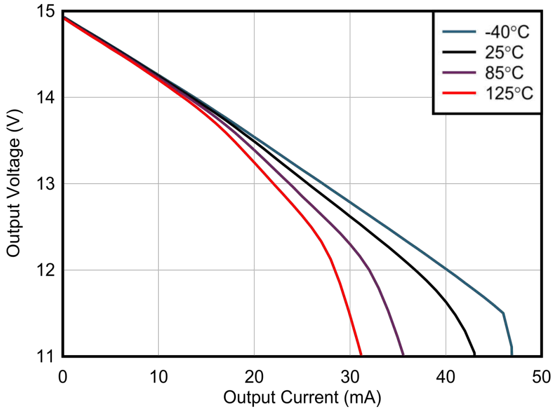
Figure 6-38. Gain Nonlinearity



V_{OUT} = ±10V G = 16V/V

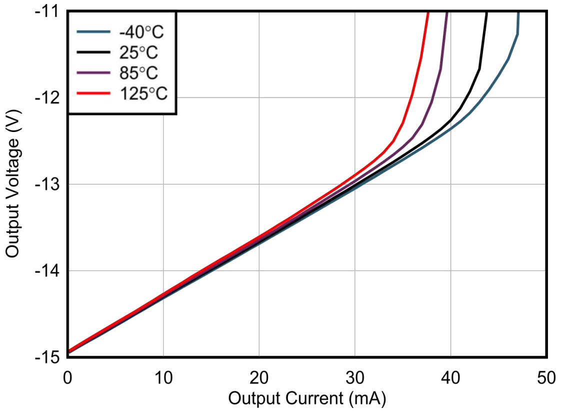
Typical unit shown

Figure 6-39. Gain Nonlinearity



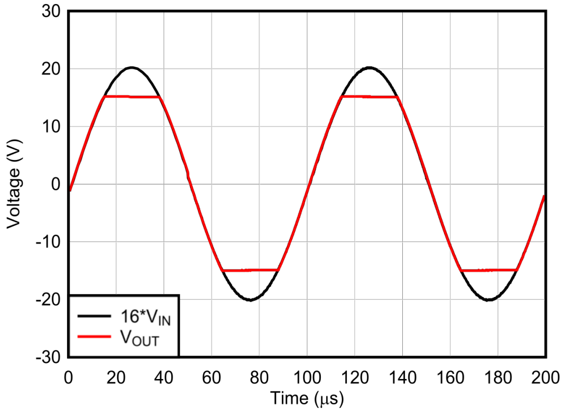
V_S = ±18V V_{OUT} = ±15V G = 16V/V

Figure 6-40. Positive Output Voltage vs Output Current



V_S = ±18V V_{OUT} = ±15V G = 16V/V

Figure 6-41. Negative Output Voltage vs Output Current

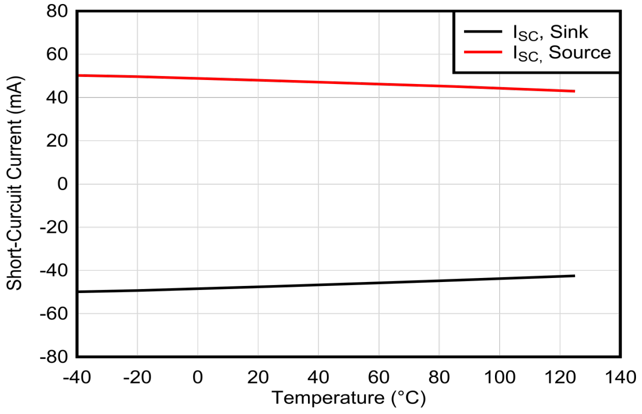


G = 16V/V

Figure 6-42. Overload Recovery

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



Short to V_{SOUT}/ 2

G = 1V/V

Figure 6-43. Output Short-Circuit Current vs Temperature

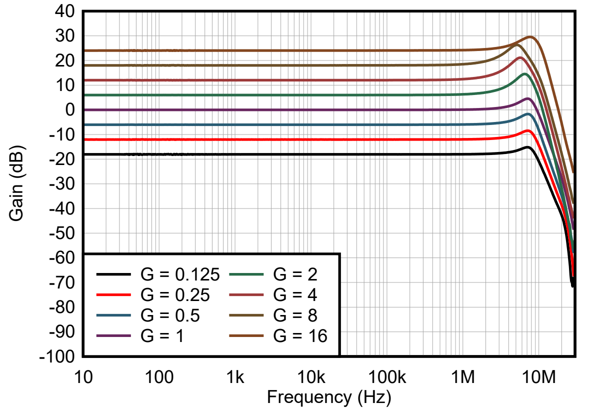
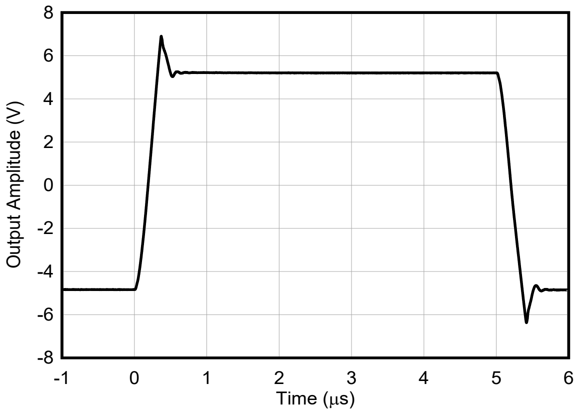
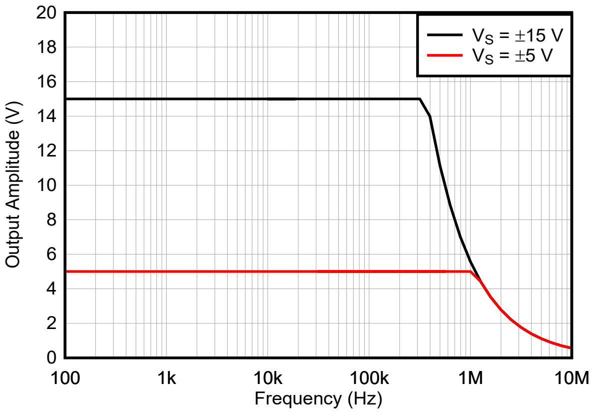


Figure 6-44. Gain vs Frequency



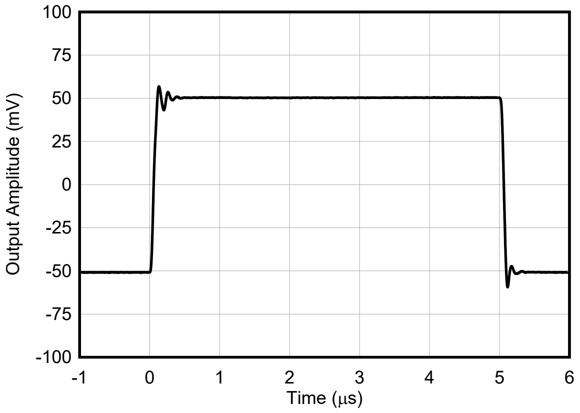
G = 1V/V

Figure 6-45. Large-Signal Step Response



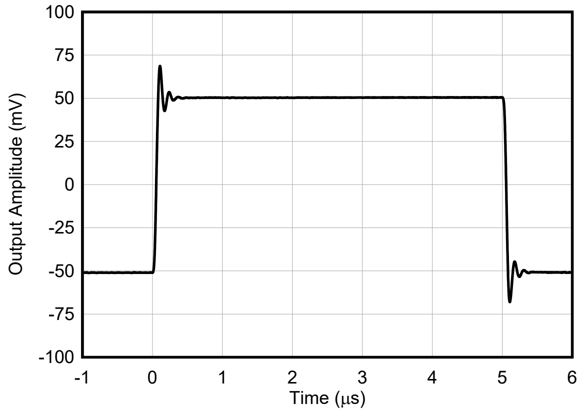
G = 1V/V

Figure 6-46. Large-Signal Step Response vs Frequency



G = 0.125V/V

Figure 6-47. Small-Signal Step Response



G = 0.25V/V

Figure 6-48. Small-Signal Step Response

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)

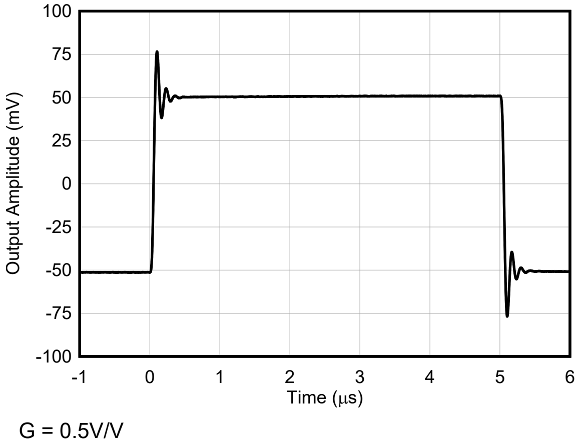


Figure 6-49. Small-Signal Step Response

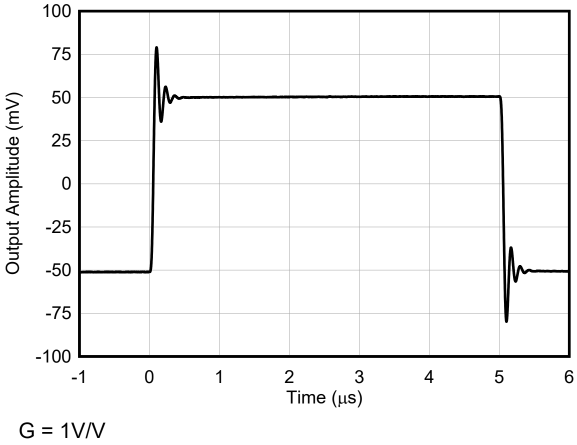


Figure 6-50. Small-Signal Step Response

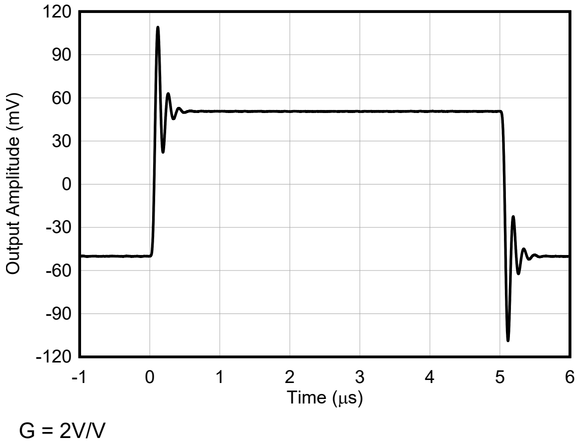


Figure 6-51. Small-Signal Step Response

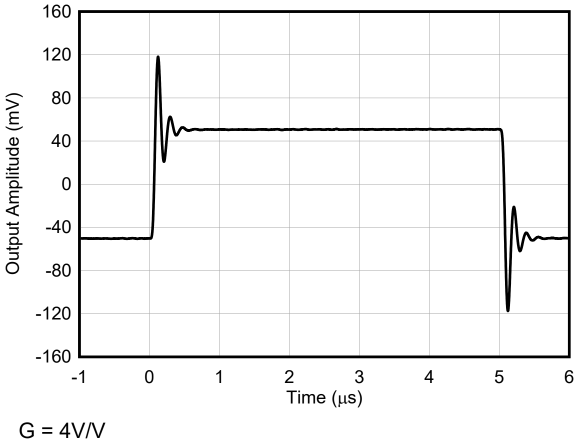


Figure 6-52. Small-Signal Step Response

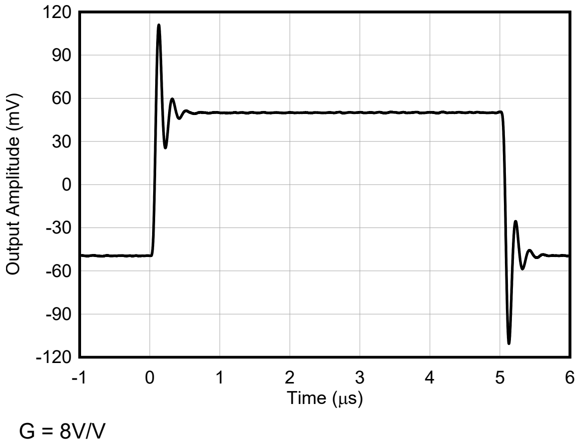


Figure 6-53. Small-Signal Step Response

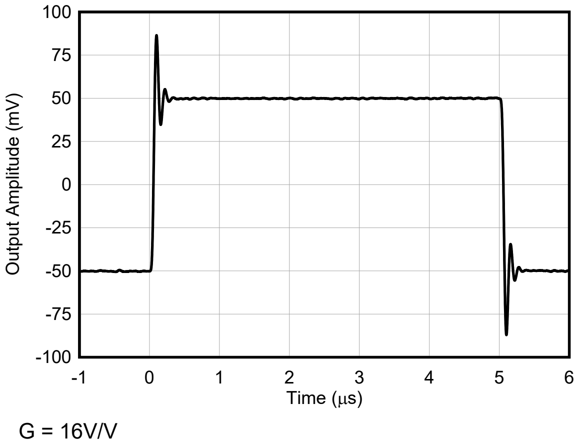
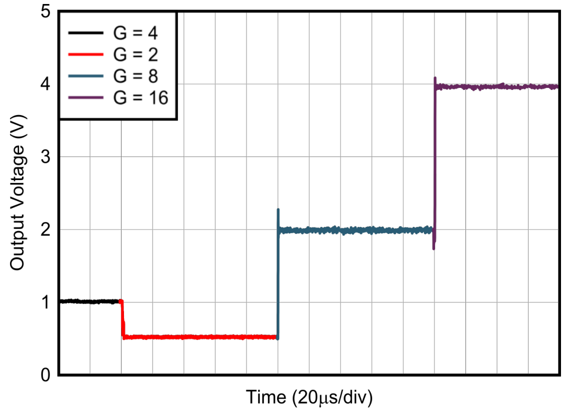


Figure 6-54. Small-Signal Step Response

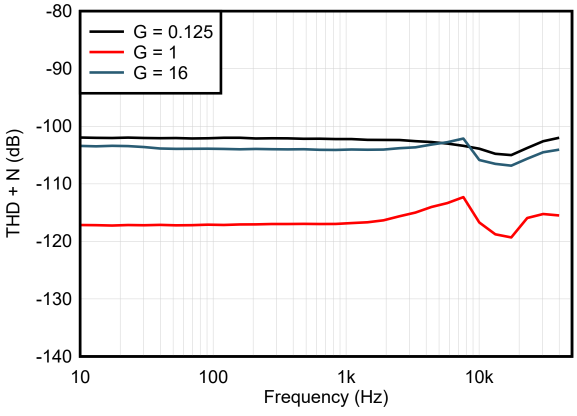
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



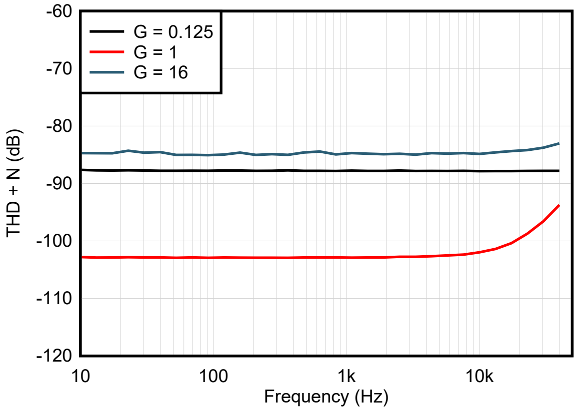
V_{IN} = 250mV_{PP}

Figure 6-55. Gain Switching Transient Response



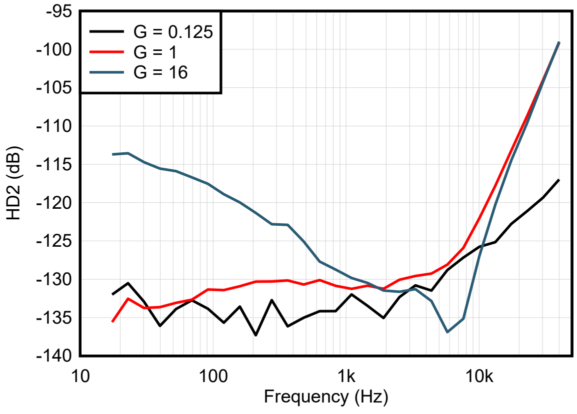
10Hz to 22kHz band-pass filter $V_{OUTDIFF}$ > 2.5V_{PP}

Figure 6-56. Total Harmonic Distortion + Noise vs Frequency



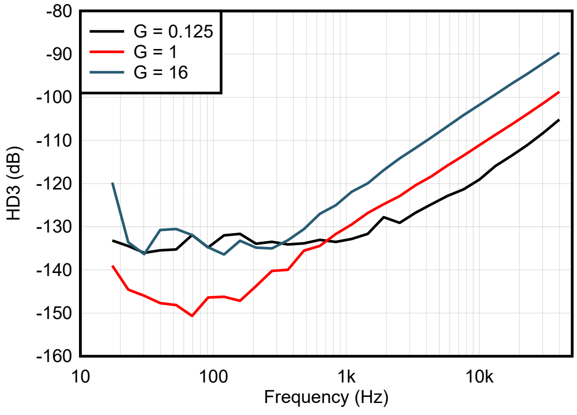
10Hz to 500kHz band-pass filter $V_{OUTDIFF}$ > 2.5V_{PP}

Figure 6-57. Total Harmonic Distortion + Noise vs Frequency



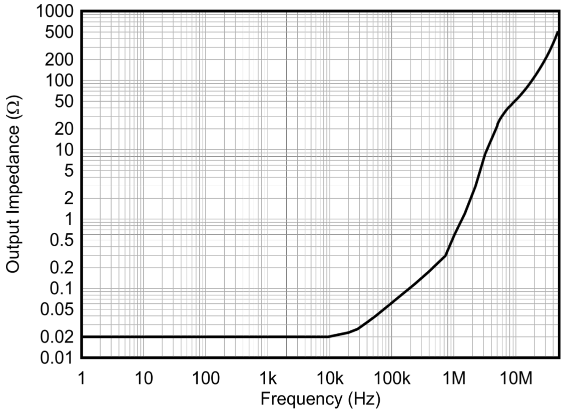
10Hz to 500kHz band-pass filter $V_{OUTDIFF}$ > 2.5V_{PP}

Figure 6-58. 2nd Harmonic Distortion vs Frequency



10Hz to 500kHz band-pass filter $V_{OUTDIFF}$ > 2.5V_{PP}

Figure 6-59. 3rd Harmonic Distortion vs Frequency

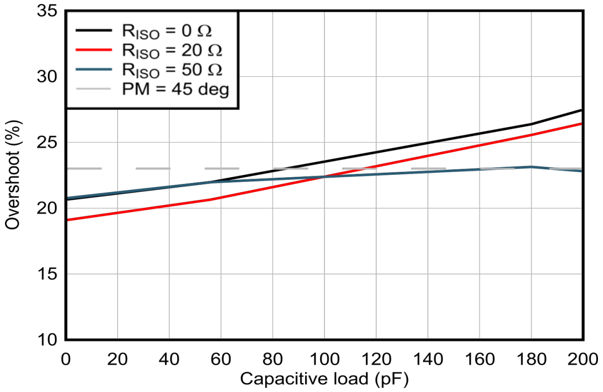


G = 1V/V

Figure 6-60. Closed-Loop Output Impedance vs Frequency

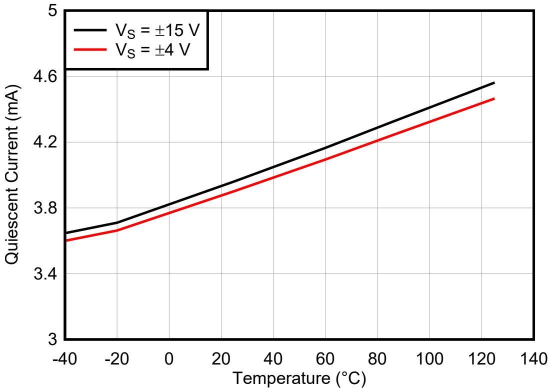
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = V_{SOUT} = ±15V, V_{ICM} = V_{REF} = 0V, R_L = 10kΩ connected to ground, and G =1V/V (unless otherwise noted)



G = 1V/V

Figure 6-61. Overshoot vs Capacitive Load



Input stage
G = 1V/V

Figure 6-62. Quiescent Current vs Temperature

7 Detailed Description

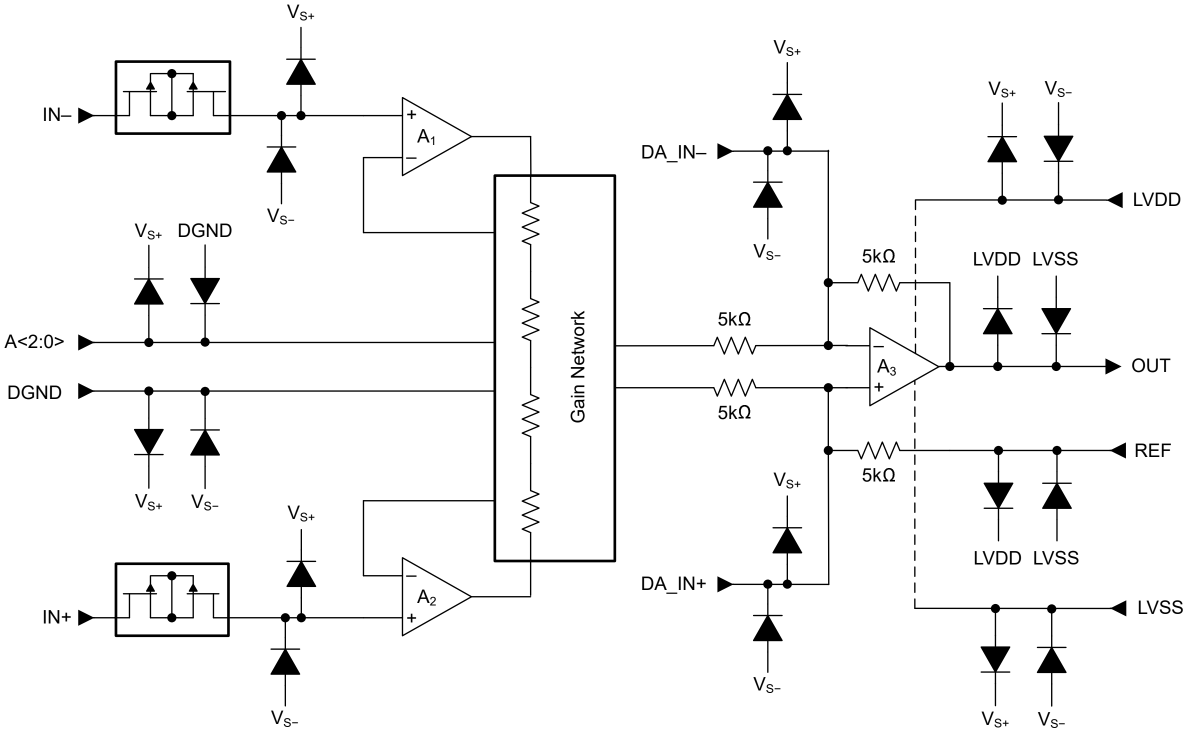
7.1 Overview

The PGA849 is a monolithic, high-voltage, precision programmable-gain instrumentation amplifier. The PGA849 combines a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, difference amplifier output stage. Eight pre-programmed binary gains are selectable using gain-select pins A0, A1, A2. Gains range from 0.125V/V to 16V/V, discussed in greater detail in Section 7.3.1.

A functional block diagram for the PGA849 is shown in the next section. The differential input voltage is fed into a pair of matched, high-impedance input, current-feedback amplifiers. An integrated precision-matched gain resistor network is used to amplify the differential input voltage. An output difference amplifier, A_3, rejects the input common-mode component and refers the output signal to the voltage level set by the REF pin.

The PGA849 output amplifier bandwidth is optimized to drive high-performance analog-to-digital converters (ADCs) with sampling rates up to 1MSPS, without the need for an additional ADC driver. The output amplifier uses a separate power supply that is independent of the input-stage power supply. When driving an ADC, use a low-impedance connection from LVDD and LVSS to the ADC power supplies. This configuration protects the ADC inputs from damage due to inadvertent overvoltage conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Gain Control

The PGA849 uses three pins to set the amplifier gain. These gain select pins are set with respect to DGND. This configuration simplifies the design when compared to programmable-gain amplifiers requiring a SPI or other digital interface options for gain changes. Figure 7-1 shows the gain-setting block diagram. Table 7-1 lists the gain options. Any gain select pin that is not driven by an external source is automatically biased at DGND using internal pulldown options.

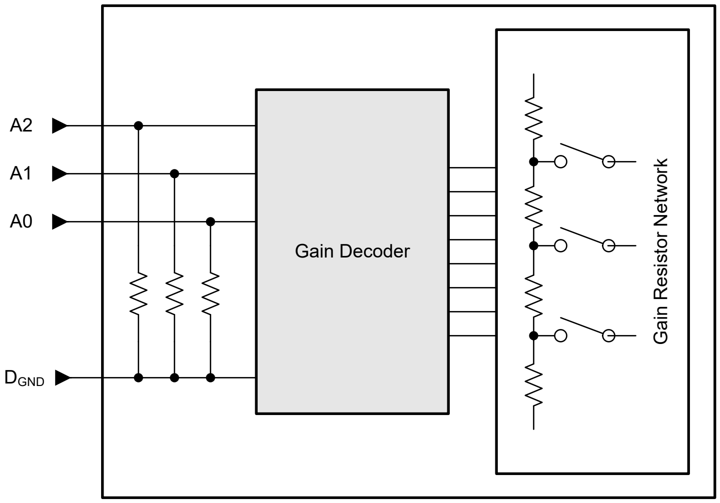


Figure 7-1. PGA849 Gain Setting Block Diagram

Table 7-1. Gain Options

A2:A0	GAIN
000	0.125
001	0.25
010	0.5
011	1
100	2
101	4
110	8
111	16

7.3.2 Input Protection

The inputs of the PGA849 are individually protected for voltages up to ±40V beyond either supply. For example, an input common-mode voltage anywhere between –55V and +55V does not cause damage when powered from ±15V supplies. Internal circuitry on each input provides low series impedance under normal signal conditions, thus maintaining high performance under normal operating conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 4.8mA. Figure 7-2 shows the input protection functionality during an overvoltage condition.

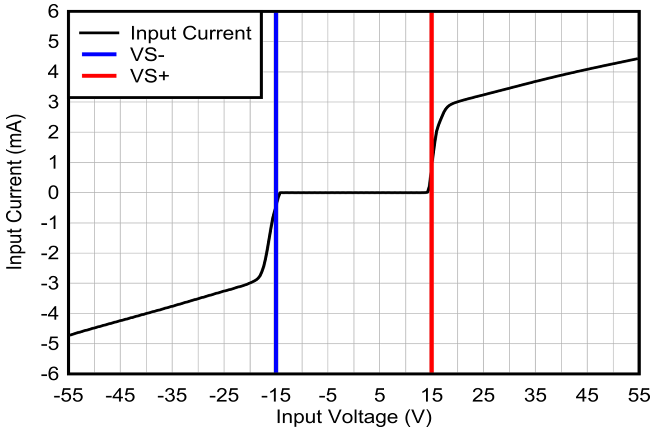


Figure 7-2. Input Current vs Input Overvoltage

Figure 7-3 shows that during an input overvoltage condition, current flows through the input protection diodes into the power supplies. In applications where the power supplies are unable to sink current, place Zener diode clamps (ZD1 and ZD2) on the power supplies to provide a current pathway to ground.

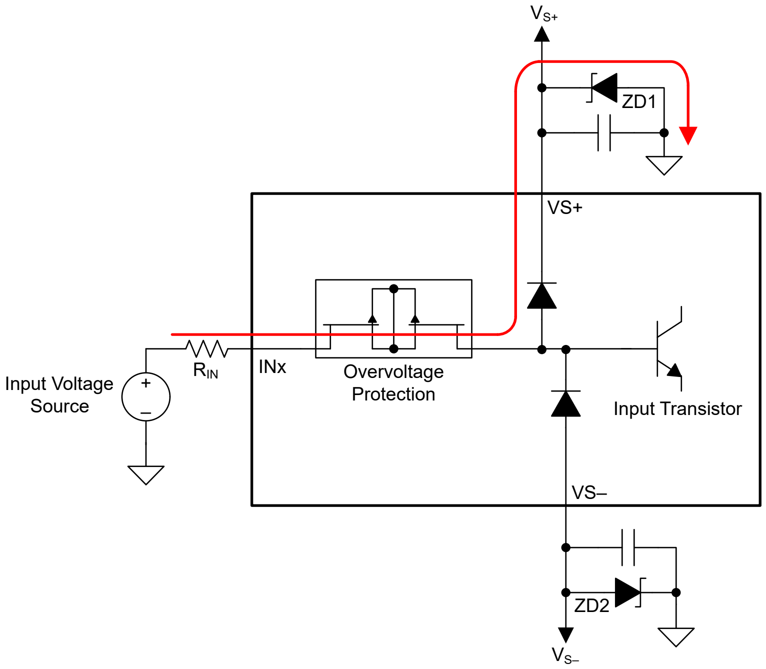


Figure 7-3. Input Current Path During an Overvoltage Condition

7.3.3 Using the Output Difference Amplifier to Shape Noise

The functional block diagram in Section 7.2 shows that the PGA849 output-stage difference amplifier uses a 5kΩ feedback resistor between the output and the inverting input. External direct access to the inverting and noninverting inputs of the difference amplifier is provided through the DA_IN– and DA_IN+ pins, respectively. This option allows circuit designers to add external capacitors in parallel with the internal resistors to implement noise-filtering or noise-shaping techniques. These pins are also used to implement customized attenuating gains for the output stage. Consider the following important factors when designing parallel circuits with the internal resistors:

- The accuracy of the internal resistor network is 0.01% or better. This accuracy results in a common-mode rejection (CMRR) of 80dB or better. Mismatched leakage currents on these pins can cause CMRR degradation.
- The internal resistors have ±15% absolute resistance variation and must be considered when implementing custom attenuating gains or noise filters.

CAUTION

Do not treat these pins as outputs, nor use the pins to source or sink current. Excessive currents through the feedback resistors can cause permanent damage to internal circuitry.

7.4 Device Functional Modes

The PGA849 has a single functional mode and operates when the input-stage power supply is greater than ±4V (8V) and the output-stage power supply is greater than ±2.25V (4.5V); see also Section 6.3.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The PGA849 is a monolithic, high-voltage, high-bandwidth, precision programmable gain instrumentation amplifier with a single-ended output. The PGA849 combines a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, differential amplifier output stage. The PGA849 is equipped with eight binary-gain settings, from 0.125V/V to 16V/V, using three digital gain-selection pins: A0, A1, and A2.

The PGA849 is designed to work with applications such as factory automation and control, analog input modules, data acquisition, test and measurement, and semiconductor test.

8.1.1 Linear Operating Input Range

The linear operating input voltage range of the PGA849 input circuitry extends within 3V (maximum) of the negative power supply to 2.5V (maximum) of the positive power supply, and maintains excellent common-mode rejection throughout this range at all temperatures. The linear operating input common-mode range is a function of the input common-mode voltage, input differential voltage, gain, and output common-mode voltage.

The valid common-mode range to enable valid output voltage at no load condition are shown in Figure 8-1 to Figure 8-4.

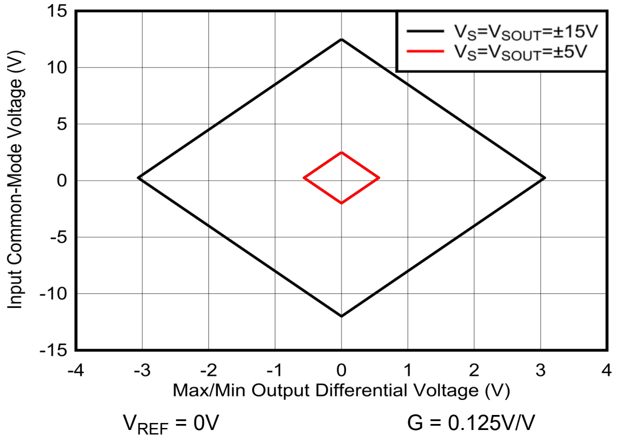


Figure 8-1. Input Common-Mode Voltage vs Output Voltage

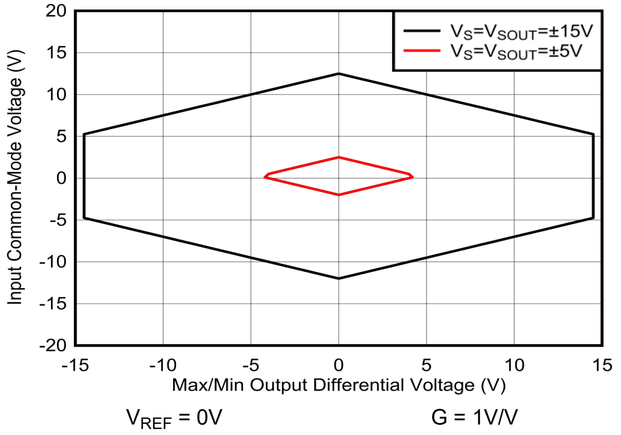
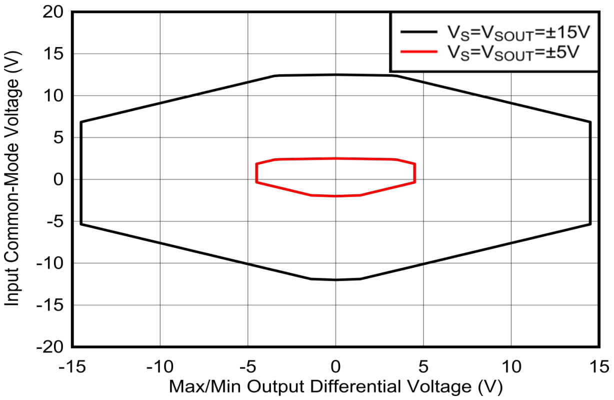
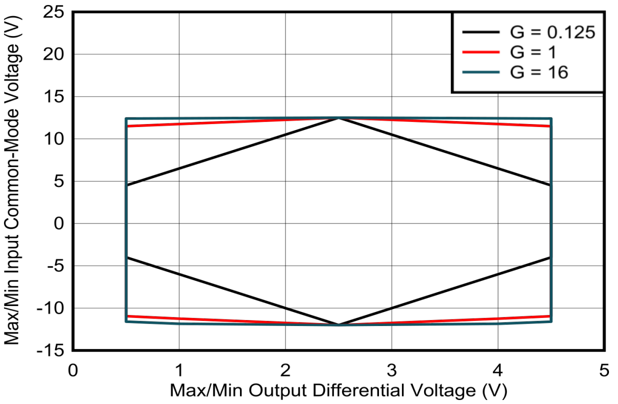


Figure 8-2. Input Common-Mode Voltage vs Output Voltage



V_{REF} = 0V G = 16V/V

Figure 8-3. Input Common-Mode Voltage vs Output Voltage



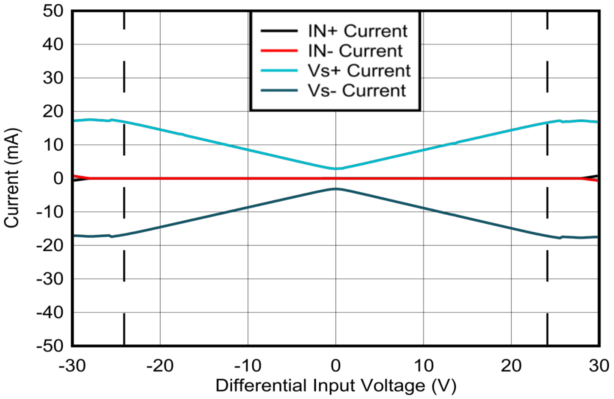
V_S = ±15V V_{SOUT} = 5V
V_{REF} = 2.5V

Figure 8-4. Input Common-Mode Voltage vs Output Voltage

8.1.2 Current Consumption with Differential Inputs

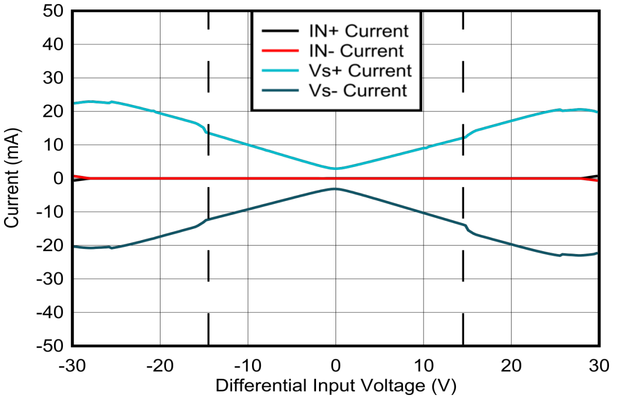
Programmable gain amplifiers such as the PGA849 use internal resistors to set the gain. Consequently, the current consumption is increased by the current that passes through these resistors. The largest supply current consumption occurs at G = 1V/V when applying large amplitude differential signals.

Figure 8-5 to Figure 8-8 show typical current consumption versus input differential voltage for the input stage supply, and the current drawn by the PGA849 inputs when the device is overdriven. The dashed vertical reference lines outline the linear operating region of the device at that given gain (V_{IN}DIFF), outside of this region is when the inputs of the device are overdriven.



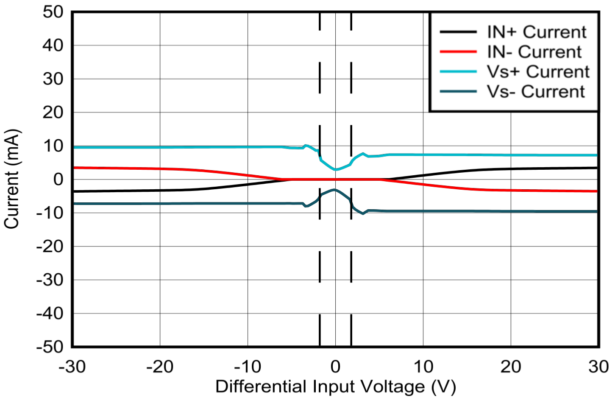
V_S = V_{SOUT} = ±15V V_{ICM} = V_{REF} = 0V
V_{IN}DIFF = ±24.1V G = 0.125V/V

Figure 8-5. Current Consumption versus Differential Input Voltage



V_S = V_{SOUT} = ±15V V_{ICM} = V_{REF} = 0V
V_{IN}DIFF = ±14.5V G = 1V/V

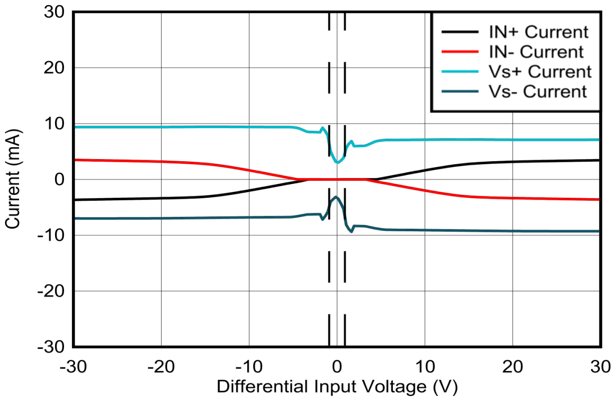
Figure 8-6. Current Consumption versus Differential Input Voltage



$V_S = V_{SOUT} = \pm 15V$ $V_{ICM} = V_{REF} = 0V$

$V_{IN}DIFF = \pm 1.8V$ G = 8V/V

Figure 8-7. Current Consumption versus Differential Input Voltage



$V_S = V_{SOUT} = \pm 15V$ $V_{ICM} = V_{REF} = 0V$

$V_{IN}DIFF = \pm 0.9V$ G = 16V/V

Figure 8-8. Current Consumption versus Differential Input Voltage

8.2 Typical Applications

8.2.1 Driving a Single-Ended Input SAR ADC

Figure 8-9 shows the schematic for a 16-bit, precision, 1MSPS, successive approximation register (SAR), analog-to-digital converter (ADC). This circuit is used to measure the driving capability of the PGA849 with the ADS8860 single-ended input ADC.

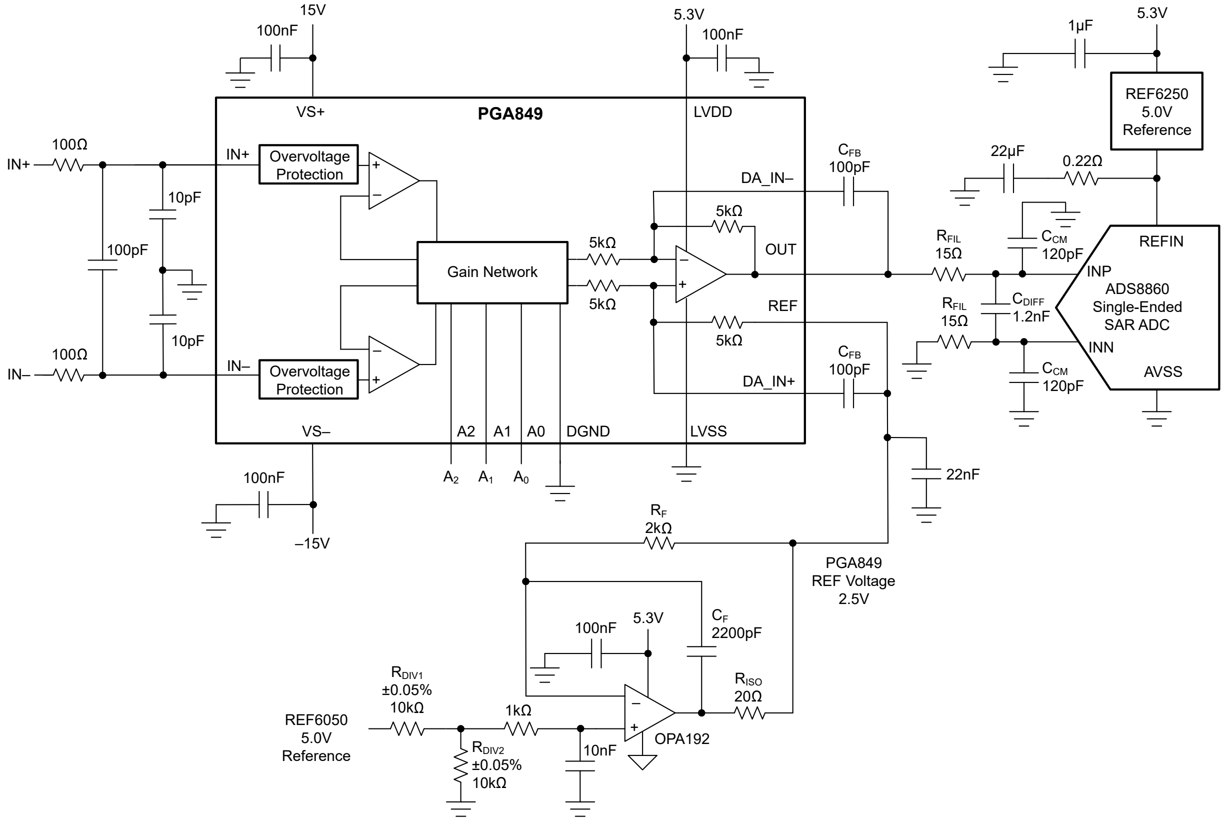


Figure 8-9. Driving the ADS8860 SAR ADC

The circuit accepts single-ended or differential input signals. The PGA849 operates with independent input and output power supplies. In this example, ±15V power supplies are used to power the input-stage, and a unipolar 5.3V supply powers the output-stage. The PGA849 output stage supply is powered by the same 5.3V ADC supply. The 5.3V output supply operation prevents overloading the ADC inputs during PGA overdrive conditions. The REF6250 is selected as the ADC voltage reference. The REF6250 is a low-noise, low-drift, precision, 5V reference connected to the ADS8860 reference input ADC REFIN pin.

The PGA849 output voltage is developed with respect to the REF pin. The REF pin is set to the SAR ADC midscale voltage by dividing the REF6250 ADC reference with a precision resistive voltage divider. The OPA192 buffer drives the PGA849 REF pin. The OPA192 is a precision amplifier with low offset, low drift and 10MHz bandwidth.

8.2.1.1 Design Requirements

The design requirements for the application driving the ADS8860 ADC are listed in the following table.

Table 8-1. Design Parameters

PARAMETER	VALUE
Supply voltages	VS± = ±15V, LVDD = 5.3V, LVSS = GND, ADC REFIN = 5V
PGA849 reference pin	V_{REF} = 2.5V
Full-scale range of ADC	FSR = 5V
Sampling rate of ADC	f_{SAMPLE} = 1MSPS
PGA gain	0.125, 0.25, 0.5, 1, 2,4, 8, 16
Input voltages (V_{PP}, differential)	25V, 16V, 8V, 4V, 2V, 1V, 0.5V, 0.25V
Signal frequency	1kHz
RC kickback filter	R_{FIL} = 15Ω, C_{DIFF} = 1.2nF, C_{CM} = 120pF

8.2.1.2 Detailed Design Procedure

The first filter located at the input of the PGA (see Figure 8-9) helps reduce electromagnetic interference (EMI) and radio frequency interference (RFI), high-frequency, extrinsic noise. This filter can be customized per the application bandwidth and antialiasing requirements.

The second filter is provided by C_{FB} in parallel with the PGA 5kΩ feedback resistors. The PGA resistors are ±15% absolute tolerance, as such, consider the effect of the tolerance on the filter cutoff frequency. C_{FB} = 100pF results in a filter cutoff frequency of 318kHz. On the high side of the resistor tolerance, the filter frequency changes to 277kHz. The device allows for the flexibility to modify the C_{FB} capacitor value to adjust bandwidth, with a trade-off on the broadband noise of the circuit.

The third filter placed at the ADS8860 inputs works as a charge reservoir filter to drive the SAR ADC. The charge kickback filter reduces the instantaneous charge demand of the amplifier, maintaining low distortion that otherwise can degrade because of incomplete ADC sample-and-hold settling. The RC filter combination (R_{FIL}, C_{DIFF}) is tuned for ADC sample-and-hold settling and total harmonic distortion (THD) performance, while maintaining stability of the PGA. High-grade C0G capacitors are used everywhere in the signal path for the low distortion properties.

The PGA849 front-end, accounting for all three filters, provides a nominal $f_{–3dB}$ bandwidth of 310kHz. On the high side of the internal 5kΩ feedback resistor tolerance, the PGA849 $f_{–3dB}$ bandwidth changes to 271kHz and the circuit maintains –0.1dB flatness to 41kHz.

The ADS8860 requires a full-scale input in the range of 0V to the 5V ADC reference. The PGA849 REF pin is set to a nominal voltage of 2.5V to shift the signal to the ADC midscale voltage.

The PGA849 REF voltage is generated by feeding the REF6250 5V reference through a 10kΩ-to-10kΩ precision voltage divider implemented with ±0.05% tolerance, low-drift ±5ppm/°C resistors. Drive the PGA849 REF pin with a low-impedance source, and use an op amp like the OPA192 as a buffer to drive the REF pin.

The OPA192 buffer is configured in a dual-feedback configuration to provide stability while driving the REF pin and 22nF bypass capacitor. R_{ISO} is a 20Ω isolation resistor that provides separation of two feedback paths for optimized stability. Feedback path number one is through feedback resistor, R_F = 2kΩ, connected directly to the REF pin. Feedback path number two is through feedback capacitor C_F = 2nF connected to the output of the op amp. The circuit provides a loop gain phase margin of 86°. The noninverting input of the OPA192 buffer has a low-pass filter with R = 1kΩ, C = 10nF to reduce the resistive divider thermal noise. Using any other load capacitance requires recalculation of the stability components: R_F, C_F, and R_{ISO}. If modifying the REF bypass capacitance, verify the circuit is stable with simulation using the OPA192 TINA-TI model (or PSpice®-for-TI model), and confirm the circuit provides more than 60° of phase margin.

8.2.1.3 Application Curves

Table 8-2 lists the PGA849 output voltage with different gain configurations, and Figure 8-10 shows the PGA849 output voltage with a gain of 2.

Table 8-2. PGA849 Output Voltage with Different Gain Configurations

Input (mV)	Reference (V)	A2:A0	PGA Gain (V/V)	Minimum Output (V)	Maximum Output (V)
±50	2.5	000	0.125	2.494	2.506
		001	0.25	2.488	2.512
		010	0.5	2.475	2.525
		011	1	2.450	2.550
		100	2	2.400	2.600
		101	4	2.300	2.700
		110	8	2.100	2.900
		111	16	1.700	3.300

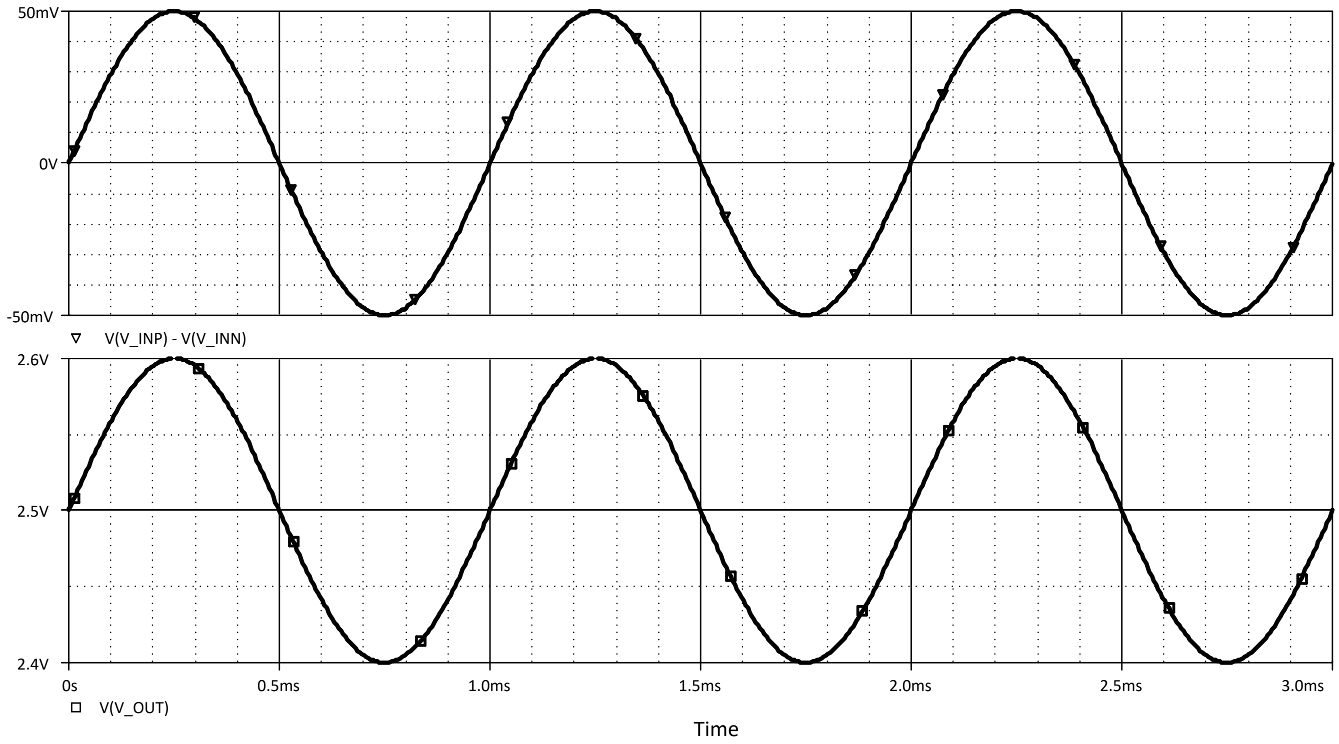


Figure 8-10. PGA849 Output Voltage with a Gain of 2, Reference = 2.5V

8.3 Power Supply Recommendations

The nominal performance of the PGA849 is specified with input-stage supply and output-stage supply voltages of ±15V, and V_{ICM} and V_{REF} at mid-supply. Within the specified limits, custom input common-mode and output reference voltages can be used without compromising performance; see also Section 6.3. To prevent damage to internal circuitry, the output-stage power supplies are clamped to stay within the input-stage supply voltage levels; see also Section 7.2.

CAUTION

Supply voltages higher than 40V (±20V) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in Section 6.6 of this data sheet.

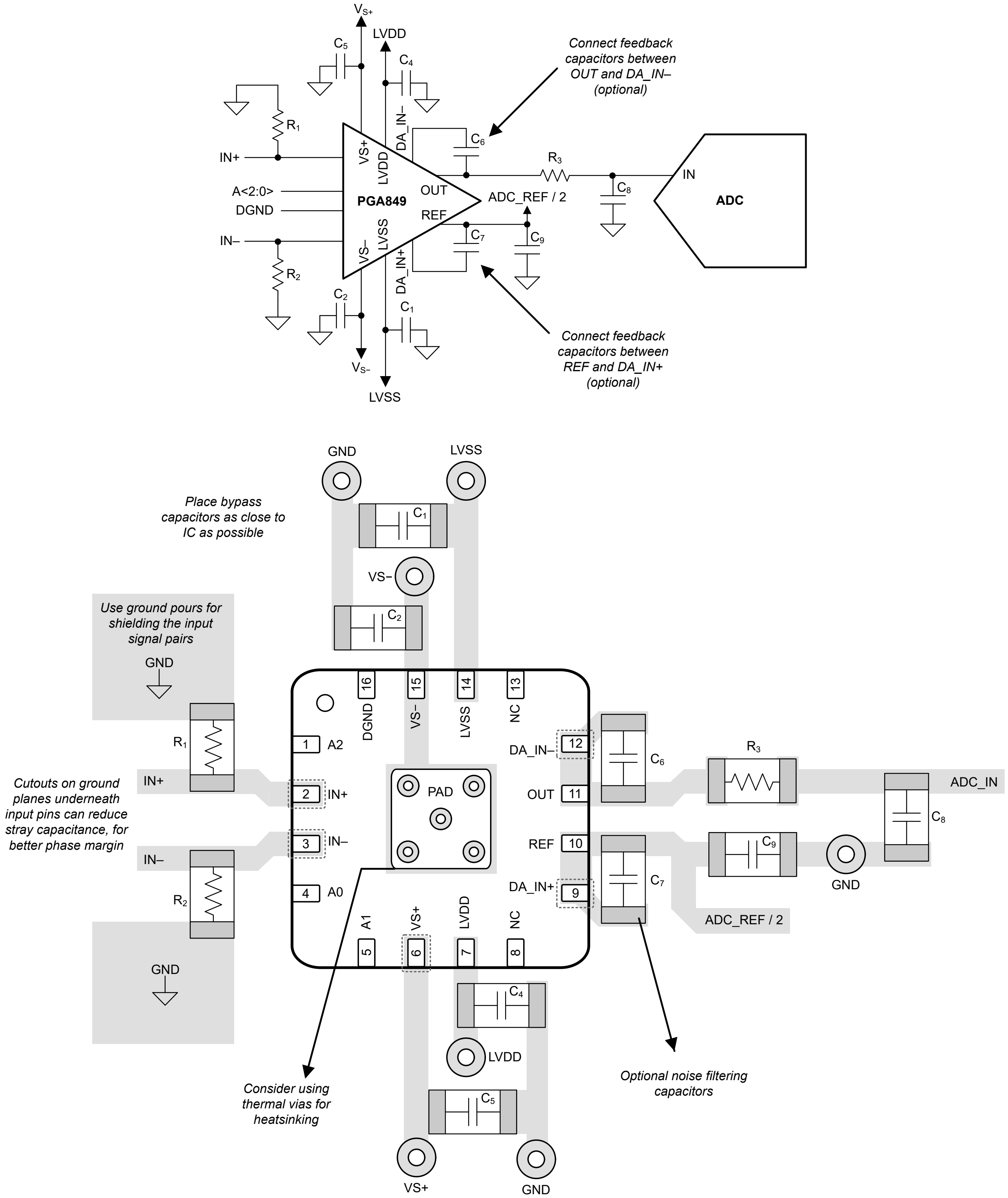
8.4 Layout

8.4.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- To avoid converting common-mode signals into differential signals and thermal electromotive forces (EMFs), make sure that both input paths are symmetrical and well-matched for source impedance and capacitance.
- Noise can propagate into analog circuitry through the power pins of the device and of the circuit as a whole. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Leakage on the DA_IN+ and DA_IN– pins can cause in a dc offset error in the output voltages. Additionally, excessive parasitic capacitance at these pins can result in decreased phase margin and affect the stability of the output stage. If these pins are not used to implement deliberate capacitive feedback, follow best practices to minimize leakage and parasitic capacitance.
- Follow best practices to minimize leakage and parasitic capacitance, which includes implementing *keep-out* areas in any ground planes that lie immediately below the input pins.
- Minimize the number of thermal junctions. If possible, route the signal path using a single layer without vias.
- Keep sufficient distance from major thermal energy sources (circuits with high power dissipation). If not possible, place the device so that the effects of the thermal energy source on the high and low sides of the differential signal path are evenly matched.
- Keep the traces as short as possible.

8.4.2 Layout Example



Connect feedback capacitors between OUT and DA_IN– (optional)

Connect feedback capacitors between REF and DA_IN+ (optional)

Place bypass capacitors as close to IC as possible

Use ground pours for shielding the input signal pairs

Cutouts on ground planes underneath input pins can reduce stray capacitance, for better phase margin

Consider using thermal vias for heatsinking

Optional noise filtering capacitors

Figure 8-11. Example Schematic and Associated PCB Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

9.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design and simulation tools web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Comprehensive Error Calculation for Instrumentation Amplifiers* application note
- Texas Instruments, *Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2024) to Revision A (December 2024)	Page
• Changed the document status from *Advance Information* to *Production Data*	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA849RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PGA849	Samples
XPGA849RGTR	ACTIVE	VQFN	RGT	16	3000	TBD	Call TI	Call TI	-40 to 125		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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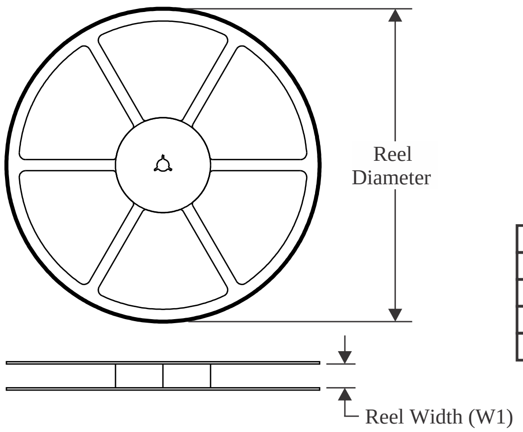
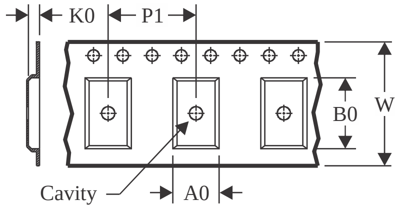
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

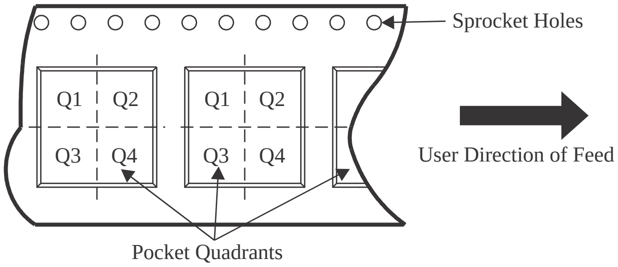


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

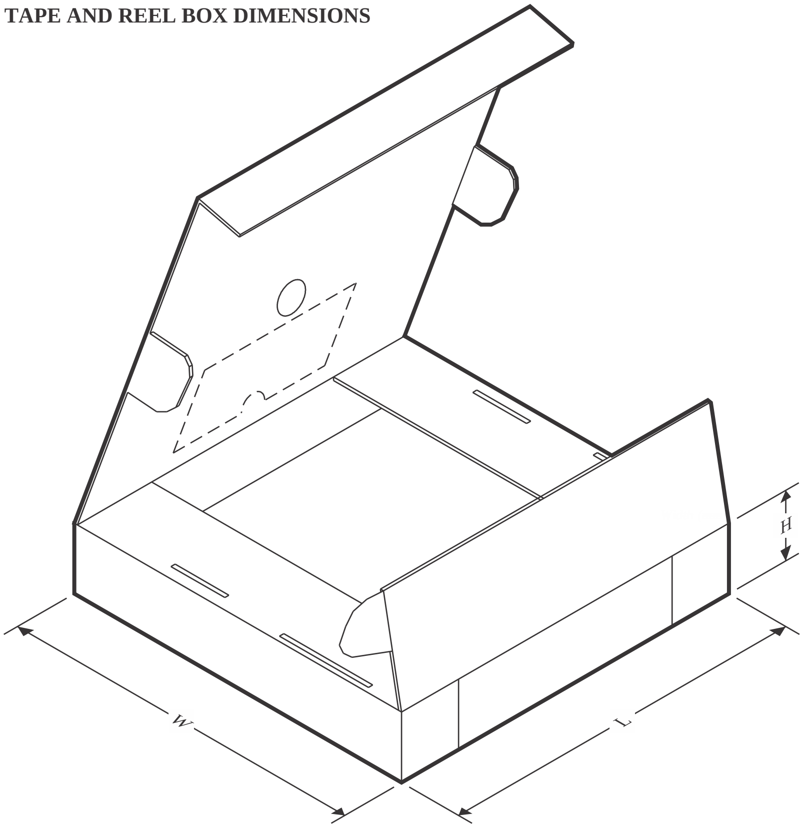
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA849RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

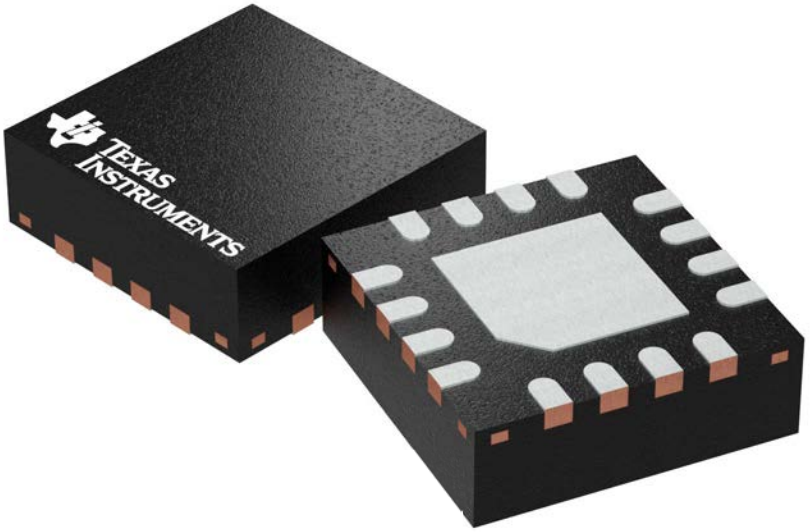
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA849RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

RGT 16

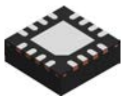
VQFN - 1 mm max height

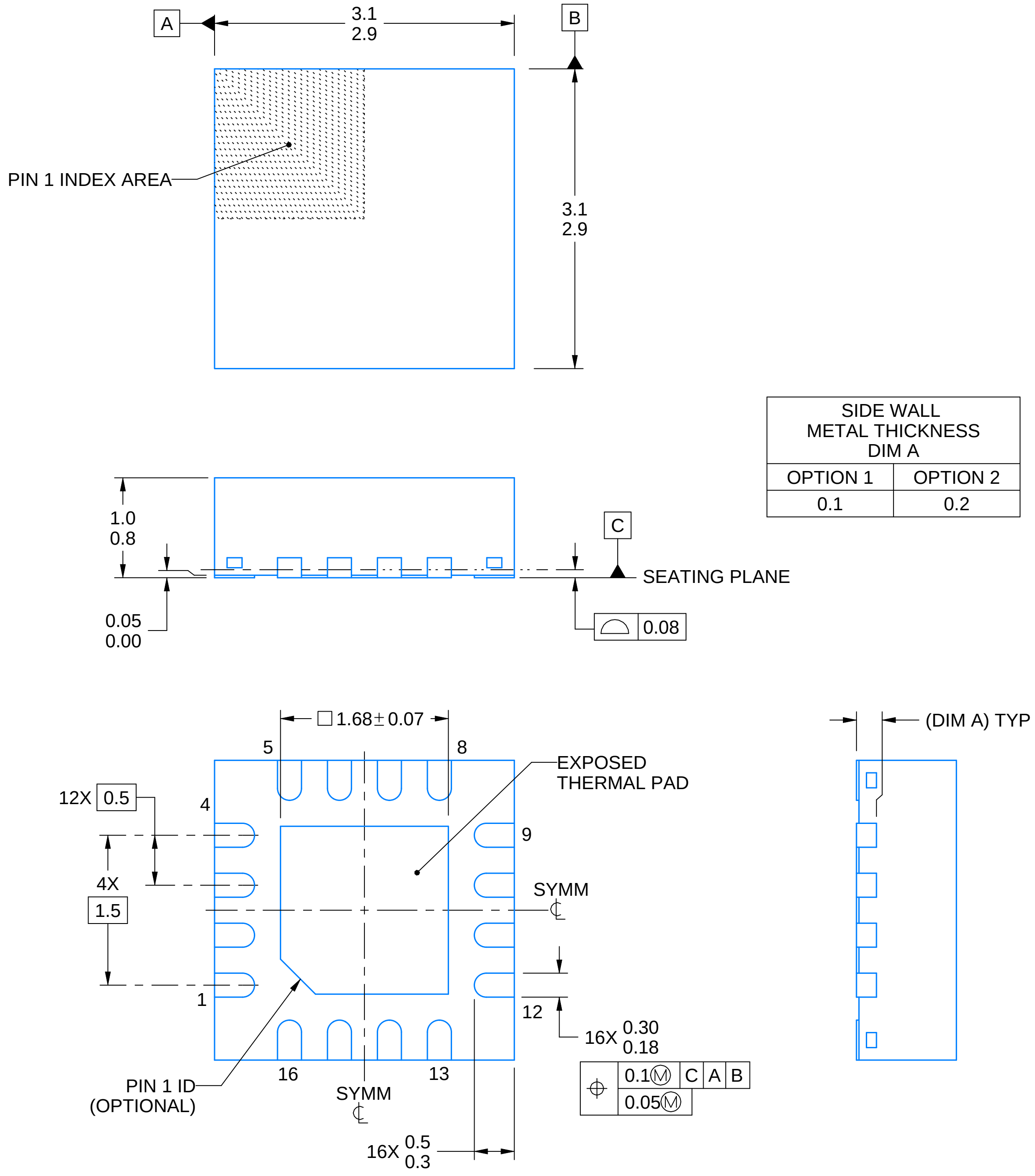
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/I



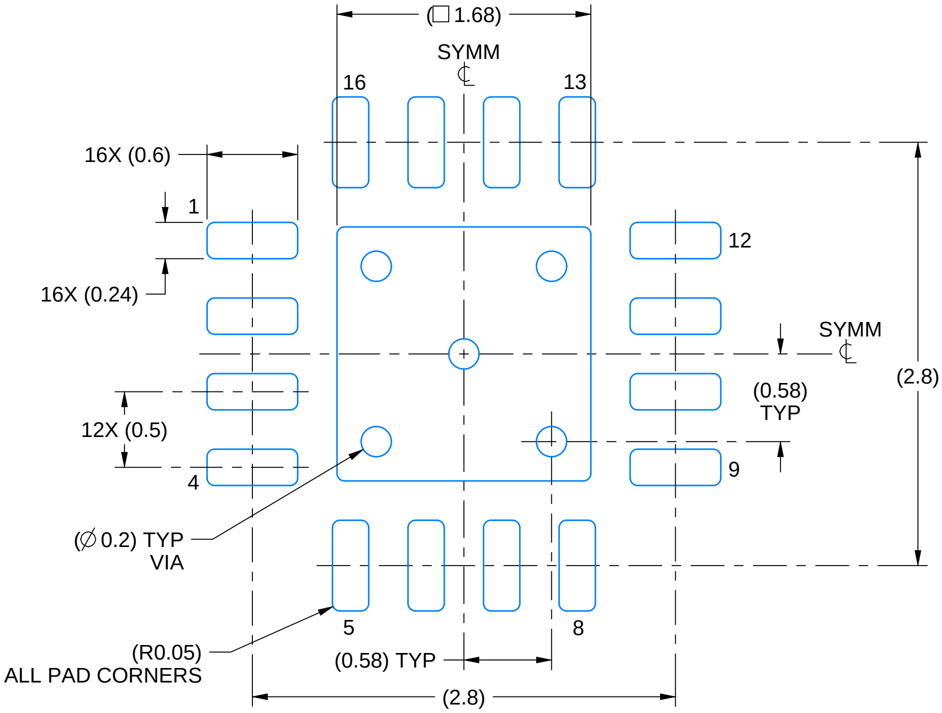


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

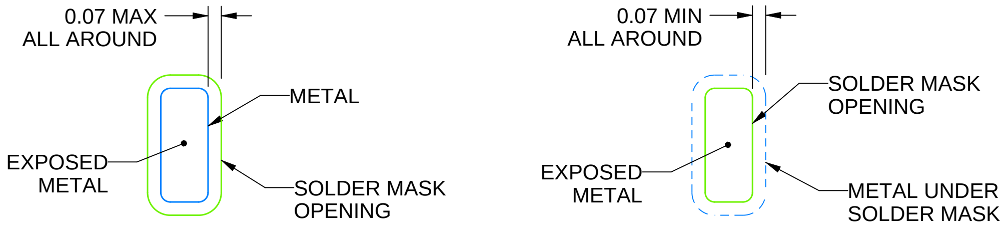
4222419/D 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



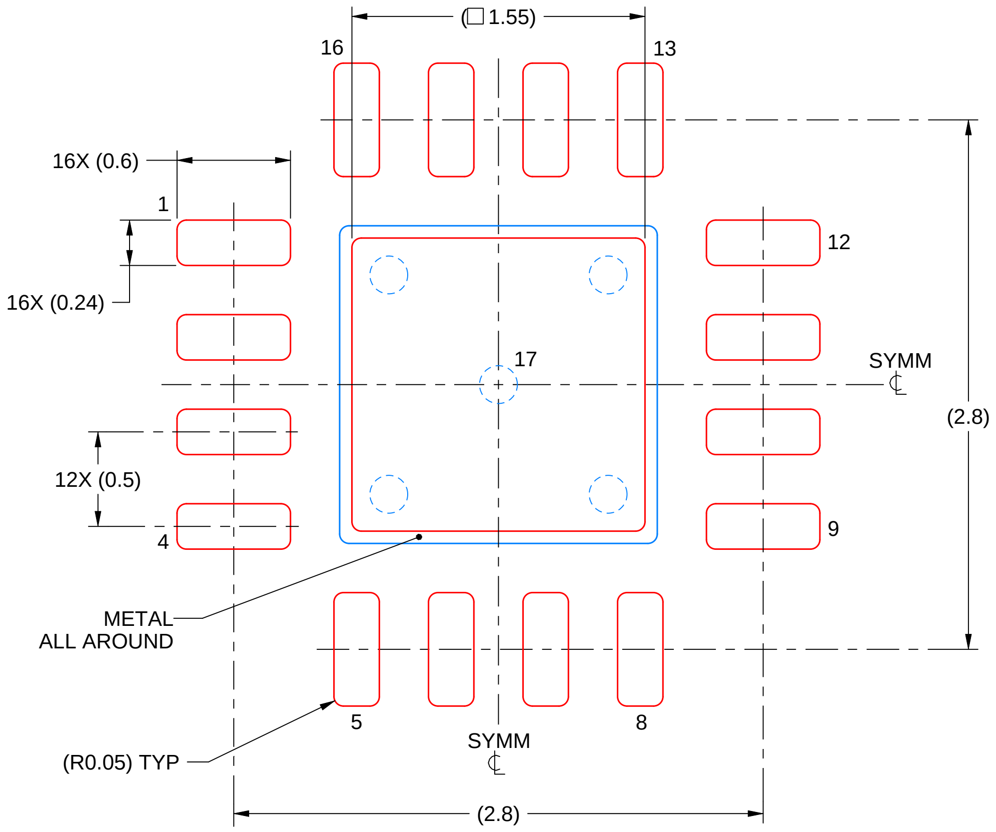
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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