

20-A, 4.75-V to 14-V INPUT, NON-ISOLATED, WIDE-OUTPUT, DIGITAL POWERTRAIN™ MODULE

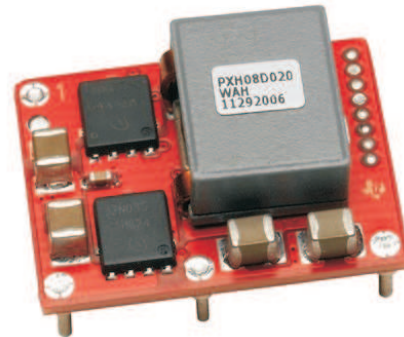
Check for Samples: [PTD08A020W](#)

FEATURES

- Up to 20-A Output Current
- 4.75-V to 14-V Input Voltage
- Programmable Wide-Output Voltage (0.7 V to 3.6 V)
- Efficiencies up to 96%
- Digital I/O
 - PWM signal
 - INHIBIT
 - Current limit flag (FAULT)
 - Synchronous Rectifier Enable (SRE)
- Analog I/O
 - Temperature
 - Output current
- Safety Agency Approvals: (Pending)
 - UL/IEC/CSA-C22.2 60950-1
- Operating Temperature: –40°C to 85°C

APPLICATIONS

- Digital Power Systems using UCD92XX Digital Controllers



DESCRIPTION

The PTD08A020W is a high-performance 20-A rated, non-isolated digital PowerTrain module. This module is the power conversion section of a digital power system which incorporates TI's UCD7230 MOSFET driver IC. The PTD08A020W must be used in conjunction with a digital power controller such as the UCD9240 or UCD9110 family. The PTD08A020W receives control signals from the digital controller and provides parametric and status information back to the digital controller. Together, PowerTrain modules and a digital power controller form a sophisticated, robust, and easily configured power management solution.

Operating from an input voltage range of 4.75 V to 14 V, the PTD08A020W provides step-down power conversion to a wide range of output voltages from, 0.7 V to 3.6 V. The wide input voltage range makes the PTD08A020W particularly suitable for advanced computing and server applications that utilize a loosely regulated 8-V, 9.6-V or 12-V intermediate distribution bus. Additionally, the wide input voltage range increases design flexibility by supporting operation with tightly regulated 5-V or 12-V intermediate bus architectures.

The module incorporates output over-current and temperature monitoring which protects against most load faults. Output current and module temperature signals are provided for the digital controller to permit user defined over-current and over-temperature warning and fault scenarios.

The module uses double-sided surface mount construction to provide a low profile and compact footprint. Package options include both through-hole and surface mount configurations that are lead (Pb) - free and RoHS compatible.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

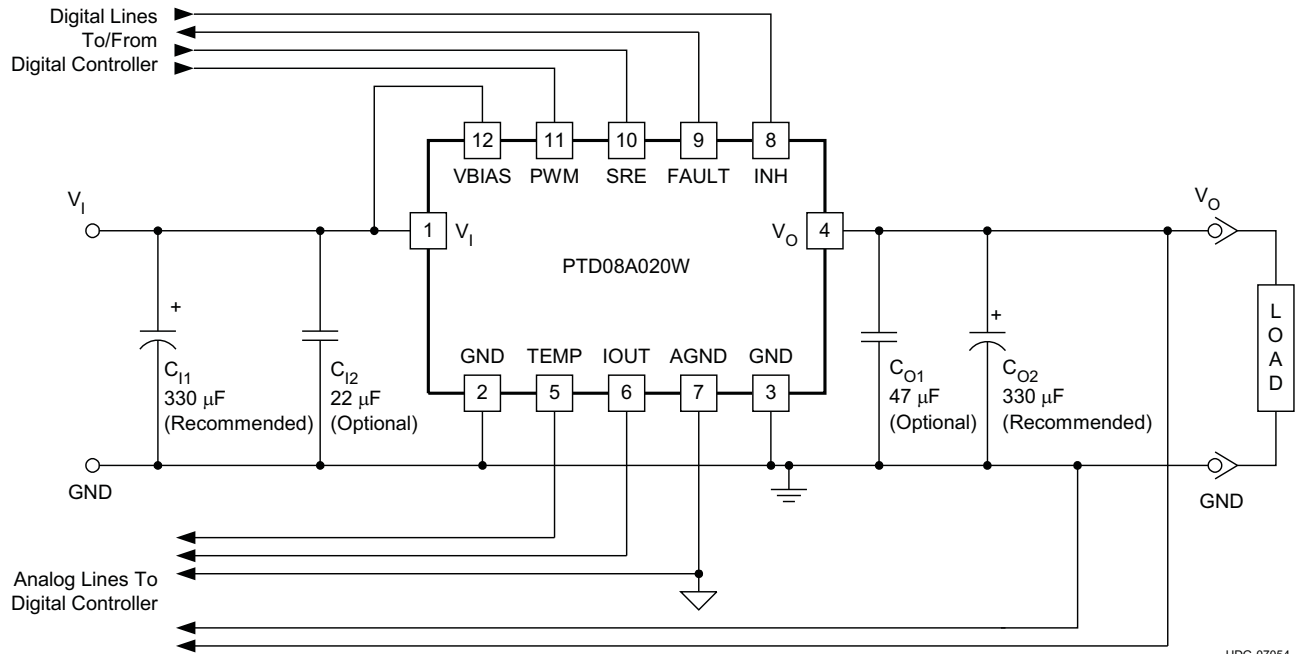
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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Standard PTD08A020W Application



UDG-07054

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

DATASHEET TABLE OF CONTENTS

DATASHEET SECTION	PAGE NUMBER
ENVIRONMENTAL AND ABSOLUTE MAXIMUM RATINGS	3
ELECTRICAL CHARACTERISTICS TABLE	4
TERMINAL FUNCTIONS	5
TYPICAL CHARACTERISTICS ($V_I = 12V$)	6
TYPICAL CHARACTERISTICS ($V_I = 5V$)	8
TYPICAL APPLICATION SCHEMATIC	10
GRAPHICAL USER INTERFACE VALUES	11
TRAY DRAWINGS	12

ENVIRONMENTAL AND ABSOLUTE MAXIMUM RATINGS

(Voltages are with respect to GND)

				UNIT
V_I	Input voltage		16	V
V_B	Bias voltage		16	V
T_A	Operating temperature range	Over V_I range	-40 to 85	°C
T_{wave}	Wave soldering temperature	Surface temperature of module body or pins for 5 seconds maximum.	suffix AD 260	
T_{stg}	Storage temperature	Storage temperature of module removed from shipping package	-55 to 125	
T_{pkg}	Packaging temperature	Shipping Tray or Tape and Reel storage or bake temperature	45	
	Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted	suffix AD 250	G
	Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000 Hz	15	grams
	Weight		7.4	
MTBF	Reliability	Per Telcordia SR-332, 50% stress, $T_A = 40^\circ\text{C}$, ground benign	9.26	10^6 Hr
	Flammability	Meets UL94V-O		

ELECTRICAL CHARACTERISTICS

PTD08A020W

$T_A = 25^\circ\text{C}$, $F_{\text{SW}} = 350\text{kHz}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$, $V_B = V_I$, $C_{I1} = 330\ \mu\text{F}$, $C_{I2} = 22\ \mu\text{F}$ ceramic, $C_{O1} = 47\ \mu\text{F}$ ceramic, $C_{O2} = 330\ \mu\text{F}$, and $I_O = I_{O(\text{max})}$ (unless otherwise stated)

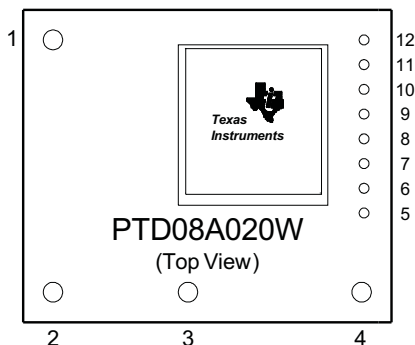
PARAMETER		TEST CONDITIONS		PTD08A010W			UNIT
				MIN	TYP	MAX	
I_O	Output current	Over V_O range	25°C, natural convection		0	20	A
V_I	Input voltage range	Over I_O range		4.75	14 ⁽¹⁾		V
V_{OAdj}	Output voltage adjust range	Over I_O range		0.7 ⁽¹⁾	3.6		V
η	Efficiency	$I_O = 20\text{ A}$, $f_s = 350\text{ kHz}$	$V_O = 3.3\text{ V}$	91%			
			$V_O = 2.5\text{ V}$	89%			
			$V_O = 1.8\text{ V}$	86%			
			$V_O = 1.5\text{ V}$	84%			
			$V_O = 1.2\text{ V}$	83%			
			$V_O = 1.0\text{ V}$	80%			
V_{OPP}	V_O Ripple (peak-to-peak)	20-MHz bandwidth		20		mV _{PP}	
V_B	Bias voltage			4.75	14		V
V_B $UVLO$	Bias voltage under voltage lockout	V_B increasing		4.25	4.5	4.75	V
		V_B decreasing		4.0	4.25	4.5	
I_B	Bias current	Inhibit (pin 8) to AGND		Standby		5	mA
				Switching		42	
V_{IH}	High-level input voltage	SRE, INH, & PWM input levels		2.0	5.5		V
V_{IL}	Low-level input voltage			0.8			
	PWM input	Frequency range		300	500		kHz
		Pulse width limits		130		ns	
	TEMP output	Range		-40	125		°C
		Accuracy, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		-4.0	+6.0		
		Slope		10		mV/°C	
		Offset, $T_A = 0^\circ\text{C}$		500		mV	
V_{OH}	FAULT output	High-level output voltage, $I_{\text{FAULT}} = 4\text{ mA}$		2.7	3.3		V
V_{OL}		Low-level output voltage, $I_{\text{FAULT}} = 4\text{ mA}$		0	0.6		
I_{LIM}		Overcurrent threshold; Reset, followed by auto-recovery		35		A	
	IOUT output	Range		0.15	3.5		V
		Gain		46	66	86	
		Offset		0.44	0.6	0.76	V
		Output Impedance		10	15	20	kΩ
C_I	External input capacitance	Nonceramic		330 ⁽²⁾		μF	
		Ceramic		22 ⁽²⁾			
C_O	External output capacitance	Capacitance Value	Nonceramic	330 ⁽³⁾	10,000 ⁽⁴⁾		μF
			Ceramic	47 ⁽³⁾	⁽³⁾		
		Equivalent series resistance (non-ceramic)		1 ⁽⁵⁾		mΩ	

- (1) The maximum input voltage is duty cycle limited to $(V_O / (130\text{ns} \times F_{\text{SW}}))$ or 14 V, whichever is less. The maximum allowable input voltage is a function of switching frequency.
- (2) A 22 μF ceramic input capacitor is recommended for operation. An additional 330 μF bulk capacitor rated for a minimum of 500mA rms of ripple current is recommended. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.
- (3) A 47 μF ceramic output capacitor is recommended for operation. An additional 330 μF bulk capacitor is recommended for improved transient response. See the related Application Information section for further guidance. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.
- (4) 10,000 μF is the calculated maximum output capacitance given a 1V/msec output voltage rise time. Additional capacitance or increasing the output voltage rise rate may trigger the overcurrent threshold at start-up.
- (5) This is the minimum ESR for all non-ceramic output capacitance. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
V _I	1	The positive input voltage power node to the module, which is referenced to common GND.
GND	2	This is the common ground connection for the V _I and V _O power connections.
	3	
V _O	4	The regulated positive power output with respect to GND.
TEMP	5	Temperature sense output. The voltage level on this pin represents the temperature of the module.
IOUT	6	Current sense output. The voltage level on this pin represents the average output current of the module.
AGND	7	Analog ground return. It is the 0 V _{dc} reference for the control inputs.
INH ⁽¹⁾	8	The inhibit pin is a negative logic input that is referenced to AGND. Applying a low-level signal to this pin disables the module and turns off the output voltage. A 10 kΩ pull-up to 3.3 V or 5 V is required if the INH signal is not used.
FAULT	9	Current limit flag. The Fault signal is a 3.3 V digital output which is latched high after an over-current condition. The Fault is reset after two complete PWM cycles without an over-current condition (third rising edge of the PWM).
SRE	10	Synchronized Rectifier Enable. This pin is a high impedance digital input. A 3.3 V or 5 V logic level signals is used to enable the synchronous rectifier switch. When this signal is high, the module will source and sink output current. When this signal is low, the module will only source current.
PWM	11	This is the PWM input pin. It is a high impedance digital input that accepts 3.3 V or 5 V logic level signals up to 500 MHz.
VBIAS	12	Bias voltage supply required to power internal circuitry. For optimal performance connect VBIAS to V _I .

(1) Denotes negative logic: Open = Normal operation, Ground = Function active



TYPICAL CHARACTERISTICS ⁽¹⁾ ⁽²⁾

CHARACTERISTIC DATA ($V_I = 12\text{ V}$)

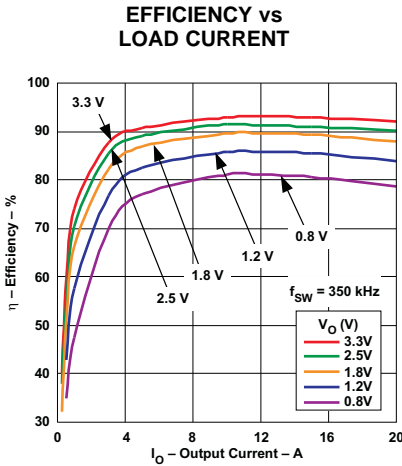


Figure 1.

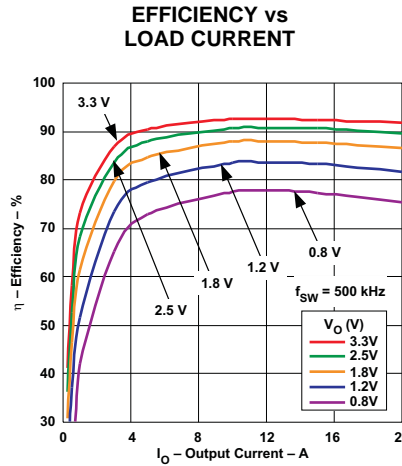


Figure 2.

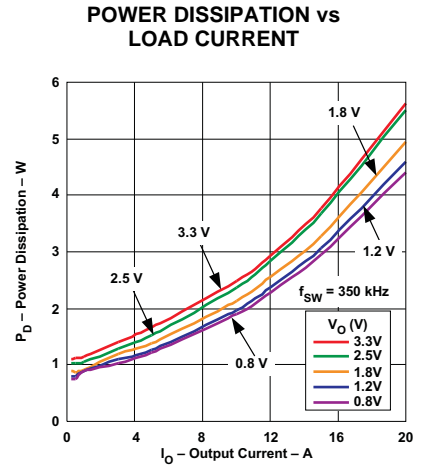


Figure 3.

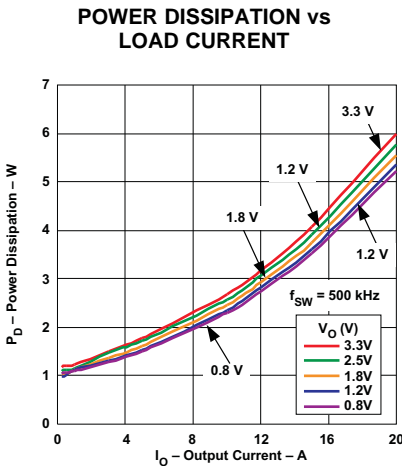


Figure 4.

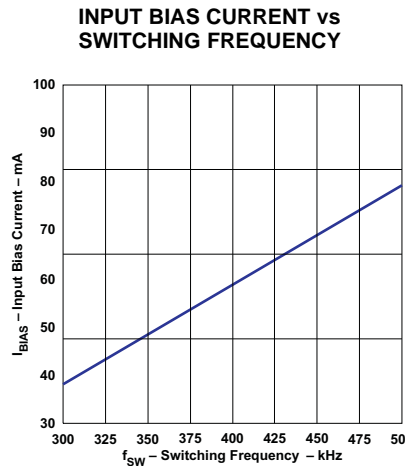


Figure 5.

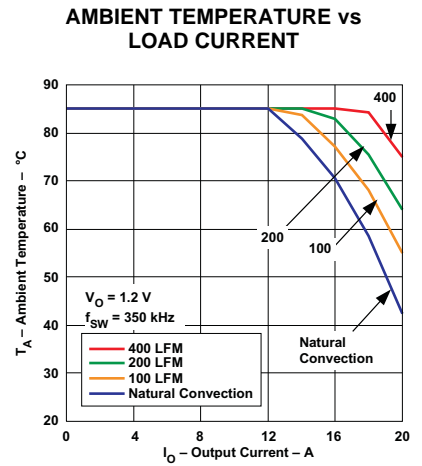


Figure 6. Safe Operating Area

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1 thru Figure 5.
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. Please refer to the mechanical specification for more information. Applies to Figure 6 thru Figure 9.

TYPICAL CHARACTERISTICS^{(3) (4)} (continued)

AMBIENT TEMPERATURE vs LOAD CURRENT

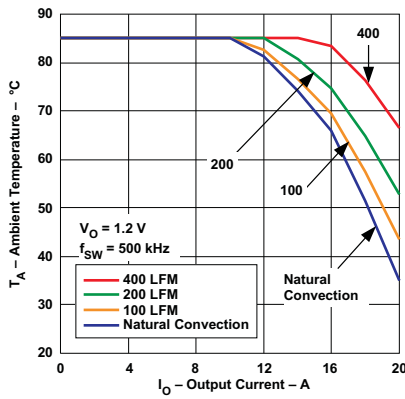


Figure 7. Safe Operating Area

AMBIENT TEMPERATURE vs LOAD CURRENT

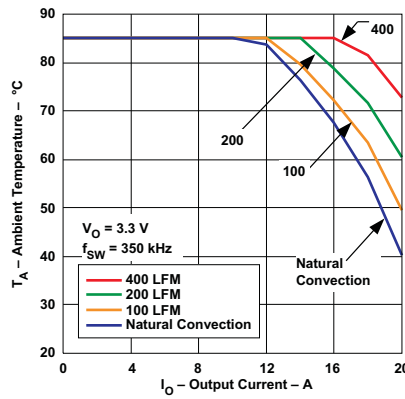


Figure 8. Safe Operating Area

AMBIENT TEMPERATURE vs LOAD CURRENT

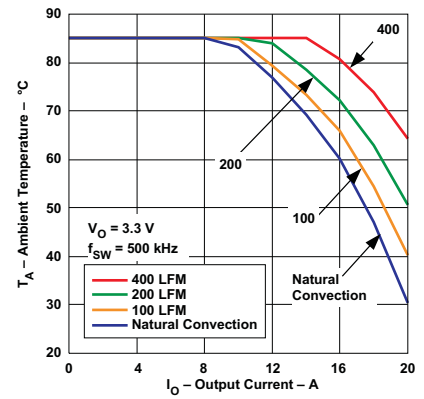


Figure 9. Safe Operating Area

TYPICAL CHARACTERISTICS ⁽¹⁾ ⁽²⁾

CHARACTERISTIC DATA ($V_I = 5\text{ V}$)

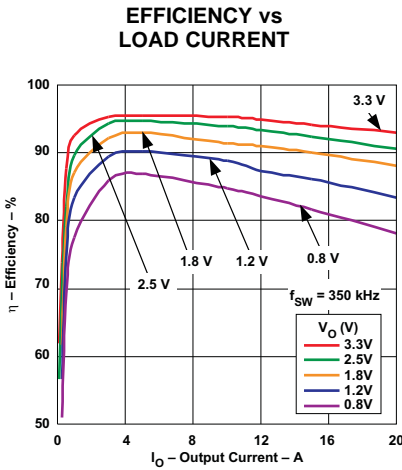


Figure 10.

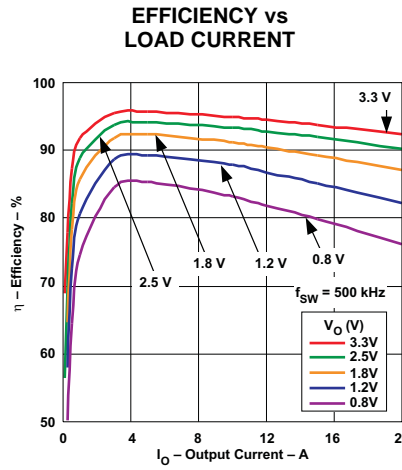


Figure 11.

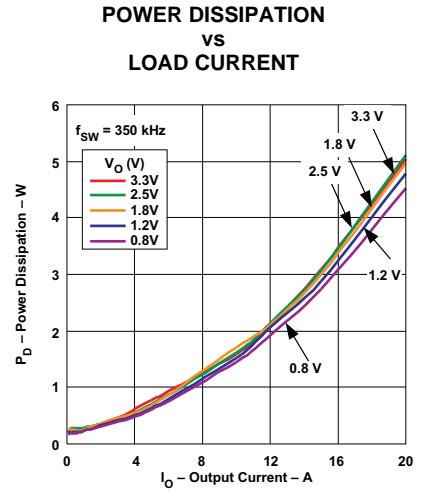


Figure 12.

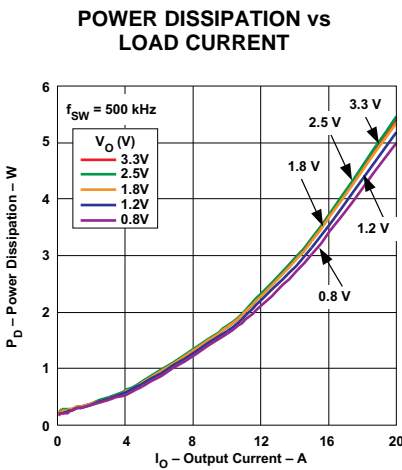


Figure 13.

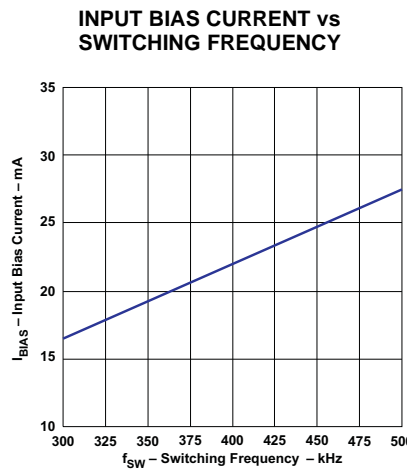


Figure 14.

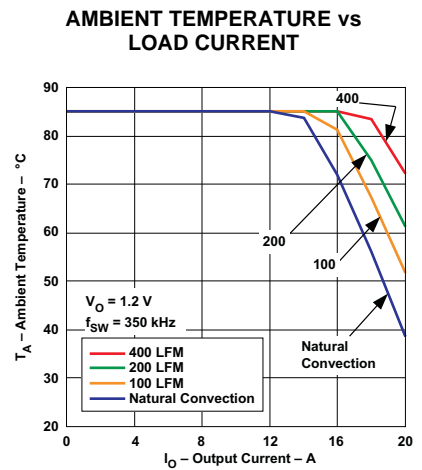


Figure 15. Safe Operating Area

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 10 thru Figure 14.
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. Please refer to the mechanical specification for more information. Applies to Figure 15 thru Figure 18.

TYPICAL CHARACTERISTICS⁽³⁾ ⁽⁴⁾ (continued)

AMBIENT TEMPERATURE vs LOAD CURRENT

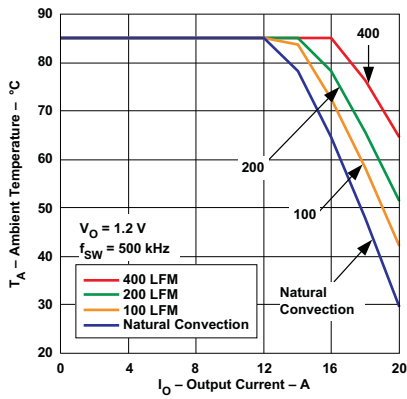


Figure 16. Safe Operating Area

AMBIENT TEMPERATURE vs LOAD CURRENT

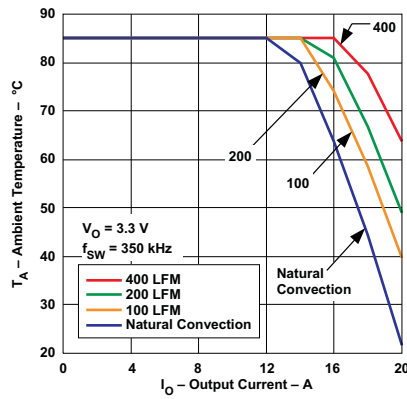


Figure 17. Safe Operating Area

AMBIENT TEMPERATURE vs LOAD CURRENT

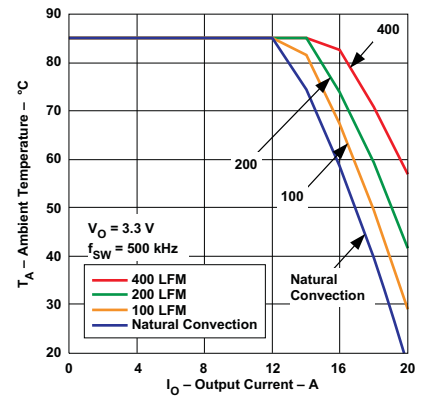


Figure 18. Safe Operating Area

APPLICATION INFORMATION

Digital Power

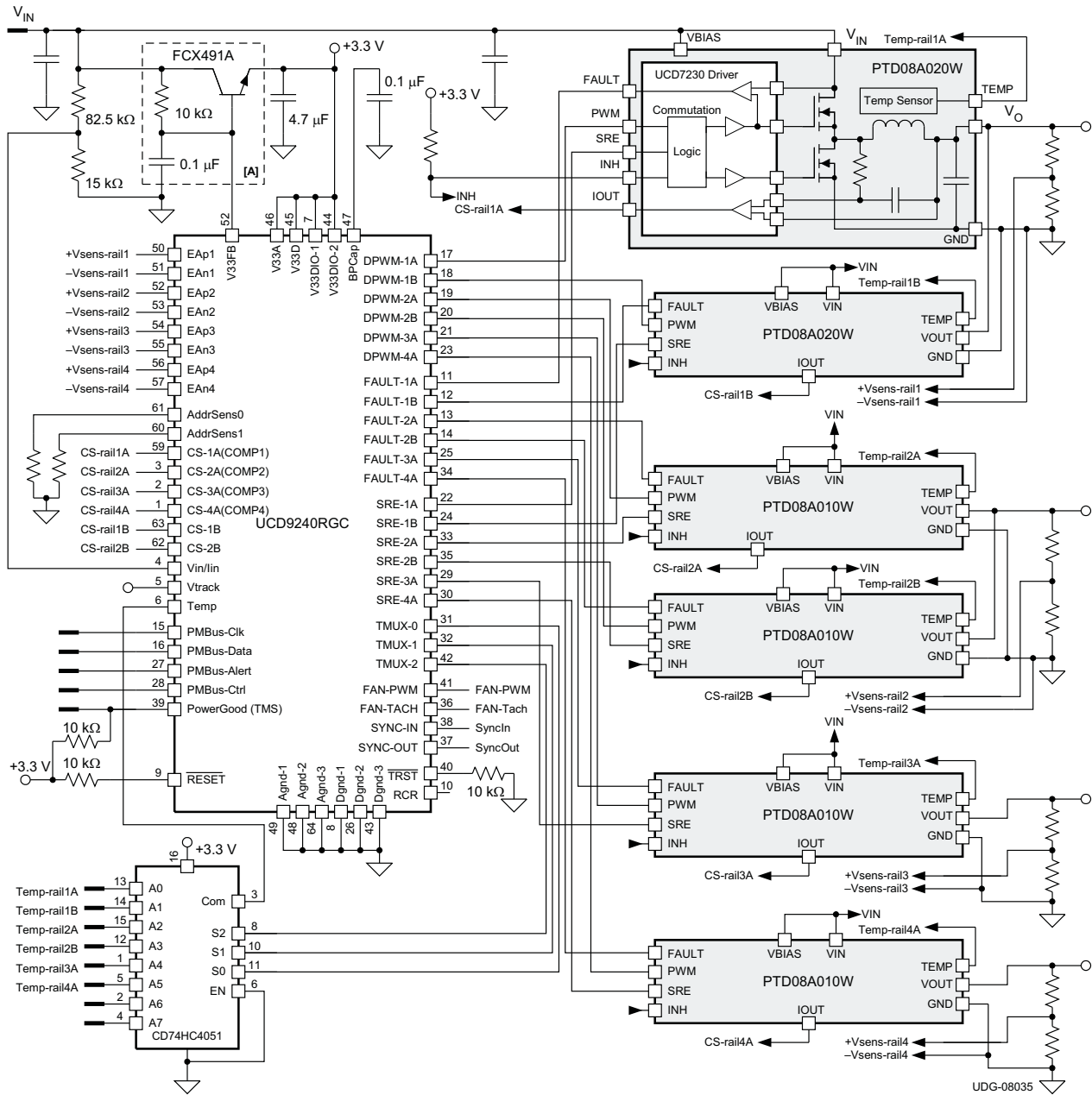


Figure 19. Typical Application Schematic

Figure 19 shows the UCD9240 power supply controller working in a system which requires the regulation of four independent power supplies. The loop for each power supply is created by the respective voltage outputs feeding into the Error ADC differential inputs, and completed by DPWM outputs feeding into the UCD7230 drivers which are shown on the PTD08A010W and PTD08A020W modules.

UCD9240 Graphical User Interface (GUI)

When using the UCD9240 digital controller along with digital PowerTrain modules to design a digital power system, several internal parameters of the modules are required to run the Fusion Digital Power Designer GUI. See the plant parameters below for the PTD08A010W and PTD08A020W digital PowerTrain modules.

Table 1. PTD08A010W Plant Parameters

PTD08A010W Plant Parameters			
L (μH)	DCR (mΩ)	Rds-on-hi (mΩ)	Rds-on-lo (mΩ)
0.90	2.2	3.6	3.6

Table 2. PTD08A020W Plant Parameters

PTD08A020W Plant Parameters			
L (μH)	DCR (mΩ)	Rds-on-hi (mΩ)	Rds-on-lo (mΩ)
1.0	1.5	5.0	2.5

Internal output capacitance is present on the digital PowerTrain modules themselves. When using the GUI interface this capacitance information must be included along with any additional external capacitance. See the capacitor parameters below for the PTD08A010W and PTD08A020W digital PowerTrain modules.

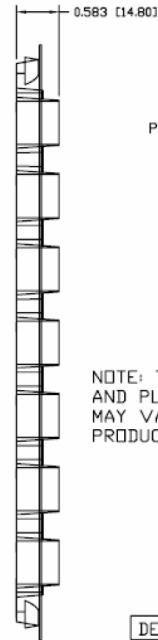
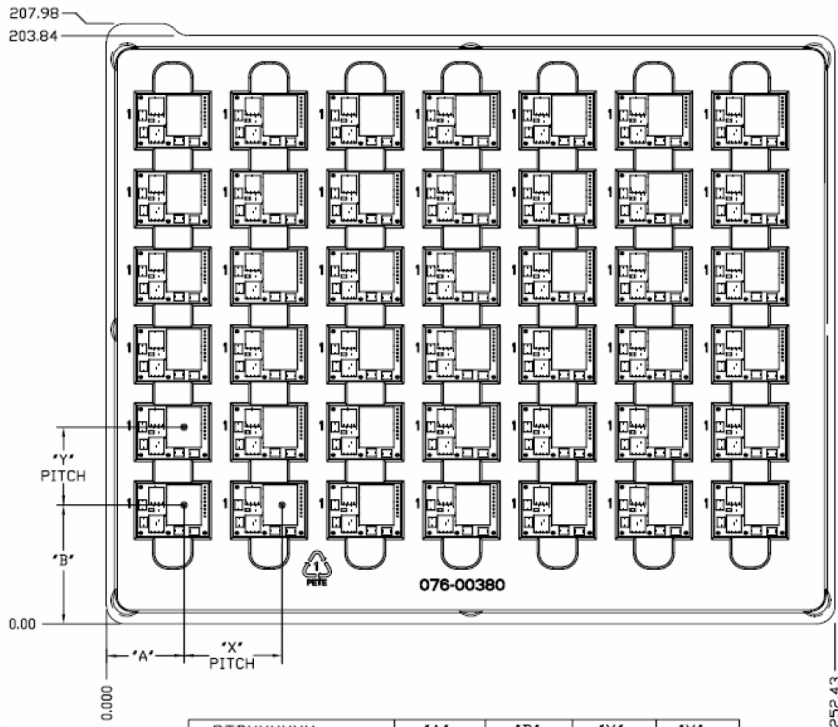
Table 3. PTD08A010W Capacitor Parameters

PTD08A010W Capacitor Parameters			
C (μF)	ESR (mΩ)	ESL (nH)	Quantity
47	1.5	2.5	1

Table 4. PTD08A020W Capacitor Parameters

PTD08A020W Capacitor Parameters			
C (μF)	ESR (mΩ)	ESL (nH)	Quantity
47	1.5	2.5	2

TRAY



NOTE: THE INDUCTOR IS USED TO PICK AND PLACE THE MODULE. IT'S LOCATION MAY VARY FROM PACKAGE STYLE. SEE PRODUCT TABLE

DEVICES/TRAY	42
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PTDXXXXXX	*A*	*B*	*X*	*Y*
PTD08A020	26.83	41.13	34.00	27.00
ALL DIMENSIONS ARE IN MILLIMETER.				

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTD08A020WAD	Active	Production	Through-Hole Module (EGP) 12	42 TIW TRAY	In-Work	SN	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85	
PTD08A020WAD.Z	Active	Production	Through-Hole Module (EGP) 12	42 TIW TRAY	Yes	SN	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

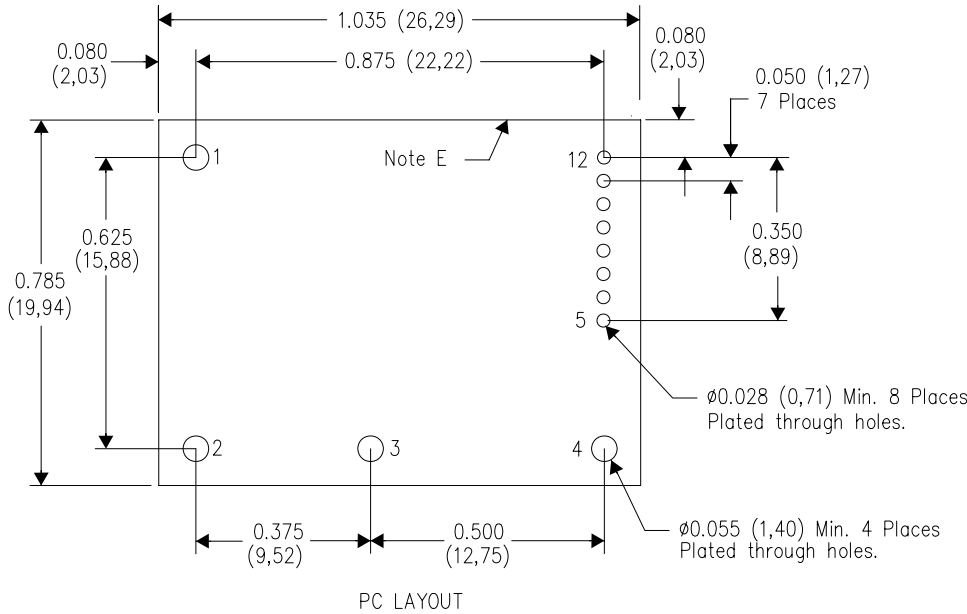
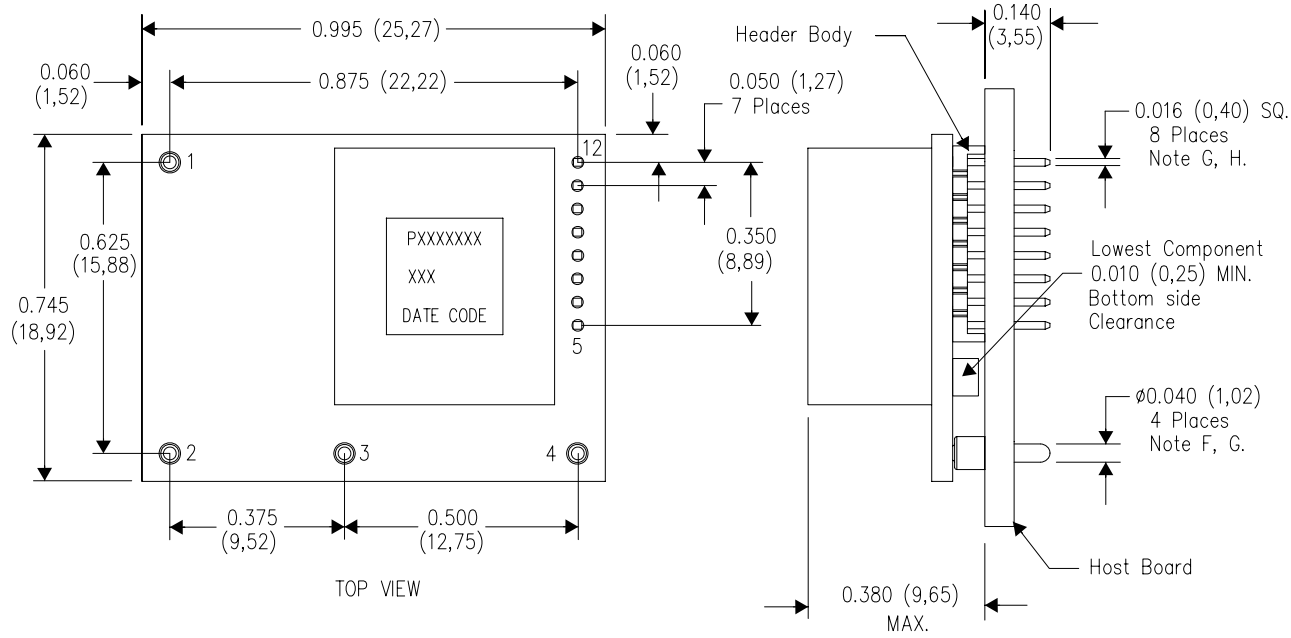
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MECHANICAL DATA

EGP (R-PDSS-T12)

DOUBLE SIDED MODULE



4209185/C 02/10

- NOTES:
- A. All linear dimensions are in inches (mm).
 - B. This drawing is subject to change without notice.
 - C. 2 place decimals are ± 0.030 ($\pm 0,76$ mm).
 - D. 3 place decimals are ± 0.010 ($\pm 0,25$ mm).
 - E. Recommended keep out area for user components.
 - F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
 - G. Header pins are 0.016 (0,40) SQ.
 - H. All pins: Material - Copper Alloy
Finish - Tin (100%) over Nickel plate

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