SCANSTA111 Enhanced SCAN Bridge
Multidrop Addressable IEEE 1149.1 (JTAG) Port

Check for Samples: SCANSTA111

FEATURES

- True IEEE 1149.1 Hierarchical and Multidrop Addressable Capability
- The 7 Slot Inputs Support Up to 121 Unique Addresses, an Interrogation Address, Broadcast Address, and 4 Multi-Cast Group Addresses (Address 000000 is Reserved)
- 3 IEEE 1149.1-Compatible Configurable Local Scan Ports
- Mode Register<sub>0</sub> Allows Local TAPs to be Bypassed, Selected for Insertion Into the Scan Chain Individually, or Serially in Groups of Two or Three
- Transparent Mode can be Enabled with a Single Instruction to Conveniently Buffer the Backplane IEEE 1149.1 Pins to those on a Single Local Scan Port
- LSP ACTIVE Outputs Provide Local Port Enable Signals for Analog Busses Supporting IEEE 1149.4.
- General Purpose Local Port Pass-Through Bits are Useful for Delivering Write Pulses for FPGA Programming or Monitoring Device Status.
- Known Power-Up State
- TRST on All Local Scan Ports
- 32-Bit TCK Counter
- 16-Bit LFSR Signature Compactor
- Local TAPs can become TRI-STATE via the OE Input to Allow an Alternate Test Master to Take Control of the Local TAPs (LSP<sub>0-2</sub> Have a TRI-STATE Notification Output)
- 3.0-3.6V V<sub>CC</sub> Supply Operation
- Power-Off High Impedance Inputs and Outputs
- Supports Live Insertion/Withdrawal

DESCRIPTION

The SCANSTA111 extends the IEEE Std. 1149.1 test bus into a multidrop test bus environment. The advantage of a multidrop approach over a single serial scan chain is improved test throughput and the ability to remove a board from the system and retain test access to the remaining modules. Each SCANSTA111 supports up to 3 local IEEE 1149.1 scan rings which can be accessed individually or combined serially. Addressing is accomplished by loading the instruction register with a value matching that of the Slot inputs. Backplane and inter-board testing can easily be accomplished by parking the local TAP Controllers in one of the stable TAP Controller states via a Park instruction. The 32-bit TCK counter enables built in self test operations to be performed on one port while other scan chains are simultaneously tested.
Table 1. Glossary

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>LFSR</td>
<td>Linear Feedback Shift Register. When enabled, will generate a 16-bit signature of sampled serial test data.</td>
</tr>
<tr>
<td>LSP</td>
<td>Local Scan Port. A four signal port that drives a local (i.e., non-backplane) scan chain (e.g., TCK0, TMS0, TDO0, TDI0).</td>
</tr>
<tr>
<td>Local</td>
<td>Local is used to describe IEEE Std. 1149.1 compliant scan rings and the SCANSTA111 Test Access Port that drives them. The term local was adopted from the system test architecture that the 'STA111 will most commonly be used in; namely, a system test backplane with a 'STA111 on each card driving up to 3 local scan rings per card. (Each card can contain multiple 'STA111s, with 3 local scan ports per 'STA111.)</td>
</tr>
<tr>
<td>Parked/Unparked</td>
<td>Parked, unpark, and unparked, are used to describe the state of the LSP controller and the state of the local TAP controllers (the local TAP controllers refers to the TAP controllers of the scan components that make up a local scan ring). Park is also used to describe the action of parking a LSP (transitioning into one of the Parked LSP controller states). It is important to understand that when a LSP controller is in one of the parked states, TMSn is held constant, thereby holding or parking the local TAP controllers in a given state.</td>
</tr>
<tr>
<td>TAP</td>
<td>Test Access Port as defined by IEEE Std. 1149.1.</td>
</tr>
<tr>
<td>Selected/Unselected</td>
<td>Selected and Unselected refers to the state of the 'STA111 Selection Controller. A selected 'STA111 has been properly addressed and is ready to receive Level 2 protocol. Unselected 'STA111s monitor the system test backplane, but do not accept Level 2 protocol (except for the GOTOWAIT instruction). The data registers and LSPs of unselected 'STA111s are not accessible from the system test master.</td>
</tr>
<tr>
<td>Active Scan Chain</td>
<td>The Active Scan Chain refers to the scan chain configuration as seen by the test master at a given moment. When a 'STA111 is selected with all of its LSPs parked, the active scan chain is the current scan register only. When a LSP is unparked, the active scan chain becomes: TDI0 → the current 'STA111 register → the local scan ring registers → a PAD bit → TDO0. Refer to Table 6 for Unparked configurations of the LSP network.</td>
</tr>
<tr>
<td>Level 1 Protocol</td>
<td>Level 1 is the protocol used to address a 'STA111.</td>
</tr>
<tr>
<td>Level 2 Protocol</td>
<td>Level 2 is the protocol that is used once a 'STA111 is selected. Level 2 protocol is IEEE Std. 1149.1 compliant when an individual 'STA111 is selected.</td>
</tr>
<tr>
<td>PAD</td>
<td>A one bit register that is placed at the end of each local scan port scan-chain. The PAD bit eliminates the prop delay that would be added by the 'STA111 LSPN logic between TDI0 and TDO0 or TDO1 by buffering and synchronizing the LSP TDI inputs to the falling edge of TCK0, thus allowing data to be scanned at higher frequencies without violating setup and hold times.</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit, the right-most position in a register (bit 0).</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit, the left-most position in a register.</td>
</tr>
</tbody>
</table>
ARCHITECTURE

Figure 1 shows the basic architecture of the ‘STA111. The device’s major functional blocks are illustrated here. The TAP Controller, a 16-state state machine, is the central control for the device. The instruction register and various test data registers can be scanned to exercise the various functions of the ‘STA111 (these registers behave as defined in IEEE Std. 1149.1). The ‘STA111 selection controller provides the functionality that allows the 1149.1 protocol to be used in a multi-drop environment. It primarily compares the address input to the slot identification and enables the ‘STA111 for subsequent scan operations. The Local Scan Port Network (LSPN) contains multiplexing logic used to select different port configurations. The LSPN control block contains the Local Scan Port Controllers (LSPC) for each Local Scan Port (LSP0, LSP1 ... LSPn). This control block receives input from the ‘STA111 instruction register, mode registers, and the TAP controller. Each local port contains all four boundary scan signals needed to interface with the local TAPs plus the optional Test Reset signal (TRST).
## PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>No. Pins</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>3</td>
<td>N/A</td>
<td>Power</td>
</tr>
<tr>
<td>GND</td>
<td>3</td>
<td>N/A</td>
<td>Ground</td>
</tr>
<tr>
<td>TMSB</td>
<td>1</td>
<td>I</td>
<td>BACKPLANE TEST MODE SELECT: Controls sequencing through the TAP Controller of the 'STA111. Also controls sequencing of the TAPs which are on the local scan chains. This input has a 25KΩ pull-up resistor and no ESD clamp diode (ESD is controlled with an alternate method). When the device is power-off (VDD floating), this input appears to be a capacitive load to ground(^{(1)}). When VDD = 0V (i.e.; not floating but tied to VSS) this input appears to be a capacitive load with the pull-up to ground.</td>
</tr>
<tr>
<td>TDIb</td>
<td>1</td>
<td>I</td>
<td>BACKPLANE TEST DATA INPUT: All backplane scan data is supplied to the 'STA111 through this input pin. This input has a 25KΩ pull-up resistor and no ESD clamp diode (ESD is controlled with an alternate method). When the device is power-off (VDD floating), this input appears to be a capacitive load to ground(^{(1)}). When VDD = 0V (i.e.; not floating but tied to VSS) this input appears to be a capacitive load with the pull-up to ground.</td>
</tr>
<tr>
<td>TDOb</td>
<td>1</td>
<td>O</td>
<td>BACKPLANE TEST DATA OUTPUT: This output drives test data from the 'STA111 and the local I/O TEST MODE SELECT OUTPUTS: Individual output for each of the local scan ports. TMS is for TDOb, TRIST is for TDO1, etc. This output has 12mA of drive current.</td>
</tr>
<tr>
<td>TCKb</td>
<td>1</td>
<td>I</td>
<td>TEST CLOCK INPUT FROM THE BACKPLANE: This is the master clock signal that controls all scan operations of the 'STA111 and of the local scan ports. This input has no pull-up resistor and no ESD clamp diode (ESD is controlled with an alternate method). When the device is power-off (VDD floating), this input appears to be a capacitive load to ground(^{(2)}). When VDD = 0V (i.e.; not floating but tied to VSS) this input appears to be a capacitive load with the pull-up to ground.</td>
</tr>
<tr>
<td>TRSTb</td>
<td>1</td>
<td>I</td>
<td>TEST RESET: An asynchronous reset signal (active low) which initializes the 'STA111 logic. This input has a 25KΩ pull-up resistor and no ESD clamp diode (ESD is controlled with an alternate method). When the device is power-off (VDD floating), this input appears to be a capacitive load to ground(^{(2)}). When VDD = 0V (i.e.; not floating but tied to VSS) this input appears to be a capacitive load with the pull-up to ground.</td>
</tr>
<tr>
<td>TRIST((B,0-2))</td>
<td>4</td>
<td>O</td>
<td>TRI-STATE NOTIFICATION OUTPUT: This signal is asserted high when the associated TDO is TRI-STATEd. Associated means TRIST B is for TDOb, TRIST I is for TDO1, etc. This output has 12mA of drive current.</td>
</tr>
<tr>
<td>A0</td>
<td>1</td>
<td>I</td>
<td>BACKPLANE PASS-THROUGH INPUT: A general purpose input which is driven to the Yn of a single selected LSP. (Not available when multiple LSPs are selected). This input has an internal pull-up resistor.</td>
</tr>
<tr>
<td>Y0</td>
<td>1</td>
<td>O</td>
<td>BACKPLANE PASS-THROUGH OUTPUT: A general purpose output which is driven from the An of a single selected LSP. (Not available when multiple LSPs are selected). This output has 24mA of drive current.</td>
</tr>
<tr>
<td>S0((0-6))</td>
<td>7</td>
<td>I</td>
<td>SLOT IDENTIFICATION: The configuration of these pins is used to identify (assign a unique address to) each 'STA111 on the system backplane.</td>
</tr>
<tr>
<td>OE</td>
<td>1</td>
<td>I</td>
<td>OUTPUT ENABLE for the Local Scan Ports, active low. When high, this active-low control signal TRI-STATEs all local scan ports on the 'STA111, to enable an alternate resource to access one or more of the three local scan chains.</td>
</tr>
<tr>
<td>TDO((0-2))</td>
<td>3</td>
<td>O</td>
<td>TEST DATA OUTPUTS: Individual output for each of the local scan ports. These outputs have 24mA of drive current.</td>
</tr>
<tr>
<td>TDI((0-2))</td>
<td>3</td>
<td>I</td>
<td>TEST DATA INPUTS: Individual scan data input for each of the local scan ports.</td>
</tr>
<tr>
<td>TMS((0-2))</td>
<td>3</td>
<td>O</td>
<td>TEST MODE SELECT OUTPUTS: Individual output for each of the local scan ports. TMSn does not provide a pull-up resistor (which is assumed to be present on a connected TMS input, per the IEEE 1149.1 requirement). These outputs have 24mA of drive current.</td>
</tr>
<tr>
<td>TCK((0-2))</td>
<td>3</td>
<td>O</td>
<td>LOCAL TEST CLOCK OUTPUTS: Individual output for each of the local scan ports. These are buffered versions of TCKk. These outputs have 24mA of drive current.</td>
</tr>
<tr>
<td>TRST((0-2))</td>
<td>3</td>
<td>O</td>
<td>LOCAL TEST RESETS: A gated version of TRST B. These outputs have 24mA of drive current.</td>
</tr>
<tr>
<td>A((0-1))</td>
<td>2</td>
<td>I</td>
<td>LOCAL PASS-THROUGH INPUTS: General purpose inputs which can be driven to the backplane pin Yn. (Only on LSP0 and LSP1. Only available when a single LSP is selected). These inputs have an internal pull-up resistor.</td>
</tr>
<tr>
<td>Y((0-1))</td>
<td>2</td>
<td>O</td>
<td>LOCAL PASS-THROUGH OUTPUT: General purpose outputs which can be driven from the backplane pin An. (Only on LSP0 and LSP1. Only available when a single LSP is selected). These outputs have 24mA of drive current.</td>
</tr>
</tbody>
</table>

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\(^{(1)}\) Refer to the IBIS model on our website for I/O characteristics.

\(^{(2)}\) Refer to the IBIS model on our website for I/O characteristics.
PIN DESCRIPTIONS (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>No. Pins</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LSP_ACTIVE</td>
<td>(0-2)</td>
<td>O</td>
<td>LOCAL ANALOG TEST BUS ENABLE: These analog pins serve as enable signals for analog busses supporting the IEEE 1149.4 Mixed-Signal Test Bus standard, or for backplane physical layer changes (therefore; TTL to LVDS). These outputs have 12mA of drive current.</td>
</tr>
<tr>
<td>TRIST</td>
<td>(0-2)</td>
<td>O</td>
<td>LOCAL TRI-STATE NOTIFICATION OUTPUTS: This signal is high when the local scan ports are TRI-STATEd. These pins are used for backplane physical layer changes (i.e.; TTL to LVDS). These outputs have 12mA of drive current.</td>
</tr>
<tr>
<td>TEST ENABLE</td>
<td>1</td>
<td>I</td>
<td>TEST ENABLE INPUT: This pin is used for factory test and should be tied to VCC for normal operation.</td>
</tr>
</tbody>
</table>

APPLICATION OVERVIEW

ADDRESSING SCHEME - The SCANSTA111 architecture extends the functionality of the IEEE 1149.1 Standard by supplementing that protocol with an addressing scheme which allows a test controller to communicate with specific 'STA111s within a network of 'STA111s. That network can include both multi-drop and hierarchical connectivity. In effect, the 'STA111 architecture allows a test controller to dynamically select specific portions of such a network for participation in scan operations. This allows a complex system to be partitioned into smaller blocks for testing purposes. The 'STA111 provides two levels of test-network partitioning capability. First, a test controller can select individual 'STA111s, specific sets of 'STA111s (multi-cast groups), or all 'STA111s (broadcast). This 'STA111-selection process is supported by a Level-1 communication protocol. Second, within each selected 'STA111, a test controller can select one or more of the chip's three local scan-ports. That is, individual local ports can be selected for inclusion in the (single) scan-chain which a 'STA111 presents to the test controller. This mechanism allows a controller to select specific terminal scan-chains within the overall scan network. The port-selection process is supported by a Level-2 protocol.

HIERARCHICAL SUPPORT - Multiple SCANSTA111’s can be used to assemble a hierarchical boundary-scan tree. In such a configuration, the system tester can configure the local ports of a set of 'STA111s so as to connect a specific set of local scan-chains to the active scan chain. Using this capability, the tester can selectively communicate with specific portions of a target system. The tester's scan port is connected to the backplane scan port of a root layer of 'STA111s, each of which can be selected using multi-drop addressing. A second tier of 'STA111s can be connected to this root layer, by connecting a local port (LSP) of a root-layer 'STA111 to the backplane port of a second-tier 'STA111. This process can be continued to construct a multi-level scan hierarchy. 'STA111 local ports which are not cascaded into higher-level 'STA111s can be thought of as the terminal leaves of a scan tree. The test master can select one or more target leaves by selecting and configuring the local ports of an appropriate set of 'STA111s in the test tree.

Check with your ATPG tool vendor to ensure support of this feature.

STATE MACHINES

The 'STA111 is IEEE 1149.1-compatible, in that it supports all required 1149.1 operations. In addition, it supports a higher level of protocol, (Level 1), that extends the IEEE 1149.1 Std. to a multi-drop environment.

In multi-drop scan systems, a scan tester can select individual 'STA111s for participation in upcoming scan operations. STA111 selection is accomplished by simultaneously scanning a device address out to multiple 'STA111s. Through an on-chip address matching process, only those 'STA111s whose statically-assigned address matches the scanned-out address become selected to receive further instructions from the scan tester. SCANSTA111 selection is done using a Level-1 protocol, while follow-on instructions are sent to selected 'STA111s by using a Level-2 protocol.

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The 'STA111 contains three distinct but coupled state-machines (see Figure 2). The first of these is the TAP-control state-machine, which is used to drive the 'STA111’s scan ports in conformance with the 1149.1 Standard. The second is the 'STA111-selection state-machine (Figure 3). The third state-machine actually consists of three identical but independent state-machines (see Figure 4), one per 'STA111 local scan port. Each of these scan port selection state-machines allows individual local ports to be inserted into and removed from the 'STA111s overall scan chain.

The 'STA111 selection state-machine performs the address matching which gives the 'STA111 its multi-drop capability. That logic supports single-'STA111 access, multi-cast, and broadcast. The 'STA111-selection state-machine implements the chip’s Level-1 protocol.
The 'STA111’s scan port-configuration state-machine is used to control the insertion of local scan ports into the overall scan chain, or the isolation of local ports from the chain. From the perspective of a system’s (single) scan controller, each 'STA111 presents only one scan chain to the master. The 'STA111 architecture allows one or more of the 'STA111’s local ports to be included in the active scan chain.

Each local port can be parked in one of four stable states (Parked-TLR, Parked-RTI, Parked-Pause-DR or Parked-Pause-IR), either individually or simultaneously with other local ports. Parking a chain removes that local chain from the active scan chain. Conversely, a parked chain can be unparked, causing the corresponding local port to be inserted into the active scan chain.

As shown in Figure 4, the 'STA111’s three scan port-configuration state-machines allow each of the part’s local ports to occupy a different state at any given time. For example, some ports may be parked, perhaps in different states, while other ports participate in scan operations. The state-diagram shows that some state transitions depend on the current state of the TAP-control state-machine. As an example, a local port which is presently in the Parked-RTI state does not become unparked (i.e., enter the Unparked state) until the 'STA111 receives an UNPARK instruction and the 'STA111’s TAP state-machine enters the Run-Test/Idle state.

Similarly, certain transitions of the scan port-configuration state-machine can force the 'STA111’s LSP-control state-machine into specific states. For example, when a local port is in the Unparked state, the 'STA111 receives the PARKRTI instruction and the TAP is transitioned through Run-Test/Idle state, the Local Port controller enters the Parked-RTI state in which TMS_n will be held low until the port is later unparked. Once the Park-RTI instruction has been updated into the instruction register the TAP MUST be transitioned through the Run-Test/Idle state. While TMS_n is held low, all devices on that local scan chain remain in their current TAP State (the RTI TAP controller state in this example).

The 'STA111’s scan port-configuration state-machine implements part of the 'STA111’s Level-2 protocol. In addition, the 'STA111 provides a number of Level-2 instructions for functions other than local scan port configuration. These instructions provide access to and control of various registers within the 'STA111. This set of instructions includes:

- **BYPASS**
- **CNTRSEL**
- **EXTTEST**
- **LFSRON**
- **SAMPLE/PRELOAD**
- **LFSROFF**
- **IDCODE**
- **CNTRON**
- **MODESEL**
- **CNTROFF**
- **MCGRSEL**
- **GOTOWAIT**
- **LFSRSEL**
Figure 5 illustrates how the ‘STA111’s state-machines interact. The ‘STA111-selection state-machine enables or disables operation of the chip's three port-selection state-machines. In ‘STA111s which are selected via Level-1 protocol (either as individual ‘STA111s or as members of broadcast or multi-cast groups), Level-2 protocol commands can be used to park or unpark local scan ports. Note that most transitions of the port-configuration state-machines are gated by particular states of the ‘STA111’s TAP-control state-machine, as shown in Figure 4 or Figure 5.

Following a hardware reset, the TAP controller state-machine is in the Test-Logic-Reset (TLR) state; the ‘STA111-selection state-machine is in the Wait-For-Address state; and each of the three port-selection state-machines is in the Parked-TLR state. The ‘STA111 is then ready to receive Level-1 protocol, followed by Level-2 protocol.
### TESTER/SCANSTA111 INTERFACE

An IEEE 1149.1 system tester sends instructions to a 'STA111 via that 'STA111’s backplane scan-port. Following test logic reset, the 'STA111’s selection state-machine is in the *Wait-For-Address* state. When the 'STA111’s TAP controller is sequenced to the *Shift-IR* state, data shifted in through the TDI_B input is shifted into the 'STA111’s instruction register. Note that prior to successful selection of a 'STA111, data is not shifted out of the instruction register and out through the 'STA111’s TDO_B output, as it is during normal scan operations. Instead, as each new bit enters the instruction register's most-significant bit, data shifted out from the least-significant bit is discarded.

When the instruction register is updated with the address data, the 'STA111’s address-recognition logic compares the seven least-significant bits of the instruction register with the 7-bit assigned address which is statically present on the S(0-6) inputs. Simultaneously, the scanned-in address is compared with the reserved Broadcast and Multi-cast addresses. If an address match is detected, the 'STA111-selection state-machine enters one of the two selected states. If the scanned address does not match a valid single-slot address or one of the reserved broadcast/multi-cast addresses, the 'STA111-selection state-machine enters the *Unselected* state.

Note that the SLOT inputs should not be set to a value corresponding to a multi-cast group, or to the broadcast address. Also note that the single 'STA111 selection process must be performed for all 'STA111s which are subsequently to be addressed in multi-cast mode. This is required because each such device's Multicast Group Register (MCGR) must be programmed with a multi-cast group number, and the MCGR is not accessible to the test controller until that 'STA111 has first entered the *Selected-Single-'STA111* state.

Once a 'STA111 has been selected, Level-2 protocol is used to issue commands and to access the chip's various registers.

### REGISTER SET

The SCANSTA111 includes a number of registers which are used for 'STA111 selection and configuration, scan data manipulation, and scan-support operations. These registers can be grouped as shown in Table 2.

The specific fields and functions of each of these registers are detailed in the section of this document titled Data Register Descriptions.

Note that when any of these registers is selected for insertion into the 'STA111’s scan-chain, scan data enters through that register's most-significant bit. Similarly, data that is shifted out of the register is fed to the scan input of the next-downstream device in the scan-chain.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>BSDL Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction Register</td>
<td>INSTRUCTION</td>
<td>'STA111 addressing and instruction-decode IEEE Std. 1149.1 required register</td>
</tr>
<tr>
<td>Boundary-Scan Register</td>
<td>BOUNDARY</td>
<td>IEEE Std. 1149.1 required register</td>
</tr>
<tr>
<td>Bypass Register</td>
<td>BYPASS</td>
<td>IEEE Std. 1149.1 required register</td>
</tr>
<tr>
<td>Device Identification Register</td>
<td>IDCODE</td>
<td>IEEE Std. 1149.1 optional register</td>
</tr>
<tr>
<td>Multi-Cast Group Register</td>
<td>MCGR</td>
<td>'STA111-group address assignment</td>
</tr>
<tr>
<td>Mode Register_0</td>
<td>MODE</td>
<td>'STA111 local-port configuration and control bits</td>
</tr>
<tr>
<td>Mode Register_1</td>
<td>N/A</td>
<td>'STA111 local-port configuration and control bits (1)(2)</td>
</tr>
<tr>
<td>Mode Register_2</td>
<td>MODE2</td>
<td>'STA111 Shared GPIO configuration bits</td>
</tr>
<tr>
<td>Linear-Feedback Shift Register</td>
<td>LFSR</td>
<td>'STA111 scan-data compaction (signature generation)</td>
</tr>
<tr>
<td>TCK Counter Register</td>
<td>CNTR</td>
<td>Local-port TCK clock-gating (for BIST)</td>
</tr>
<tr>
<td>Dedicated GPIO Register_(0-n)</td>
<td>N/A</td>
<td>'STA111 Dedicated GPIO control bits (2)</td>
</tr>
<tr>
<td>Shared GPIO Register_(0-n)</td>
<td>SGPIOn</td>
<td>'STA111 Shared GPIO control bits</td>
</tr>
</tbody>
</table>

(1) One dedicated and one shared GPIO register exists for each LSP that supports dedicated and/or shared GPIO (maximum of eight shared and eight dedicated GPIO registers).

(2) HDL version only
LEVEL 1 PROTOCOL (ADDRESSING MODES)

Table 3. SCANSTA111 Address Modes

<table>
<thead>
<tr>
<th>Address Type</th>
<th>Hex Address</th>
<th>Binary Address</th>
<th>TDO&lt;sub&gt;B&lt;/sub&gt; State</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direct Address</td>
<td>00 to 39, 40 to 7F, (80 to FF&lt;sup&gt;(1)&lt;/sup&gt;)</td>
<td>00000000 to 01111010 01000000 to 01111111 (10000000 to 11111111)&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>Normal IEEE Std. 1149.1</td>
</tr>
<tr>
<td>Interrogation Address</td>
<td>3A</td>
<td>00111010</td>
<td>Force strong 0' or weak 1' as ones-complement address is shifted out.</td>
</tr>
<tr>
<td>Broadcast Address</td>
<td>3B</td>
<td>00111011</td>
<td>Always TRI-STATEd</td>
</tr>
<tr>
<td>Multi-Cast Group 0</td>
<td>3C</td>
<td>00111100</td>
<td>Always TRI-STATEd</td>
</tr>
<tr>
<td>Multi-Cast Group 1</td>
<td>3D</td>
<td>00111101</td>
<td>Always TRI-STATEd</td>
</tr>
<tr>
<td>Multi-Cast Group 2</td>
<td>3E</td>
<td>00111110</td>
<td>Always TRI-STATEd</td>
</tr>
<tr>
<td>Multi-Cast Group 3</td>
<td>3F</td>
<td>00111111</td>
<td>Always TRI-STATEd</td>
</tr>
</tbody>
</table>

<sup>(1)</sup> Hex addresses 80' to FF' are only available when using the eighth address bit in the HDL version of the SCANSTA111. The Silicon part has seven address lines and will treat the most-significant address bit as a don't care.

The SCANSTA111 supports single and multiple modes of addressing a 'STA111. The single mode selects one 'STA111 and is called Direct Addressing. More than one 'STA111 device can be selected via the Broadcast and Multi-Cast Addressing modes.

DIRECT ADDRESSING: The 'STA111 enters the Wait-For-Address state when:

1. its TAP Controller enters the Test-Logic-Reset state, or
2. its instruction register is updated with the GOTOWAIT instruction (while either selected or unselected).

Each 'STA111 within a scan network must be statically configured with a unique address via its S<sub>(0-6)</sub> inputs. While the 'STA111 controller is in the Wait-For-Address state, data shifted into bits 6 through 0 of the instruction register is compared with the address present on the S<sub>(0-6)</sub> inputs in the Update-IR state. If the seven (7) LSBs of the instruction register match the address on the S<sub>(0-6)</sub> inputs, (see Figure 6) the 'STA111 becomes selected, and is ready to receive Level 2 Protocol (i.e., further instructions). When the 'STA111 is selected, its device identification register is inserted into the active scan chain.

All 'STA111s whose S<sub>(0-6)</sub> address does not match the instruction register address become unselected. An unselected 'STA111 will remain unselected until either its TAP Controller enters the Test-Logic-Reset state, or its instruction register is updated with the GOTOWAIT instruction.

BROADCAST ADDRESSING:

The Broadcast Address allows a tester to simultaneously select all 'STA111s in a test network. This mode is useful in testing systems which contain multiple identical boards. To avoid bus contention between scan-path output drivers on different boards, each 'STA111's TDO<sub>B</sub> buffer is always TRI-STATEd while in Broadcast mode. In this configuration, the on-chip Linear Feedback Shift Register (LFSR) can be used to accumulate a test result signature for each board that can be read back later by direct-addressing each board's 'STA111.

MULTICAST ADDRESSING:

As a way to make the broadcast mechanism more selective, the 'STA111 provides a Multi-cast addressing mode. A 'STA111's multi-cast group register (MCGR) can be programmed to assign that 'STA111 to one of four (4) Multi-Cast groups. When 'STA111s in the Wait-For-Address state are updated with a Multi-Cast address, all 'STA111s whose MCGR matches the Multi-Cast group will become selected. As in Broadcast mode, TDO<sub>B</sub> is always TRI-STATEd while in Multi-cast mode.
Figure 6. Direct Addressing: Device Address Loaded into Instruction Register

Figure 7. Broadcast Addressing: Address Loaded into Instruction Register

Figure 8. Multi-Cast Addressing: Address Loaded into Instruction Register
LEVEL 2 PROTOCOL

Once the SCANSTA111 has been successfully addressed and selected, its internal registers may be accessed via Level-2 Protocol. Level-2 Protocol is compliant to IEEE Std. 1149.1 TAP protocol with one exception: if the STA111 is selected via the Broadcast or Multi-Cast address, TDOB is always TRI-STATED. (The TDOB buffer must be implemented this way to prevent bus contention.) Upon being selected, (i.e., the STA111 Selection controller transitions from the Wait-For-Address state to one of the Selected states), each of the local scan ports (LSP0, LSP1, LSP2) remains parked in one of the following four TAP Controller states: Test-Logic-Reset, Run-Test/Idle, Pause-DR, or Pause-IR and the active scan chain consists of: TDIb through the instruction register (or the IDCODE register) and out through TDOB.

TDIB → Instruction Register → TDOB

The UNPARK instruction (described later) is used to insert one or more local scan ports into the active scan chain. Table 6 describes which local ports are inserted into the chain, and in what order.

LEVEL 2 INSTRUCTION TYPES

There are two types of instructions (reference Table 4):

1. Instructions that insert a STA111 register into the active scan chain so that the register can be captured or updated (BYPASS, SAMPLE/PRELOAD, EXTEST, ID-CODE, MODESEL, MCGRSEL, LFSR-SEL, CNTRSEL).

2. Instructions that configure local ports or control the operation of the linear feedback shift register and counter registers (UNPARK, PARKTRL, PARKRTI, PARK-PAUSE, GOTOWAIT, SOFTRESET, LFSRON, LFSROFF, CNTRON, CNTROFF). These instructions, along with any other yet undefined Op-Codes, will cause the device identification register to be inserted into the active scan chain.

### Table 4. Level 2 Protocol and Op-Codes

<table>
<thead>
<tr>
<th>Instructions</th>
<th>Hex Op-Code</th>
<th>Binary Op-Code</th>
<th>Data Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>BYPASS</td>
<td>FF</td>
<td>1111 1111</td>
<td>Bypass Register</td>
</tr>
<tr>
<td>EXTEST</td>
<td>00</td>
<td>0000 0000</td>
<td>Boundary-Scan Register</td>
</tr>
<tr>
<td>SAMPLE/PRELOAD</td>
<td>81</td>
<td>1000 0001</td>
<td>Boundary-Scan Register</td>
</tr>
<tr>
<td>IDCODE</td>
<td>AA</td>
<td>1010 1010</td>
<td>Device Identification Register</td>
</tr>
<tr>
<td>UNPARK</td>
<td>E7</td>
<td>1110 0111</td>
<td>Device Identification Register</td>
</tr>
<tr>
<td>PARKTLR</td>
<td>C5</td>
<td>1100 0101</td>
<td>Device Identification Register</td>
</tr>
<tr>
<td>PARKRTI</td>
<td>84</td>
<td>1000 0100</td>
<td>Device Identification Register</td>
</tr>
<tr>
<td>PARKPAUSE</td>
<td>C6</td>
<td>1100 0110</td>
<td>Device Identification Register</td>
</tr>
<tr>
<td>GOTOWAIT (1)</td>
<td>C3</td>
<td>1100 0011</td>
<td>Device Identification Register</td>
</tr>
<tr>
<td>MODESEL</td>
<td>8E</td>
<td>1000 1110</td>
<td>Mode Register0</td>
</tr>
<tr>
<td>MODESEL1</td>
<td>82</td>
<td>1000 0010</td>
<td>Mode Register1</td>
</tr>
<tr>
<td>MODESEL2</td>
<td>83</td>
<td>1000 0011</td>
<td>Mode Register2</td>
</tr>
<tr>
<td>MODESEL3</td>
<td>85</td>
<td>1000 0101</td>
<td>Mode Register3</td>
</tr>
<tr>
<td>MCGRSEL</td>
<td>03</td>
<td>0000 0011</td>
<td>Multi-Cast Group Register</td>
</tr>
<tr>
<td>SOFTRESET</td>
<td>88</td>
<td>1000 1000</td>
<td>Device Identification Register</td>
</tr>
<tr>
<td>LFSRSEL</td>
<td>C9</td>
<td>1100 1001</td>
<td>Linear Feedback Shift Register</td>
</tr>
<tr>
<td>LFSRON</td>
<td>0C</td>
<td>0000 1100</td>
<td>Device Identification Register</td>
</tr>
<tr>
<td>LFSROFF</td>
<td>8D</td>
<td>1000 1101</td>
<td>Device Identification Register</td>
</tr>
<tr>
<td>CNTRSEL</td>
<td>CE</td>
<td>1100 1110</td>
<td>32-Bit TCK Counter Register</td>
</tr>
<tr>
<td>CNTRON</td>
<td>0F</td>
<td>0000 1111</td>
<td>Device Identification Register</td>
</tr>
<tr>
<td>CNTROFF</td>
<td>90</td>
<td>1001 0000</td>
<td>Device Identification Register</td>
</tr>
<tr>
<td>DEFAULT_BYPASS (2)</td>
<td>07</td>
<td>0000 0111</td>
<td>Set Bypass_reg as default data register</td>
</tr>
<tr>
<td>TRANSPARENT0</td>
<td>A0</td>
<td>1010 0000</td>
<td>Transparent Enable Register0</td>
</tr>
<tr>
<td>TRANSPARENT1</td>
<td>A1</td>
<td>1010 0001</td>
<td>Transparent Enable Register1</td>
</tr>
<tr>
<td>TRANSPARENT2</td>
<td>A2</td>
<td>1010 0010</td>
<td>Transparent Enable Register2</td>
</tr>
<tr>
<td>TRANSPARENT3</td>
<td>A3</td>
<td>1010 0011</td>
<td>Transparent Enable Register3</td>
</tr>
</tbody>
</table>

(1) All other instructions act on selected STA111s only.

(2) Commands added to HDL version of STA111.
Table 4. Level 2 Protocol and Op-Codes (continued)

<table>
<thead>
<tr>
<th>Instructions</th>
<th>Hex Op-Code</th>
<th>Binary Op-Code</th>
<th>Data Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRANSPARENT4</td>
<td>A4</td>
<td>1010 0100</td>
<td>Transparent Enable Register₄</td>
</tr>
<tr>
<td>TRANSPARENT5</td>
<td>A5</td>
<td>1010 0101</td>
<td>Transparent Enable Register₅</td>
</tr>
<tr>
<td>TRANSPARENT6</td>
<td>A6</td>
<td>1010 0110</td>
<td>Transparent Enable Register₆</td>
</tr>
<tr>
<td>TRANSPARENT7</td>
<td>A7</td>
<td>1010 0111</td>
<td>Transparent Enable Register₇</td>
</tr>
<tr>
<td>DGPIO₀</td>
<td>B0</td>
<td>1011 0000</td>
<td>Dedicated GPIO Register₀</td>
</tr>
<tr>
<td>DGPIO₁</td>
<td>B1</td>
<td>1011 0001</td>
<td>Dedicated GPIO Register₁</td>
</tr>
<tr>
<td>DGPIO₂</td>
<td>B2</td>
<td>1011 0010</td>
<td>Dedicated GPIO Register₂</td>
</tr>
<tr>
<td>DGPIO₃</td>
<td>B3</td>
<td>1011 0011</td>
<td>Dedicated GPIO Register₃</td>
</tr>
<tr>
<td>DGPIO₄</td>
<td>B4</td>
<td>1011 0100</td>
<td>Dedicated GPIO Register₄</td>
</tr>
<tr>
<td>DGPIO₅</td>
<td>B5</td>
<td>1011 0101</td>
<td>Dedicated GPIO Register₅</td>
</tr>
<tr>
<td>DGPIO₆</td>
<td>B6</td>
<td>1011 0110</td>
<td>Dedicated GPIO Register₆</td>
</tr>
<tr>
<td>DGPIO₇</td>
<td>B7</td>
<td>1011 0111</td>
<td>Dedicated GPIO Register₇</td>
</tr>
<tr>
<td>SGPIO₀</td>
<td>B8</td>
<td>1011 1000</td>
<td>Shared GPIO Register₀</td>
</tr>
<tr>
<td>SGPIO₁</td>
<td>B9</td>
<td>1011 1001</td>
<td>Shared GPIO Register₁</td>
</tr>
<tr>
<td>SGPIO₂</td>
<td>BA</td>
<td>1011 1010</td>
<td>Shared GPIO Register₂</td>
</tr>
<tr>
<td>SGPIO₃</td>
<td>BB</td>
<td>1011 1011</td>
<td>Shared GPIO Register₃</td>
</tr>
<tr>
<td>SGPIO₄</td>
<td>BC</td>
<td>1011 1100</td>
<td>Shared GPIO Register₄</td>
</tr>
<tr>
<td>SGPIO₅</td>
<td>BD</td>
<td>1011 1101</td>
<td>Shared GPIO Register₅</td>
</tr>
<tr>
<td>SGPIO₆</td>
<td>BE</td>
<td>1011 1110</td>
<td>Shared GPIO Register₆</td>
</tr>
<tr>
<td>SGPIO₇</td>
<td>BF</td>
<td>1011 1111</td>
<td>Shared GPIO Register₇</td>
</tr>
<tr>
<td>Other Undefined</td>
<td>TBD</td>
<td>TBD</td>
<td>Device Identification Register</td>
</tr>
</tbody>
</table>

LEVEL 2 INSTRUCTION DESCRIPTIONS:

**BYPASS**: The **BYPASS** instruction selects the bypass register for insertion into the active scan chain when the 'STA111 is selected.**

**EXTEST**: The **EXTEST** instruction selects the boundary-scan register for insertion into the active scan chain. The boundary-scan register consists of seven sample only shift cells connected to the S(0-6) and OE inputs. On the 'STA111, the **EXTEST** instruction performs the same function as the **SAMPLE/PRELOAD** instruction, since there aren't any scannable outputs on the device.

**SAMPLE/PRELOAD**: The **SAMPLE/PRELOAD** instruction selects the boundary-scan register for insertion into the active scan chain. The boundary-scan register consists of seven sample only shift cells connected to the S(0-6) and OE inputs.

**IDCODE**: The **IDCODE** instruction selects the device identification register for insertion into the active scan chain. When **IDCODE** is the current active instruction the device identification 0FC0F01F Hex is captured upon exiting the Capture-DR state.

**UNPARK**: This instruction unparks the Local Scan Port Network and inserts it into the active scan chain as configured by Mode Register₀ (and Mode Register₁ in the HDL) (see Table 6). Unparked LSPs are sequenced synchronously with the 'STA111’s TAP controller. When a LSP has been parked in the **Test-Logic-Reset or Run-Test/Idle** state, it will not become unparked until the 'STA111’s TAP Controller enters the Run-Test/Idle state following the **UNPARK** instruction. An LSP which has been parked in **Test-Logic-Reset** will be parked in **Run-Test/Idle** upon update of an **UNPARK** instruction. If an LSP has been parked in one of the stable pause states (Pause-DR or Pause-IR), it will not become unparked until the 'STA111’s TAP Controller enters the respective pause state. (See **Figure 9** through **Figure 12**).

**PARKTLR**: This instruction causes all unparked LSPs to be parked in the **Test-Logic-Reset** TAP controller state and removes the LSP network from the active scan chain. The LSP controllers keep the LSPs parked in the **Test-Logic-Reset** state by forcing their respective TMSₙ output with a constant logic 1 while the LSP controller is in the **Parked-TLR** state (see **Figure 4**).
PARKRTI: This instruction causes all unparked LSPs to be parked in the Run-Test/Idle state. The update of the PARKRTI instruction MUST immediately be followed by a TMSB=0 (to enter the RTI state) in order to assure stability. When a LSP \( n \) is active (unparked), its TMS \( n \) signals follow TMSB and the LSP \( n \) controller state transitions are synchronized with the TAP Controller state transitions of the ‘STA111. When the instruction register is updated with the PARKRTI instruction, TMS \( n \) will be forced to a constant logic 0, causing the unparked local TAP Controllers to be parked in the Run-Test/Idle state. When an LSP \( n \) is parked, it is removed from the active scan chain.

PARKPAUSE: The PARKPAUSE instruction has dual functionality. It can be used to park unparked LSPs or to unpark parked LSPs. The instruction places all unparked LSPs in one of the TAP Controller pause states. A local port does not become parked until the ‘STA111’s TAP Controller is sequenced through Exit1-DR/IR into the Update-DR/IR state. When the ‘STA111 TAP Controller is in the Exit1-DR or Exit1-IR state and TMSB is high, the LSP controller forces a constant logic 0 onto TMSL thereby parking the port in the Pause-DR or Pause-IR state respectively (see Figure 4). Another instruction can then be loaded to reconfigure the local ports or to deselect the ‘STA111 (therefore, MODESEL, GOTOWAIT, and so on).

If the PARKPAUSE instruction is given to a whose LSPs are parked in Pause-IR or Pause-DR, the parked LSPs will become unparked when the ‘STA111’s TAP controller is sequenced into the respective Pause state.

The PARKPAUSE instruction was implemented with this dual functionality to enable backplane testing (interconnect testing between boards) with simultaneous Updates and Captures.

Simultaneous Update and Capture of several boards can be performed by parking LSPs of the different boards in the Pause-DR TAP controller state, after shifting the data to be updated into the boundary registers of the components on each board. The broadcast address is used to select all ‘STA111s connected to the backplane. The PARKPAUSE instruction is scanned into the selected ‘STA111s and the ‘STA111 TAP controllers are sequenced to the Pause-DR state where the LSPs of all ‘STA111s become unparked. The local TAP controllers are then sequenced through the Update-DR, Select-DR, Capture-DR, Exit1-DR, and parked in the Pause-DR state, as the ‘STA111 TAP controller is sequenced into the Update-DR state. When a LSP is parked, it is removed from the active scan chain.

GOTOWAIT: This instruction is used to return all ‘STA111s to the Wait-For-Address state. All unparked LSPs will be parked in the Test-Logic-Reset TAP controller state (see Figure 5).

MODESEL: The MODESEL instruction inserts Mode Register \( _0 \) into the active scan chain. Mode Register \( _0 \) determines the LSPN configuration for a device with up to five (5) LSPs (only three in Silicon). Bit 7 of Mode Register \( _0 \) is a read-only counter status flag.

MODESEL \( _n \): The MODESEL \( _n \) instruction inserts Mode Register \( _n \) (\( n = 1 \) to 3) into the active scan chain. Mode Register \( _n \) determines the LSPN configuration for LSP 5, 6 and 7 (if they exist), and Mode Register \( _c \) determines the Shared GPIO configuration.

MCGRSSEL: This instruction inserts the multi-cast group register (MCGR) into the active scan chain. The MCGR is used to group ‘STA111s into multi-cast groups for parallel TAP sequencing (therefore, to simultaneously perform identical scan operations).

SOFTWARE: This instruction causes all 3 Port configuration controllers (see Figure 4) to enter the Parked-TLR state, which forces TMSB high; this parks each local port in the Test-Logic-Reset state within 5 TCKB cycles.

LFSRSEL: This instruction inserts the linear feedback shift register (LFSR) into the active scan chain, allowing a compacted signature to be shifted out of the LFSR during the Shift-DR state. (The signature is assumed to have been computed during earlier LFSRON shift operations.) This instruction disables the LFSR register’s feedback circuitry, turning the LFSR into a standard 16-bit shift register. This allows a signature to be shifted out of the register, or a seed value to be shifted into it.

LFSRON: Once this instruction is executed, the linear feedback shift register samples data from the active scan path (including all unparked TDI\( _n \)) during the Shift-DR state. Data from the scan path is shifted into the linear feedback shift register and compacted. This allows a serial stream of data to be compressed into a 16-bit signature that can subsequently be shifted out using the LFSRSEL instruction. The linear feedback shift register is not placed in the scan chain during this mode. Instead, the register samples the active scan-chain data as it flows from the LSPN to TDOB.

LFSROFF: This instruction terminates linear feedback shift register sampling. The LFSR retains its current state after receiving this instruction.
**CNTRSEL:** This instruction inserts the 32-bit TCK counter shift register into the active scan chain. This allows the user to program the number of n TCK cycles to send to the parked local ports once the **CNTRON** instruction is issued (e.g., for BIST operations). Note that to ensure completion of countdown, the ‘STA111 should receive at least n TCK pulses.

**CNTRON:** This instruction enables the TCK counter. The counter begins counting down on the first rising edge of TCK following the Update-IR TAP controller state and is decremented on each rising edge of TCK thereafter. When the TCK counter reaches terminal count, 00000000 Hex, TCKn of all parked LSP's is held low. This function overrides Mode Register0 TCK control bit (bit-3).

If the **CNTRON** instruction is issued when the TCK counter is 00000000 (terminal count) the local TCKs of parked LSPs will be gated. The counter will begin counting on the rising edge of TCK when the TCK counter is loaded with a non-zero value following a **CNTRSEL** instruction (see BIST Support in Special Features section for an example).

**CNTROFF:** This instruction disables the TCK counter, and TCKn control is returned to Mode Register0 (bit 3).

**DEFAULT_BYPASS:** This instruction selects the Bypass register to be the default for SCANSTA111 commands that do not explicitly require a data register. The default after RESET is the Device ID register.

---

**Figure 9. Local Scan Port Synchronization from Parked-TLR State**

**Figure 10. Local Scan Port Synchronization from Parked-RTI State**
REGISTER DESCRIPTIONS

INSTRUCTION REGISTER

The instruction shift register is an 8-bit register that is in series with the scan chain whenever the TAP Controller of the SCANSTA111 is in the Shift-IR state. Upon exiting the Capture-IR state, the value XXXXXXX01 is captured into the instruction register, where XXXXXXX represents the value on the S(0-6) inputs. When the STA111 controller is in the Wait-For-Address state, the instruction register is used for STA111 selection via address matching. In addressing individual STA111s, the chip's addressing logic performs a comparison between a statically-configured (hard-wired) value on that STA111's slot inputs, and an address which is scanned into the chip's instruction register. Binary address codes 000000 through 111010 (00 through 3A Hex) are reserved for addressing individual STA111s. Address 3B Hex is for Broadcast mode.

During multi-cast (group) addressing, a scanned-in address is compared against the (previously scanned-in) contents of a STA111's Multi-Cast Group register. Binary address codes 111110 through 111111 (3A through 3F Hex) are reserved for multi-cast addressing, and should not be assigned as STA111 slot-input values.

BOUNDARY-SCAN REGISTER

The boundary-scan register is a sample only shift register containing cells from the S(0-6) and OE inputs. The register allows testing of circuitry external to the STA111. It permits the signals flowing between the system pins to be sampled and examined without interfering with the operation of the on-chip system logic.

The scan chain is arranged as follows:

TDI_B → OE → S_6 → S_5 → S_4 → S_3 → S_2 → S_1 → S_0 → TDO_B

BYPASS REGISTER

The bypass register is a 1-bit register that operates as specified in IEEE Std. 1149.1 once the STA111 has been selected. The register provides a minimum length serial path for the movement of test data between TDI_B and the LSPN. This path can be selected when no other test data register needs to be accessed during a board-level test operation. Use of the bypass register shortens the serial access-path to test data registers located in other components on a board-level test data path.

MULTI-CAST GROUP REGISTER

Multi-cast is a method of simultaneously communicating with more than one selected STA111. The multi-cast group register (MCGR) is a 2-bit register used to determine which multi-cast group a particular STA111 is assigned to. Four addresses are reserved for multi-cast addressing. When a STA111 is in the Wait-For-Address state and receives a multi-cast address, and if that STA111's MCGR contains a matching value for that multi-cast address, the STA111 becomes selected and is ready to receive Level 2 Protocol (i.e., further instructions).

The MCGR is initialized to 00 upon entering the Test-Logic-Reset state.

### Table 5. Multi-Cast Group Register Addressing

<table>
<thead>
<tr>
<th>MCGR Bits 1,0</th>
<th>Hex Address</th>
<th>Binary Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>3C</td>
<td>00111100</td>
</tr>
<tr>
<td>01</td>
<td>3D</td>
<td>00111101</td>
</tr>
<tr>
<td>10</td>
<td>3E</td>
<td>00111110</td>
</tr>
<tr>
<td>11</td>
<td>3F</td>
<td>00111111</td>
</tr>
</tbody>
</table>

The following actions are used to perform multi-cast addressing:

1. Assign all target STA111s to a multi-cast group by writing each individual target STA111's MCGR with the same multi-cast group code (see Table 5). This configuration step must be done by individually addressing each target STA111, using that chip's assigned slot value.
2. Scan out the multi-cast group address through the TDI_B input of all STA111s. Note that this occurs in parallel, resulting in the selection of only those STA111s whose MCGR was previously programmed with the matching multi-cast group code.
MODE REGISTER<sub>0</sub>

Mode Register<sub>0</sub> is an 8-bit data register used primarily to configure the Local Scan Port Network. Mode Register<sub>0</sub> is initialized to 00000001 binary upon entering the Test-Logic-Reset state. Bits 0, 1, 2, and 4 are used for scan chain configuration as described in Table 6. When the UNPARK instruction is executed, the scan chain configuration is as shown in Table 6 below. When all LSPs are parked, the scan chain configuration is TDI<sub>B</sub> → STA111-register → TDO<sub>B</sub>. Bit 3 is used for TCK<sub>n</sub> configuration, see Table 7.

<table>
<thead>
<tr>
<th>Mode Register(s)</th>
<th>Scan Chain Configuration (if unparked)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR0: X000X000</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>MR0: X000X001</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;0&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>MR0: X000X010</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;1&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>MR0: X000X011</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;0&lt;/sub&gt; → PAD → LSP&lt;sub&gt;1&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>MR0: X000X100</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;2&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>MR0: X000X101</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;0&lt;/sub&gt; → PAD → LSP&lt;sub&gt;2&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>MR0: X000X110</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;1&lt;/sub&gt; → PAD → LSP&lt;sub&gt;2&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>MR0: X000X111</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;0&lt;/sub&gt; → PAD → LSP&lt;sub&gt;1&lt;/sub&gt; → PAD → LSP&lt;sub&gt;2&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>MR0: X010X000</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;3&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>MR0: X010X001</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;0&lt;/sub&gt; → PAD → LSP&lt;sub&gt;3&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>MR0: X010X010</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;1&lt;/sub&gt; → PAD → LSP&lt;sub&gt;3&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>MR0: X010X011</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;0&lt;/sub&gt; → PAD → LSP&lt;sub&gt;1&lt;/sub&gt; → PAD → LSP&lt;sub&gt;5&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>MR0: X110X111</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;0&lt;/sub&gt; → PAD → LSP&lt;sub&gt;1&lt;/sub&gt; → PAD → LSP&lt;sub&gt;2&lt;/sub&gt; → PAD → LSP&lt;sub&gt;3&lt;/sub&gt; → PAD → LSP&lt;sub&gt;4&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>MR0: X000X000MR1: XXXX0001 (2)</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;5&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>MR0: X000X001MR1: XXXX0001 (2)</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;0&lt;/sub&gt; → PAD → LSP&lt;sub&gt;5&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>MR0: X000X100MR1: XXXX001 (2)</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;1&lt;/sub&gt; → PAD → LSP&lt;sub&gt;5&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>MR0: X110X111MR1: XXXX001 (2)</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;0&lt;/sub&gt; → PAD → LSP&lt;sub&gt;1&lt;/sub&gt; → PAD → LSP&lt;sub&gt;2&lt;/sub&gt; → PAD → LSP&lt;sub&gt;3&lt;/sub&gt; → PAD → LSP&lt;sub&gt;4&lt;/sub&gt; → PAD → LSP&lt;sub&gt;5&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>MR0: X000X000MR1: XXXX010 (2)</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;6&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>MR0: X110X111MR1: XXXX111 (2)</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → LSP&lt;sub&gt;0&lt;/sub&gt; → PAD → LSP&lt;sub&gt;1&lt;/sub&gt; → PAD → LSP&lt;sub&gt;2&lt;/sub&gt; → PAD → LSP&lt;sub&gt;3&lt;/sub&gt; → PAD → LSP&lt;sub&gt;4&lt;/sub&gt; → PAD → LSP&lt;sub&gt;5&lt;/sub&gt; → PAD → LSP&lt;sub&gt;6&lt;/sub&gt; → PAD → LSP&lt;sub&gt;7&lt;/sub&gt; → PAD → TDO&lt;sub&gt;B&lt;/sub&gt;</td>
</tr>
<tr>
<td>MR0: XXXXXXXXMR1: XXXXXXXX (2)</td>
<td>TDI&lt;sub&gt;B&lt;/sub&gt; → Register → TDO&lt;sub&gt;B&lt;/sub&gt; (Loopback)</td>
</tr>
</tbody>
</table>

(1) In a device with 8 LSPs there are 2<sup>8</sup> possible LSPN configurations: No LSPs, each individual LSP, combinations of 2 to 7 LSPs, and all 8 LSPs.

(2) Mode Register<sub>1</sub> is only available in the HDL version (up to eight LSPs). The Silicon version has three LSPs and uses Mode Register<sub>0</sub> for LSP selection.

<table>
<thead>
<tr>
<th>Bit 3</th>
<th>LSP n</th>
<th>TCK n</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Parked</td>
<td>Stopped</td>
</tr>
<tr>
<td>0</td>
<td>Parked</td>
<td>Free-running</td>
</tr>
<tr>
<td>1</td>
<td>Unparked</td>
<td>Free-running</td>
</tr>
<tr>
<td>0</td>
<td>Unparked</td>
<td>Free-running</td>
</tr>
<tr>
<td>X</td>
<td>Parked-TLR</td>
<td>Stopped after 512 clock pulses</td>
</tr>
</tbody>
</table>
Bit 3 is normally set to logic 0 so that TCK\textsubscript{n} is free-running when the local scan ports are parked in the Parked-RTI, Parked-Pause-DR or Parked-Pause-IR state. When the local ports are parked, bit 3 can be programmed with logic 1, forcing all of the LSP TCK\textsubscript{n}’s to stop. This feature can be used in power sensitive applications to reduce the power consumed by the test circuitry in parts of the system that are not under test. When in the Parked-TLR state, TCK\textsubscript{n} is gated (stopped) after 512 clock pulses have been received on TCK\textsubscript{B} independent of the bit 3 value.

Bit 7 is a status bit for the TCK counter. Bit 7 is only set (logic 1) when the TCK counter is on and has reached terminal count (zero). It is cleared (logic 0) when the counter is loaded following a CNTRSEL instruction. The power-on value for bit 7 is 0.

Bits 5 and 6 are optional in the HDL to support five LSPs with a single Mode Register\textsubscript{0}. A second Mode Register\textsubscript{1} may be added to allow support of up to eight LSPs.

**Table 8. Mode Register\textsubscript{0}**

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
<td>TCK Counter Status</td>
<td>LSP\textsubscript{4}</td>
<td>LSP\textsubscript{3}</td>
<td>TD\textsubscript{B} to TDO\textsubscript{B}</td>
<td>Loopback</td>
<td>TCK Free Running Disable</td>
<td>LSP\textsubscript{2}</td>
<td>LSP\textsubscript{1}</td>
</tr>
<tr>
<td>Used in Silicon</td>
<td>Y</td>
<td>N</td>
<td>N</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Default Value</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

**Table 9. Mode Register\textsubscript{1}**

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>LSP\textsubscript{7}</td>
<td>LSP\textsubscript{6}</td>
</tr>
<tr>
<td>Used in Silicon</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Default Value</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**Table 10. Mode Register\textsubscript{2}**

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
<td>LSP\textsubscript{2}/GPIO\textsubscript{4}</td>
<td>LSP\textsubscript{2}/GPIO\textsubscript{5}</td>
<td>LSP\textsubscript{2}/GPIO\textsubscript{4}</td>
<td>LSP\textsubscript{2}/GPIO\textsubscript{3}</td>
<td>LSP\textsubscript{2}/GPIO\textsubscript{2}</td>
<td>LSP\textsubscript{1}/GPIO\textsubscript{1}</td>
<td>LSP\textsubscript{0}/GPIO\textsubscript{0}</td>
<td></td>
</tr>
<tr>
<td>Used in Silicon</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Default Value</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**DEVICE IDENTIFICATION REGISTER**

The device identification register (IDREG) is a 32-bit register compliant with IEEE Std. 1149.1. When the IDCODE instruction is active, the identification register is loaded with the Hex value upon leaving the Capture-DR state (on the rising edge of the TCK\textsubscript{B}). Refer to the currently available BSDL file on our website for the most accurate Device ID.

**LINEAR FEEDBACK SHIFT REGISTER**

The 'STA111 contains a signature compactor which supports test result evaluation in a multi-chain environment. The signature compactor consists of a 16-bit linear-feedback shift register (LFSR) which can monitor local-port scan data as it is shifted upstream from the 'STA111’s local-port network. Once the LFSR is enabled, the LFSR's state changes in a reproducible way as each local-port data bit is shifted in from the local-port network. When all local-port data has been scanned in, the LFSR contains a 16-bit signature value which can be compared against a signature computed for the expected results vector.

The LFSR uses the following feedback polynomial:

\[
F(x) = x^{16} + x^{12} + x^{3} + x + 1
\]  \hspace{1cm} (1)
This signature compactor is used to compress serial data shifted in from the local scan chain, into a 16-bit
signature. This signature can then be shifted out for comparison with an expected value. This allows users to test
long scan chains in parallel, via Broadcast or Multi-Cast addressing modes, and check only the 16-bit signatures
from each module. The LFSR is initialized with a value of 0000 Hex upon reset.

32-BIT TCK COUNTER REGISTER

The 32-bit TCK counter register enables BIST testing that requires n TCK cycles, to be run on a parked LSP
while another STA111 port is being tested. The CNTRSEL instruction can be used to load a count-down value
into the counter register via the active scan chain. When the counter is enabled (via the CNTRON instruction),
and the LSP is parked, the local TCKs will stop and be held low when terminal count is reached.

The TCK counter is initialized with a value of 00000000 Hex upon reset.

<table>
<thead>
<tr>
<th>BIT</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Input (HDL only)</td>
</tr>
<tr>
<td>6</td>
<td>Input (HDL only)</td>
</tr>
<tr>
<td>5</td>
<td>Input (HDL only)</td>
</tr>
<tr>
<td>4</td>
<td>Input (HDL only)</td>
</tr>
<tr>
<td>3</td>
<td>Output (HDL only)</td>
</tr>
<tr>
<td>2</td>
<td>Output (HDL only)</td>
</tr>
<tr>
<td>1</td>
<td>Output (HDL only)</td>
</tr>
<tr>
<td>0</td>
<td>Output (HDL only)</td>
</tr>
</tbody>
</table>

Table 11. Dedicated GPIO Register

<table>
<thead>
<tr>
<th>BIT</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
</tr>
<tr>
<td>6</td>
<td>Reserved</td>
</tr>
<tr>
<td>5</td>
<td>Reserved</td>
</tr>
<tr>
<td>4</td>
<td>Reserved</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
</tr>
<tr>
<td>2</td>
<td>Input (TDI)</td>
</tr>
<tr>
<td>1</td>
<td>Output (TDO)</td>
</tr>
<tr>
<td>0</td>
<td>Output (TMS)</td>
</tr>
</tbody>
</table>

Table 12. Shared GPIO Register

<table>
<thead>
<tr>
<th>BIT</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
</tr>
<tr>
<td>6</td>
<td>Reserved</td>
</tr>
<tr>
<td>5</td>
<td>Reserved</td>
</tr>
<tr>
<td>4</td>
<td>Reserved</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>Reserved</td>
</tr>
<tr>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

SPECIAL FEATURES

TRANSPARENT MODE

While this mode is activated, the selected LSP n ports will follow the backplane ports. TRSTn is a buffered
version of TRSTB, TCKn is a buffered version of TCKB, TMSn is a buffered version of TMSB, TDOn is a buffered
version of TDIB and TDOB is a buffered version of TDIn. TRISTB and TRISTn are asserted when the state
machine is in either the Shift-DR or Shift-IR states. The unselected LSPs are placed in the PARKTLR state, and
their clocks are gated after 512 TCKB clock cycles.

Transparent Mode is controlled by 8 new instructions, TRANSPARENT0 through TRANSPARENT7. Transparent
Mode overrides any other active mode. When one of the transparent mode instruction is shifted into the
instruction register and the tap controller goes through the UPDATE-IR state, TRSTn will go high, and TMSn will
go low. This will force the targets connected to the LSPn ports to go into the RTI state. Then as the STA111
state machine goes into the RTI state, all of the LSPn signals will follow the back-plane signals. This is identical
to the method that is typically used to unpark an LSP. The STA111 will remain in this mode until a TRSTB is
asserted or a power cycle forces a reset. Once in the Transparent Mode, the STA111 will not be able to be reset
by a 5 TMS high reset.

The sequence of operations to use Transparent Mode on an LSP are as follows (example uses LSP0):

1. IR-Scan the STA111 address into the instruction register (address a STA111).
2. IR-Scan the TRANSPARENT0 instruction to enable Transparent Mode on LSP0. Transparent Mode is
   enabled when the TAP enters the RTI state at the end of this shift operation (TRST0, TDO0, TMS0 and TCK0
   become buffered versions of TRSTB, TDIB, TMSB and TCKB and TDOB becomes a buffered version of TDIB).

   NOTE
   Transparent Mode will persist until the STA111 is reset using TRSTB. The GOTOWAIT and SOFTRESET instructions
   will not work in this mode.
BIST SUPPORT

The sequence of instructions to run BIST testing on a parked SCANSTA111 port is as follows:

1. Pre-load the Boundary register of the device under test if needed.
2. Issue the **CNTRSEL** instruction and initialize (load) the TCK counter to 00000000 Hex. Note that the TCK counter is initialized to 00000000 Hex upon **Test-Logic-Reset**, so this step may not be necessary.
3. Issue the **CNTRON** instruction to the ‘STA111, to enable the TCK counter.
4. Shift the **PARKRTI** instruction into the ‘STA111 instruction register and **BIST** instruction into the instruction register of the device under test. With the counter on (at terminal count) and the LSP parked, the local TCK is gated.
5. Issue the **CNTRSEL** instruction to the ‘STA111.
6. Load the TCK counter (Shift the 32-bit value representing the number of TCKₙ cycles needed to execute the BIST operation into the TCK counter register). The Self test will begin on the rising edge of TCKₙ following the **Update-DR** TAP controller state.
7. Bit 7 of Mode Register₀ can be scanned to check the status of the TCK counter, (**MODESEL** instruction followed by a **Shift-DR**). Bit 7 logic 0 means the counter has not reached terminal count, logic 1 means that the counter has reached terminal count and the BIST operation has completed.
8. Execute the **CNTROFF** instruction.
9. Unpark the LSP and scan out the result of the BIST operation

RESET

Reset operations can be performed at three levels. The highest level resets all ‘STA111 registers and all of the local scan chains of selected and unselected ‘STA111s. This Level 1 reset is performed whenever the ‘STA111 TAP Controller enters the **Test-Logic-Reset** state. **Test-Logic-Reset** can be entered synchronously by forcing TMSₙ high for at least five (5) TCKₙ pulses, or asynchronously by asserting the TRSTₙ pin. A Level 1 reset forces all ‘STA111s into the **Wait-For-Address** state, parks all local scan chains in the **Test-Logic-Reset** state, and initializes all ‘STA111 registers.

The **SOFTRESET** instruction is provided to perform a Level 2 reset of all LSP’s of selected ‘STA111s. **SOFTRESET** forces all TMSₙ signals high, placing the corresponding local TAP Controllers in the **Test-Logic-Reset** state within five (5) TCKₙ cycles.

The third level of reset is the resetting of individual local ports. An individual LSP can be reset by parking the port in the **Test-Logic-Reset** state via the **PARKTLR** instruction. To reset an individual LSP that is parked in one of the other parked states, the LSP must first be unparked via the **UNPARK** instruction.

PORT SYNCHRONIZATION

When a LSP is not being accessed, it is placed in one of the four TAP Controller states: **Test-Logic-Reset**, **Run-Test/Idle**, **Pause-DR**, or **Pause-IR**. The ‘STA111 is able to park a local chain by controlling the local Test Mode Select outputs (TMSₙ₀₋₂) (see Figure 4). TMSₙ is forced high for parking in the **Test-Logic-Reset** state, and forced low for parking in **Run-Test/Idle**, **Pause-IR**, or **Pause-DR** states. Local chain access is achieved by issuing the **UNPARK** instruction. The LSPs do not become unparked until the ‘STA111 TAP Controller is sequenced through a specified synchronization state. Synchronization occurs in the **Run-Test/Idle** state for LSPs parked in **Test-Logic-Reset** or **Run-Test/Idle**; and in the **Pause-DR** or **Pause-IR** state for ports parked in **Pause-DR** or **Pause-IR**, respectively.

Figure 11 and Figure 12 show the waveforms for synchronization of a local chain that was parked in the **Test-Logic-Reset** state. Once the **UNPARK** instruction is received in the instruction register, the LSPC forces TMSₙ low on the falling edge of TCKₙ.
This moves the local chain TAP Controllers to the synchronization state (*Run-Test/Idle*), where they stay until synchronization occurs. If the next state of the 'STA111 TAP Controller is *Run-Test/Idle*, TMS<sub>n</sub> is connected to TMS<sub>B</sub> and the local TAP Controllers are synchronized to the 'STA111 TAP Controller as shown in Figure 12. If the next state after *Update-IR* were *Select-DR*, TMS<sub>n</sub> would remain low and synchronization would not occur until the 'STA111 TAP Controller entered the *Run-Test/Idle* state, as shown in Figure 11.

Each local port has its own Local Scan Port Controller. This is necessary because the LSPN can be configured in any one of eight (8) possible combinations. Either one, some, or all of the local ports can be accessed simultaneously. Configuring the LSPN is accomplished with Mode Register<sub>0</sub>, in conjunction with the UNPARK instruction.

The LSPN can be unparked in one of seven different configurations (Si device), as specified by bits 0-2 of Mode Register<sub>0</sub>. Using multiple ports presents not only the task of synchronizing the 'STA111 TAP Controller with the TAP Controllers of an individual local port, but also of synchronizing the individual local ports to one another.

When multiple local ports are selected for access, it is possible that two ports are parked in different states. This could occur when previous operations accessed the two ports separately and parked them in the two different states. The LSP Controllers handle this situation gracefully. Figure 12 shows the UNPARK instruction being used to access LSP<sub>0</sub>, LSP<sub>1</sub>, and LSP<sub>2</sub> in series (Mode Register<sub>0</sub> = XXX0X111 binary). LSP<sub>0</sub> and LSP<sub>1</sub> become active as the 'STA111 controller is sequenced through the *Run-Test/Idle* state. LSP<sub>2</sub> remains parked in the *Pause-DR* state until the 'STA111 TAP Controller is sequenced through the *Pause-DR* state. At that point, all three local ports are synchronized for access via the active scan chain.
PARAMETERIZED DESIGN (HDL)

In order to support a large number of applications, the ‘STA111 HDL is parameterized as described:

- **Number of Local Scan Ports (LSPs):** The ‘STA111 HDL is able to simulate/synthesize a device that contains from 1 to 8 LSPs. LSP_0 through LSP_4 are controlled via Mode Register_0 and LSP_5 through LSP_7 are controlled via Mode Register_1. The silicon version of the ‘STA111 is synthesized with three LSPs, LSP_0 through LSP_2.

- **Number of Address Pins:** The ‘STA111 has a selectable number of address bits (S_0 - S_n, where n can range from 5 to 7). Addresses 3A through 3F hex are reserved for address interrogation, broadcast and multicast addressing. The silicon version of the ‘STA111 is synthesized with seven address pins.

- **Pass-Through Pins:** Each of the LSPs (0-n) may selectively have or not have Pass-through pins. Pass-through pins are described in more detail below. The silicon version of the ‘STA111 is synthesized with Pass-through pins on LSP_0 and LSP_1.

- **Number/Type of GPIO bits:** The ‘STA111 has both dedicated and shared GPIO (General Purpose I/O). Each dedicated group of GPIO bits supports from 0 to 4 dedicated inputs and 0 to 4 dedicated outputs. There are provisions for specifying the default (power-up) value. TMS_(0-n), TDO_(0-n) and TDI_(0-n) are also dual purpose pins functioning as LSP or GPIO. TMS_n and TDO_n are outputs, TDI_n is an input in the GPIO mode. The silicon version of the ‘STA111 is synthesized with shared GPIO on all three available LSPs. The silicon version of the ‘STA111 does not support dedicated GPIO.

Throughout this datasheet, notations exist to clarify the differences between features available on the Silicon version and the HDL version.

KNOWN POWER-UP STATE

The ‘STA111 has a known power-up condition. This is the same state that the device is in after a TRST reset. This happens at power-up without the presence of a TCK_B.

Reset can also occur via a 5 TMS high reset or a SOFTRESET command.

POWER-OFF HIGH IMPEDANCE INPUTS AND OUTPUTS

The ‘STA111 backplane test port features power-off high impedance inputs and outputs.

The TDI_B, TMS_B, and TRST_B inputs have a 25KΩ pull-up resistor and no ESD clamp diode (ESD is controlled with an alternate method). When the device is power-off (V_DD floating), these inputs appear to be a capacitive load to ground. When V_DD = 0V (i.e.; not floating but tied to V_SS) these inputs appear to be capacitive with the pull-up to ground.

The TCK_B input has no pull-up resistor and no ESD clamp diode (ESD is controlled with an alternate method). When the device is power-off (V_DD floating), the input appears to be a capacitive load to ground. When V_DD = 0V (i.e.; not floating but tied to V_SS) the input appears to be a capacitive load to ground.

When the device is power-off (V_DD = 0V or floating), the TDO_B output appears to be a capacitive load.

TRIST

TRST_B: Assertion of TRST_B will return the device back to its known power-up state.

TRST_n: TRST_n is an output on the LSP side of the ‘STA111. While the LSP state-machine (level 2 protocol) is in the Parked-TLR state the TRST_n pin will be driven low. In all other states the TRST_n pin will be driven high.

PHYSICAL LAYER CHANGES

TRIST for TDO_0 and TDO_n are signals for enabling an external buffer circuit between the ‘STA111 and the backplane/LSP. This would allow, for example, a CMOS-to-LVDS converter to drive an LVDS JTAG backplane test bus. These signals are always driving. A separate TRIST is provided for each LSP to report a TRI-STATE on TDO when the LSP is not in a shift state.
SVF DRIVEN, SELF-CHECKING TEST BENCH

The 'STA111 consists of 3 types of pins, dot1 backplane pins, dot1 LSP pins and support pins. The command interpreter of the test bench is able to translate a limited set of SVF commands to the dot1 backplane pins. The SVF shift commands contain both the stimulus (TDI\textsubscript{B}) and expected response (TDO\textsubscript{B}).

The interpreter is able to parse the following commands: ENDDR, ENDIR, RUNTEST, SDR, SIR, STATE, TRST.

PASS-THROUGH PINS

Each LSP may selectively have two pass-through pins. The pair of pass-through pins consist of an input (A\textsubscript{n}) and an output (Y\textsubscript{n}). The LSP pass-through output (Y\textsubscript{n}) drives the level being received by the backplane pass-through input (A\textsubscript{B}). Conversely, the level on the LSP pass-through input (A\textsubscript{n}) drives the backplane pass-through output (Y\textsubscript{B}).

The Pass-through pins are available only when a single LSP is selected. For each LSP these pins will be enabled when the level 2 protocol state-machine is not in the Parked-TLR state. When not enabled they are TRI-STATED.

LSP GATING

While the LSP state-machine (level 2 protocol) is in the Parked-TLR state, the four LSP signals shall be controlled as shown in Table 13 below. Upon entry into the Parked-TLR state (power-up, reset, PARKTLR or GOTOWAIT) a counter in the LSP state-machine allows 512 TCK\textsubscript{B} clock pulses to occur on TCK\textsubscript{n} before gating. Once gated, TCK\textsubscript{n} will drive a logic 0.

Letting 512 TCK\textsubscript{B} pulses pass through to TCK\textsubscript{n} allows a five high TMS reset to occur on over 100 levels of hierarchy before the 'STA111 gates TCK\textsubscript{n} (for power saving in a free-running clock system).

<table>
<thead>
<tr>
<th>LSP Connection</th>
<th>Drive State</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDO\textsubscript{n}</td>
<td>Pull-up resistor to provide a weak HIGH</td>
</tr>
<tr>
<td>TMS\textsubscript{n}</td>
<td>Pull-up resistor to provide a weak HIGH</td>
</tr>
<tr>
<td>TDI\textsubscript{n}</td>
<td>Pull-up resistor to provide a weak HIGH</td>
</tr>
<tr>
<td>TCK\textsubscript{n}</td>
<td>TCK\textsubscript{B} for 512 pulses, then gated LOW</td>
</tr>
</tbody>
</table>

The 'STA111 does not require that any clock pulses are received on TCK\textsubscript{B} while in the Parked-TLR state.

Setting Bit 3 of Mode Register\textsubscript{0} to 1 gates TCK\textsubscript{n} when in the Parked-RTI, Parked-Pause-DR and Parked-Pause-IR states. Default is free-running (bit 3 = 0). The value stored in bit 3 of Mode Register\textsubscript{0} does not effect the requirement of 512 clock pulses before gating TCK\textsubscript{n} in the Parked-TLR state. (See section on MODE REGISTER\textsubscript{0}).

IEEE 1149.4 SUPPORT

The 'STA111 provides support for a switched analog bus. Each LSP has an unparked-TLR notification pin (LSP\_ACTIVE\textsubscript{0-2}) which is low (0) when the LSP is in Parked-TLR and high (1) otherwise. This signal can be used to enable/disable analog switches external to the 'STA111.

GPIO CONNECTIONS

General Purpose I/O (GPIO) pins are registered inputs and outputs that are parameterized in the HDL. The two types of GPIOs than can be used in the 'STA111 are described in the next two sections. The silicon version of the 'STA111 supports shared GPIO on all three available LSPs. The silicon version of the 'STA111 does not support dedicated GPIO.

DEDICATED: Each LSP supports up to four (4) dedicated inputs and up to four (4) dedicated outputs. These are separate, dedicated GPIO signals controlled by dedicated GPIO registers (one register per LSP). The GPIO outputs are updated during the UPDATE-DR state and the GPIO input values are written to the corresponding GPIO register during the CAPTURE-DR state. Dedicated GPIO operation is not supported in the silicon version of the 'STA111.
LSP SHARED: In the shared mode of operation, the dot1 LSP pins TDI<sub>n</sub>, TDO<sub>n</sub> and TMS<sub>n</sub> pins become GPIO pins. TMS<sub>n</sub> and TDO<sub>n</sub> are outputs, TDIn is an input in the GPIO mode.

The sequence of operations to use shared GPIOs on an LSP are as follows (example uses LSP<sub>n</sub>):

1. IR-Scan the 'STA111 address into the instruction register (address a 'STA111).
2. IR-Scan the MODESEL<sub>3</sub> instruction into the instruction register to select Mode Register<sub>3</sub> (Shared GPIO configuration register) as the data register.
3. DR-Scan 00000001 into Mode Register<sub>3</sub> to enable GPIOs on LSP<sub>n</sub>. The GPIOs will be enabled when the TAP enters the RTI state at the end of this shift operation (TDO<sub>0</sub> and TMS<sub>0</sub> will be forced to logic 0 as defined by the default value in the Shared GPIO Register<sub>0</sub>).
4. IR-Scan the SGPIO<sub>0</sub> instruction into the instruction register to select the Shared GPIO Register<sub>0</sub> as the data register.
5. DR-Scan 00000001 into the Shared GPIO Register<sub>0</sub> to set TDO<sub>0</sub> and TMS<sub>0</sub> to a logic 1 (when TAP enters Update-DR). During this operation, when the TAP enters Capture-DR, the present value on the TDI<sub>0</sub> pin and the values of TDO<sub>0</sub> and TMS<sub>0</sub> (as set by Shared GPIO Register<sub>0</sub>) will be captured into bits 2, 1 and 0 of the shift register and will be scanned out 00000X00 (X = value present on TDI<sub>0</sub> when TAP enters Capture-DR).
6. Step 5 can be repeated to generate waveforms on TDO<sub>n</sub> and TMS<sub>n</sub>. If step 5 was repeated with 00000001 as data, TDO<sub>n</sub> and TMS<sub>n</sub> would be set to a logic 0 (when TAP state = Update-DR) and 00000111 would be scanned out (X = value present on TDI<sub>0</sub> when TAP enters Capture-DR).
7. IR-Scan the GOTOWAIT or SOFTRESET instruction, or generate a TRST<sub>B</sub> reset to disable the GPIOs.

ADDRESS INTERROGATION

The 'STA111 has four states that it can go to from the Wait-For-Address state: Unselected, Singularly-selected, Multi/Broadcast-selected, and Address-interrogation (see Figure 13).

After a reset (or GOTOWAIT command) has been issued, the 'STA111 TAP is sequenced to the Capture-IR state where XXXXXXX01 is loaded into the shift register. Upon entering the Shift-IR state, the instruction register is filled with the address interrogation value (3A hex) which is loaded into the address register as the TAP is sequenced into the Update-IR state. On the next loop through Capture-IR the shift register is loaded with the ones-complement of the slot address. In the Shift-IR state the address interrogation value is loaded into the instruction register. The value presented on TDO<sub>0</sub> will be a wired-and address of all of the 'STA111s on the bus. As this value is being shifted out, each 'STA111 will monitor its TDO<sub>0</sub> to see if it is receiving the same value it is driving. If the device shifts all bits of its ones-complement address and never gets a compare error it will tri-state TDO<sub>0</sub> and go to the Wait-For-Reset state. Alternately, if the device sees a compare error while it is shifting its ones-complement address it will stop shifting its address and tri-state TDO<sub>0</sub> until the next shift operation; during the next Shift-IR operation it will again try to present its address (if the previous instruction was 3A hex) while monitoring TDO<sub>0</sub>.

Shifting 3A hex into the instruction registers of the 'STA111s will continue until all 'STA111s have presented their address. At this time all devices will be waiting to be reset, and if a 3A is shifted into the 'STA111 instruction registers the address read by the tester will be all weak 1s due to all TDO<sub>n</sub>’s being tri-stated. Reading all ones will signal the tester that address interrogation is complete. Since all ones signifies the end of Address-Interrogation, no device can have an address of all zeros (ones-complement).

If at any time, during the address interrogation mode, any other instruction besides 3A hex is shifted into the instruction register, then the 'STA111 will exit the interrogation mode. Also, the 'STA111’s state machine will go to the Wait-For-Address state.

This address interrogation scheme presumes that TDO<sub>B</sub> is capable of driving a weak 1 and that an 'STA111 driving a 0 will overdrive an 'STA111 driving a weak 1.

The following is an example of the Address-Interrogation function. Assume there are three 'STA111s (U1, U2 and U3) on a dot1 backplane with slot addresses 010100, 100000 and 000001 respectively (assuming 6 address pins).

1. The ‘STA111s are reset and the interrogation address/op-code (3A hex) is shifted into the instruction registers.
2. At the end of the instruction shift (Update-IR) the 'STA111 address registers are loaded with 3A hex.
3. The TAPs are sequenced to Capture-IR and the shift registers latch the ones-complement slot addresses (U1=101011, U2=011111 and U3=111110).
4. The TAPs are sequenced to *Shift-IR* and the LSB of the interrogation address is presented on the TDI_B’s. Concurrently, the LSBs of the ones-complement slot addresses are presented on the respective TDO_B’s.

5. The weak 1 being driven on U1 and U2 is overdriven by the 0 from U3. U1 and U2 enter the *Wait-For-Next-Interrogation* state.

6. The shift operation continues and U3 finishes shifting its ones-complement address (111110) out on TDO_B. U3 enters the *Wait-For-Reset* state when the TAP enters *Update-IR*.

7. The TAPs are again sequenced to *Capture-IR* and U1 and U2 shift registers latch the ones-complement addresses (U1=101011, U2=011111).

8. The TAPs are sequenced to *Shift-IR* and the LSB of the interrogation address is presented on the TDI_B’s. Concurrently, the LSBs of the ones-complement addresses are presented on the respective TDO_B’s.

9. Since both U1 and U2 are driving a weak 1 the shift continues.

10. Again U1 and U2 drive weak 1 and the shift continues.

11. U2’s weak 1 is overdriven by U1’s 0 and U2 enters the *Wait-For-Next-Interrogation* state.

12. The shift operation continues and U1 finishes shifting its ones-complement address (101011) out on TDO_B. U1 enters the *Wait-For-Reset* state.

13. The instruction shift operation is repeated and U2 shifts its ones-complement address (011111) out on TDO_B. U2 enters the *Wait-For-Reset* state.

14. The instruction shift operation is repeated, however, all devices have been interrogated and are waiting for a reset. The master device will receive all ones. This implies that there can not be an STA111 with address 0!

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**Figure 13. Address Interrogation State Machine**

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**ABSOLUTE MAXIMUM RATINGS (1)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V\textsubscript{CC})</td>
<td>−0.3V to +4.0V</td>
</tr>
<tr>
<td>DC Input Diode Current (I\textsubscript{IL})</td>
<td>(V_\text{IL} = −0.5V)</td>
</tr>
<tr>
<td>DC Input Voltage (V\textsubscript{I})</td>
<td>−0.5V to +3.9V</td>
</tr>
<tr>
<td>DC Output Diode Current (I\textsubscript{OL})</td>
<td>(V_\text{OL} = −0.5V)</td>
</tr>
<tr>
<td>DC Output Voltage (V\textsubscript{O})</td>
<td>−0.3V to +3.9V</td>
</tr>
<tr>
<td>DC Output Source/Sink Current (I\textsubscript{O})</td>
<td>±50 mA</td>
</tr>
<tr>
<td>DC V\textsubscript{CC} or Ground Current per Output Pin</td>
<td>±50 mA</td>
</tr>
<tr>
<td>DC Latchup Source or Sink Current</td>
<td>±300 mA</td>
</tr>
<tr>
<td>Junction Temperature (Plastic)</td>
<td>+150°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (Solder, 4sec)</td>
<td>49L BGA 235°C</td>
</tr>
<tr>
<td>Max Pkg Power Capacity @ 25°C</td>
<td>49L BGA 1.47 W</td>
</tr>
<tr>
<td>Thermal Resistance (θ\textsubscript{JA})</td>
<td>49L BGA 85°C/W</td>
</tr>
<tr>
<td>Package Derating</td>
<td>49L BGA 11.8 mW/°C above 25°C</td>
</tr>
<tr>
<td>ESD Last Passing Voltage (Min)</td>
<td>I/O 2000V</td>
</tr>
<tr>
<td></td>
<td>Inputs 1000V</td>
</tr>
</tbody>
</table>

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

**RECOMMENDED OPERATING CONDITIONS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V\textsubscript{CC})</td>
<td>3.0V to 3.6V</td>
</tr>
<tr>
<td>Input Voltage (V\textsubscript{I})</td>
<td>0V to V\textsubscript{CC}</td>
</tr>
<tr>
<td>Output Voltage (V\textsubscript{O})</td>
<td>0V to V\textsubscript{CC}</td>
</tr>
<tr>
<td>Operating Temperature (T\textsubscript{A})</td>
<td>Industrial −40°C to +85°C</td>
</tr>
</tbody>
</table>

**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating supply voltage and temperature ranges unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_\text{IH})</td>
<td>Minimum High Input Voltage</td>
<td>(V_{\text{OUT}} = 0.1V ) or (V_{\text{CC}} −0.1V)</td>
<td>2.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_\text{IL})</td>
<td>Maximum Low Input Voltage</td>
<td>(V_{\text{OUT}} = 0.1V ) or (V_{\text{CC}} −0.1V)</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{OH}})</td>
<td>Minimum High Output Voltage (\text{TDQ}<em>{\text{B}}, \text{TCK}</em>{\text{B}}, \text{TMS}<em>{\text{B}}, \text{TDQ}</em>{\text{O}})</td>
<td>(I_{\text{OUT}} = −100\mu A)</td>
<td>(V_{\text{IN}} (\text{TDL}<em>{\text{B}}, \text{TMS}</em>{\text{B}}, \text{TCK}<em>{\text{B}}) = V</em>{\text{IH}})</td>
<td>(V_{\text{CC}} − 0.2V)</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{OL}})</td>
<td>Minimum Low Output Voltage (\text{TDQ}<em>{\text{B}}, \text{TCK}</em>{\text{B}}, \text{TMS}<em>{\text{B}}, \text{TDQ}</em>{\text{O}})</td>
<td>(I_{\text{OUT}} = −24mA, V_{\text{IN}} ) on (S_{\text{O}}) &amp; (TDI_{\text{B}}) &amp; (V_{\text{TH}}), (V_{\text{IL}}) All Outputs Loaded</td>
<td>2.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{DH}})</td>
<td>Minimum High Output Voltage (\text{TRIST}<em>{\text{B}}, \text{TRIST}</em>{\text{O}})</td>
<td>(I_{\text{OUT}} = −100\mu A)</td>
<td>(V_{\text{CC}} − 0.2V)</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{DL}})</td>
<td>Minimum Low Output Voltage (\text{TRIST}<em>{\text{B}}, \text{TRIST}</em>{\text{O}}, \text{LSP_ACTIVE}_{\text{O}})</td>
<td>(I_{\text{OUT}} = −12mA, ) All Outputs Loaded</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{OL}})</td>
<td>Maximum Low Output Voltage (\text{TDQ}<em>{\text{B}}, \text{TCK}</em>{\text{B}}, \text{TMS}<em>{\text{B}}, \text{TDQ}</em>{\text{O}})</td>
<td>(I_{\text{OUT}} = +100\mu A, V_{\text{IN}} (\text{TDL}<em>{\text{B}}, \text{TMS}</em>{\text{B}}, \text{TCK}<em>{\text{B}}) = V</em>{\text{IL}})</td>
<td>0.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{OH}})</td>
<td>Maximum Low Output Voltage (\text{TDQ}<em>{\text{B}}, \text{TCK}</em>{\text{B}}, \text{TMS}<em>{\text{B}}, \text{TDQ}</em>{\text{O}})</td>
<td>(I_{\text{OUT}} = +24mA, V_{\text{IN}} ) on (S_{\text{O}}) &amp; (TDI_{\text{B}}) &amp; (V_{\text{IH}}), (V_{\text{IL}}) All Outputs Loaded</td>
<td>0.55</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>
### DC ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating supply voltage and temperature ranges unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{OL}</td>
<td>Maximum Low Output Voltage (TRIST_B, TRIST(0-2), Y_B)</td>
<td>I_{OUT} = +100 \mu A</td>
<td>0.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{OL}</td>
<td>Maximum Low Output Voltage (TRIST_B, TRIST(0-2), LSP_ACTIVE(0-2))</td>
<td>I_{OUT} = +12 mA All Outputs Loaded</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_{IN}</td>
<td>Maximum Input Leakage Current (TCK_B, S(0-6))</td>
<td>V_{IN} = V_{CC} or GND</td>
<td>±5.0</td>
<td>\mu A</td>
<td></td>
</tr>
<tr>
<td>I_{CC}</td>
<td>Maximum Quiescent Supply Current</td>
<td>TDI_B, TMS_B, TRST_B, TDI(0-2) = V_{CC} or GND</td>
<td>1.65</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_{CCD}</td>
<td>Maximum Dynamic Supply Current</td>
<td></td>
<td>130</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_{OFF}</td>
<td>Power Off Leakage Current</td>
<td>TDO_B, TCK(0-2), TMS(0-2), TDO(0-2), TRST(0-2)</td>
<td>V_{CC} = GND, V_{IN} = 3.6V</td>
<td>±5.0</td>
<td>\mu A</td>
</tr>
<tr>
<td>I_{ILR}</td>
<td>TDI(0-2), TDI_B, OE, TRST_B, A(0-1), A_B, TMS_B</td>
<td>V_{IN} = GND</td>
<td>-45</td>
<td>-180</td>
<td>\mu A</td>
</tr>
<tr>
<td>I_{IN}</td>
<td>TDI(0-2), TDI_B, OE, TRST_B, A(0-1), A_B, TMS_B</td>
<td>V_{IN} = V_{CC}</td>
<td>+5.0</td>
<td>\mu A</td>
<td></td>
</tr>
<tr>
<td>I_{OZ}</td>
<td>Maximum TRI-STATE Leakage Current</td>
<td>V_{IN} (OE) = V_{IH}, V_{IN} (TRST_B) = V_{IL}, V_{O} = V_{CC}, GND</td>
<td>±5.0</td>
<td>\mu A</td>
<td></td>
</tr>
</tbody>
</table>

### AC ELECTRICAL CHARACTERISTICS

Over recommended operating supply voltage and temperature ranges unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{PHL1}, t_{PLH1}</td>
<td>Propagation Delay TCK_B to TCK(0-2)</td>
<td></td>
<td>8.0</td>
<td>12.0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{PHL2}, t_{PLH2}</td>
<td>Propagation Delay TCK_B to TDO(0-2)</td>
<td></td>
<td>11.5</td>
<td>16.0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{PLH3}</td>
<td>Propagation Delay TRST_B to TMS_B</td>
<td></td>
<td>13.5</td>
<td>19.0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{PLH4}</td>
<td>Propagation Delay TRST_B to TRST(0-2)</td>
<td></td>
<td>13.0</td>
<td>19.0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{PLH5}, t_{PLH5}</td>
<td>Propagation Delay TCK_B to TDO_B</td>
<td></td>
<td>10.5</td>
<td>15.0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{PLH6}, t_{PLH6}</td>
<td>Propagation Delay A_B to Y_B(0-1)</td>
<td></td>
<td>5.0</td>
<td>9.0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{PLH7}, t_{PLH7}</td>
<td>Propagation Delay A(0-1) to Y_B</td>
<td></td>
<td>6.5</td>
<td>10.0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{PLH8}, t_{PLH8}</td>
<td>Propagation Delay TCK_B to LSP_ACTIVE(0-2)</td>
<td></td>
<td>13.0</td>
<td>19.0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{PLH9}, t_{PLH9}</td>
<td>Enable Time TCK_B to TDO(0-2)</td>
<td></td>
<td>12.0</td>
<td>17.0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{PLH10}, t_{PLH10}</td>
<td>Disable Time TCK_B to TDO(0-2)</td>
<td></td>
<td>11.5</td>
<td>16.0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{PLH11}, t_{PLH11}</td>
<td>Propagation Delay TCK_B to TRIST(0-2)</td>
<td></td>
<td>11.5</td>
<td>17.0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{PLH12}, t_{PLH12}</td>
<td>Enable Time TCK_B to TDO_B</td>
<td></td>
<td>12.5</td>
<td>17.0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{PLH13}, t_{PLH13}</td>
<td>Disable Time TCK_B to TDO_B</td>
<td></td>
<td>12.5</td>
<td>17.0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{PLH14}, t_{PLH14}</td>
<td>Propagation Delay TCK_B to TRIST_B</td>
<td></td>
<td>12.5</td>
<td>18.0</td>
<td>ns</td>
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<tr>
<td>t_{PLH15}, t_{PLH15}</td>
<td>Propagation Delay TMS_B to TMS(0-2)</td>
<td></td>
<td>7.0</td>
<td>11.0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{PLH16}, t_{PLH16}</td>
<td>Propagation Delay TDI_B to TDO(0-2)</td>
<td></td>
<td>7.0</td>
<td>11.0</td>
<td>ns</td>
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<tr>
<td>t_{PLH17}, t_{PLH17}</td>
<td>Enable Time OE to TMS(0-2)</td>
<td></td>
<td>7.5</td>
<td>11.0</td>
<td>ns</td>
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<tr>
<td>t_{PLH18}, t_{PLH18}</td>
<td>Disable Time OE to TMS(0-2)</td>
<td></td>
<td>5.0</td>
<td>10.0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{PLH19}, t_{PLH19}</td>
<td>Enable Time OE to TRST(0-2)</td>
<td></td>
<td>8.0</td>
<td>11.0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{PLH20}, t_{PLH20}</td>
<td>Disable Time OE to TRST(0-2)</td>
<td></td>
<td>6.5</td>
<td>10.0</td>
<td>ns</td>
</tr>
</tbody>
</table>
### AC ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating supply voltage and temperature ranges unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PZL19, PZH19} )</td>
<td>Enable Time ( \overline{OE} ) to ( TDO ) ((0-2))</td>
<td></td>
<td></td>
<td>8.5</td>
<td>12.0</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{PLZ19, PHL19} )</td>
<td>Disable Time ( \overline{OE} ) to ( TDO ) ((0-2))</td>
<td></td>
<td></td>
<td>7.5</td>
<td>12.0</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{PHL20, PZH20} )</td>
<td>Propagation Delay ( \overline{OE} ) to ( \text{TRIST} ) ((0-2))</td>
<td></td>
<td></td>
<td>8.0</td>
<td>13.0</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{PLZ21, PZL21} )</td>
<td>Enable Time ( \overline{OE} ) to ( TCK ) ((0-2))</td>
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<td></td>
<td>7.5</td>
<td>11.0</td>
<td>ns</td>
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<tr>
<td>( t_{PHL21, PHL21} )</td>
<td>Disable Time ( \overline{OE} ) to ( TCK ) ((0-2))</td>
<td></td>
<td></td>
<td>6.5</td>
<td>10.0</td>
<td>ns</td>
</tr>
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### AC ELECTRICAL CHARACTERISTICS

Over recommended operating supply voltage and temperature ranges unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{S} )</td>
<td>Setup Time, ( TMS ) to ( TCK \uparrow )</td>
<td></td>
<td></td>
<td>2.0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{H} )</td>
<td>Hold Time, ( TMS ) to ( TCK \uparrow )</td>
<td></td>
<td></td>
<td>1.0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{S} )</td>
<td>Setup Time, ( TDI ) to ( TCK \uparrow )</td>
<td></td>
<td></td>
<td>2.0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{H} )</td>
<td>Hold Time, ( TDI ) to ( TCK \uparrow )</td>
<td></td>
<td></td>
<td>1.0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{S} )</td>
<td>Setup Time, ( TDI ) ((0-2)) to ( TCK \uparrow )</td>
<td></td>
<td></td>
<td>1.5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{H} )</td>
<td>Hold Time, ( TDI ) ((0-2)) to ( TCK \uparrow )</td>
<td></td>
<td></td>
<td>1.5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{W} )</td>
<td>Clock Pulse Width, ( TCK ) ((H \text{ or } L))</td>
<td></td>
<td></td>
<td>10.0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{WL} )</td>
<td>Reset Pulse Width, ( \text{TRST} ) ((L))</td>
<td></td>
<td></td>
<td>2.5</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{REC} )</td>
<td>Recovery Time, ( TCK \uparrow ) from ( \text{TRST} )</td>
<td></td>
<td></td>
<td>2.0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( F_{\text{MAX}} )</td>
<td>Maximum Clock Frequency</td>
<td></td>
<td></td>
<td>25.0</td>
<td>MHz</td>
<td></td>
</tr>
</tbody>
</table>
AC LOADING AND WAVEFORMS

![AC Test Circuit Diagram]

**Figure 14.** AC Test Circuit (CL includes probe and jig capacitance)

<table>
<thead>
<tr>
<th>V_I</th>
<th>C_L</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.0V</td>
<td>50 pF</td>
</tr>
</tbody>
</table>

**AC Waveforms**

![AC Waveforms Diagram]

**Figure 15.** Waveforms for an Unparked STA111 in the Shift-DR (IR) TAP Controller State
Figure 16. Reset Waveforms

Figure 17. Output Enable Waveforms
Timing Waveforms
(Input Characteristics; f = 1MHz, \( t_r = t_f = 2.5\, \text{ns} \))

**Figure 18. Waveform for Inverting and Non-inverting Functions**

**Figure 19. TRI-STATE Output High Enable and Disable Times for Logic**

**Figure 20. Propagation Delay, Pulse Width and \( t_{\text{REC}} \) Waveforms**

**Figure 21. TRI-STATE Output Low Enable and Disable Times for Logic**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>( V_{\text{CC}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{IN}(H)} )</td>
<td>2.7 - 3.6V</td>
</tr>
<tr>
<td>( V_{\text{IN}} )</td>
<td>2.7V</td>
</tr>
<tr>
<td>( V_{\text{mi}} )</td>
<td>1.5V</td>
</tr>
<tr>
<td>( V_{\text{mo}} )</td>
<td>1.5V</td>
</tr>
<tr>
<td>( V_x )</td>
<td>( V_{\text{OL}} + 0.3V )</td>
</tr>
<tr>
<td>( V_y )</td>
<td>( V_{\text{OH}} - 0.3V )</td>
</tr>
</tbody>
</table>

**CAPACITANCE & I/O CHARACTERISTICS**


**REVISION HISTORY**

April, 2013 – Changed layout of National Data Sheet to TI format.

February, 2010 – Revisions to clarify shared GPIO operation in the silicon version. No specification changes or changes to operation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (3)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCANSTA111MT</td>
<td>NRND</td>
<td>TSSOP</td>
<td>DGG</td>
<td>48</td>
<td>38</td>
<td>Non-RoHS &amp; Green</td>
<td>Call TI</td>
<td>Level-2-235C-1 YEAR</td>
<td>-40 to 85</td>
<td>SCANSTA111MT</td>
<td></td>
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<tr>
<td>SCANSTA111MT NOPB</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>DGG</td>
<td>48</td>
<td>38</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>SCANSTA111MT</td>
<td>Samples</td>
</tr>
<tr>
<td>SCANSTA111MTX NOPB</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>DGG</td>
<td>48</td>
<td>1000</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>SCANSTA111MT</td>
<td>Samples</td>
</tr>
<tr>
<td>SCANSTA111SM</td>
<td>NRND</td>
<td>NFBGA</td>
<td>NZA</td>
<td>49</td>
<td>416</td>
<td>Non-RoHS &amp; Green</td>
<td>Call TI</td>
<td>Level-3-235C-168 HR</td>
<td>-40 to 85</td>
<td>SCANSTA111 SM</td>
<td>Samples</td>
</tr>
<tr>
<td>SCANSTA111SMX NOPB</td>
<td>ACTIVE</td>
<td>NFBGA</td>
<td>NZA</td>
<td>49</td>
<td>2000</td>
<td>RoHS &amp; Green</td>
<td>SNAGCU</td>
<td>Level-4-260C-72 HR</td>
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<td>SCANSTA111 SM</td>
<td>Samples</td>
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<tr>
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<td>NRND</td>
<td>NFBGA</td>
<td>NZA</td>
<td>49</td>
<td>2000</td>
<td>Non-RoHS &amp; Green</td>
<td>Call TI</td>
<td>Level-3-235C-168 HR</td>
<td>-40 to 85</td>
<td>SCANSTA111 SM</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE**: Product device recommended for new designs.

**LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.

**OBsolete**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.**: The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

---

### REEL DIMENSIONS

- **Reel Diameter**
- **Reel Width (W1)**

### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Pocket Quadrants**
- **Sprocket Holes**
- **User Direction of Feed**

---

### Pack Materials - Page 1

---

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<td>TSSOP</td>
<td>DGG</td>
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<td>330.0</td>
<td>24.4</td>
<td>8.6</td>
<td>13.2</td>
<td>1.6</td>
<td>12.0</td>
<td>24.0</td>
<td>Q1</td>
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<tr>
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<td>NFBGA</td>
<td>NZA</td>
<td>49</td>
<td>2000</td>
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<td>7.3</td>
<td>7.3</td>
<td>2.1</td>
<td>12.0</td>
<td>16.0</td>
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<td>330.0</td>
<td>16.4</td>
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<td>7.3</td>
<td>2.1</td>
<td>12.0</td>
<td>16.0</td>
<td>Q1</td>
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</tbody>
</table>

*All dimensions are nominal*
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

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<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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<td>2000</td>
<td>356.0</td>
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<td>35.0</td>
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</tbody>
</table>
## TUBE

*T - Tube height

*L - Tube length

*W - Tube width

*B - Alignment groove width

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Name</th>
<th>Package Type</th>
<th>Pins</th>
<th>SPQ</th>
<th>L (mm)</th>
<th>W (mm)</th>
<th>T (µm)</th>
<th>B (mm)</th>
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<td>SCANSTA111MT</td>
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<td>38</td>
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<td>10</td>
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<tr>
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<td>DGG</td>
<td>TSSOP</td>
<td>48</td>
<td>38</td>
<td>495</td>
<td>10</td>
<td>2540</td>
<td>5.79</td>
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<td>SCANSTA111MT/NOPB</td>
<td>DGG</td>
<td>TSSOP</td>
<td>48</td>
<td>38</td>
<td>495</td>
<td>10</td>
<td>2540</td>
<td>5.79</td>
</tr>
</tbody>
</table>
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Name</th>
<th>Package Type</th>
<th>Pins</th>
<th>SPQ</th>
<th>Unit array matrix</th>
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<th>L (mm)</th>
<th>W (mm)</th>
<th>KO (µm)</th>
<th>P1 (mm)</th>
<th>CL (mm)</th>
<th>CW (mm)</th>
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<td>NFBGA</td>
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<td>416</td>
<td>13 X 32</td>
<td>150</td>
<td>322.6</td>
<td>135.9</td>
<td>7620</td>
<td>9.4</td>
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<tr>
<td>SCANSTA111SM/NOPB</td>
<td>NZA</td>
<td>NFBGA</td>
<td>49</td>
<td>416</td>
<td>13 X 32</td>
<td>150</td>
<td>322.6</td>
<td>135.9</td>
<td>7620</td>
<td>9.4</td>
<td>11.8</td>
<td>11.55</td>
</tr>
</tbody>
</table>
MECHANICAL DATA

NZA0049A

DIMENSIONS ARE IN MILLIMETERS

SLC49A (Rev B)
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
8. Board assembly site may have different recommendations for stencil design.
NOTES:  
A. All linear dimensions are in millimeters. 
B. This drawing is subject to change without notice. 
C. Body dimensions do not include mold protrusion not to exceed 0.15. 
D. Falls within JEDEC MO-153
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