Currents, conventional P-N junction diodes or Schottky diodes are used to mitigate this issue. Unfortunately the forward voltage drop for these diodes is still considered high (approximately 0.6 V for normal diodes and 0.4 V for Schottky). With 10 A of currents flowing through these diodes, the power dissipation can reach as high as 6 W. This in turn will raise the temperature inside the junction box where these diodes normally reside and reduce module reliability.

The advantage of the SM74611 is that it has a lower forward voltage drop than P-N junction and Schottky diodes. It has a typical average forward voltage drop of 26 mV at 8 A of current. This translates into typical power dissipation of 208 mW, which is significantly lower than the 3.2 W of conventional Schottky diodes. The SM74611 is also footprint and pin compatible with conventional D2PAK Schottky diodes, making it a drop-in replacement in many applications.

装置信息

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SM74611</td>
<td>TO-263 (3)</td>
<td>10.18 mm × 8.41 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

 Typical Application in a Junction Box

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## 4 Revision History

### Changes from Revision A (November 2014) to Revision B

- Added Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ................................................................. 1

### Changes from Original (December 2012) to Revision A

- Added new junction temperature for \( t \leq 1 \) hour ................................................................. 3
- Added Thermal Table .................................................. 4
- Changed typical characteristic curves ........................................... 5
5 Pin Configuration and Functions

![Diagram of KTT Package 3-Pin TO-263 Top View]

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANODE 1&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>I</td>
<td>Connect both of these pins to the negative side of the PV cells</td>
</tr>
<tr>
<td>ANODE 3&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CATHODE 2&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>O</td>
<td>Pin 2 and the DAP are shorted internally. Connect the DAP to the positive side of the PV cells</td>
</tr>
<tr>
<td>DAP&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Pin 1 and Pin 3 must be connected together for proper operation.
(2) Package drawing at the end of datasheet is shown without Pin 2 being trimmed.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC reverse voltage</td>
<td>30</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Forward current</td>
<td>24</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Junction temperature, t ≤ 1 hour</td>
<td>135</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, T&lt;sub&gt;stg&lt;/sub&gt;</td>
<td>–65</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) System must be thermally managed so as not to exceed maximum junction temperature.
6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±1000</td>
<td>V</td>
</tr>
<tr>
<td>±250</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC reverse voltage</td>
<td></td>
<td>28</td>
<td>V</td>
</tr>
<tr>
<td>Junction temperature (T_J)</td>
<td>−40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Forward current</td>
<td>0</td>
<td>15</td>
<td>A</td>
</tr>
</tbody>
</table>

(1) System must be thermally managed so as not to exceed maximum junction temperature

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC (1)</th>
<th>SM74611 KTT (TO-263)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{JA} Junction-to-ambient thermal resistance</td>
<td>40.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{JC(top)} Junction-to-case (top) thermal resistance</td>
<td>42.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{JB} Junction-to-board thermal resistance</td>
<td>23.0</td>
<td>°C/W</td>
</tr>
<tr>
<td>ψ_{JT} Junction-to-top characterization parameter</td>
<td>9.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>ψ_{JB} Junction-to-board characterization parameter</td>
<td>22.0</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{JC(bot)} Junction-to-case (bottom) thermal resistance</td>
<td>0.5</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{F(AVG)} Forward current</td>
<td>I_F = 8 A T_J = 25°C</td>
<td>8</td>
<td>15</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>V_{F(AVG)} Forward voltage</td>
<td>I_F = 8 A T_J = 25°C</td>
<td></td>
<td></td>
<td>26</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>I_F = 15 A T_J = 125°C</td>
<td></td>
<td></td>
<td>695</td>
<td>mW</td>
</tr>
<tr>
<td>P_D Power dissipation</td>
<td>I_F = 8 A T_J = 25°C</td>
<td>208</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T_J = 125°C</td>
<td></td>
<td></td>
<td>450</td>
<td></td>
</tr>
<tr>
<td></td>
<td>−40°C to 125°C(1)</td>
<td></td>
<td></td>
<td>575</td>
<td></td>
</tr>
<tr>
<td>D Duty cycle</td>
<td>I_F = 8 A T_J = 25°C</td>
<td>99.5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T_J = 125°C</td>
<td>96.0%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{R} Reverse leakage current</td>
<td>V_{REVERSE} = 28 V</td>
<td>0.3</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>T_J = 25°C</td>
<td></td>
<td></td>
<td>3.3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>T_J = 125°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Limits −40°C to 125°C apply over the entire junction temperature range for operation. Limits appearing in normal type apply for T_A = T_J = 25°C.
6.6 Typical Characteristics

Figure 1. Average Forward Voltage (Anode to Cathode) Over Temperature

Figure 2. Power Dissipation Over Temperature

Figure 3. Reverse Current Over Temperature (Cathode to Anode)
7 Detailed Description

7.1 Overview
The SM74611 is designed for use as a bypass diode in photovoltaic modules. The SM74611 uses a charge pump to drive an N-channel FET to provide a resistive path for the bypass current to flow.

7.2 Functional Block Diagram

![Block Diagram](image)

7.3 Feature Description
The operational description is described in the following sections. See Figure 4 and Figure 5.

7.3.1 From \( t_0 \) to \( t_1 \)
When cells in the solar panels are shaded, the FET Q1 is off and the bypass current flows through the body diode of the FET as shown on Figure 4. This current produces a voltage drop \( (V_F) \) across ANODE and CATHODE terminal of the bypass diode. During this time, the charge pump circuitry is active and charging capacitor C1 to a higher voltage.

7.3.2 At \( t_1 \)
Once the voltage on the capacitor reaches its predetermined voltage level, the charge pump is disabled and the capacitor voltage is used to drive the FET through the FET driver stage.

7.3.3 From \( t_1 \) to \( t_2 \)
When the FET is active, it provides a low resistive path for the bypass current to flow thus minimizing the power dissipation across ANODE and CATHODE. Because the FET is active, the voltage across the ANODE and CATHODE is too low to operate the charge pump. During this time, the stored charge on C1 is used to supply the controller as well as drive the FET.

7.3.4 At \( t_2 \)
When the voltage on the capacitor C1 reaches its predetermined lower level, the FET driver shuts off the FET. The bypass current will then begin to flow through the body diode of the FET, causing the FET body diode voltage drop of approximately 0.6 V to appear across ANODE and CATHODE. The charge pump circuitry is re-activated and begins charging the capacitor C1. This cycle repeats until the shade on the panel is removed and the string current begins to flow through the PV cells instead of the body diode of the FET.
Feature Description (continued)

The key factor to minimizing the power dissipation on the device is to keep the FET on at a high duty cycle. The average forward voltage drop will then be reduced to a much lower voltage than for a Schottky or regular P-N junction diode.

![Graph showing ANODE to CATHODE Voltage (Ch1) With $I_{\text{BYPASS}} = 15$ A (Ch4) for SM74611 in Junction Box at 85°C Ambient]

Figure 5. ANODE to CATHODE Voltage (Ch1) With $I_{\text{BYPASS}} = 15$ A (Ch4) for SM74611 in Junction Box at 85°C Ambient

7.4 Device Functional Modes

7.4.1 FET Q1 OFF

Initially, the internal FET Q1 is OFF. This is between $t_0$ and $t_1$ as shown in Figure 5. When current begins flowing from ANODE to CATHODE, the FET Q1 body diode conducts with a voltage drop $V_F$.

7.4.2 FET Q1 ON

The FET Q1 is ON between $t_1$ and $t_2$ as shown in Figure 5. During this time, the FET gate is driven and current flows through the FET through a low resistive path.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The SM74611 smart bypass diode is a drop-in replacement for traditional bypass diodes used in photovoltaic (PV) applications. When compared to a typical diode, which has a typical 0.7-V drop during forward conduction, the SM74611 dissipates significantly less power and allows PV applications such as solar junction boxes to run much cooler.

8.2 Typical Application
The application diagram shown in Figure 6 shows 3 SM74611 Smart Bypass Diodes connected in series, each providing a bypass path for 8 solar cells for a total of 24 solar cells.

---

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Figure 6. Solar Junction Box
Typical Application (continued)

8.2.1 Design Requirements

Table 1 lists the parameters for Figure 6

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum input voltage $V_{IN_{MIN}}$</td>
<td>1 V</td>
</tr>
<tr>
<td>Maximum input voltage $V_{IN_{MAX}}$</td>
<td>28 V</td>
</tr>
<tr>
<td>Maximum forward current $I_{MAX}$</td>
<td>20 A</td>
</tr>
<tr>
<td>Junction temperature range $T_J$</td>
<td>–40°C to 125°C</td>
</tr>
</tbody>
</table>

8.2.2 Detailed Design Procedure

The SM74611 is primarily used in solar junction boxes to improve the efficiency compared to commonly used P-N junction or Schottky diodes. The junction boxes have 2 or 3 diodes in series connected across the solar panel, each diode connected across a substring of solar cells, as shown in Figure 6. Standard bodies like IEC and UL mandate certain thermal tests for bypass diodes in junction boxes. At the time of this writing, the applicable specifications include IEC61215, IEC61646, EN 50548, IEC62790, and UL3730. The test procedures across these specifications are similar and include the following:

- Apply temperature probe to the diode (in the case of SM74611 the smart bypass diode) body
- Apply 75 ± 50°C to the junction box, containing the 2 to 3 (smart bypass) diodes
- Apply panel-rated, short-circuit current through the box for 1 hour
- Increase the current to 1.25 times the rated value and continue testing for another 1 hour

While the specifications may not specify how the temperature must be maintained, it is expected that there will be no air flow as in a real application behind a solar panel. Also there may be no specification of how the temperature is raised from room to 750°C. TI recommends a gradual and controlled increase to avoid shock to the product under test. Using a good climate chamber or oven is needed to ensure uniformity and consistency of temperature during test and from test of one junction box to another. Similar precautions are also necessary with the thermocouples and temperature probes used during the tests. It is a good idea to check the equipment used with the certification body. The junction box should be operational after these tests. Due to body diode pulses, a simple diode tester cannot be used to test the Smart Bypass Diode. An example testing scheme is shown in Application Curve. To avoid component failure, the Smart Bypass Diode junction temperature must not exceed the maximum rating during these tests. See Absolute Maximum Ratings for the SM74611 limits. The junction temperature is calculated based on the measured values from the temperature probe.

The temperature probe could be applied on the top (plastic case) or bottom (tab) of the SM74611 body, as shown in Figure 7. Methods of applying this probe vary from Kapton tape, 2K-resins (for top) to soldering (bottom tab). It is good to check with the certification body regarding the acceptable method.

Figure 7. Temperature Probe Attachment During Thermal Test
Because the SM74611 Smart Bypass Diode cycles the FET ON and OFF to recharge the charge pump, occasionally the body diode conducts instead of the FET. Therefore the drop across the Smart Bypass Diode is not constant even at constant load. Due to this switching behavior, a normal diode tester cannot be used to test the operation of the Smart Bypass Diode. The following test scheme is provided, as an example, with junction box application consideration. See Figure 8 while reading the following test steps:

**Figure 8. Example Test Setup for SM74611**

**Step 1:** Testing Forward voltage drop (set R such that If => 1 A)
- Toggle S1 to position 1
- Make sure to see If reading of 10V/R
- Measure Voltage across 3 SM74611 or 1 ea SM74611
- If the setup is working properly, Vf will be less than 150 mV (Rdson losses)

**Potential Fault Conditions**
- SM74611 FET is not turning ON -> the measured voltage will be > 500 mV
- SM74611 device is not soldered and open -> No If current is seen

**Step 2:** Testing Reverse voltage turn OFF
- Toggle S1 to position 2
- Measure current Ir which is expected to be < 1 µA

**Potential Fault Conditions**
- SM74611 FET is shorted or board short is present, the measured current Ir is same as If but with reverse polarity. (This is only in the case of testing each SM74611 and not applicable for testing 3 together).
8.2.3 Application Curve

![Application Curve Diagram]

Figure 9. Start-Up Related to Input Voltage from the Panel

9 Power Supply Recommendations

The SM74611 is designed to be implemented as bypass diode in photovoltaic modules. System designer must ensure that the voltage level from solar modules does not exceed 28 V. At the time of this writing, the applicable specifications include IEC61215, IEC61646, EN 50548, IEC62790, and UL3730. This is because the SM74611 can protect against a maximum of –28 V as a bypass diode. The internal MOSFET of SM74611 can pass up to 15-A current. Drawing more current can damage the internal MOSFET permanently.

10 Layout

10.1 Layout Guidelines

Some layout guidelines must be followed to ensure proper conduction from ANODE to CATHODE pins. ANODE and CATHODE traces carrying the load current must be wide to reduce the amount of parasitic trace inductance as shown in Figure 10.

10.2 Layout Example

![Layout Example Diagram]

Figure 10. Layout Example for SM74611
11 Device and Documentation Support

11.1 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks
E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary
SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SM74611KTTR</td>
<td>ACTIVE</td>
<td>DDPAK/TO-263</td>
<td>KTT</td>
<td>3</td>
<td>500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SN</td>
<td>Level-3-245C-168 HR</td>
<td>-40 to 125</td>
<td>SM74611KTT</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A₀</td>
<td>Dimension designed to accommodate the component width</td>
</tr>
<tr>
<td>B₀</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K₀</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P₁</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- Q₁, Q₂, Q₃, Q₄
- Sprocket Holes
- User Direction of Feed

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W₁ (mm)</th>
<th>A₀ (mm)</th>
<th>B₀ (mm)</th>
<th>K₀ (mm)</th>
<th>P₁ (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>SM74611KTTR</td>
<td>DDPAK/TO-263</td>
<td>KTT</td>
<td>3</td>
<td>500</td>
<td>330.0</td>
<td>24.4</td>
<td>10.6</td>
<td>15.8</td>
<td>4.9</td>
<td>16.0</td>
<td>24.0</td>
<td>Q₂</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SM74611KTTR</td>
<td>DDPACK/TO-263</td>
<td>KTT</td>
<td>3</td>
<td>500</td>
<td>340.0</td>
<td>340.0</td>
<td>38.0</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0.13) per side.
⚠️ Falls within JEDEC TO-263 variation AA, except minimum lead thickness and minimum exposed pad length.
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