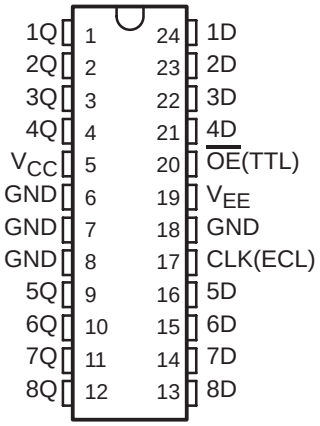
SN10KHT5574
OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS

SDZS010 − JANUARY 1990 − REVISED OCTOBER 1990

- **10KH Compatible**
- **ECL Clock and TTL Control Inputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise**
- **Package Options Include "Small Outline" Packages and Standard Plastic DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The eight flip-flops of the SN10KHT5574 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels that were set up at the D inputs.

A buffered output-enable input ($\overline{OE}$) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable input $\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

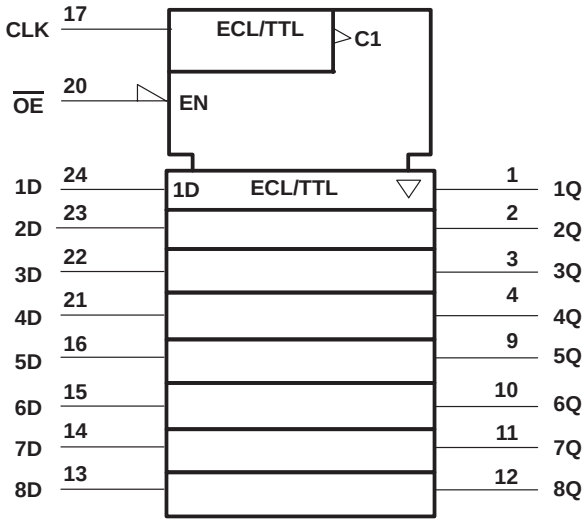
The SN10KHT5574 is characterized for operation from 0°C to 75°C.

FUNCTION TABLE

INPUTS			OUTPUT (TTL)
$\overline{OE}$	CLK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q_0
H	X	X	Z

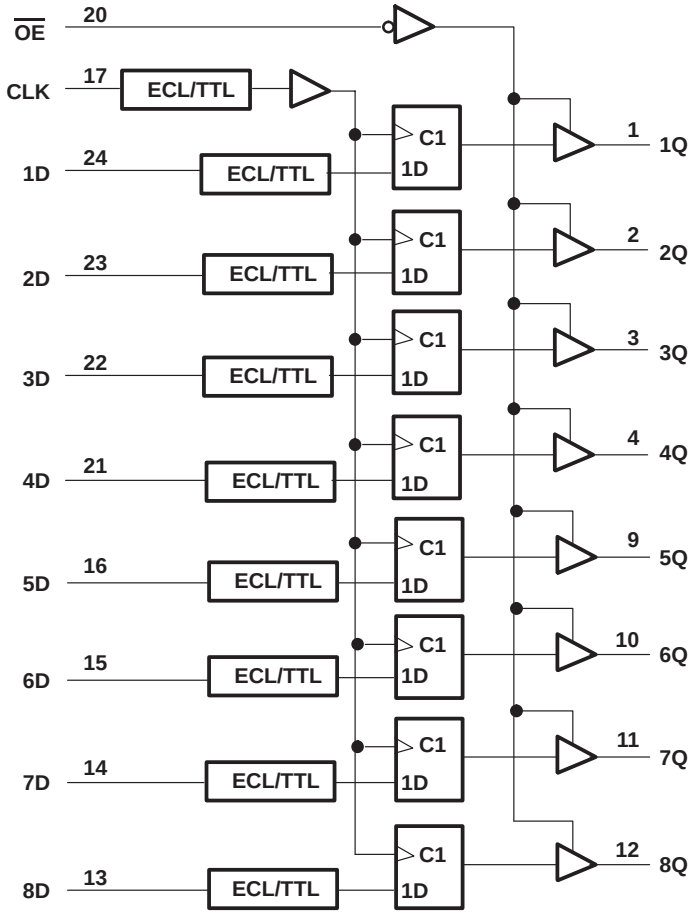
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251−1443

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Supply voltage range, V_{EE} . . . . . −8 V to 0 V
Input voltage range: TTL (see Note 1) . . . . . −1.2 V to 7 V
ECL . . . . . V_{EE} to 0 V
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Input current range, (TTL) . . . . . −30 mA to 5 mA
Current into any output in the low state . . . . . 96 mA
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	TTL supply voltage		4.5	5	5.5	V
V_{EE}	ECL supply voltage		−4.94	−5.2	−5.46	V
V_{IH}	TTL high-level input voltage		2			V
V_{IL}	TTL low-level input voltage				0.8	V
V_{IH}	ECL high-level input voltage‡	T_A = 0°C	−1170		−840	mV
		T_A = 25°C	−1130		−810	
		T_A = 75°C	−1070		−735	
V_{IL}	ECL low-level input voltage‡	T_A = 0°C	−1950		−1480	mV
		T_A = 25°C	−1950		−1480	
		T_A = 75°C	−1950		−1450	
I_{IK}	TTL input clamp current				−18	mA
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current				48	mA
T_A	Operating free-air temperature range		0		75	°C

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{OE}$ only	V_{CC} = 4.5 V,	V_{EE} = −4.94 V,	I_I = −18 mA				−1.2	V
V_{OH}		V_{CC} = 4.5 V,	V_{EE} = −5.2 V ±5%,	I_{OH} = −3 mA		2.4	3.3		V
		V_{CC} = 4.5 V,	V_{EE} = −5.2 V ±5%,	I_{OH} = −15 mA		2	3.1		
V_{OL}		V_{CC} = 4.5 V,	V_{EE} = −5.2 V ±5%,	I_{OL} = 48 mA			0.38	0.55	V
I_I	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 7 V				0.1	mA
I_{IH}	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 2.7 V				20	µA
I_{IL}	$\overline{OE}$ only	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = 0.5 V				−0.5	mA
I_{IH}	Data inputs and CLK	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −840 mV	T_A = 0°C			350	µA
		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −810 mV	T_A = 25°C			350	
		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −735 mV	T_A = 75°C			350	
I_{IL}	Data inputs and CLK	V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_I = −1950 mV	T_A = 0°C	0.5			µA
					T_A = 25°C	0.5			
					T_A = 75°C	0.5			
I_{OZH}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_O = 2.7 V				50	µA
I_{OZL}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_O = 0.5 V				−50	µA
I_{OS}‡		V_{CC} = 5.5 V,	V_{EE} = −5.46 V,	V_O = 0 V		−100		−225	mA
I_{CCH}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				66	95	mA
I_{CCL}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				76	110	mA
I_{CCZ}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				74	106	mA
I_{EE}		V_{CC} = 5.5 V,	V_{EE} = −5.46 V				−43	−61	mA
C_i		V_{CC} = 5.5 V,	V_{EE} = −5.2 V,	f = 10 MHz			5		pF
C_o		V_{CC} = 5.5 V,	V_{EE} = −5.2 V,	f = 10 MHz			7		pF

† All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements

			V_{CC} = 4.5 V to 5.5 V, V_{EE} = −4.94 V to −5.46 V, T_A = MIN to MAX§		UNIT
			MIN	MAX	
t_w	Pulse duration	CLK high	4		ns
		CLK low	4		
t_{su}	Setup time before CLK↑	Data high	1		ns
		Data low	1		
t_h	Hold time after CLK↑	Data high	1		ns
		Data low	1		

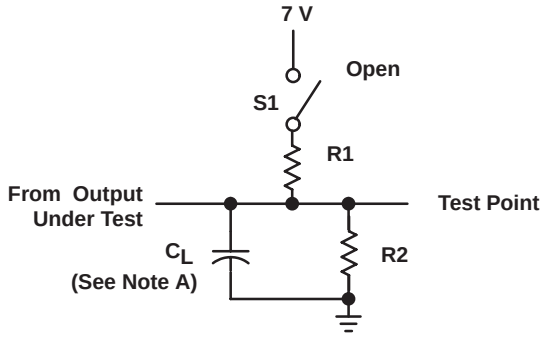
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
f_{max}			200	300		MHz
t_{PLH}	CLK	Q	2.3	4.1	7	ns
t_{PHL}			2.9	4.6	7.4	
t_{PZH}	$\overline{OE}$	Q	1.9	3.6	6.3	ns
t_{PZL}			2.7	4.8	7.7	
t_{PHZ}	$\overline{OE}$	Q	2.1	3.9	6.1	ns
t_{PLZ}			0.5	3.4	6.3	

† All typical values are at V_{CC} = 5 V, V_{EE} = −5.2 V, T_A = 25°C.

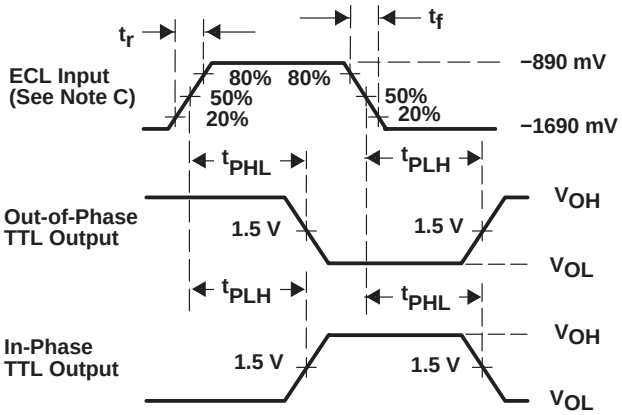
PARAMETER MEASUREMENT INFORMATION



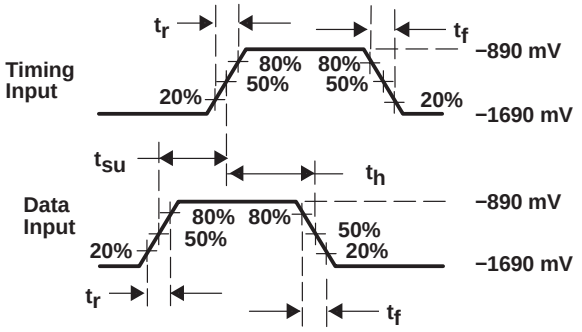
LOAD CIRCUIT

SWITCH POSITION TABLE

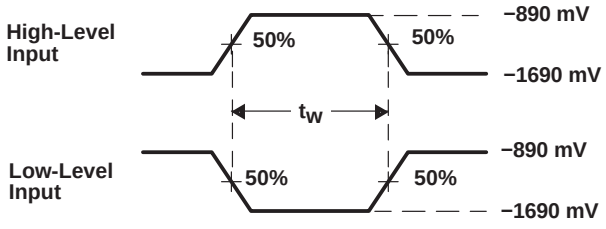
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



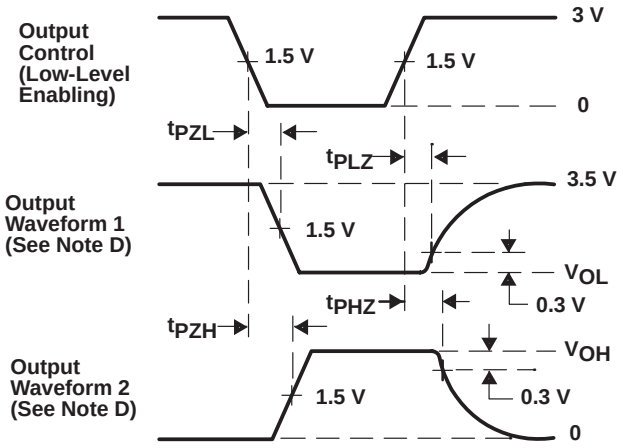
VOLTAGE WAVEFORMS
ECL-INPUT PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
TTL ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. For TTL inputs, input pulses are supplied by generators having the following characteristics PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 1.5 ns, t_f ≤ 1.5 ns.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load circuit and voltage waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN10KHT5574DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	10KHT5574	Samples
SN10KHT5574DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	10KHT5574	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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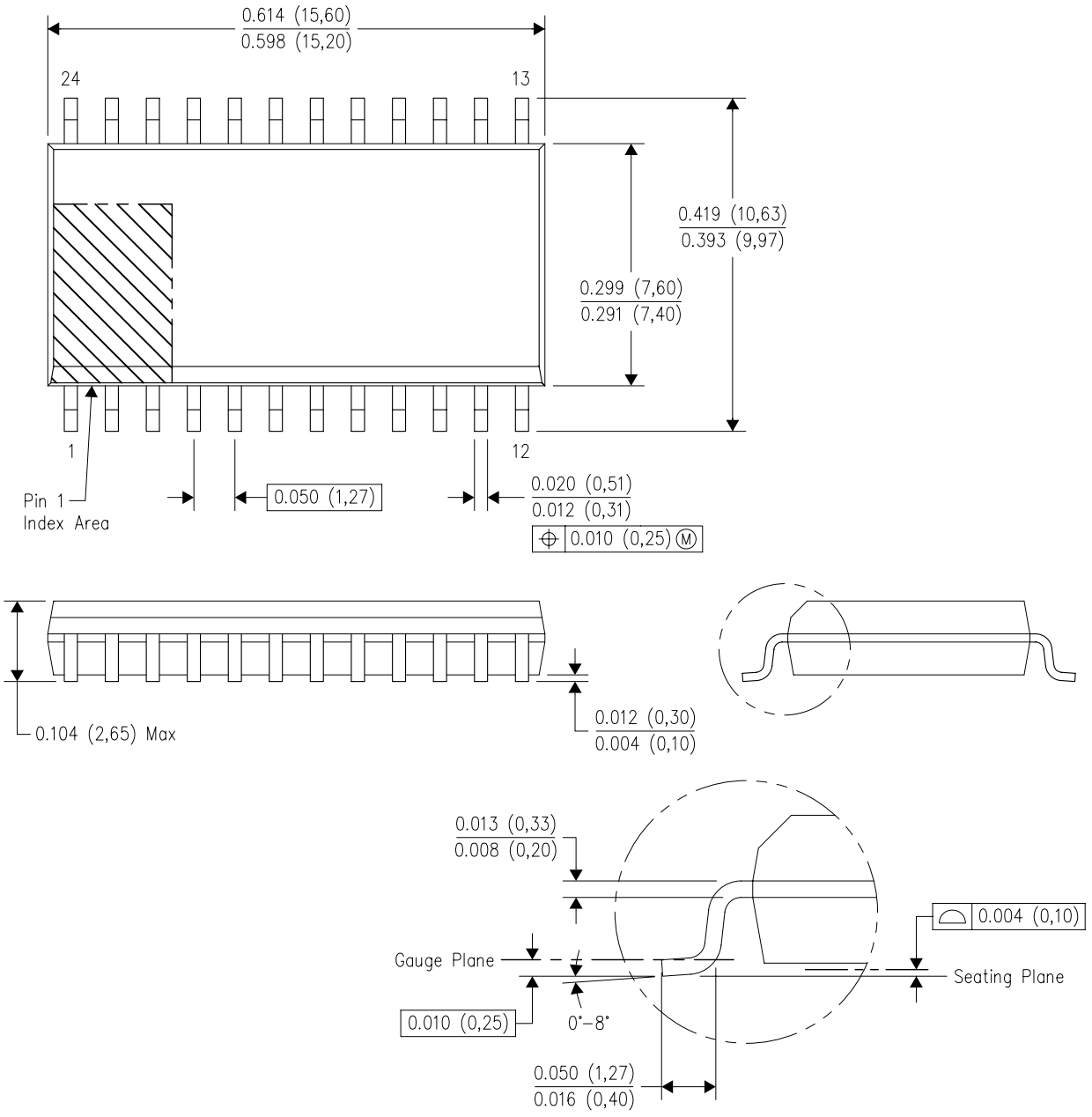
DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265