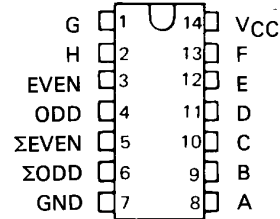


SN54180, SN74180 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

DECEMBER 1972 – REVISED MARCH 1988

SN54180 . . . J OR W PACKAGE
SN74180 . . . N PACKAGE

(TOP VIEW)



FUNCTION TABLE

INPUTS			OUTPUTS	
Σ OF H's AT A THRU H	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = high level, L = low level, X = irrelevant

description

These universal, monolithic, 9-bit (8 data bits plus 1 parity bit) parity generators/checkers, utilize familiar Series 54/74 TTL circuitry and feature odd/even outputs and control inputs to facilitate operation in either odd or even-parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

The SN54180/SN74180 are fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs at a low logic level. A fan-out to 20 normalized loads is provided at a high logic level to facilitate the connection of unused inputs to used inputs. Typical power dissipation is 170 mW.

The SN54180 is characterized for operation over the full military temperature range of -55°C to 125°C ; and the SN74180 is characterized for operation from 0°C to 70°C .

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54180 Circuits	-55°C to 125°C
SN74180 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54180			SN74180			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}\text{C}$

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2
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SN54180, SN74180

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54180			SN74180			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage				0.8			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 μA	2.4	3.3		2.4	3.3		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH} High-level input current	Any data input			40			40	μA
	Even or odd input			80			80	
I _{IL} Low-level input current	Any data input			-1.6			-1.6	mA
	Even or odd input			-3.2			-3.2	
I _{OS} Short-circuit output current §	V _{CC} = MAX	-20		-55	-18		-55	mA
I _{CC} Supply current	V _{CC} = MAX, See Note 2		34	49		34	56	mA

NOTE 2: I_{CC} is measured with even and odd inputs at 4.5 V, all other inputs and outputs open.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

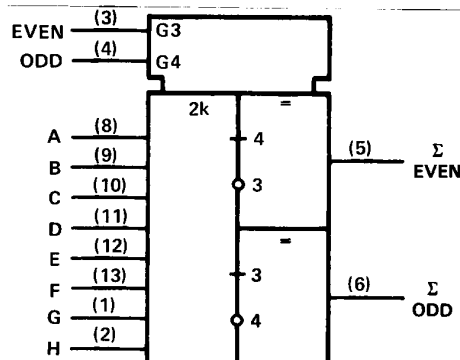
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Data	Σ Even	C _L = 15 pF, R _L = 400 Ω, Odd input grounded, See Note 3	40	60	ns	
t _{PHL}				45	68		
t _{PLH}	Data	Σ Odd		32	48	ns	
t _{PHL}				25	38		
t _{PLH}	Data	Σ Even		C _L = 15 pF, R _L = 400 Ω, Even input grounded, See Note 3	32	48	ns
t _{PHL}					25	38	
t _{PLH}	Data	Σ Odd	40		60	ns	
t _{PHL}			45		68		
t _{PLH}	Even or Odd	Σ Even or Σ Odd	C _L = 15 pF, R _L = 400 Ω, See Note 3		13	20	ns
t _{PHL}					7	10	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

logic symbol†



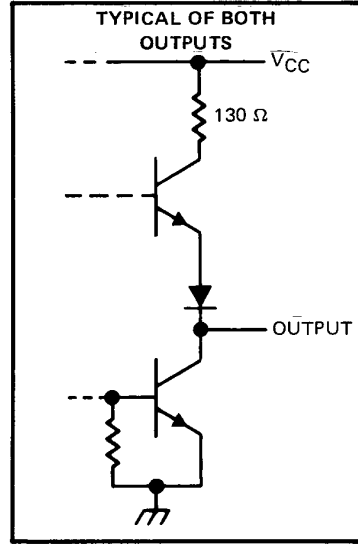
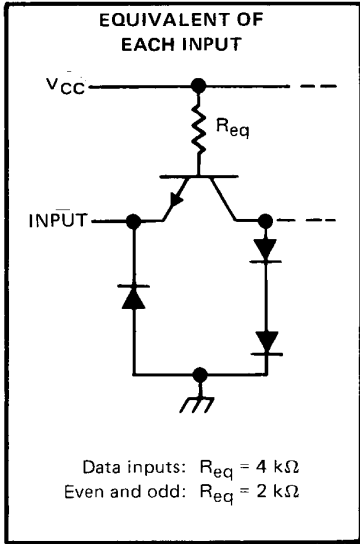
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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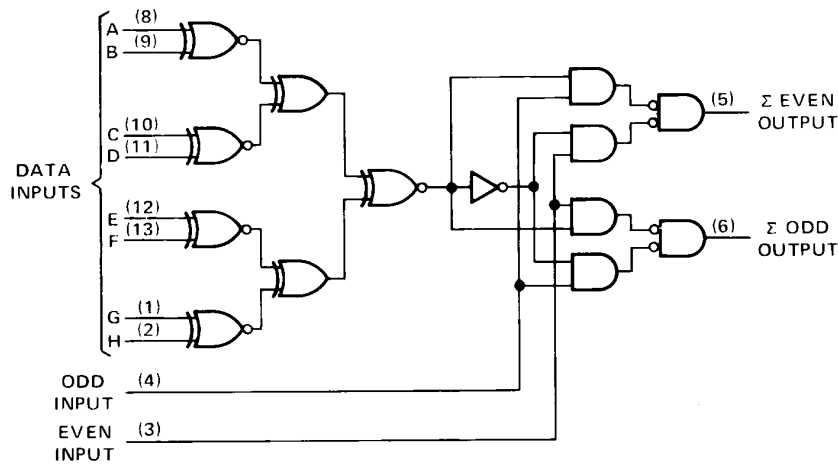
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SN54180, SN74180
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

schematics of inputs and outputs



logic diagram (positive logic)



2

TTL Devices

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN54180J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54180J	Samples
SNJ54180J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54180J	Samples
SNJ54180J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54180J	Samples
SNJ54180W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54180W	Samples
SNJ54180W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54180W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



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NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



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