

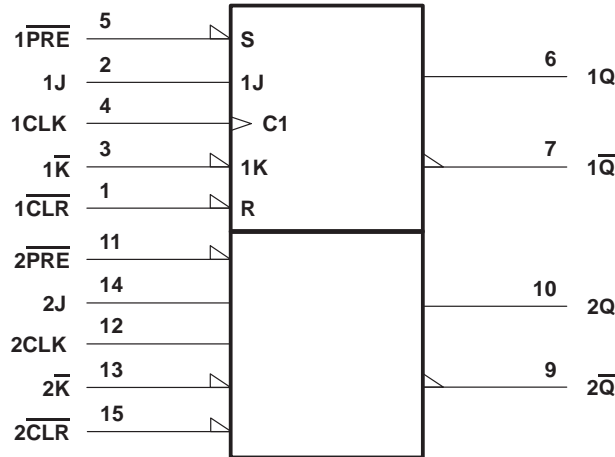


# SN54F109, SN74F109

## DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDFS047A – MARCH 1987 – REVISED OCTOBER 1993

### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-1.2 V to 7 V
Input current range .....	-30 mA to 5 mA
Voltage range applied to any output in the high state .....	-0.5 V to $V_{CC}$
Current into any output in the low state .....	40 mA
Operating free-air temperature range: SN54F109 .....	-55°C to 125°C
SN74F109 .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

### recommended operating conditions

	SN54F109			SN74F109			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8	V
$I_{IK}$ Input clamp current			-18			-18	mA
$I_{OH}$ High-level output current			-1			-1	mA
$I_{OL}$ Low-level output current			20			20	mA
$T_A$ Operating free-air temperature	-55		125	0		70	°C

# SN54F109, SN74F109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54F109			SN74F109			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$	-1.2			-1.2			V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -1\text{ mA}$	2.5	3.4		2.5	3.4		V
	$V_{CC} = 4.75\text{ V}$ , $I_{OH} = -1\text{ mA}$	2.7						
$V_{OL}$	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 20\text{ mA}$	0.3 0.5			0.3 0.5			V
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$	0.1			0.1			mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$	20			20			$\mu\text{A}$
$I_{IL}$	J, $\bar{K}$ , CLK	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.5\text{ V}$			-0.6			mA
	$\bar{PRE}$ or $\bar{CLR}$				-1.8			
$I_{OS}^\ddagger$	$V_{CC} = 5.5\text{ V}$ , $V_O = 0$	-60	-150		-60	-150		mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$ , See Note 2	11.7 17			11.7 17			mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2:  $I_{CC}$  is measured with J,  $\bar{K}$ , CLK, and  $\bar{PRE}$  grounded then with J,  $\bar{K}$ , CLK, and  $\bar{CLR}$  grounded.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

		$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		SN54F109		SN74F109		UNIT
		'F74						
		MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	0	100	0	70	0	90	MHz
$t_w$	Pulse duration	CLK high, $\bar{PRE}$ or $\bar{CLR}$ low		4	4	4	4	ns
		CLK low		5	5	5	5	
$t_{su}$	Setup time, data before CLK $\uparrow$	High		3	3	3	3	ns
		Low		3	3	3	3	
	Setup time, inactive-state before CLK $\uparrow$ §	$\bar{PRE}$ or $\bar{CLR}$ to CLK		2	2	2	2	
$t_h$	Hold time, data after CLK $\uparrow$	High		1	1	1	1	ns
		Low		1	1	1	1	

§ Inactive-state setup time is also referred to as recovery time.

**switching characteristics (see Note 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 500\ \Omega$ , $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 500\ \Omega$ , $T_A = \text{MIN to MAX}^\parallel$				UNIT
			'F109			SN54F109		SN74F109		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			100	150		70		90	MHz	
$t_{PLH}$	CLK	Q or $\bar{Q}$	3	4.9	7	3	9	3	8	ns
$t_{PHL}$			3.6	5.8	8	3.6	10.5	3.6	9.2	
$t_{PLH}$	$\bar{PRE}$ or $\bar{CLR}$	Q or $\bar{Q}$	2.4	4.8	7	2.4	9	2.4	8	ns
$t_{PHL}$			2.7	6.6	9	2.7	11.5	2.7	10.5	

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-9758001Q2A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9758001Q2A SNJ54F 109FK
<a href="#">5962-9758001QEA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9758001QE A SNJ54F109J
<a href="#">5962-9758001QFA</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9758001QF A SNJ54F109W
<a href="#">JM38510/34102B2A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34102B2A
JM38510/34102B2A.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34102B2A
<a href="#">JM38510/34102BEA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34102BEA
JM38510/34102BEA.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34102BEA
<a href="#">JM38510/34102BFA</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34102BFA
JM38510/34102BFA.A	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34102BFA
<a href="#">M38510/34102B2A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34102B2A
<a href="#">M38510/34102BEA</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34102BEA
<a href="#">M38510/34102BFA</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 34102BFA
<a href="#">SN74F109D</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	0 to 70	F109
<a href="#">SN74F109DR</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F109
SN74F109DR.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	F109
<a href="#">SN74F109N</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F109N
SN74F109N.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74F109N

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SNJ54F109FK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9758001Q2A SNJ54F 109FK
SNJ54F109FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9758001Q2A SNJ54F 109FK
<a href="#">SNJ54F109J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9758001QE A SNJ54F109J
SNJ54F109J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9758001QE A SNJ54F109J
<a href="#">SNJ54F109W</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9758001QF A SNJ54F109W
SNJ54F109W.A	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9758001QF A SNJ54F109W

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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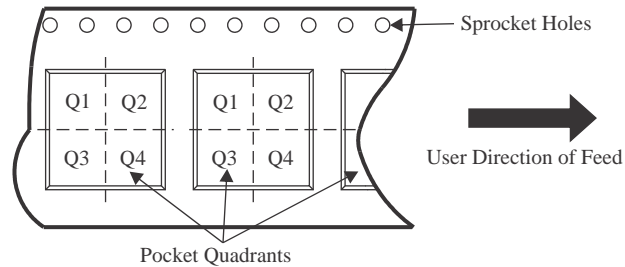
**OTHER QUALIFIED VERSIONS OF SN54F109, SN74F109 :**

- Catalog : [SN74F109](#)
- Military : [SN54F109](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


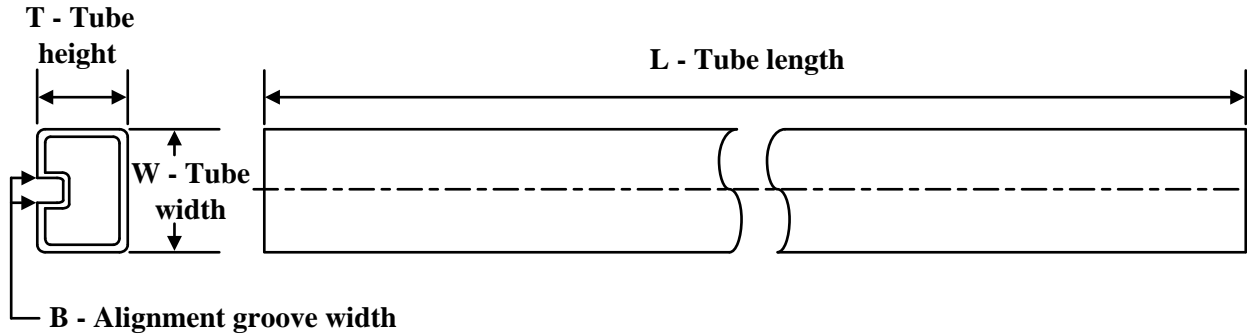
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F109DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F109DR	SOIC	D	16	2500	340.5	336.1	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9758001Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9758001QFA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/34102B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/34102B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/34102BF A	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/34102BF A.A	W	CFP	16	25	506.98	26.16	6220	NA
M38510/34102B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/34102BF A	W	CFP	16	25	506.98	26.16	6220	NA
SN74F109N	N	PDIP	16	25	506	13.97	11230	4.32
SN74F109N	N	PDIP	16	25	506	13.97	11230	4.32
SN74F109N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74F109N.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54F109FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54F109FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54F109W	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54F109W.A	W	CFP	16	25	506.98	26.16	6220	NA

D (R-PDSO-G16)

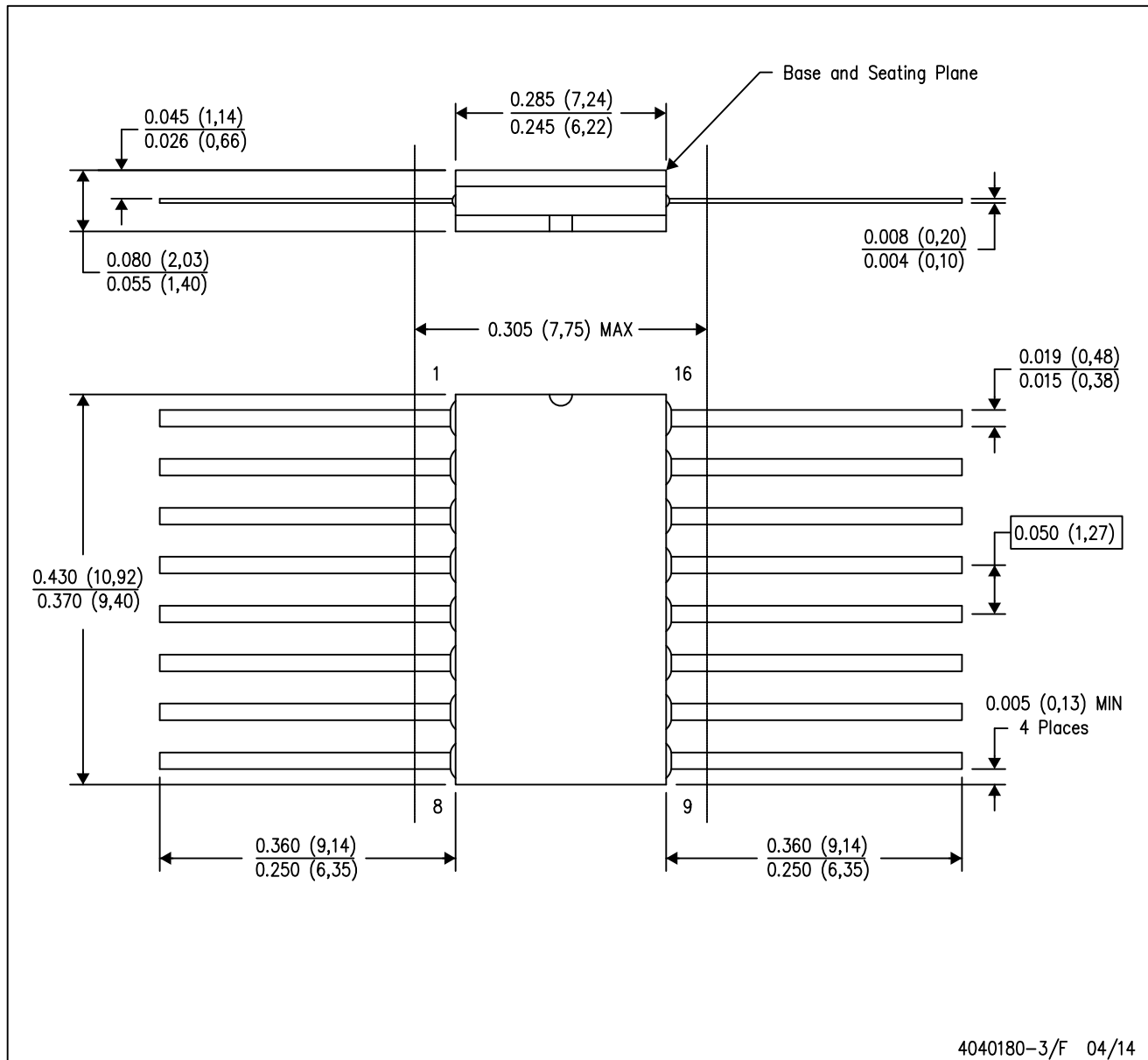
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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