For Driving Low-Threshold-Voltage MOS Inputs

description

These 2-input open-collector NAND gates feature high-output voltage ratings for interfacing with low-threshold-voltage MOS logic circuits or other 12-volt systems. Although the output is rated to withstand 15 volts, the VCC terminal is connected to the standard 5-volt source.

The SN5426 and SN54LS26 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7426 and SN74LS26 are characterized for operation from 0°C to 70°C.

logic diagram

![Logic Diagram](image)

positive logic

\[ Y = \overline{AB} \]

logic symbol†

![Logic Symbol](image)

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.
SN5426, SN54LS26, SNSN7426, SN74LS26
QUADRUPLE 2-INPUT
HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

schematics

Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1) ........................................... 7 V
Input voltage: '26 ................................................................. 5.5 V
'LS26 ............................................................................. 7 V
Operating free-air temperature: SN54' .................................. -55°C to 125°C
SN74' ........................................................................... 0°C to 70°C
Storage temperature range ...................................................... -65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.
### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SN54LS26</th>
<th>SN74LS26</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC (Supply Voltage)</td>
<td>4.5 to 5.5 V</td>
<td>4.75 to 5.25 V</td>
<td>V</td>
</tr>
<tr>
<td>VIH (High-level Input Voltage)</td>
<td>2 V</td>
<td>2 V</td>
<td></td>
</tr>
<tr>
<td>ViL (Low-level Input Voltage)</td>
<td>0.7 V</td>
<td>0.8 V</td>
<td></td>
</tr>
<tr>
<td>VOH (High-level Output Voltage)</td>
<td>15 V</td>
<td>15 V</td>
<td></td>
</tr>
<tr>
<td>IOL (Low-level Output Current)</td>
<td>4 mA</td>
<td>8 mA</td>
<td>mA</td>
</tr>
<tr>
<td>TA (Operating Free-air Temperature)</td>
<td>-65°C to 125°C</td>
<td>0°C to 70°C</td>
<td>°C</td>
</tr>
</tbody>
</table>

### Electrical Characteristics Over Recommended Operating Free-air Temperature Range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions†</th>
<th>SN54LS26</th>
<th>SN74LS26</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>VCC = MIN, I1 = 18 mA</td>
<td>-1.5 mA</td>
<td>-1.5 mA</td>
<td>V</td>
</tr>
<tr>
<td>IOH</td>
<td>VCC = MIN, VIH = MAX, VOH = 12 V</td>
<td>80 µA</td>
<td>80 µA</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>VCC = MIN, VIH = MAX, VOH = 15 V</td>
<td>1 mA</td>
<td>1 mA</td>
<td>mA</td>
</tr>
<tr>
<td>VOH</td>
<td>VCC = MIN, VIH = 2 V, IOL = 4 mA</td>
<td>0.25 mA</td>
<td>0.25 mA</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VCC = MIN, VIH = 2 V, IOL = 8 mA</td>
<td>0.35 mA</td>
<td>0.35 mA</td>
<td></td>
</tr>
<tr>
<td>IIL</td>
<td>VCC = MAX, VI = 7 V</td>
<td>0.1 mA</td>
<td>0.1 mA</td>
<td>mA</td>
</tr>
<tr>
<td>III</td>
<td>VCC = MAX, VIH = 2.7 V</td>
<td>20 µA</td>
<td>20 µA</td>
<td>mA</td>
</tr>
<tr>
<td>ICC</td>
<td>VCC = MAX, VI = 0.4 V</td>
<td>-0.4 mA</td>
<td>-0.4 mA</td>
<td>mA</td>
</tr>
<tr>
<td>ICCCH</td>
<td>VCC = MAX, VI = 0</td>
<td>0.8 mA</td>
<td>0.8 mA</td>
<td>mA</td>
</tr>
<tr>
<td>ICCCL</td>
<td>VCC = MAX, VI = 4.5 V</td>
<td>2.4 mA</td>
<td>2.4 mA</td>
<td></td>
</tr>
</tbody>
</table>

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at VCC = 5 V, TA = 25°C.

### Switching Characteristics, VCC = 5 V, TA = 25°C (see note 2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>From (Input)</th>
<th>To (Output)</th>
<th>Test Conditions</th>
<th>Min</th>
<th>TYP</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPLH</td>
<td>A or B</td>
<td>Y</td>
<td>R_L = 2 kΩ, C_L = 15 µF</td>
<td>17</td>
<td>32</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tPHL</td>
<td></td>
<td></td>
<td></td>
<td>15</td>
<td>28</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**Note 2:** Load circuits and voltage waveforms are shown in Section 1.
SN5426, SN7426
QUADRUPEL 2-INPUT
HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

**Recommended Operating Conditions**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SN5426</th>
<th>SN7426</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>VCC</code> - Supply voltage</td>
<td>MIN</td>
<td>NOM</td>
<td>MAX</td>
</tr>
<tr>
<td></td>
<td>4.5</td>
<td>5.5</td>
<td>5.75</td>
</tr>
<tr>
<td><code>VIL</code> - High-level input voltage</td>
<td>2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td><code>VIL</code> - Low-level input voltage</td>
<td>0.8</td>
<td>0.8</td>
<td></td>
</tr>
<tr>
<td><code>VOH</code> - High-level output voltage</td>
<td>15</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td><code>IoL</code> - Low-level output current</td>
<td>16</td>
<td>16</td>
<td>mA</td>
</tr>
<tr>
<td><code>TA</code> - Operating free-air temperature</td>
<td>-55</td>
<td>125</td>
<td>0</td>
</tr>
</tbody>
</table>

**Electrical Characteristics**

Over recommended operating free-air temperature range (unless otherwise noted):

<table>
<thead>
<tr>
<th>Parameter</th>
<th>TEST CONDITIONS</th>
<th>SN5426</th>
<th>SN7426</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>VIL</code></td>
<td><code>VCC = MIN, VIL = 0.8 V</code></td>
<td>-1.5</td>
<td>-1.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td><code>VCC = MIN, VIL = 0.7 V</code></td>
<td>50</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td><code>VCC = MIN, VIL = 0.8 V</code></td>
<td>1</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td><code>VCC = MIN, VIL = 0.7 V</code></td>
<td>1</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td><code>IOH</code></td>
<td><code>VCC = MIN, VOH = 2 V</code></td>
<td>0.4</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td><code>IOH</code></td>
<td><code>VCC = MAX, VIH = 5.6 V</code></td>
<td>1</td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td><code>IVL</code></td>
<td><code>VCC = MAX, VI = 2.4 V</code></td>
<td>40</td>
<td>40</td>
<td>mA</td>
</tr>
<tr>
<td><code>IVL</code></td>
<td><code>VCC = MAX, VI = 0.4 V</code></td>
<td>1.6</td>
<td>1.6</td>
<td>mA</td>
</tr>
<tr>
<td><code>ICCH</code></td>
<td><code>VCC = MAX, VI = 0</code></td>
<td>4</td>
<td>4</td>
<td>mA</td>
</tr>
<tr>
<td><code>ICCL</code></td>
<td><code>VCC = MAX, VI = 4.5 V</code></td>
<td>12</td>
<td>12</td>
<td>mA</td>
</tr>
</tbody>
</table>

1For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2All typical values are at `VCC = 5 V, TA = 25°C`.

**Switching Characteristics**

`VCC = 5 V, TA = 25°C` (see note 2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>fPLH</code></td>
<td>A or B</td>
<td>Y</td>
<td><code>RL = 1 kΩ, CL = 15 pF</code></td>
<td>16</td>
<td>24</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><code>fPHL</code></td>
<td></td>
<td></td>
<td></td>
<td>11</td>
<td>17</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**Note 2:** Load circuits and voltage waveforms are shown in Section 1.
**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**

- Reel Diameter
- Reel Width (W1)

**TAPE DIMENSIONS**

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component thickness
- K0: Dimension designed to accommodate the component length
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- Pocket Quadrants
- Sprocket Holes
- User Direction of Feed

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74LS26DR</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>330.0</td>
<td>16.4</td>
<td>6.5</td>
<td>9.0</td>
<td>2.1</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74LS26DR</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
## TUBE

![Diagram of a tube with dimensions labeled: T - Tube height, W - Tube width, B - Alignment groove width, L - Tube length.]

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Name</th>
<th>Package Type</th>
<th>Pins</th>
<th>SPQ</th>
<th>L (mm)</th>
<th>W (mm)</th>
<th>T (µm)</th>
<th>B (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5962-7602001VDA</td>
<td>W</td>
<td>CFP</td>
<td>14</td>
<td>25</td>
<td>506.98</td>
<td>26.16</td>
<td>6220</td>
<td>NA</td>
</tr>
<tr>
<td>7602001DA</td>
<td>W</td>
<td>CFP</td>
<td>14</td>
<td>25</td>
<td>506.98</td>
<td>26.16</td>
<td>6220</td>
<td>NA</td>
</tr>
<tr>
<td>JM38510/32102BDA</td>
<td>W</td>
<td>CFP</td>
<td>14</td>
<td>25</td>
<td>506.98</td>
<td>26.16</td>
<td>6220</td>
<td>NA</td>
</tr>
<tr>
<td>M38510/32102BDA</td>
<td>W</td>
<td>CFP</td>
<td>14</td>
<td>25</td>
<td>506.98</td>
<td>26.16</td>
<td>6220</td>
<td>NA</td>
</tr>
<tr>
<td>SN74LS26N</td>
<td>N</td>
<td>PDIP</td>
<td>14</td>
<td>25</td>
<td>506</td>
<td>13.97</td>
<td>11230</td>
<td>4.32</td>
</tr>
<tr>
<td>SN74LS26N</td>
<td>N</td>
<td>PDIP</td>
<td>14</td>
<td>25</td>
<td>506</td>
<td>13.97</td>
<td>11230</td>
<td>4.32</td>
</tr>
<tr>
<td>SNJ54LS26W</td>
<td>W</td>
<td>CFP</td>
<td>14</td>
<td>25</td>
<td>506.98</td>
<td>26.16</td>
<td>6220</td>
<td>NA</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
EXAMPLE BOARD LAYOUT

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

SEE DETAIL A
SEE DETAIL B

SYMM
SYMM

1

14

12X (.100 )
[2.54]

14X (Ø .039)
[1]

14X (Ø .063)
[1.6]

.002 MAX
[0.05]
ALL AROUND

.002 MAX
[0.05]
ALL AROUND

 DETAIL A
SCALE: 15X

 DETAIL B
13X, SCALE: 15X

.002 MAX
[0.05]
ALL AROUND

.002 MAX
[0.05]
ALL AROUND

SOLDER MASK OPENING

METAL

SOLDER MASK OPENING

METAL

SCALE: 15X

SEE DETAIL A
SEE DETAIL B

SYMM
SYMM

1

14

12X (.100 )
[2.54]

14X (Ø .039)
[1]

14X (Ø .063)
[1.6]

.002 MAX
[0.05]
ALL AROUND

.002 MAX
[0.05]
ALL AROUND

SOLDER MASK OPENING

METAL

SOLDER MASK OPENING

METAL

SCALE: 15X
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
\[ \text{Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.} \]
\[ \text{Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.} \]
E. Reference JEDEC MS-012 variation AB.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
\[\警惕\] Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
\[\警惕\] The 20 pin end lead shoulder width is a vendor option, either half or full width.
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