SN5473, SN54LS73A, SN7473, SN74LS73A
DUAL J-K FLIP-FLOPS WITH CLEAR

- Package Options Include Plastic "Small Outline" Packages, Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

**Description**

The '73, and 'H73, contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '73, and 'H73, are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS73A contains two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the \( \bar{Q} \) output high.

The SN5473, SN54H73, and the SN54LS73A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7473, and the SN74LS73A are characterized for operation from 0°C to 70°C.

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**Function Table - '73**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR, CLK, J, K</td>
<td>Q, ( \bar{Q} )</td>
</tr>
</tbody>
</table>

- L X X X L H
- H L L L Q L \( \bar{Q} \)
- H L H L H L
- H L L H L H
- H L H H TOGGLE

**Function Table - 'LS73A**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR, CLK, J, K</td>
<td>Q, ( \bar{Q} )</td>
</tr>
</tbody>
</table>

- L X X X L H
- H L L L Q L \( \bar{Q} \)
- H L H L H L
- H L L H L H
- H L H H TOGGLE
- H L X X Q L \( \bar{Q} \)

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logic symbols†

†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs
logic diagrams (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Specification</th>
<th>'73</th>
<th>'LS73A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, (V_{CC}) (See Note 1)</td>
<td>7 V</td>
<td>7 V</td>
</tr>
<tr>
<td>Input voltage:</td>
<td>5.5 V</td>
<td></td>
</tr>
<tr>
<td>Operating free-air temperature range:</td>
<td>(-55^\circ C) to (125^\circ C)</td>
<td>(-65^\circ C) to (150^\circ C)</td>
</tr>
<tr>
<td>Storage temperature range</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE 1: Voltage values are with respect to network ground terminal.
recommended operating conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SN5473</th>
<th>SN7473</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;CC&lt;/sub&gt; Supply voltage</td>
<td>4.5  5  5.5</td>
<td>4.75 5  5.25</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IH&lt;/sub&gt; High-level input voltage</td>
<td>2</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IL&lt;/sub&gt; Low-level input voltage</td>
<td>0.8</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>I&lt;sub&gt;OH&lt;/sub&gt; High-level output current</td>
<td>-0.4</td>
<td>-0.4</td>
<td>mA</td>
</tr>
<tr>
<td>I&lt;sub&gt;OL&lt;/sub&gt; Low-level output current</td>
<td>16</td>
<td>16</td>
<td>mA</td>
</tr>
<tr>
<td>t&lt;sub&gt;W&lt;/sub&gt; Pulse duration</td>
<td>CLK high 20</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>CLK low 47</td>
<td>47</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>CLR low 25</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;tu&lt;/sub&gt; Input setup time before CLK↑</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;th&lt;/sub&gt; Input hold time after CLK↓</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>T&lt;sub&gt;A&lt;/sub&gt; Operating free-air temperature</td>
<td>-55  125  0</td>
<td>0  70</td>
<td>°C</td>
</tr>
</tbody>
</table>

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>TEST CONDITIONS†</th>
<th>SN5473</th>
<th>SN7473</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;IK&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = MIN, I&lt;sub&gt;I&lt;/sub&gt; = -12 mA</td>
<td>-1.5</td>
<td>-1.5</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = MIN, I&lt;sub&gt;O&lt;/sub&gt; = -0.4 mA, V&lt;sub&gt;IH&lt;/sub&gt; = 2 V, V&lt;sub&gt;IL&lt;/sub&gt; = 0.8 V</td>
<td>2.4  3.4</td>
<td>2.4  3.4</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = MIN, I&lt;sub&gt;O&lt;/sub&gt; = 16 mA, V&lt;sub&gt;IH&lt;/sub&gt; = 2 V, V&lt;sub&gt;IL&lt;/sub&gt; = 0.8 V</td>
<td>0.2  0.4</td>
<td>0.2  0.4</td>
<td>V</td>
</tr>
<tr>
<td>I&lt;sub&gt;I&lt;/sub&gt;</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = MAX, V&lt;sub&gt;I&lt;/sub&gt; = 5.5 V</td>
<td>1</td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td>I&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>J or K, CLR or CLK</td>
<td>40</td>
<td>40</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = MAX, V&lt;sub&gt;I&lt;/sub&gt; = 2.4 V</td>
<td>80</td>
<td>80</td>
<td>μA</td>
</tr>
<tr>
<td>I&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>J or K, CLR</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = MAX, V&lt;sub&gt;I&lt;/sub&gt; = 0.4 V</td>
<td>-1.6</td>
<td>-1.6</td>
</tr>
<tr>
<td></td>
<td>CLR or CLK</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = MAX, V&lt;sub&gt;I&lt;/sub&gt; = 0.4 V</td>
<td>-3.2</td>
<td>-3.2</td>
</tr>
<tr>
<td>I&lt;sub&gt;OHS&lt;/sub&gt;§</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = MAX</td>
<td>-20</td>
<td>-57</td>
<td>-18</td>
</tr>
<tr>
<td>I&lt;sub&gt;ICC&lt;/sub&gt;†</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = MAX, See Note 2</td>
<td>10</td>
<td>20</td>
<td>10  20</td>
</tr>
</tbody>
</table>

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.
§ Not more than one output should be shorted at a time.
† Average per flip-flop.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and Q̅ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)

<table>
<thead>
<tr>
<th>Parameter#</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>f&lt;sub&gt;MAX&lt;/sub&gt;</td>
<td>CLR</td>
<td>Q</td>
<td>R&lt;sub&gt;L&lt;/sub&gt; = 400 Ω, C&lt;sub&gt;L&lt;/sub&gt; = 15 pF</td>
<td>15  20</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;PLH&lt;/sub&gt;</td>
<td>CLR</td>
<td>Q</td>
<td>Q</td>
<td>16  25</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;PHL&lt;/sub&gt;</td>
<td>CLR</td>
<td>Q</td>
<td>Q̅</td>
<td>25  40</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;PHH&lt;/sub&gt;</td>
<td>CLK</td>
<td>Q</td>
<td>Q̅</td>
<td>16  25</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t&lt;sub&gt;PLH&lt;/sub&gt;</td>
<td>CLK</td>
<td>Q̅</td>
<td>Q</td>
<td>25  40</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#f<sub>MAX</sub> = maximum clock frequency; t<sub>PLH</sub> = propagation delay time, low-to-high-level output; t<sub>PHL</sub> = propagation delay time, high-to-low-level output.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.
### recommended operating conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SN54LS73A</th>
<th>SN74LS73A</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} ) Supply voltage</td>
<td>( 4.5 )</td>
<td>( 5 )</td>
<td>( 5.5 )</td>
</tr>
<tr>
<td>( V_{IH} ) High-level input voltage</td>
<td>2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>( V_{IL} ) Low-level input voltage</td>
<td>0.7</td>
<td>0.8</td>
<td></td>
</tr>
<tr>
<td>( I_{OH} ) High-level output current</td>
<td>0.4</td>
<td>0.4</td>
<td></td>
</tr>
<tr>
<td>( I_{OL} ) Low-level output current</td>
<td>4</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{CLK}} ) Clock frequency</td>
<td>0</td>
<td>30</td>
<td>0</td>
</tr>
<tr>
<td>( t_{W} ) Pulse duration</td>
<td>CL</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>( t_{SU} ) Set up time-before ( \text{CLK} \downarrow )</td>
<td>data high or low</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>( t_{H} ) Hold time-data after ( \text{CLK} \downarrow )</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>( T_A ) Operating free-air temperature</td>
<td>-55</td>
<td>125</td>
<td>0</td>
</tr>
</tbody>
</table>

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>TEST CONDITIONS†</th>
<th>SN54LS73A</th>
<th>SN74LS73A</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IK} )</td>
<td>( V_{CC} = \text{MIN}, \ I_I = -18 \text{ mA} )</td>
<td>( -1.5 )</td>
<td>( -1.5 )</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>( V_{CC} = \text{MIN}, \ I_{OH} = -0.4 \text{ mA} )</td>
<td>( 2.5 )</td>
<td>3.4</td>
<td>2.7</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>( V_{CC} = \text{MIN}, \ I_{OL} = 4 \text{ mA} )</td>
<td>( 0.25 )</td>
<td>0.4</td>
<td>0.25</td>
</tr>
<tr>
<td>( I_I ) J or K</td>
<td>( V_{CC} = \text{MAX}, \ V_I = 7 \text{ V} )</td>
<td>0.1</td>
<td>0.1</td>
<td></td>
</tr>
<tr>
<td>CLR</td>
<td>( V_{CC} = \text{MAX}, \ V_I = 7 \text{ V} )</td>
<td>0.3</td>
<td>0.3</td>
<td></td>
</tr>
<tr>
<td>CLK</td>
<td>( V_{CC} = \text{MAX}, \ V_I = 7 \text{ V} )</td>
<td>0.4</td>
<td>0.4</td>
<td></td>
</tr>
<tr>
<td>( I_{IH} ) J or K</td>
<td>( V_{CC} = \text{MAX}, \ V_I = 2.7 \text{ V} )</td>
<td>20</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>CLR</td>
<td>( V_{CC} = \text{MAX}, \ V_I = 2.7 \text{ V} )</td>
<td>60</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td>CLK</td>
<td>( V_{CC} = \text{MAX}, \ V_I = 2.7 \text{ V} )</td>
<td>80</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>( I_{IL} ) J or K</td>
<td>( V_{CC} = \text{MAX}, \ V_I = 0.4 \text{ V} )</td>
<td>-0.4</td>
<td>-0.4</td>
<td></td>
</tr>
<tr>
<td>CLR or CLK</td>
<td>( V_{CC} = \text{MAX}, \ V_I = 0.4 \text{ V} )</td>
<td>-0.8</td>
<td>-0.8</td>
<td></td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>( V_{CC} = \text{MAX}, \text{ See Note 4} )</td>
<td>-20</td>
<td>-100</td>
<td>-20</td>
</tr>
<tr>
<td>( I_{CC} ) (Total)</td>
<td>( V_{CC} = \text{MAX}, \text{ See Note 2} )</td>
<td>4</td>
<td>6</td>
<td>4</td>
</tr>
</tbody>
</table>

† For conditions shown as \( \text{MIN or MAX} \), use the appropriate value specified under recommended operating conditions.
‡ All typical values are at \( V_{CC} = 5 \text{ V}, \ T_A = 25^\circ \text{C} \).
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

**NOTE 2:** With all outputs open, \( I_{CC} \) is measured with the Q and \( \overline{Q} \) outputs high in turn. At the time of measurement, the clock input is grounded.

**NOTE 4:** For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with \( V_{CC} = 2.25 \text{ V} \) and \( 1.25 \text{ V} \) for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

### switching characteristics, \( V_{CC} = 5 \text{ V}, \ T_A = 25^\circ \text{C} \) (see note 3)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{\text{PLH}} )</td>
<td>CLR or CLK</td>
<td>( Q ) or ( \overline{Q} )</td>
<td>( R_L = 2 \text{ kΩ}, \ C_L = 15 \text{ pF} )</td>
<td>( 30 )</td>
<td>( 45 )</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{PHL}} )</td>
<td>CLR or CLK</td>
<td>( Q ) or ( \overline{Q} )</td>
<td>( R_L = 2 \text{ kΩ}, \ C_L = 15 \text{ pF} )</td>
<td>( 15 )</td>
<td>( 20 )</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE 3:** Load circuits and voltage waveforms are shown in Section 1.
## Packaging Information

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<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>5962-9675101QCA</td>
<td>ACTIVE</td>
<td>CDIP</td>
<td>J</td>
<td>14</td>
<td>1</td>
<td>TBD</td>
<td>Call TI</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>5962-9675101QC A SNJ54LS73AJ</td>
<td>Samples</td>
</tr>
<tr>
<td>5962-9675101QDA</td>
<td>ACTIVE</td>
<td>CFP</td>
<td>W</td>
<td>14</td>
<td>1</td>
<td>TBD</td>
<td>Call TI</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>5962-9675101QDA A SNJ54LS73AW</td>
<td>Samples</td>
</tr>
<tr>
<td>5962-9675101QDA</td>
<td>ACTIVE</td>
<td>CFP</td>
<td>W</td>
<td>14</td>
<td>1</td>
<td>TBD</td>
<td>Call TI</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>5962-9675101QDA A SNJ54LS73AW</td>
<td>Samples</td>
</tr>
<tr>
<td>SN54LS73AJ</td>
<td>ACTIVE</td>
<td>CDIP</td>
<td>J</td>
<td>14</td>
<td>1</td>
<td>TBD</td>
<td>Call TI</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>SN54LS73AJ</td>
<td>Samples</td>
</tr>
<tr>
<td>SN54LS73AJ</td>
<td>ACTIVE</td>
<td>CDIP</td>
<td>J</td>
<td>14</td>
<td>1</td>
<td>TBD</td>
<td>Call TI</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>SN54LS73AJ</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74LS73AD</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>LS73A</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74LS73AD</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>LS73A</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74LS73ADR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>LS73A</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74LS73ADR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>LS73A</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74LS73ADRG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>LS73A</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74LS73ADRG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
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<td>5962-9675101QC A SNJ54LS73AJ</td>
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## Orderable Device

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<th>Orderable Device</th>
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<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
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</table>
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS73A, SN74LS73A :

• Catalog: SN74LS73A

• Military: SN54LS73A

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications
TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

---

**PACKAGE MATERIALS INFORMATION**

---

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<td>SOIC</td>
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<td>8.0</td>
<td>16.0</td>
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</table>

*All dimensions are nominal.

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers
<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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*All dimensions are nominal*
MECHANICAL DATA

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E. Reference JEDEC MS-012 variation AB.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
**MECHANICAL DATA**

**N (R-PDIP-T**)**

**PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN

<table>
<thead>
<tr>
<th>DIM</th>
<th>PINS **</th>
<th>14</th>
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<th>18</th>
<th>20</th>
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<tbody>
<tr>
<td>A MAX</td>
<td>0.775 (19.69)</td>
<td>0.775 (19.69)</td>
<td>0.920 (23.37)</td>
<td>1.060 (26.92)</td>
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<tr>
<td>A MIN</td>
<td>0.745 (18.92)</td>
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<td>0.850 (21.59)</td>
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<td>VARIATION</td>
<td>MS-001</td>
<td>AA</td>
<td>BB</td>
<td>AC</td>
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</tbody>
</table>

**NOTES:**
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

⚠️ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
⚠️ The 20 pin end lead shoulder width is a vendor option, either half or full width.
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