

# SN54S182, SN74S182 LOOK-AHEAD CARRY GENERATORS

SDLS206 - DECEMBER 1972 - REVISED MARCH 1988

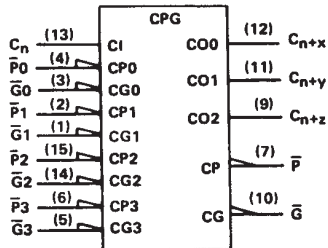
- Directly Compatible for Use With:  
SN54LS181/SN74LS181,  
SN54S281/SN74S281, SN54S381,  
SN74S381, SN54S481/SN74S481

## PIN DESIGNATIONS

ALTERNATIVE DESIGNATIONS†	DESIGNATIONS†	PIN NOS.	FUNCTION
$\bar{G}0, \bar{G}1, \bar{G}2, \bar{G}3$	G0, G1, G2, G3	3, 1, 14, 5	CARRY GENERATE INPUTS
$\bar{P}0, \bar{P}1, \bar{P}2, \bar{P}3$	P0, P1, P2, P3	4, 2, 15, 6	CARRY PROPAGATE INPUTS
$C_n$	$\bar{C}_n$	13	CARRY INPUT
$C_{n+x}, C_{n+y}, C_{n+z}$	$\bar{C}_{n+x}, \bar{C}_{n+y}, \bar{C}_{n+z}$	12, 11, 9	CARRY OUTPUTS
$\bar{G}$	Y	10	CARRY GENERATE OUTPUT
$\bar{P}$	X	7	CARRY PROPAGATE OUTPUT
VCC		16	SUPPLY VOLTAGE
GND		8	GROUND

† Interpretations are illustrated in the 'LS181, 'S181 data sheet.

## logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

## description

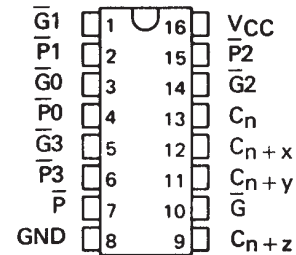
The SN54S182 and SN74S182 are high-speed, look-ahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table above.

When used in conjunction with the 'LS181 or 'S181 arithmetic logic unit (ALU), these generators provide high-speed carry look-ahead capability for any word length. Each 'S182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading 'S182 circuits to perform multilevel look-ahead is illustrated under typical application data.

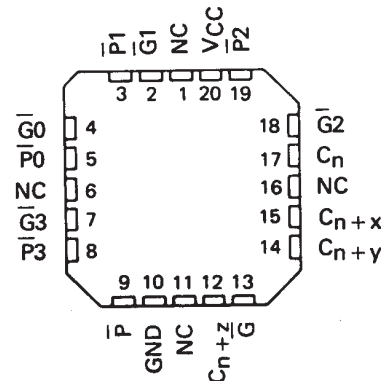
The carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions as explained on the 'LS181 and 'S181 data sheet are also applicable to and compatible with the look-ahead generator. Logic equations for the 'S182 are:

$$\begin{aligned}
 C_{n+x} &= G0 + P0 C_n & \bar{C}_{n+x} &= \overline{Y0 (X0 + C_n)} \\
 C_{n+y} &= G1 + P1 G0 + P1 P0 C_n & \bar{C}_{n+y} &= \overline{Y1 [X1 + Y0 (X0 + C_n)]} \\
 C_{n+z} &= G2 + P2 G1 + P2 P1 G0 + P2 P1 P0 C_n & \bar{C}_{n+z} &= \overline{Y2 \{ X2 + Y1 [X1 + Y0 (X0 + C_n)] \}} \\
 \bar{G} &= G3 + P3 G2 + P3 P2 G1 + P3 P2 P1 G0 & Y &= Y3 (X3 + Y2) (X3 + X2 + Y1) (X3 + X2 + X1 + Y0) \\
 \bar{P} &= P3 P2 P1 P0 & X &= X3 + X2 + X1 + X0
 \end{aligned}$$

SN54S182 . . . J OR W PACKAGE  
SN74S182 . . . D OR N PACKAGE  
(TOP VIEW)



SN54S182 . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

# SN54S182, SN74S182 LOOK-AHEAD CARRY GENERATORS

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FUNCTION TABLE FOR  $\bar{G}$  OUTPUT

INPUTS							OUTPUT
$\bar{G}_3$	$\bar{G}_2$	$\bar{G}_1$	$\bar{G}_0$	$\bar{P}_3$	$\bar{P}_2$	$\bar{P}_1$	$\bar{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR  $\bar{P}$  OUTPUT

INPUTS				OUTPUT
$\bar{P}_3$	$\bar{P}_2$	$\bar{P}_1$	$\bar{P}_0$	$\bar{P}$
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR  $C_{n+x}$  OUTPUT

INPUTS			OUTPUT
$\bar{G}_0$	$\bar{P}_0$	$C_n$	$C_{n+x}$
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE FOR  $C_{n+y}$  OUTPUT

INPUTS					OUTPUT
$\bar{G}_1$	$\bar{G}_0$	$\bar{P}_1$	$\bar{P}_0$	$C_n$	$C_{n+y}$
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

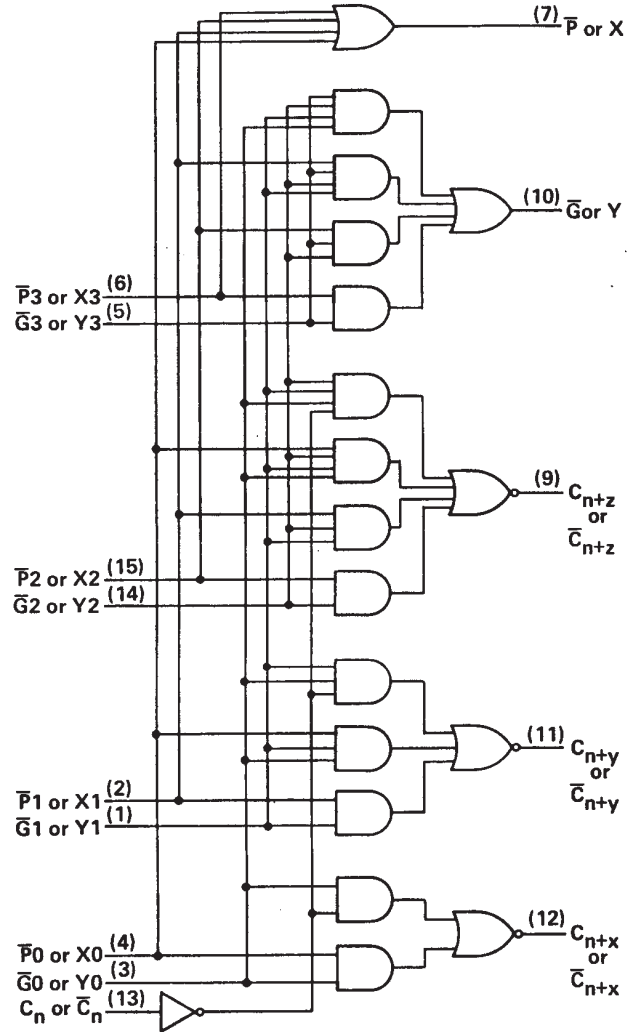
FUNCTION TABLE FOR  $C_{n+z}$  OUTPUT

INPUTS							OUTPUT
$\bar{G}_2$	$\bar{G}_1$	$\bar{G}_0$	$\bar{P}_2$	$\bar{P}_1$	$\bar{P}_0$	$C_n$	$C_{n+z}$
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = high level, L = low level, X = irrelevant

Any inputs not shown in a given table are irrelevant with respect to that output.

logic diagram (positive logic)

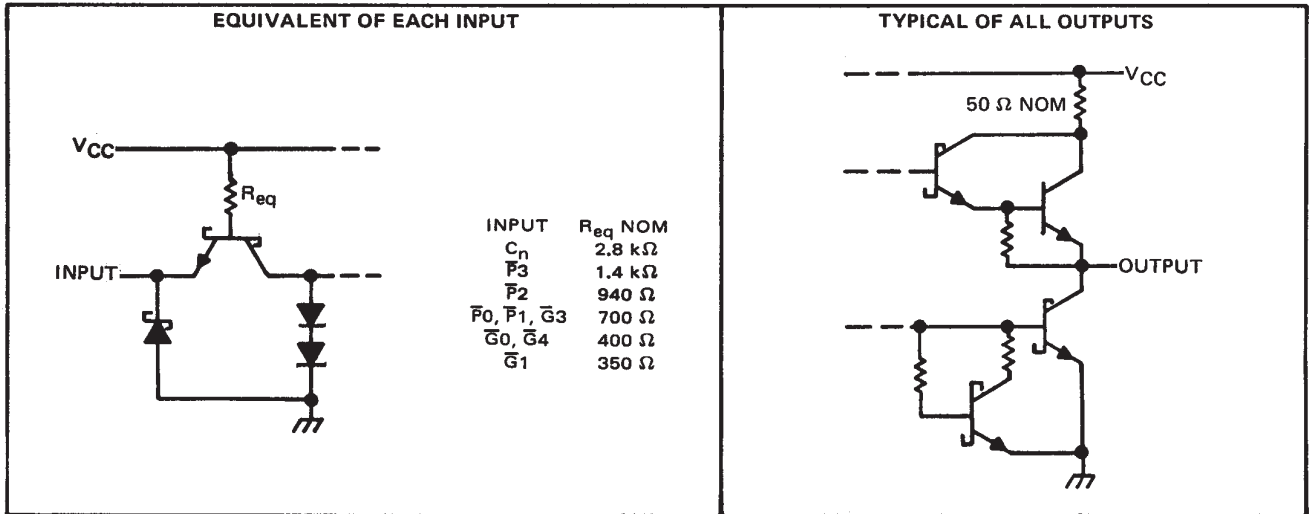


Pin numbers shown are for D, J, N, and W packages.

# SN54S182, SN74S182 LOOK-AHEAD CARRY GENERATORS

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## schematics of inputs and outputs



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54S182	-55°C to 125°C
SN74S182	0°C to 70°C
Storage temperature range	-65°C to 150°C

- NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.  
 2. This is the voltage between two emitters of a multiple-emitter input transistor. For these circuits, this rating applies to each  $\bar{G}$  input in conjunction with any other  $\bar{G}$  input or in conjunction with any  $\bar{P}$  input.

# SN54S182, SN74S182 LOOK-AHEAD CARRY GENERATORS

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## recommended operating conditions

	SN54S182			SN74S182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-1			-1	mA
Low-level output current, $I_{OL}$			20			20	mA
Operating free-air temperature, $T_A$	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S182			SN74S182			UNIT	
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
$V_{IH}$	High-level input voltage		2			2			V	
$V_{IL}$	Low-level input voltage				0.8			0.8	V	
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2			-1.2	V	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V	
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA	
$I_{IH}$	High-level input current	$C_n$ input			50			50	$\mu\text{A}$	
		$\bar{P}3$ input			100			100		
		$\bar{P}2$ input			150			150		
		$\bar{P}0, \bar{P}1, \text{ or } \bar{G}3$ input	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			200				200
		$\bar{G}0$ or $\bar{G}2$ input				350				350
		$\bar{G}1$ input				400				400
$I_{IL}$	Low-level input current	$C_n$ input			-2			-2	mA	
		$\bar{P}3$ input			-4			-4		
		$\bar{P}2$ input			-6			-6		
		$\bar{P}0, \bar{P}1, \text{ or } \bar{G}3$ input	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-8				-8
		$\bar{G}0$ or $\bar{G}2$ input				-14				-14
		$\bar{G}1$ input				-16				-16
$I_{OS}$	Short-circuit output current§	$V_{CC} = \text{MAX}$			-40		-100		mA	
$I_{CCH}$	Supply current, all outputs high	$V_{CC} = 5 \text{ V}$ , See Note 3			35		65		mA	
$I_{CCL}$	Supply current, all outputs low	$V_{CC} = \text{MAX}$ , See Note 4			69		99		mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

NOTES: 3.  $I_{CCH}$  is measured with all outputs open, inputs  $\bar{P}3$  and  $\bar{G}3$  at 4.5 V, and all other inputs grounded. MAX is determined at 5.5 V.

4.  $I_{CCL}$  is measured with all outputs open; inputs  $\bar{G}0, \bar{G}1, \text{ and } \bar{G}2$  at 4.5 V; and all other inputs grounded.

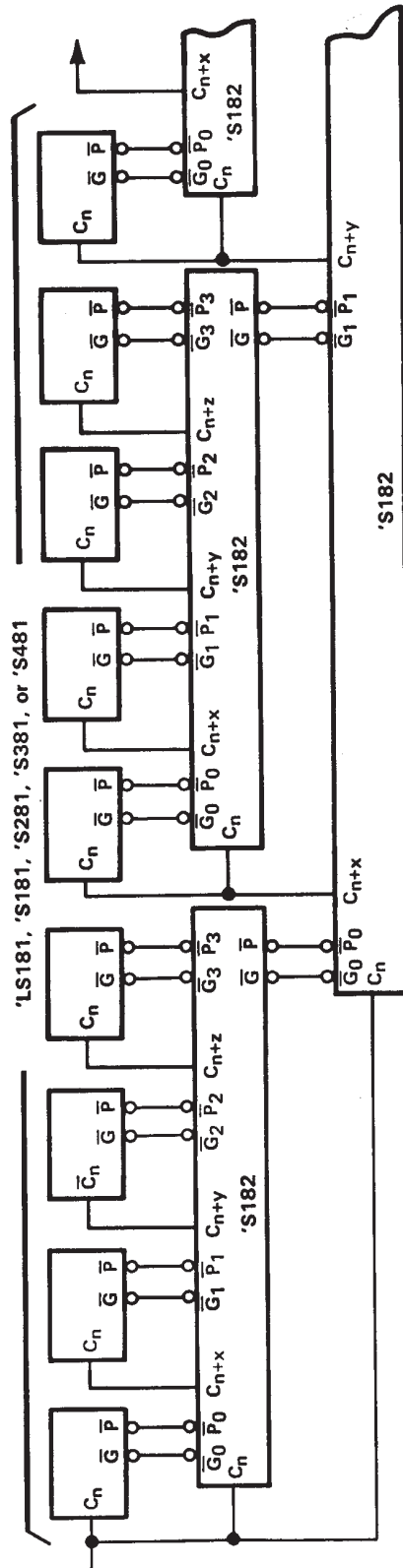
## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	$\bar{G}0, \bar{G}1, \bar{G}2, \bar{G}3,$	$C_{n+x}, C_{n+y},$	$R_L = 280 \Omega, C_L = 15 \text{ pF},$ See Note 5		4.5	7	ns
$t_{PHL}$	$P0, P1, P2, \text{ or } P3$	$\text{or } C_{n+z}$			4.5	7	
$t_{PLH}$	$\bar{G}0, \bar{G}1, \bar{G}2, \bar{G}3,$	$\bar{G}$			5	7.5	ns
$t_{PHL}$	$P1, P2, \text{ or } P3$				7	10.5	
$t_{PLH}$	$\bar{P}0, \bar{P}1, \bar{P}2, \text{ or } \bar{P}3$	$\bar{P}$			4.5	6.5	ns
$t_{PHL}$					6.5	10	
$t_{PLH}$	$C_n$	$C_{n+x}, C_{n+y},$			6.5	10	ns
$t_{PHL}$		$\text{or } C_{n+z}$			7	10.5	

NOTE 5: Load circuits and voltage waveforms are shown in Section 1.



TYPICAL APPLICATION DATA



64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS

Remaining inputs and outputs of 'LS181, 'S181, 'S281, 'S381, and 'S481 are not shown.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/07802BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 07802BEA	<a href="#">Samples</a>
M38510/07802BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 07802BEA	<a href="#">Samples</a>
SN54S182J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54S182J	<a href="#">Samples</a>
SNJ54S182FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S 182FK	<a href="#">Samples</a>
SNJ54S182J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S182J	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SNJ54S182FK	FK	LCCC	20	1	506.98	12.06	2030	NA



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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