

QUADRUPLE LOW-POWER DIFFERENTIAL RECEIVER

Check for Samples: [SN55LBC173-HIREL](#)

FEATURES

- Meets EIA Standards RS-422-A, RS-423-A, RS-485, and CCITT V.11
- Designed to Operate With Pulse Durations as Short as 20 ns
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- Input Sensitivity: ± 200 mV
- Low-Power Consumption: 20 mA (Max)
- Open-Circuit Fail-Safe Design

DESCRIPTION

The SN55LBC173 is a monolithic quadruple differential line receiver with 3-state outputs designed to meet the requirements of the EIA standards RS-422-A, RS-423-A, RS-485, and CCITT V.11. This device is optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The four receivers share two ORed enable inputs, one active when high, the other active when low. Each receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ± 200 mV over a common-mode input voltage range of 12 V to -7 V. Fail-safe design ensures that if the inputs are open circuited, the output is always high. The SN55LBC173 is designed using the Texas Instruments proprietary LinBiCMOS™ technology that provides low power consumption, high switching speeds, and robustness.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinBiCMOS is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2013, Texas Instruments Incorporated



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	KGD	SN55LBC173MKGD1	NA
		SN55LBC173MKGD2	NA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
10.5 mils.	Silicon with backgrind	Floating	AlSi(1%)Cu(0.5%)TiW	1850 nm

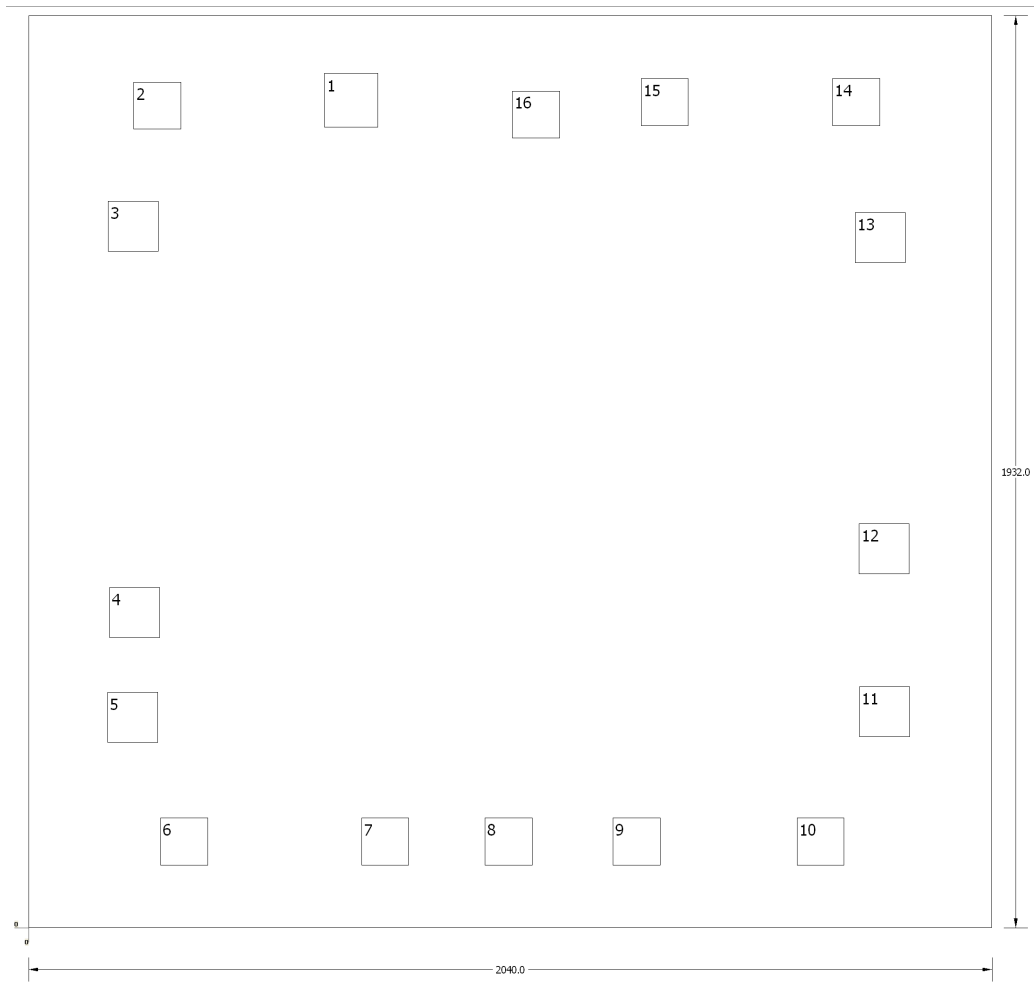


Table 1. Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
1B	1	626.5	1695	740.5	1809.5
1A	2	222.5	1690.7	323	1791.3
1Y	3	167.9	1432.1	274.8	1539
G	4	171.4	614.1	278.3	721
2Y	5	166.6	392.1	273.5	499
2A	6	279.2	132	379.7	232.6
2B	7	704.8	132	805.3	232.6
GND	8	966.2	132	1066.7	232.6
3B	9	1237.2	132	1337.7	232.6
3A	10	1626.7	132	1727.2	232.6
3Y	11	1758.7	403.7	1865.6	510.6
\bar{G}	12	1758.5	749	1865.4	855.9
4Y	13	1750.1	1408.4	1857	1515.3
4A	14	1702.2	1698.4	1802.7	1799
4B	15	1296.7	1698.4	1397.2	1799
VCC	16	1024.2	1671.9	1124.7	1772.5

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range unless otherwise noted

	Value	UNIT
V _{CC} Supply voltage range ⁽²⁾	–0.3 to 7	V
V _I Input voltage range, (A or B inputs)	±25	V
V _{ID} Differential input voltage ⁽³⁾	±25	V
Data and control voltage range	–0.3 to 7	V
T _A Operating free-air temperature range	–55 to 125	°C
T _{stg} Storage temperature range	–65 to 150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
V _{CC} Supply voltage	4.75	5	5.25	V
V _{IC} Common-mode input voltage	–7		12	
V _{IH} High-level input voltage	2			
V _{IL} Low-level input voltage			0.8	
V _{ID} Differential input voltage	–6		6	
I _{OH} High-level output current			–8	mA
I _{OL} Low-level output current			16	mA
T _A Operating free-air temperature	–55		125	°C

ELECTRICAL CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{IT+}	Positive-going input threshold voltage	I _O = -8 mA			0.2	V	
V _{IT-}	Negative-going input threshold voltage	I _O = 8 mA	-0.2			V	
V _{hys}	Hysteresis voltage (V _{IT+} - V _{IT-})			45		mV	
V _{IK}	Enable input clamp voltage	I _I = -18 mA		-0.9	-1.5	V	
V _{OH}	High-level output voltage	V _{ID} = -200 mV, I _{OH} = -8 mA	3.5	4.5		V	
V _{OL}	Low-level output voltage	V _{ID} = -200 mV, I _{OL} = 8 mA		0.3	0.5	V	
		V _{ID} = -200 mV, I _{OL} = 8 mA, T _A = 125°			0.7		
I _{OZ}	High-impedance-state output current	V _O = 0 V to V _{CC}			±20	μA	
I _I	Bus input current	A or B inputs	Other inputs at 0 V	V _{IH} = 12 V, V _{CC} = 5 V	0.7	1.15	mA
				V _{IH} = 12 V, V _{CC} = 0 V	0.8	1.15	
				V _{IH} = -7 V, V _{CC} = 5 V	-0.5	-0.9	
				V _{IH} = -7 V, V _{CC} = 0 V	-0.4	-0.9	
I _{IH}	High-level input current	V _{IH} = 5 V			±20	μA	
I _{IL}	Low-level input current	V _{IL} = 0 V			-20	μA	
I _{OS}	Short-circuit output current	V _O = 0			-80	-120	mA
I _{CC}	Supply current	Outputs enabled, I _O = 0, V _{ID} = 5 V			11	20	mA
		Outputs disabled			0.9	1.4	

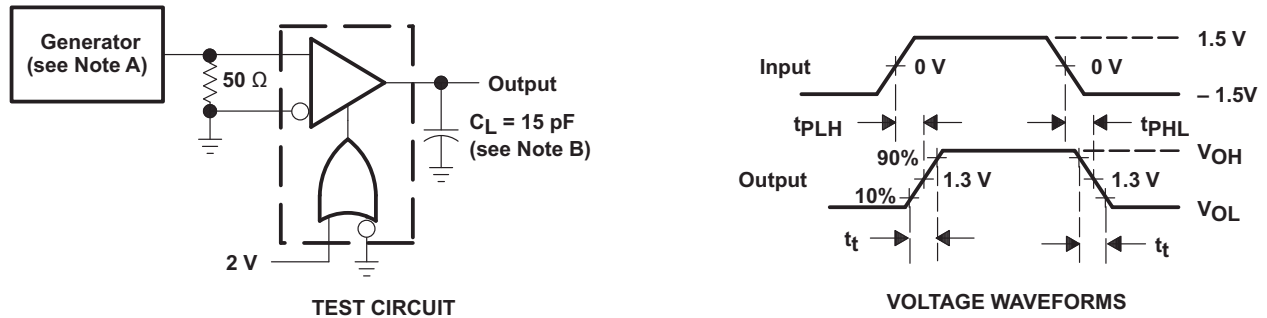
(1) All typical values are at 25°C and with a 5 V supply.

SWITCHING CHARACTERISTICS

V_{CC} = 5 V, C_L = 15 pF, over operating free-air temperature range (unless otherwise noted)

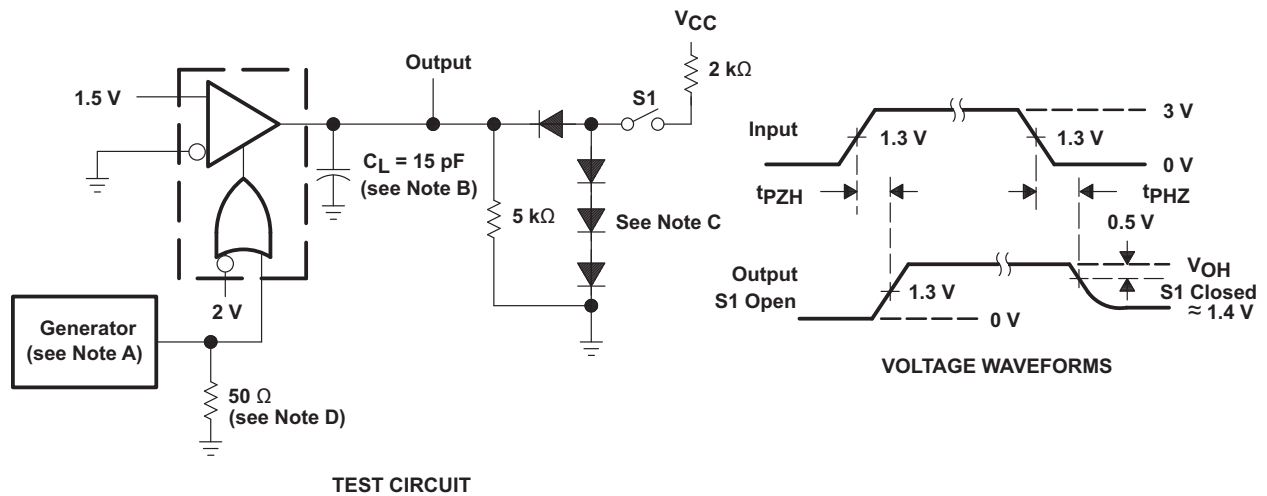
PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay time, high-to-low-level output	V _{ID} = -1.5 V to 1.5 V, See Figure 1	25°C	11	22	30	ns
			-55°C to 125°C	11		35	
t _{PLH}	Propagation delay time, low-to-high-level output	V _{ID} = -1.5 V to 1.5 V, See Figure 1	25°C	11	22	35	ns
			-55°C to 125°C	11		35	
t _{PZH}	Output enable time to high level	See Figure 2	25°C		17	40	ns
			-55°C to 125°C			45	
t _{PZL}	Output enable time to low level	See Figure 3	25°C		18	30	ns
			-55°C to 125°C			35	
t _{PHZ}	Output disable time from high level	See Figure 2	25°C		30	40	ns
			-55°C to 125°C			55	
t _{PLZ}	Output disable time from low level	See Figure 3	25°C		25	40	ns
			-55°C to 125°C			45	
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})	See Figure 1	25°C		0.5	6	ns
			-55°C to 125°C			7	
t _t	Transition time	See Figure 1	25°C		5	10	ns
			-55°C to 125°C			16	

PARAMETER MEASUREMENT INFORMATION



- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.

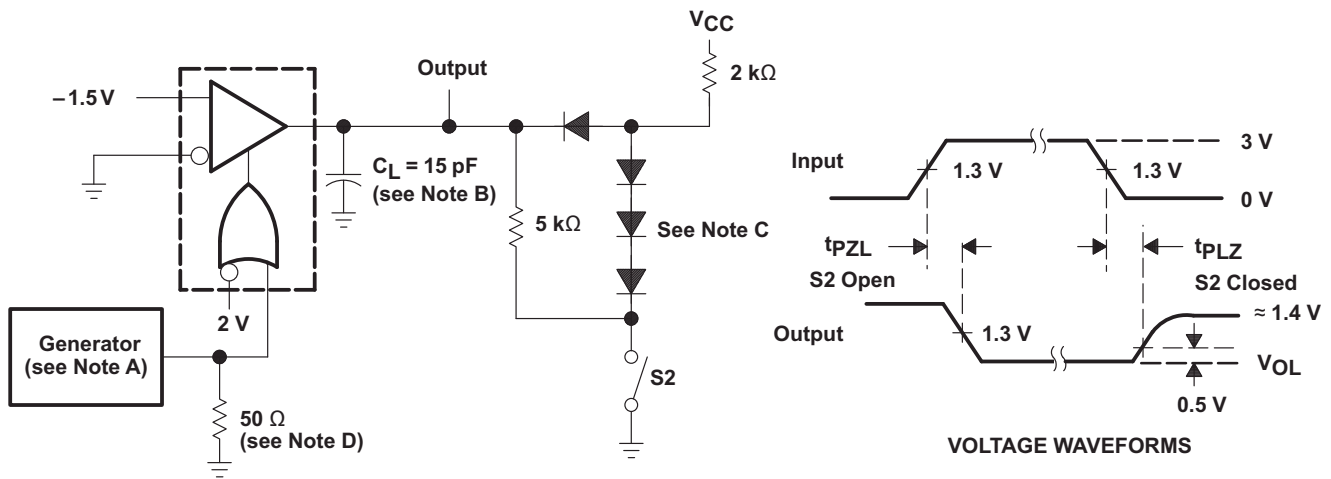
Figure 1. t_{pd} and t_t Test Circuit and Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N916 or equivalent.
- D. To test the active-low enable \overline{G} , ground G and apply an inverted input waveform to \overline{G} .

Figure 2. t_{pHZ} and t_{pZH} Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



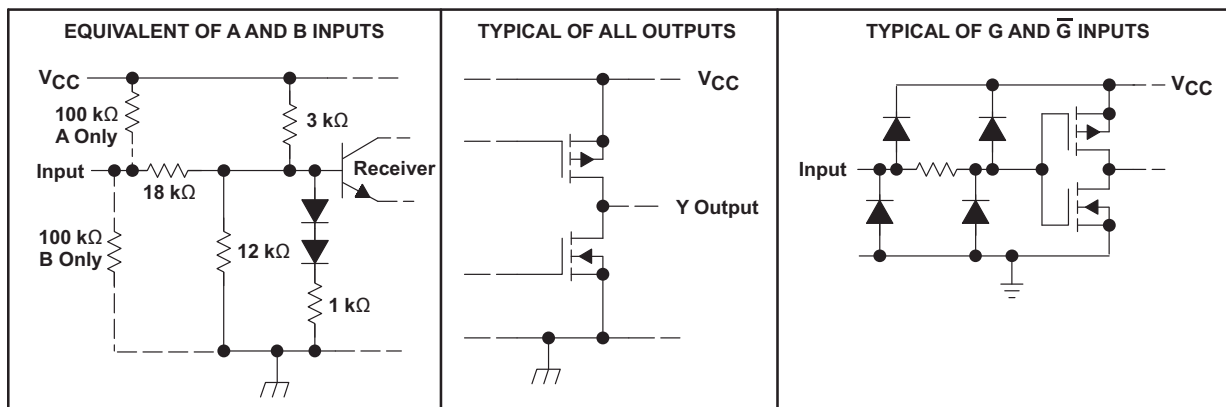
TEST CIRCUIT

- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N916 or equivalent.
- D. To test the active-low enable \overline{G} , ground G and apply an inverted input waveform to \overline{G} .

Figure 3. t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms

DEVICE INFORMATION

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



FUNCTION TABLE (EACH RECIEVER)

DIFFERENTIAL INPUTS	ENABLES		OUTPUT
	G	\bar{G}	
A - B			Y
$V_{ID} \geq 0.2 V$	H	X	H
	X	L	H
$-0.2 < V_{ID} < 0.2 V$	H	X	?
	X	L	?
$V_{ID} \leq -0.2 V$	H	X	L
	X	L	L
X	L	H	Z
Open circuit	H	X	H
	X	L	H

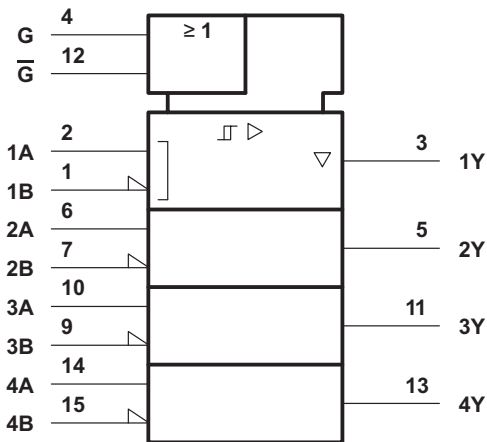


Figure 4. Logic Symbol

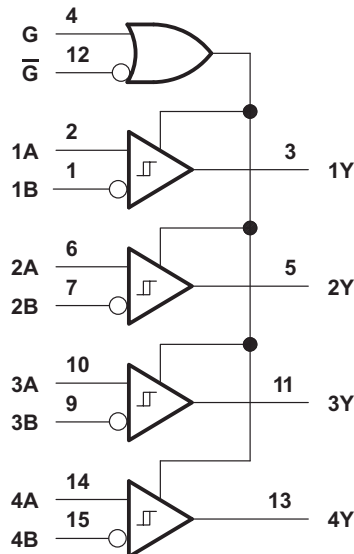


Figure 5. Logic Diagram (Positive Logic)

TYPICAL CHARACTERISTICS

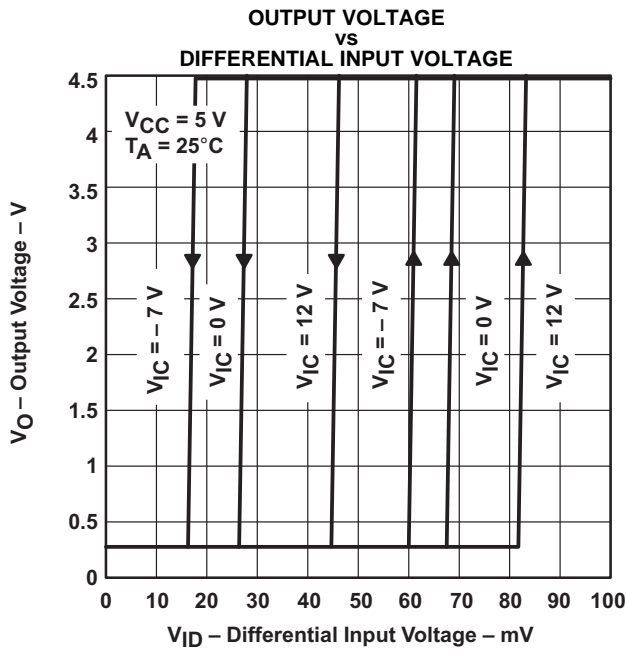


Figure 6.

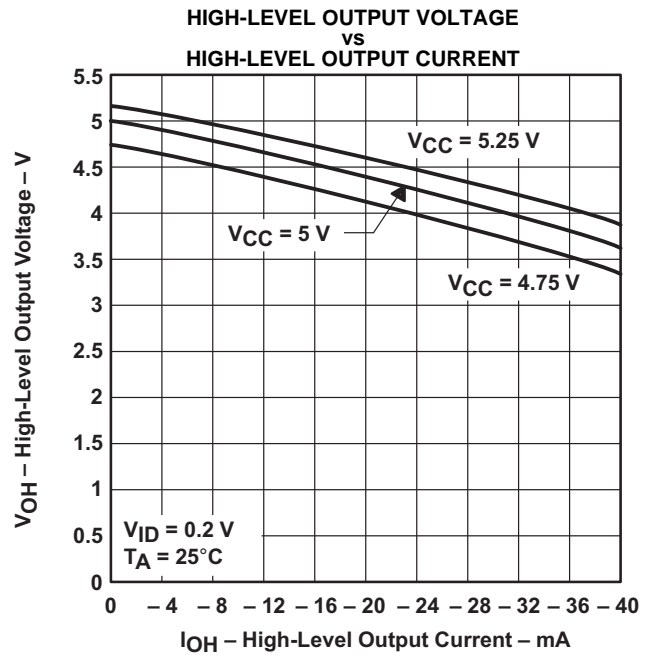


Figure 7.

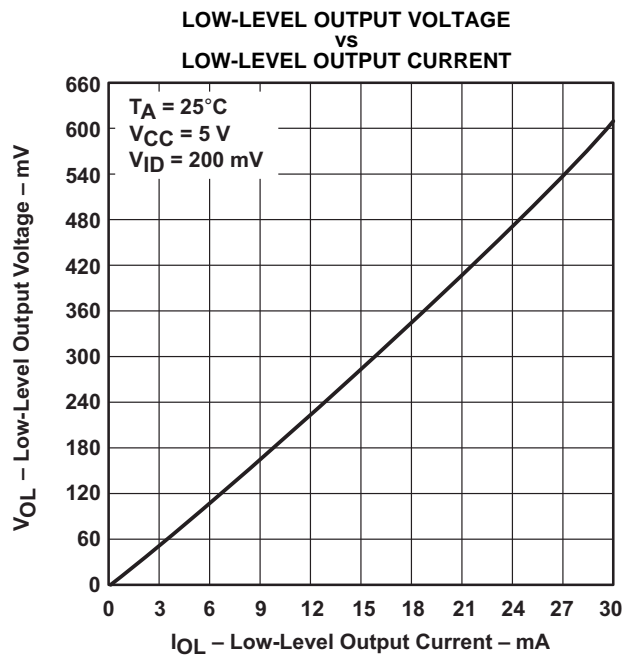


Figure 8.

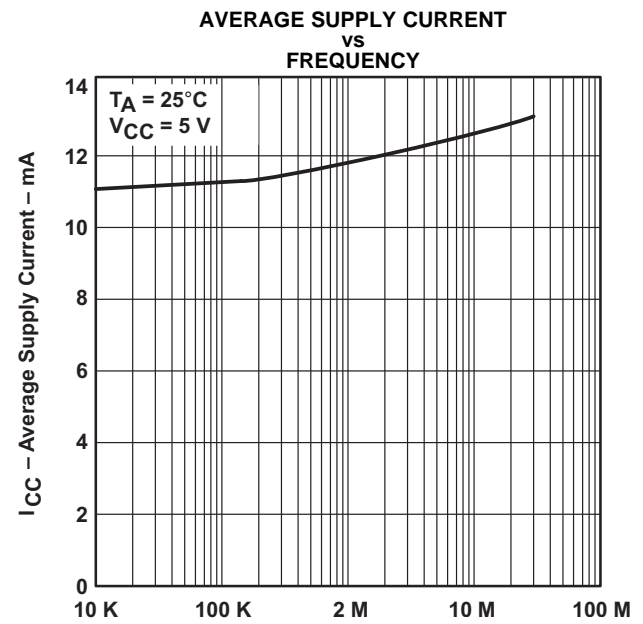
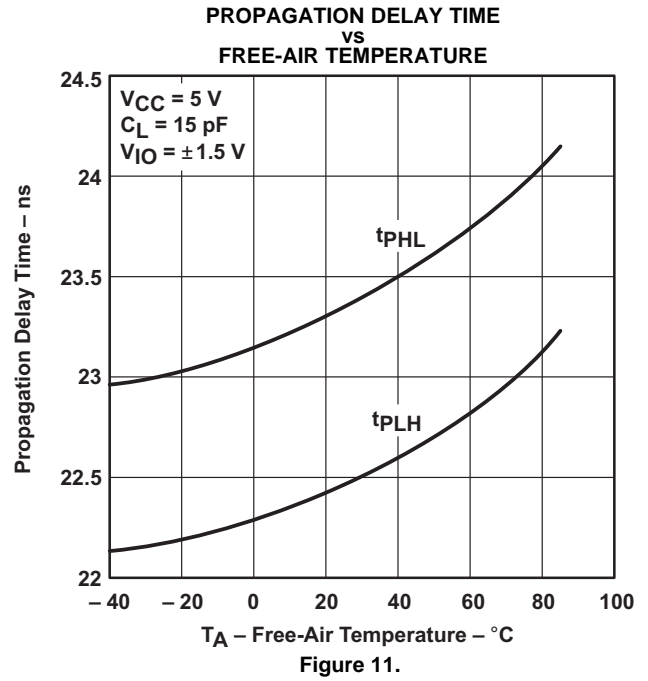
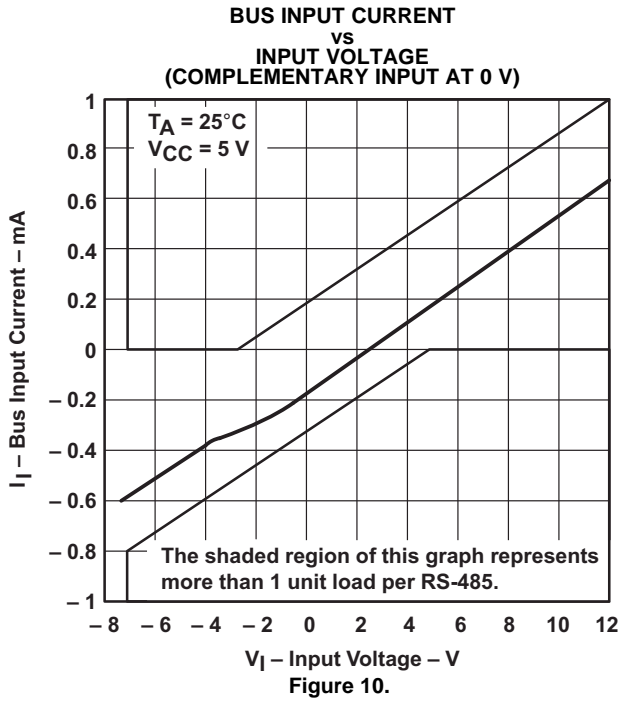


Figure 9.

TYPICAL CHARACTERISTICS (continued)



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN55LBC173MKGD1	ACTIVE	XCEPT	KGD	0	100	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125		Samples
SN55LBC173MKGD2	ACTIVE	XCEPT	KGD	0	10	TBD	Call TI	Call TI	-55 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated