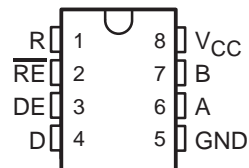


- **Meets or Exceeds the Requirements of TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27**
- **Recommended for PROFIBUS Applications**
- **Operates at Data Rates up to 35 MBaud**
- **Operating Temperature Range . . . -25°C to 85°C**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply-Current Requirement . . . 30 mA Max**
- **Wide Positive and Negative Input/Output Bus-Voltage Ranges**
- **Thermal-Shutdown Protection**
- **Driver Positive- and Negative-Current Limiting**
- **Receiver Input Hysteresis**
- **Glitch-Free Power-Up and Power-Down Protection**
- **Receiver Open-Circuit Fail-Safe Design**
- **Package Options Include Plastic Small-Outline (D) Package and (P) DIPs**

**D† OR P PACKAGE
(TOP VIEW)**



† The D package is available taped and reeled. Add the suffix R to the device type (e.g., SN65ALS1176DR).

description

The SN65ALS1176 differential bus transceiver is designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27.

The SN65ALS1176 combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The SN65ALS1176 is characterized for operation from -25°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN65ALS1176 DIFFERENTIAL BUS TRANSCEIVER

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Function Tables

DRIVERS

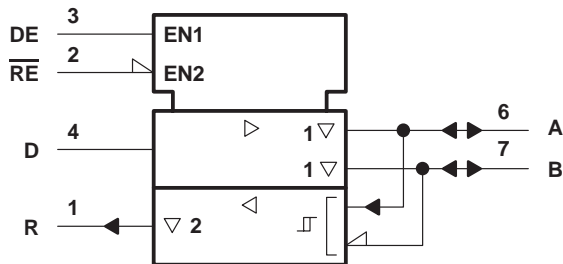
INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

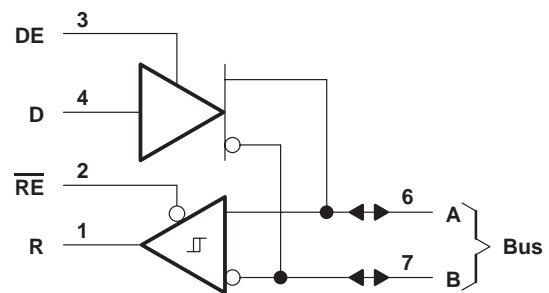
DIFFERENTIAL INPUTS A-B	ENABLE \overline{RE}	OUTPUT R
$V_{ID} \geq 0.2 V$	L	H
$-0.2 V < V_{ID} < 0.2 V$	L	?
$V_{ID} \leq -0.2 V$	L	L
X	H	Z
Inputs open	L	H

H = high level, L = low level, X = irrelevant,
? = Indeterminate, Z = high impedance (off)

logic symbol†

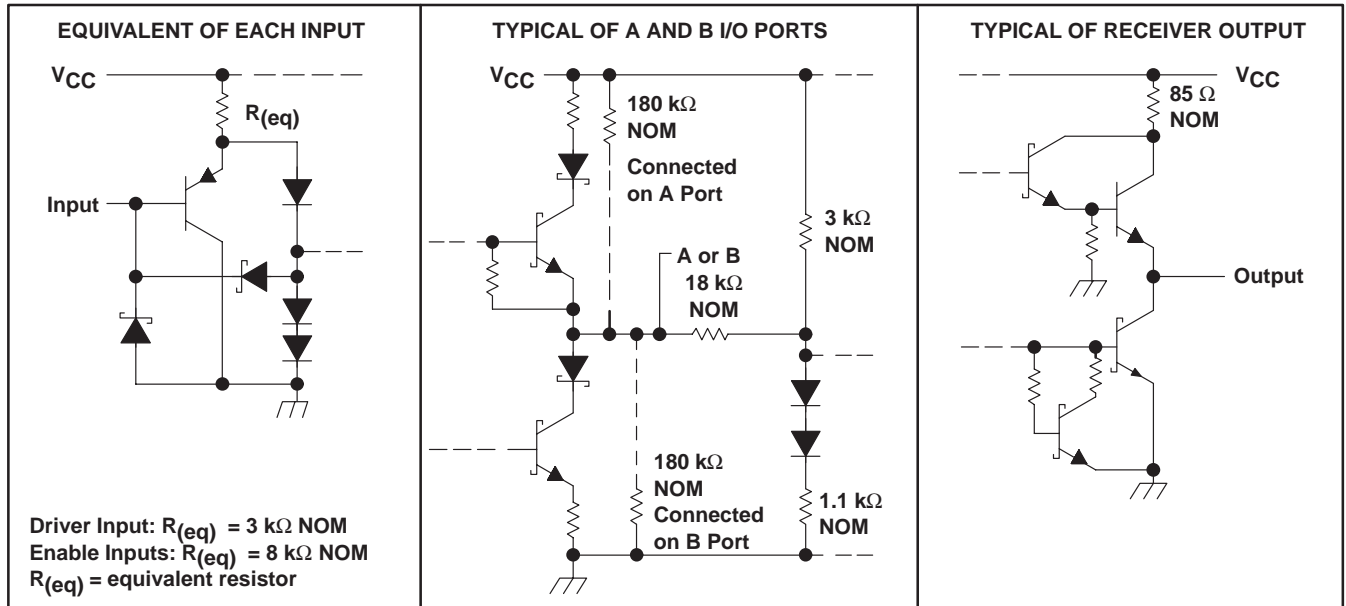


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Voltage range at any bus terminal	-7 V to 12 V
Enable input voltage, V_I	5.5 V
Package thermal impedance, θ_{JA} (see Note 2): D package	97°C/W
P package	85°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
 2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Input voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				-7	
High-level input voltage, V_{IH}	D, DE, and \overline{RE}	2			V
Low-level input voltage, V_{IL}	D, DE, and \overline{RE}			0.8	V
Differential input voltage, V_{ID} (see Note 3)				± 12	V
High-level output current, I_{OH}	Driver			-60	mA
	Receiver			-400	μ A
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		-25		85	°C

NOTE 3: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

SN65ALS1176 DIFFERENTIAL BUS TRANSCEIVER

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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITION†	MIN	TYP‡	MAX	UNIT	
V _{IK}	Input clamp voltage	I _I = -18 mA		-1.5	V	
V _O	Output voltage	I _O = 0		0	6	V
V _{OD1}	Differential output voltage	I _O = 0		1.5	6	V
V _{OD2}	Differential output voltage	R _L = 100 Ω, See Figure 1	1/2 V _{OD1} or 2§		V	
		R _L = 54 Ω, See Figure 1	2.1	2.5	5	V
V _{OD3}	Differential output voltage	V _{test} = -7 V to 12 V, See Figure 2		1.5	5	V
Δ V _{OD}	Change in magnitude of differential output voltage¶	R _L = 54 Ω or 100 Ω, See Figure 1		±0.2	V	
V _{OC}	Common-mode output voltage			3	-1	V
Δ V _{OC}	Change in magnitude of common-mode output voltage¶			±0.2		V
I _O	Output current	Outputs disabled, See Note 4	V _O = 12 V	1	mA	
			V _O = -7 V	-0.8		
I _{IH}	High-level input current	V _I = 2.4 V		20	μA	
I _{IL}	Low-level input current	V _I = 0.4 V		-400	μA	
I _{OS}	Short-circuit output current#	V _O = -4 V		-250	mA	
		V _O = 0		-150		
		V _O = V _{CC}		250		
		V _O = 8 V		250		
I _{CC}	Supply current	No load	Outputs enabled	23	30	mA
			Outputs disabled	19	26	

† The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.

§ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.

¶ Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from one logic state to the other.

Duration of the short circuit should not exceed one second for this test.

NOTE 4: This applies for both power on and power off; refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.



switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t _{d(OD)}	Differential output delay time	R _L = 54 Ω, See Figure 3	C _L = 50 pF,			15	ns
t _{sk(p)}	Pulse skew‡				0	2	ns
t _{t(OD)}	Differential output transition time				8		ns
t _{PZH}	Output enable time to high level	R _L = 110 Ω, See Figure 4	C _L = 50 pF,			80	ns
t _{PZL}	Output enable time to low level	R _L = 110 Ω, See Figure 5	C _L = 50 pF,			30	ns
t _{PHZ}	Output disable time from high level	R _L = 110 Ω, See Figure 4	C _L = 50 pF,			50	ns
t _{PLZ}	Output disable time from low level	R _L = 110 Ω, See Figure 5	C _L = 50 pF,			30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Pulse skew is defined as the |t_{PLH} – t_{PHL}| of each channel of the same device.

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V _O	V _{Oa} , V _{Ob}	V _{Oa} , V _{Ob}
V _{OD1}	V _O	V _O
V _{OD2}	V _t (R _L = 100 Ω)	V _t (R _L = 54 Ω)
V _{OD3}	None	V _t (test termination measurement 2)
Δ V _{OD}	V _t – V̄ _t	V _t – V̄ _t
V _{OC}	V _{os}	V _{os}
Δ V _{OC}	V _{os} – V̄ _{os}	V _{os} – V̄ _{os}
I _{OS}	I _{sa} , I _{sb}	None
I _O	I _{xa} , I _{xb}	I _{ia} , I _{ib}

SN65ALS1176

DIFFERENTIAL BUS TRANSCEIVER

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RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	V _O = 2.7 V,	I _O = -0.4 mA			0.2	V
V _{IT-}	Negative-going input threshold voltage	V _O = 0.5 V,	I _O = 8 mA	-0.2‡			V
V _{hys}	Hysteresis voltage (V _{IT+} - V _{IT-})				60		mV
V _{IK}	Enable-input clamp voltage	I _I = -18 mA				-1.5	V
V _{OH}	High-level output voltage	V _{ID} = 200 mV, See Figure 6	I _{OH} = -400 μA,		2.7		V
V _{OL}	Low-level output voltage	V _{ID} = -200 mV, See Figure 6	I _{OL} = 8 mA,			0.45	V
I _{OZ}	High-impedance-state output current	V _O = 0.4 V to 2.4 V				±20	μA
V _I	Line input current	Other input = 0 V, See Note 5	V _I = 12 V			1	mA
			V _I = -7 V			-0.8	
I _{IH}	High-level-enable input current	V _{IH} = 2.7 V				20	μA
I _{IL}	Low-level-enable input current	V _{IL} = 0.4 V				-100	μA
r _I	Input resistance			12	20		kΩ
I _{OS}	Short-circuit output current	V _{ID} = 200 mV,	V _O = 0	-15		-85	mA
I _{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 5: This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
t _{pd}	Propagation time	V _{ID} = -1.5 V to 1.5 V, See Figure 7	C _L = 15 pF,			25	ns	
t _{sk(p)}	Pulse skew§					0	2	ns
t _{pZH}	Output enable time to high level	C _L = 15 pF,	See Figure 8		11	18	ns	
t _{pZL}	Output enable time to low level				11	18	ns	
t _{PHZ}	Output disable time from high level						50	ns
t _{PLZ}	Output disable time from low level						30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Pulse skew is defined as the |t_{PLH} - t_{PHL}| of each channel of the same device.



PARAMETER MEASUREMENT INFORMATION

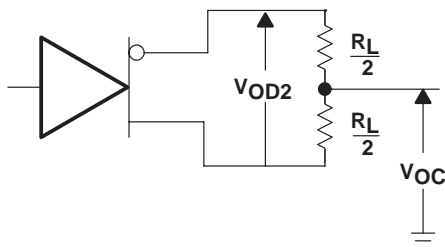


Figure 1. Driver V_{OD2} and V_{OC} Test Circuit

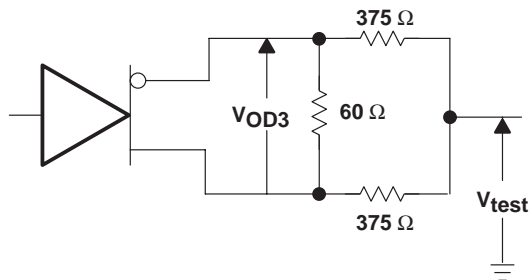
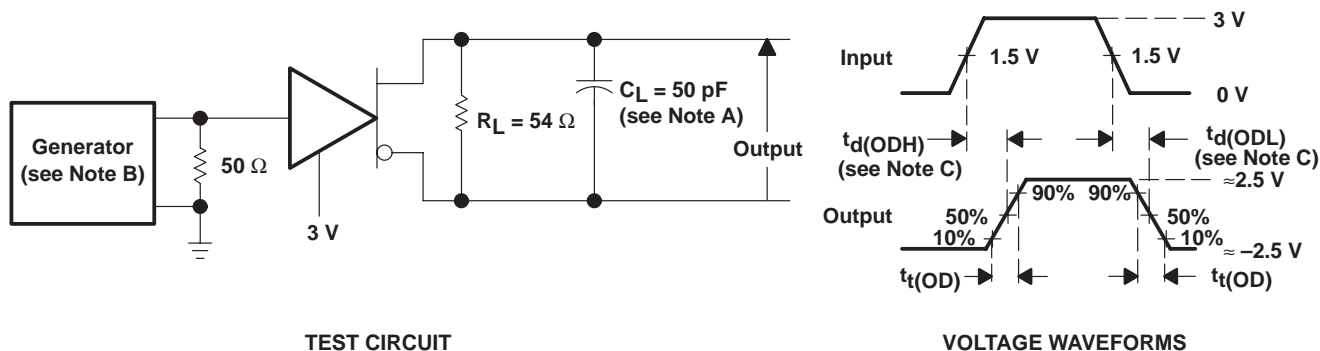


Figure 2. Driver V_{OD3} Test Circuit



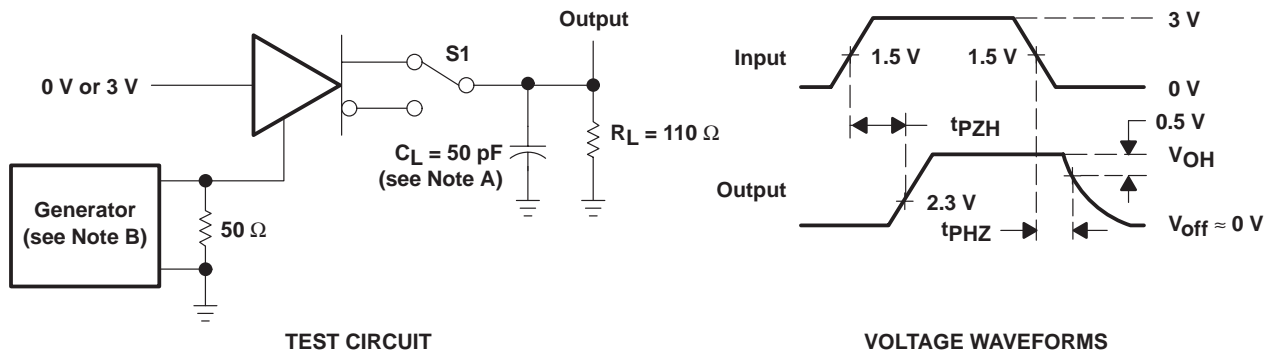
- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
 C. $t_d(OD) = t_d(ODH)$ or $t_d(ODL)$

Figure 3. Driver Differential-Output Delay and Transition Times

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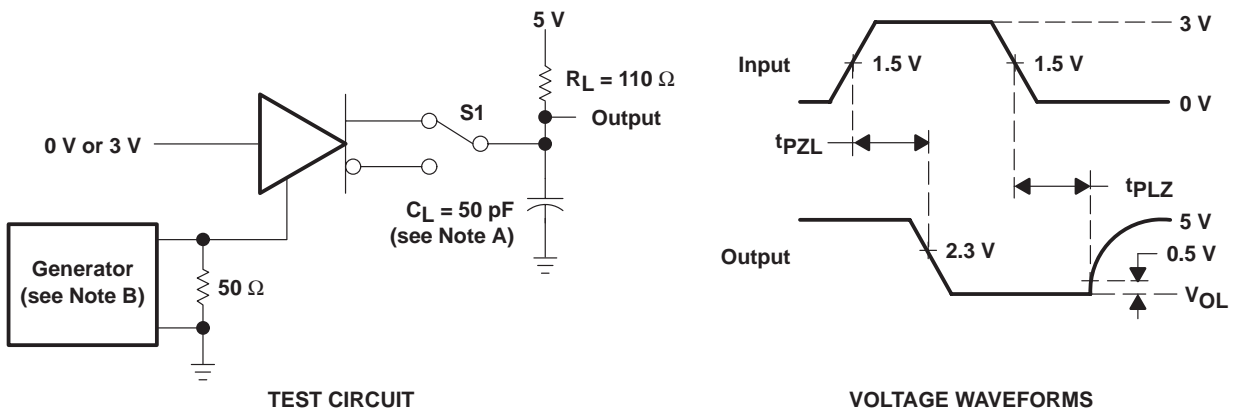
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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 4. Driver Enable and Disable Times



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 5. Driver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION

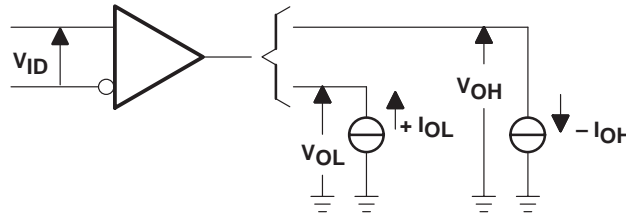
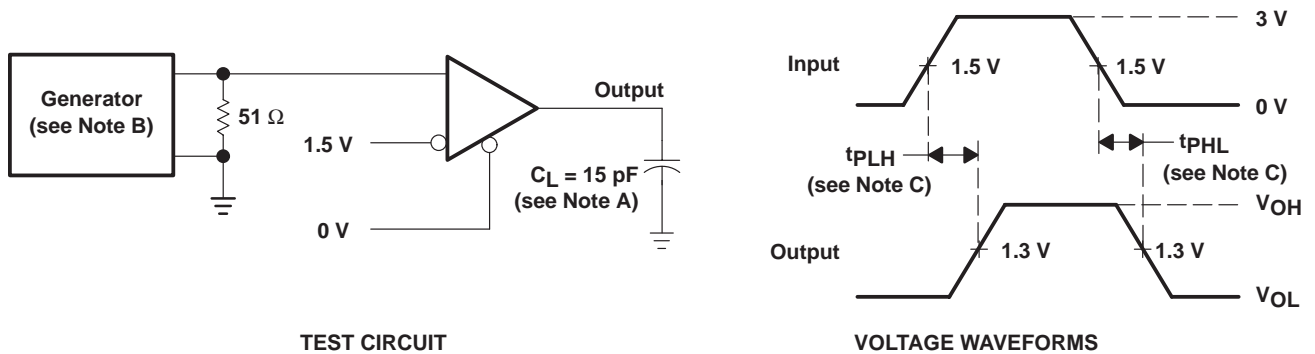


Figure 6. Receiver V_{OH} and V_{OL} Test Circuit



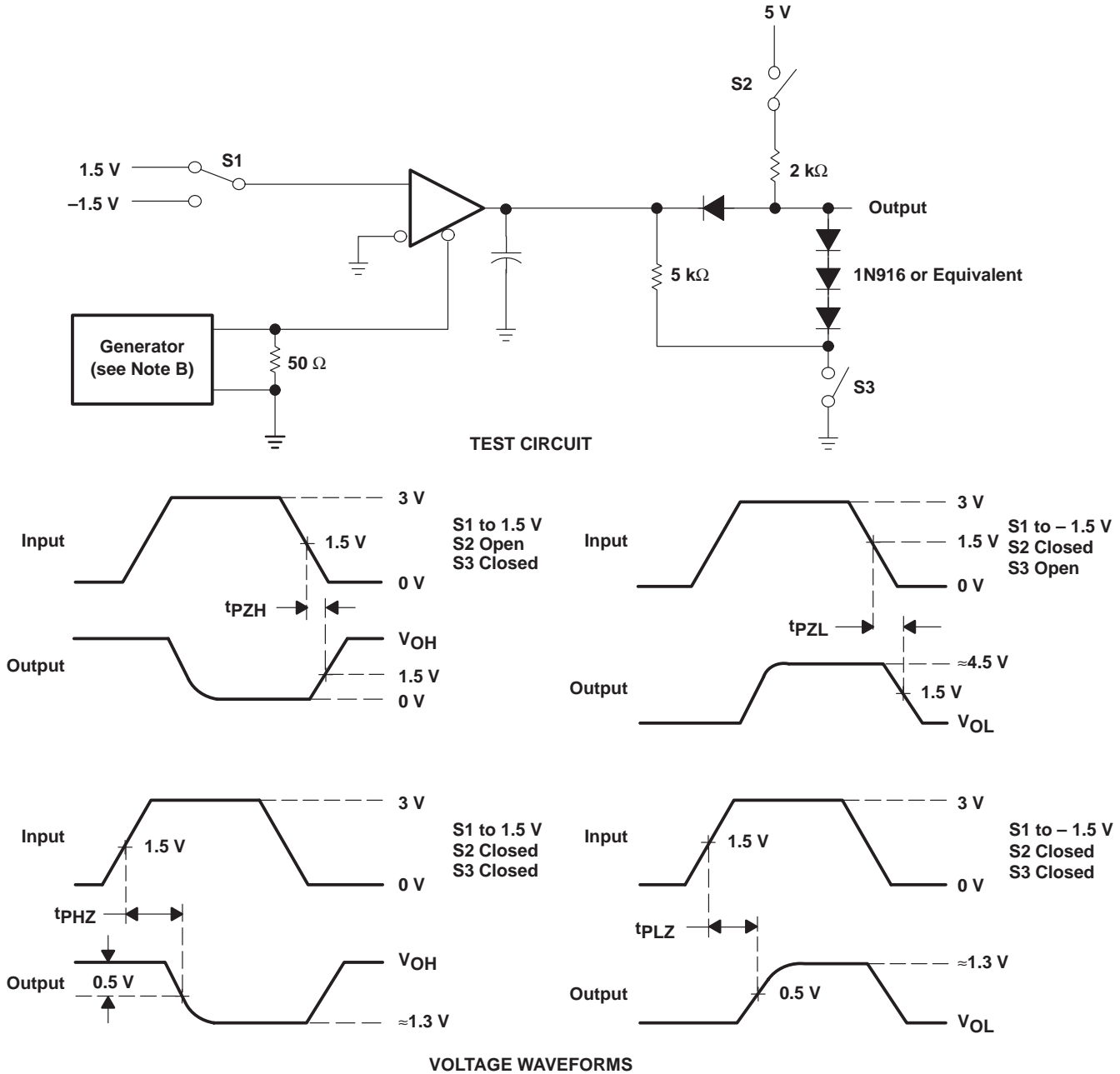
- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
 C. $t_{pd} = t_{PLH}$ or t_{PHL}

Figure 7. Receiver Propagation-Delay Times

SN65ALS1176 DIFFERENTIAL BUS TRANSCEIVER

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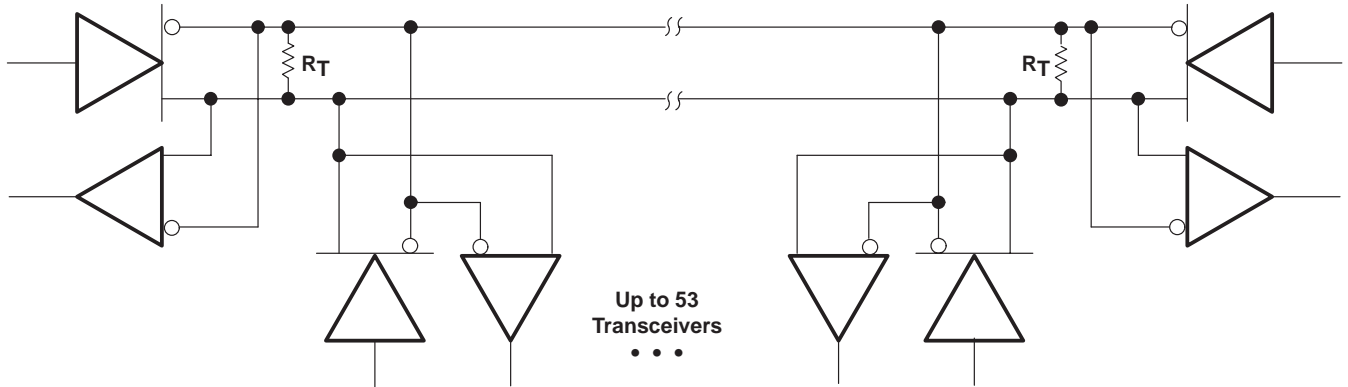
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.

Figure 8. Receiver Output Enable and Disable Times

APPLICATION INFORMATION



NOTE A: The line should terminate at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 9. Typical Application Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65ALS1176D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	6A1176	Samples
SN65ALS1176DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	6A1176	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ALS1176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ALS1176DR	SOIC	D	8	2500	340.5	338.1	20.6



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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