

SN65EPT22 3.3 V Dual LVTTTL/LVCMOS to Differential LVPECL Buffer

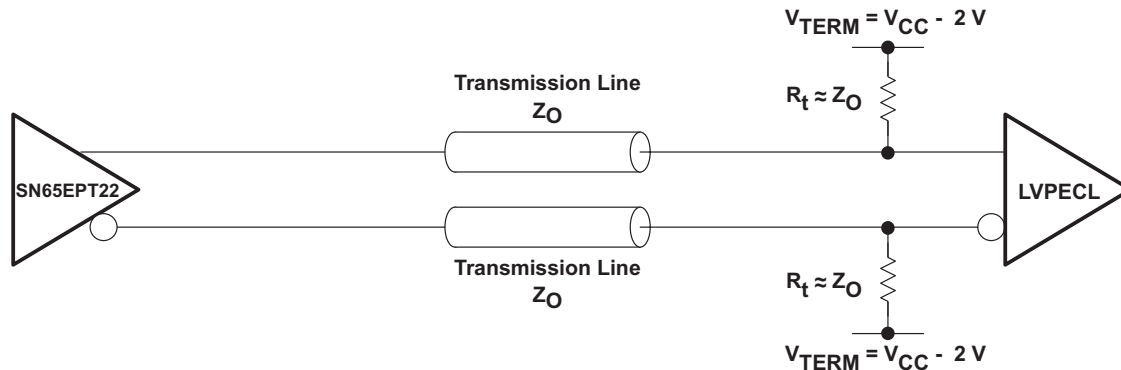
1 Features

- Dual 3.3V LVTTTL to LVPECL Buffer
- Operating Range
 - LVPECL $V_{CC} = 3.0\text{ V}$ to 3.6 V With $GND = 0\text{ V}$
- Support for Clock Frequencies to 2.0 GHz (typ)
- 420 ps Typical Propagation Delay
- Deterministic HIGH Output Value for Open Input Conditions
- Built-in Temperature Compensation
- Drop in Compatible to MC100ELT23
- PNP Single Ended Inputs for Minimal Loading

2 Applications

- Data and Clock Transmission Over Backplane
- Signaling Level Conversion

4 Simplified Schematic



3 Description

The SN65EPT22 is a low power dual LVTTTL to LVPECL translator device. The device includes circuitry to maintain known logic HIGH level when inputs are in open condition. The SN65EPT22 is housed in an industry standard SOIC-8 package and is also available in TSSOP-8 package option.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|-----------------|
| SN65EPT22 | SOIC (8) | 4.90mm x 3.91mm |
| | VSSOP (8) | 3.00mm x 3.00mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Table of Contents

| | | | |
|--|----------|---|----------|
| 1 Features | 1 | 7.5 Key Attributes..... | 4 |
| 2 Applications | 1 | 7.6 TTL Input DC Characteristics | 4 |
| 3 Description | 1 | 7.7 PECL Output DC Characteristics | 5 |
| 4 Simplified Schematic | 1 | 7.8 AC Characteristics | 5 |
| 5 Revision History | 2 | 7.9 Typical Characteristics..... | 7 |
| 6 Pin Configuration and Functions | 3 | 8 Device and Documentation Support | 8 |
| 7 Specifications | 3 | 8.1 Trademarks | 8 |
| 7.1 Absolute Maximum Ratings | 3 | 8.2 Electrostatic Discharge Caution..... | 8 |
| 7.2 Handling Ratings | 3 | 8.3 Glossary..... | 8 |
| 7.3 Power Dissipation Ratings | 4 | 9 Mechanical, Packaging, and Orderable Information | 8 |
| 7.4 Thermal Information | 4 | | |

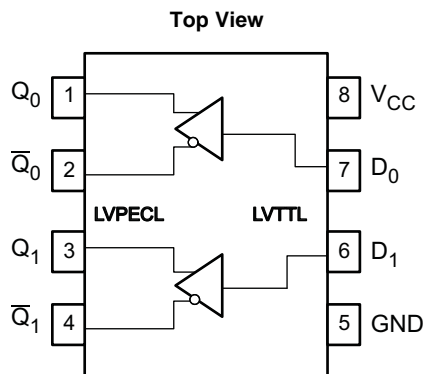
5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (November 2010) to Revision B | Page |
|---|-------------|
| • Deleted the Ordering Information table | 1 |
| • Added the Device Information table | 1 |
| • Added the Simplified Schematic | 1 |
| • Added the Handling Ratings | 3 |
| • Added the Device and Documentation Support and Mechanical, Packaging, and Orderable Information | 8 |

| Changes from Original (November 2010) to Revision A | Page |
|---|-------------|
| • Changed SN65EPT22 to EPT22 (2 places) in Ordering Information Table under Part Marking column | 1 |

6 Pin Configuration and Functions



Pin Functions

| PIN | FUNCTION |
|---|--------------------|
| D ₀ , D ₁ | LVTTTL data inputs |
| Q ₀ , \bar{Q}_0 , Q ₁ , \bar{Q}_1 | LVPECL outputs |
| V _{CC} | Positive supply |
| GND | Ground |

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

| PARAMETER | CONDITION | MIN | MAX | UNIT |
|--|--|-----|-----|------|
| Absolute supply voltage, V _{CC} | | | 6 | V |
| Absolute input voltage, V _I | GND = 0 and V _I ≤ V _{CC} | 0 | 6 | V |
| Supply voltage LVPECL | | | 3.3 | V |
| Output current | Continuous | | 50 | mA |
| | Surge | | 100 | |
| Operating temperature range | | -40 | 85 | °C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

| | | MIN | MAX | UNIT | |
|--------------------|---------------------------|--|-----|------|----|
| T _{stg} | Storage temperature range | -65 | 150 | °C | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | -4 | 4 | kV |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | -2 | 2 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Power Dissipation Ratings

| PACKAGE | CIRCUIT BOARD MODEL | POWER RATING $T_A < 25^\circ\text{C}$ (mW) | THERMAL RESISTANCE, JUNCTION TO AMBIENT NO AIRFLOW | DERATING FACTOR $T_A > 25^\circ\text{C}$ (mW/°C) | POWER RATING $T_A = 85^\circ\text{C}$ (mW) |
|---------|---------------------|--|--|--|--|
| D | Low-K | 719 | 139 | 7 | 288 |
| | High-K | 840 | 119 | 8 | 336 |
| DGK | Low-K | 469 | 213 | 5 | 188 |
| | High-K | 527 | 189 | 5 | 211 |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | D | DGK | UNIT |
|-------------------------------|--------------------------------------|--------|--------|------|
| | | 8 PINS | 8 PINS | |
| $R_{\theta\text{JB}}$ | Junction-to-board thermal resistance | 79 | 120 | °C/W |
| $R_{\theta\text{JC}}$ | Junction-to-case thermal resistance | 98 | 74 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Key Attributes

| CHARACTERISTICS | VALUE |
|---|-----------------------|
| Moisture sensitivity level | Lead free package |
| | SOIC-8 |
| | VSSOP-8 |
| Flammability rating (Oxygen Index: 28 to 34) | UL 94 V-0 at 0.125 in |
| Meets or exceeds JEDEC Spec EIA/JESD78 latchup test | |

7.6 TTL Input DC Characteristics⁽¹⁾

($V_{\text{CC}} = 3.3\text{ V}$, $\text{GND} = 0$, $T_A = -40^\circ\text{C}$ to 85°C)

| CHARACTERISTIC | | CONDITION | MIN | TYP | MAX | UNIT |
|------------------|------------------------|---------------------------------|-----|-----|------|------|
| I_{IH} | Input HIGH current | $V_{\text{IN}} = 2.7\text{ V}$ | | | 20 | μA |
| I_{IHH} | Input HIGH current max | $V_{\text{IN}} = V_{\text{CC}}$ | | | 100 | μA |
| I_{IL} | Input LOW current | $V_{\text{IN}} = 0.5\text{ V}$ | | | -0.6 | mA |
| V_{IK} | Input clamp voltage | $I_{\text{IN}} = -18\text{ mA}$ | | | -1 | V |
| V_{IH} | Input high voltage | | 2.0 | | | V |
| V_{IL} | Input low voltage | | | | 0.8 | V |

(1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7.7 PECL Output DC Characteristics⁽¹⁾

($V_{CC} = 3.3\text{ V}$; $GND = 0.0\text{ V}$)⁽²⁾

| CHARACTERISTIC | -40°C | | | 25°C | | | 85°C | | | UNIT |
|---|-------|------|------|------|------|------|------|------|------|------|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| I_{CC} Power supply current | | 39 | 45 | | 42 | 47 | | 45 | 50 | mA |
| V_{OH} Output HIGH voltage ⁽³⁾ | 2155 | 2224 | 2405 | 2155 | 2224 | 2405 | 2155 | 2224 | 2405 | mV |
| V_{OL} Output LOW voltage ⁽³⁾ | 1355 | 1441 | 1605 | 1355 | 1438 | 1605 | 1355 | 1435 | 1605 | mV |

- (1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Output parameters vary 1:1 with V_{CC}
- (3) All loading with 50Ω to $V_{CC} - 2.0\text{ V}$

7.8 AC Characteristics⁽¹⁾

($V_{CC} = 3.0\text{ V to } 3.6\text{ V}$; $GND = 0\text{ V}$)⁽²⁾

| CHARACTERISTIC | -40°C | | | 25°C | | | 85°C | | | UNIT | |
|---|--------------------------------------|-----|-----|------|-----|-----|------|-----|-----|------|----|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | |
| f_{MAX} Max switching frequency ⁽³⁾ , see Figure 5 | | 2.1 | | | 2.0 | | | 2.0 | | GHz | |
| t_{PLH} / t_{PHL} Propagation delay to differential output | 230 | | 550 | 230 | | 550 | 230 | | 550 | ps | |
| t_{SKEW} | Within device skew ⁽⁴⁾ | | 25 | 50 | 25 | | 50 | 25 | | 50 | ps |
| | Device to device skew ⁽⁵⁾ | | 100 | 200 | 100 | | 200 | 100 | | 200 | ps |
| t_{JITTER} Random clock jitter (RMS) | | 0.2 | 0.8 | | 0.2 | 0.8 | | 0.2 | 0.8 | ps | |
| t_r / t_f Output rise/fall times (20%–80%) | 150 | | 300 | 150 | | 300 | 150 | | 300 | ps | |

- (1) Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Measured using a 2.4 V source, 50% duty cycle clock source. All loading with 50Ω to $V_{CC} - 2.0\text{ V}$.
- (3) Maximum switching frequency measured at output amplitude of 300 mV_{pp} .
- (4) Skew is measured between outputs under identical transitions and conditions on any one device.
- (5) Device-to-Device Skew for identical transitions at identical V_{CC} levels.

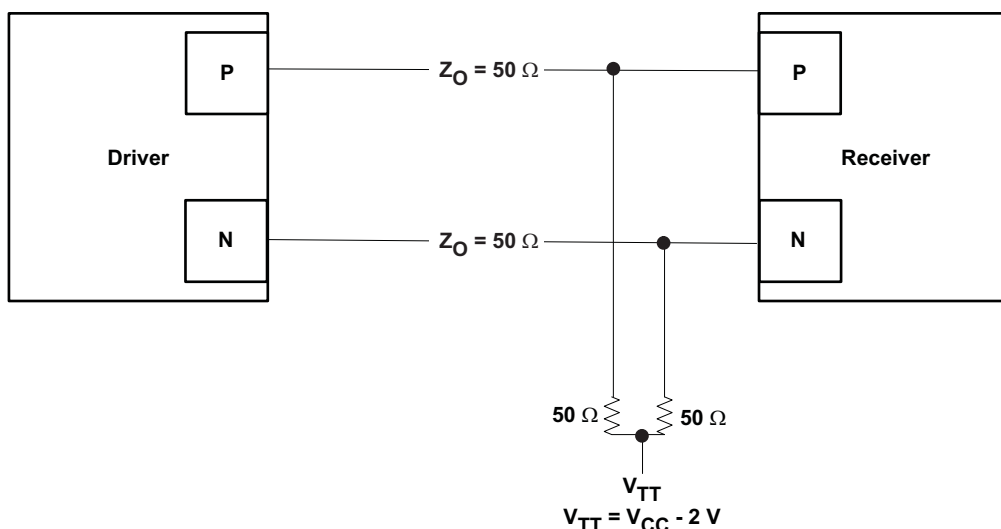


Figure 1. Termination for Output Driver

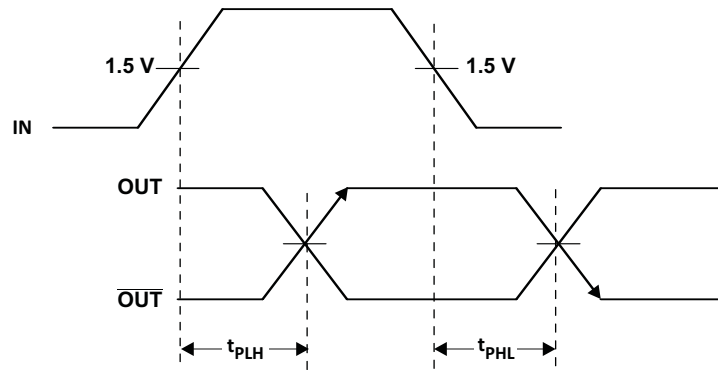


Figure 2. Output Propagation Delay

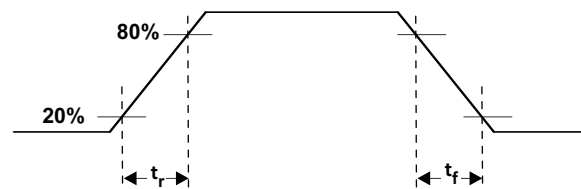


Figure 3. Output Rise and Fall Times

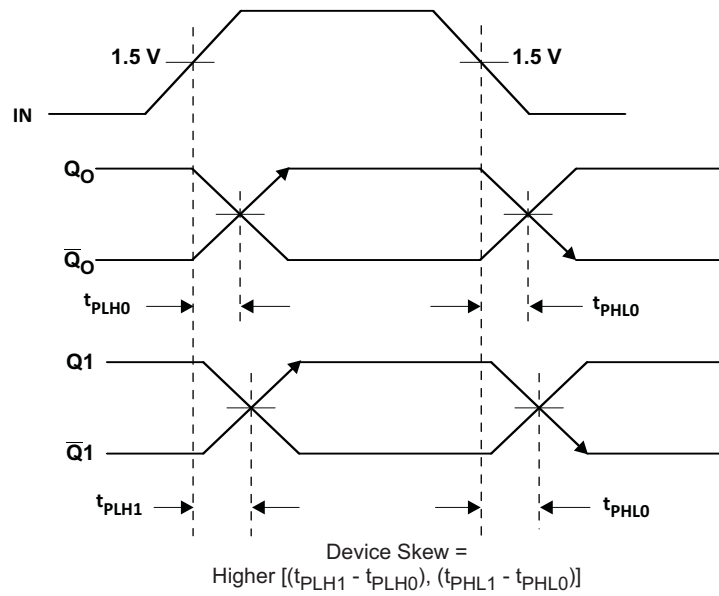


Figure 4. Device Skew

7.9 Typical Characteristics

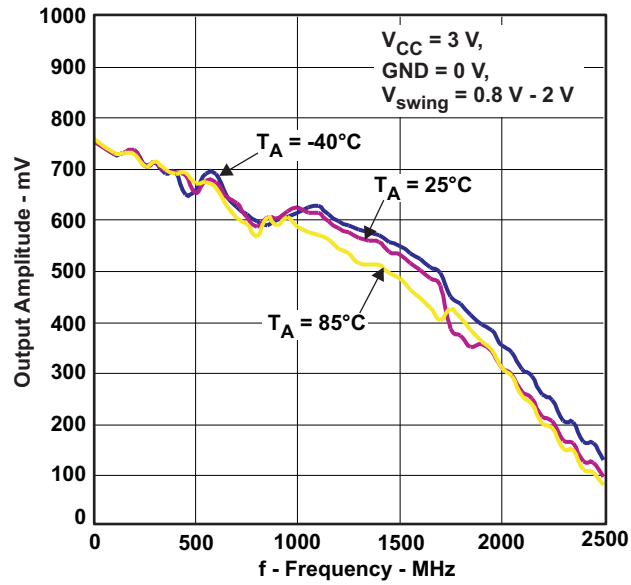


Figure 5. Output Amplitude versus Frequency

8 Device and Documentation Support

8.1 Trademarks

All trademarks are the property of their respective owners.

8.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN65EPT22D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | EPT22 | Samples |
| SN65EPT22DGK | ACTIVE | VSSOP | DGK | 8 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SIQI | Samples |
| SN65EPT22DGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SIQI | Samples |
| SN65EPT22DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | EPT22 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65EPT22DGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| SN65EPT22DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

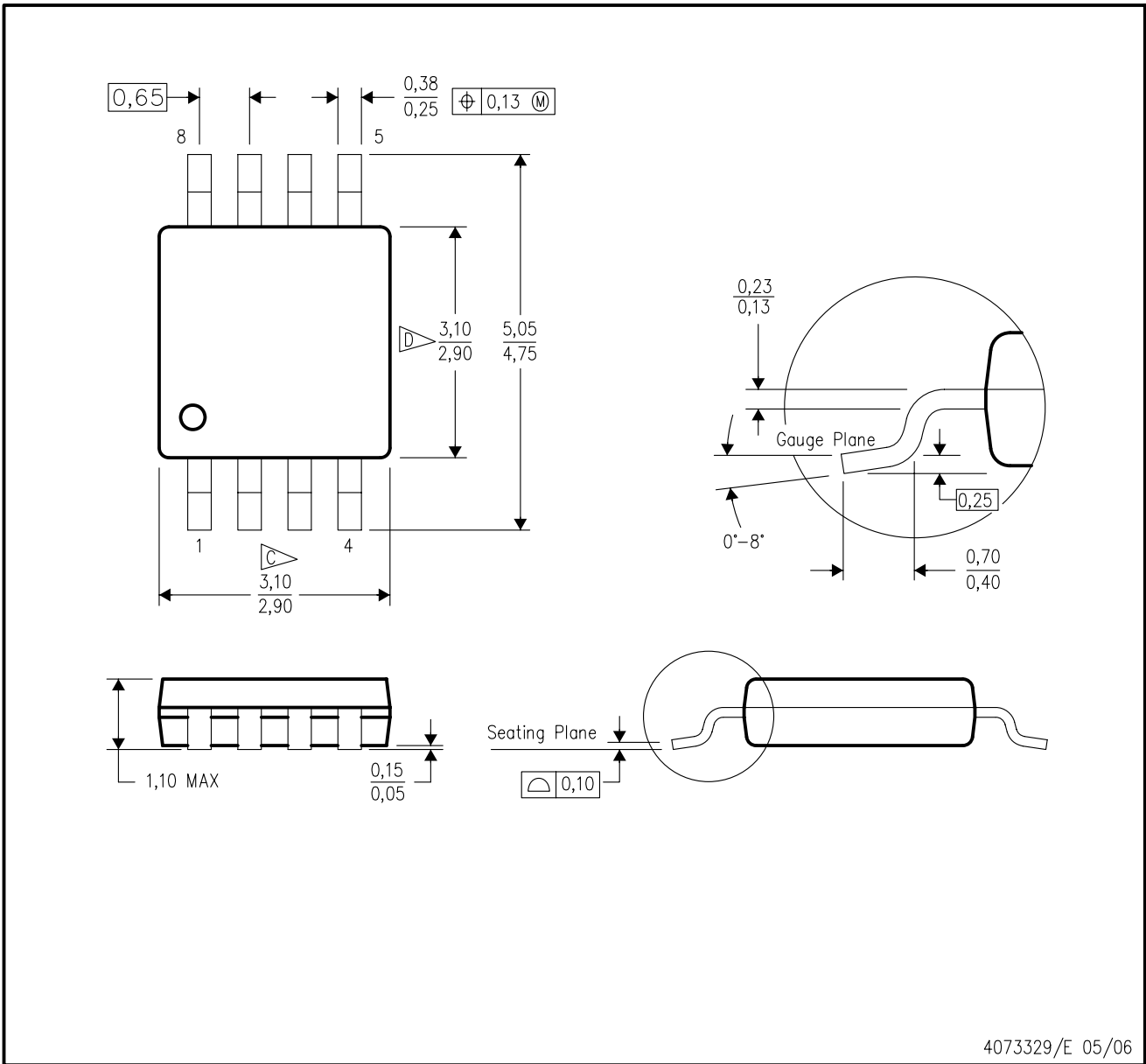
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65EPT22DGKR | VSSOP | DGK | 8 | 2500 | 853.0 | 449.0 | 35.0 |
| SN65EPT22DR | SOIC | D | 8 | 2500 | 853.0 | 449.0 | 35.0 |

DGK (S-PDSO-G8)

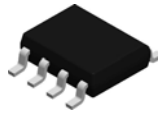
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated