TEXAS INSTRUMENTS

SN55HVD251, SN65HVD251

SLLS545G – NOVEMBER 2002 – REVISED OCTOBER 2015

SNx5HVD251 Industrial CAN Bus Transceiver

1 Features

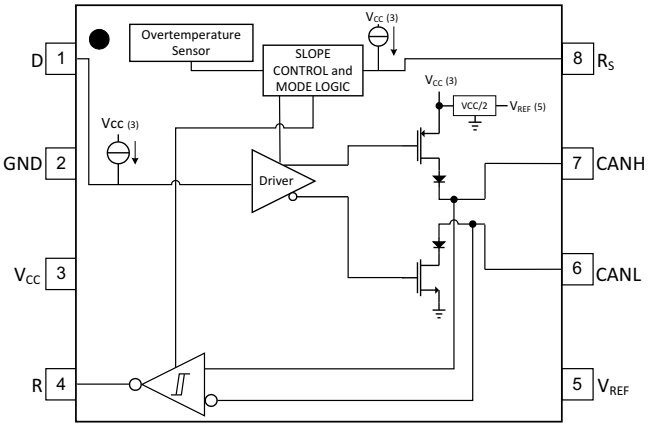
- Drop-In Improved Replacement for the PCA82C250 and PCA82C251
- Bus-Fault Protection of ±36 V
- Meets or Exceeds ISO 11898
- Signaling Rates(1) up to 1 Mbps
- High Input Impedance Allows up to 120 Nodes on a Bus
- Bus Pin ESD Protection Exceeds 14 kV HBM
- Unpowered Node Does Not Disturb the Bus
- Low-Current Standby Mode: 200-µA Typical
- Thermal Shutdown Protection
- Glitch-Free Power-Up and Power-Down CAN Bus Protection for Hot-Plugging
- DeviceNet Vendor ID #806

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in bps (bits per second).

2 Applications

- CAN Data Buses
- Industrial Automation
- SAE J1939 Standard Data Bus Interface
- NMEA 2000 Standard Data Bus Interface

Block Diagram



3 Description

The HVD251 is intended for use in applications employing the Controller Area Network (CAN) serial communication physical layer in accordance with the ISO 11898 Standard. The HVD251 provides differential transmit capability to the bus and differential receive capability to a CAN controller at speeds up to 1 megabits per second (Mbps).

Designed for operation in harsh environments, the device features cross-wire, overvoltage and loss of ground protection to ±36 V. Also featured are overtemperature protection as well as –7-V to 12-V common-mode range, and tolerance to transients of ±200 V. The transceiver interfaces the single-ended CAN controller with the differential CAN bus found in industrial, building automation, and automotive applications.

Rs, pin 8, selects one of three different modes of operation: high-speed, slope control, or low-power mode. The high-speed mode of operation is selected by connecting pin 8 to ground, allowing the transmitter output transistors to switch as fast as possible with no limitation on the rise and fall slope. The rise and fall slope can be adjusted by connecting a resistor to ground at pin 8; the slope is proportional to the pin's output current. Slope control with an external resistor value of 10 kΩ gives about 15-V / µs slew rate; 100 kΩ gives about 2-V/µs slew rate.

If a high logic level is applied to the Rs pin 8, the device enters a low-current standby mode where the driver is switched off and the receiver remains active. The local protocol controller returns the device to the normal mode when it transmits to the bus.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN55HVD251	WSON (8)	4.00 mm × 4.00 mm
SN65HVD251	SOIC (8)	4.90 mm × 3.91 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (June 2015) to Revision G — **Page**

- Changed the value of HBM "All pins" From: ±14000 V To: ±6000 V. Changed the value of "CANH, CANL and GND" From: ±6000 V To: ±14000 V in the *ESD Ratings* ... 4

Changes from Revision E (March 2010) to Revision F — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed the location of section "6.12 VREF-Pin Characteristics" to section 6.8 ... 6

Changes from Revision C (September 2005) to Revision D — **Page**

- Added device SN55HVD251 ... 1
- Added the DRJ Package. ... 1
- Changed the data sheet title From: CAN TRANSCEIVER To: INDUSTRIAL CAN TRANSCEIVER ... 1
- Deleted APPLICATIONS bullets: DeviceNet™ Data Buses, Smart Distributed Systems (SDS™), and ISO 11783 Standard Data Bus Interface ... 1
- Deleted last paragraph from the DESCRIPTION - "The HVD251 may be used..." ... 1
- Added Electrical fast transient/burst to the Abs Max Ratings table ... 4
- Deleted the condition - over recommended operating conditions (unless otherwise noted). From the RECOMMENDED OPERATING CONDITIONS table ... 5
- Added SN55HVD251 to the Operating free-air temperature, T_A in the ROC table ... 5
- Added DRJ to the Junction-to-case thermal resistance ... 5
- Added DRJ to the Junction-to-board thermal resistance ... 5

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- Added the SUPPLY CURRENT table 5
- Deleted ICC - Supply current from the DRIVER ELECTRICAL CHARACTERISTICS 5
- Added T ≥ -40°C to $V_{O(D)}$ Test Conditions in the DRIVER ELECTRICAL CHARACTERISTICS 5
- Added R_{NODE} = 330 Ω to Differential output voltage (Dominant) (second line of Test Conditions) in the DRIVER ELECTRICAL table 5
- Added a third line of Test Conditions to Differential output voltage (Dominant) in the DRIVER ELECTRICAL table 5
- Added T ≤ 85°C to $V_{OD®)}$ Test Conditions in the DRIVER ELECTRICAL CHARACTERISTICS 5
- Deleted ICC - Supply current from the RECEIVER ELECTRICAL CHARACTERISTICS 6
- Added Receiver noise rejection row to the RECEIVER ELECTRICAL CHARACTERISTIC table 6
- Added TYP values to the Differential output signal rise and fall times in the DRIVER SWITCHING CHARACTERISTIC table 7
- Changed table title From: ABSOLUTE MAXIMUM POWER DISSIPATION RATINGS To: PACKAGE DISSIPATION RATINGS 8
- Added the SON (DRJ) option to the PACKAGE DISSIPATION RATINGS table 8
- Changed Figure 1 title From: $t_{LOOP1-LOOP}$ TIME To: RECESSIVE-TO-DOMINANT LOOP DELAY 9
- Changed Figure 2 title From: $t_{LOOP2-LOOP}$ TIME To: DOMINANT-TO-RECESSIVE LOOP DELAY 9
- Changed Figure 4 From: DRIVER LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE To: DRIVER OUTPUT VOLTAGE vs OUTPUT CURRENT 9
- Changed Figure 5 From: DRIVER HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE To: DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT CURRENT 9
- Changed Figure 8 title From: DIFFERENTIAL OUTPUT FALL TIME To: DIFFERENTIAL OUTPUT TRANSITION TIME 9
- Changed Figure 12 - Driver V_{OD}, label R_{NODE} was 330Ω±1% 11
- Changed Table 1 header From: MEASURED To: DIFFERENTIAL INPUT 13
- Added Note B to Figure 22 16
- Added a row (X Open) to Table 2 - Driver 19

Changes from Revision B (September 2003) to Revision C **Page**

- Changed the front page format 1
- Changed Junction temperature, T_J - SOIC Package MAX value From 150°C To: 145°C 5
- Changed the THERMAL CHARACTERISTICS table values 7
- Changed the ABSOLUTE MAXIMUM POWER DISSIPATION RATINGS table values 8

Changes from Revision A (September 2003) to Revision B **Page**

- Changed the front page format 1
- Changed DESCRIPTION text From: and tolerance to transients of ±50 V To: and tolerance to transients of ±200 V 1

Changes from Original (November 2002) to Revision A **Page**

- Changed multiple items within the document. 1

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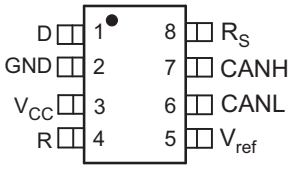
5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CANH	7	I/O	High-level CAN bus line
CANL	6	I/O	Low-level CAN bus line
D	1	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states), also called TXD, driver input
GND	2	GND	Ground connection
R	4	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states), also called RXD, receiver output
R_S	8	I	Mode select pin: strong pulldown to GND = high-speed mode, strong pull up to V_{CC} = low-power mode, 10-kΩ to 100-kΩ pulldown to GND = slope control mode
V_{CC}	3	Supply	Transceiver 5-V supply voltage
V_{REF}	5	O	Reference output voltage

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

			MIN	MAX	UNIT
Supply voltage, V_{CC}			–0.3	7	V
Voltage at any bus pin(CANH or CANL)			–36	36	V
Transient voltage per ISO 7637, pulse 1, 2, 3a, 3b		CANH, CANL	–200	200	V
Input voltage, V_I (D, Rs, or R)			–0.3	V_{CC} + 0.5	V
Receiver output current, I_O			–10	10 mA	mA
Electrical fast transient/burst	IEC 61000-4-4, Classification B	CANH, CANL	–3	3	kV
Continuous total power dissipation			(see *Dissipation Ratings*)		

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground pin.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	All pins	±6000	V
			CANH, CANL and GND	±14000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		5.5	V
Voltage at any bus terminal (separately or common mode) V_I or V_{IC}		–7 (1)		12	V
High-level input voltage, V_{IH}	D input	0.7 V_{CC}			V
Low-level input voltage, V_{IL}	D input			0.3 V_{CC}	V
Differential input voltage, V_{ID}		–6		6	V
Input voltage to Rs, $V_{I(Rs)}$		0		V_{CC}	V
Input voltage at Rs for standby, $V_{I(Rs)}$		0.75 V_{CC}		V_{CC}	V
Rs wave-shaping resistance		0		100	kΩ
High-level output current, I_{OH}	Driver	–50			mA
	Receiver	–4			
Low-level output current, I_{OL}	Driver			50	mA
	Receiver			4	
Operating free-air temperature, T_A	SN65HVD251	–40		125	°C
	SN55HVD251	–55		125	
Junction temperature, T_J				145	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

6.4 Thermal Information

THERMAL METRIC (1)		SN55HVD251	SN65HVD251		UNIT
		DRJ (SON)	D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52	44.6	66.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73	78.7	48.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Supply Current

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
I_{CC}	Supply current	Standby	Rs at V_{CC}, D at V_{CC}			275	µA
		Dominant	D at 0 V, 60-Ω load, Rs at 0 V			65	mA
		Recessive	D at V_{CC}, no load, Rs at 0 V			14	

(1) All typical values are at 25°C and with a 5-V supply.

6.6 Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	Figure 10 and Figure 11 , D at 0 V Rs at 0 V, T ≥ –40°C	2.75	3.5	4.5	V
		CANL		0.5		2	
$V_{O(R)}$	Bus output voltage (Recessive)	CANH	Figure 10 and Figure 11 , D at 0.7 V_{CC}, Rs at 0 V	2	2.5	3	
		CANL		2	2.5	3	
$V_{OD(D)}$	Differential output voltage (Dominant)		Figure 10 , D at 0 V, Rs at 0 V	1.5	2	3	V
			Figure 12 , D at 0 V, Rs at 0 V, R_{NODE} = 330 Ω	1.2	2	3.1	V
			Figure 12 , D at 0 V, Rs at 0 V, R_{NODE} = 165 Ω, V_{CC} ≥ 4.75 V	1.2	2	3.1	V
$V_{OD(R)}$	Differential output voltage (Recessive)		Figure 10 and Figure 11 , D at 0.7 V_{CC}	–120		12	mV
			D at 0.7 V_{CC}, no load, T ≤ 85°C	–0.5		0.05	V

(1) All typical values are at 25°C and with a 5-V supply.

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Electrical Characteristics: Driver (continued)

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage	Figure 18, Rs at 0 V		600		mV
I_{IH}	High-level input current, D Input	D at 0.7 V_{CC}	–40		0	µA
I_{IL}	Low-level input current, D Input	D at 0.3 V_{CC}	–60		0	µA
$I_{OS(SS)}$	Short-circuit steady-state output current	Figure 20, V_{CANH} at –7 V, CANL Open	–200			mA
		Figure 20, V_{CANH} at 12 V, CANL Open			2.5	
		Figure 20, V_{CANL} at -7 V, CANH Open	–2			
		Figure 20, V_{CANL} at 12 V, CANH Open			200	
C_O	Output capacitance	See receiver input capacitance				
I_{OZ}	High-impedance output current	See receiver input current				
$I_{IRs(s)}$	Rs input current for standby	Rs at 0.75 V_{CC}	–10			µA
$I_{IRs(f)}$	Rs input current for full speed operation	Rs at 0 V	–550		0	µA

6.7 Electrical Characteristics: Receiver

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	Rs at 0 V, (See Table 1)			750	900	mV
V_{IT-}	Negative-going input threshold voltage			500	650		
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})				100		
V_{OH}	High-level output voltage	Figure 15, I_O = –4 mA		0.8 V_{CC}			V
V_{OL}	Low-level output voltage	Figure 15, I_O = 4 mA				0.2 V_{CC}	V
I_I	Bus input current	CANH or CANL at 12 V	Other bus pin at 0 V, Rs at 0 V, D at 0.7 V_{CC}			600	µA
		CANH or CANL at 12 V, V_{CC} at 0 V				715	
		CANH or CANL at -7 V		–460			
		CANH or CANL at -7 V, V_{CC} at 0 V		–340			
C_I	Input capacitance, (CANH or CANL)	Pin-to-ground, V_I = 0.4 sin (4E6πt) + 0.5 V, D at 0.7 V_{CC}			20		pF
C_{ID}	Differential input capacitance	Pin-to-pin, V_I = 0.4 sin (4E6πt) + 0.5 V, D at 0.7 V_{CC}			10		pF
R_{ID}	Differential input resistance	D at 0.7 V_{CC}, Rs at 0 V		40		100	kΩ
R_{IN}	Input resistance, (CANH or CANL)	D at 0.7 V_{CC}, Rs at 0 V		20		50	kΩ
	Receiver noise rejection	See Figure 22					

6.8 VREF-Pin Characteristics

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Reference output voltage	–5 µA < I_O < 5 µA	0.45 V_{CC}		0.55 V_{CC}	V
		–50 µA < I_O < 50 µA	0.4 V_{CC}		0.6 V_{CC}	

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6.9 Power Dissipation Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Device power dissipation	V_{CC} = 5 V, Tj = 27°C, RL = 60 Ω, R_S at 0 V, Input to D a 500-kHz 50% duty cycle square wave		97.7		mW
		V_{CC} = 5.5 V, Tj = 130°C, RL = 60 Ω, R_S at 0 V, Input to D a 500-kHz 50% duty cycle square wave		142		mW
T_{SD}	Thermal shutdown junction temperature			165		°C

6.10 Switching Characteristics: Driver

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output	Figure 13, Rs at 0 V		40	70	ns
		Figure 13, Rs with 10 kΩ to ground		90	125	
		Figure 13, Rs with 100 kΩ to ground		500	800	
t_{pHL}	Propagation delay time, high-to-low-level output	Figure 13, Rs at 0 V		85	125	
		Figure 13, Rs with 10 kΩ to ground		200	260	
		Figure 13, Rs with 100 kΩ to ground		1150	1450	
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)	Figure 13, Rs at 0 V		45	85	
		Figure 13, Rs with 10 kΩ to ground		110	180	
		Figure 13, Rs with 100 kΩ to ground		650	900	
t_r	Differential output signal rise time	Figure 13, Rs at 0 V	35	80	100	
t_f	Differential output signal fall time		35	80	100	
t_r	Differential output signal rise time	Figure 13, Rs with 10 kΩ to ground	100	150	250	
t_f	Differential output signal fall time		100	150	250	
t_r	Differential output signal rise time	Figure 13, Rs with 100 kΩ to ground	600	950	1550	
t_f	Differential output signal fall time		600	950	1550	
t_{en}	Enable time from standby to dominant	Figure 17			0.5	µs

6.11 Switching Characteristics: Device

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{loop1}	Total loop delay, driver input to receiver output, recessive to dominant	Figure 19, Rs at 0 V		60	100	ns
		Figure 19, Rs with 10 kΩ to ground		100	150	
		Figure 19, Rs with 100 kΩ to ground		440	800	
t_{loop2}	Total loop delay, driver input to receiver output, dominant to recessive	Figure 19, Rs at 0 V		115	150	ns
		Figure 19, Rs with 10 kΩ to ground		235	290	
		Figure 19, Rs with 100 kΩ to ground		1070	1450	
t_{loop2}	Total loop delay, driver input to receiver output, dominant to recessive	Figure 19, Rs at 0 V, V_{CC} from 4.5 V to 5.1 V		105	145	ns

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6.12 Switching Characteristics: Receiver

over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output	Figure 15		35	50	ns
t_{pHL}	Propagation delay time, high-to-low-level output			35	50	
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$)				20	
t_r	Output signal rise time			2	4	
t_f	Output signal fall time			2	4	
$t_{p(sb)}$	Propagation delay time in standby	Figure 21, Rs at V_{CC}			500	

6.13 Dissipation Ratings

PACKAGE	CIRCUIT BOARD MODEL	T_A = 25°C POWER RATING	DERATING FACTOR (1) ABOVE T_A = 25°C	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
SOIC (D)	Low-K(2)	576 mW	4.8 mW/°C	288 mW	96 mW
	High-K(3)	924 mW	7.7 mW/°C	462 mW	154 mW
PDIP (P)	Low-K(2)	888 mW	7.4 mW/°C	444 mW	148 mW
	High-K(3)	1212 mW	10.1 mW/°C	606 mW	202 mW
WSON (DRJ)	Low-K(2)	403 mW	4.03 mW/°C	262 mW	100 mW
	High-K (no Vias)(3)	1081 mW	10.8 mW/°C	703 mW	270 mW
	High-K (with Vias)	2793 mW	27.9 mW/°C	1815 mW	698 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
(3) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

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6.14 Typical Characteristics

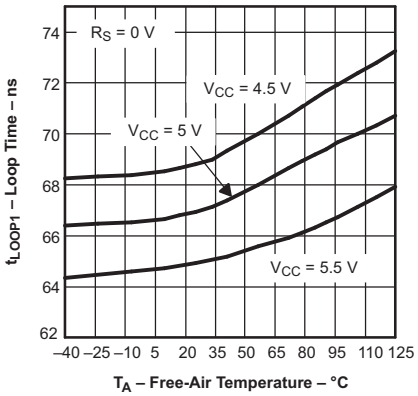

Figure 1. Recessive-to-Dominant Loop Delay vs Free-Air Temperature

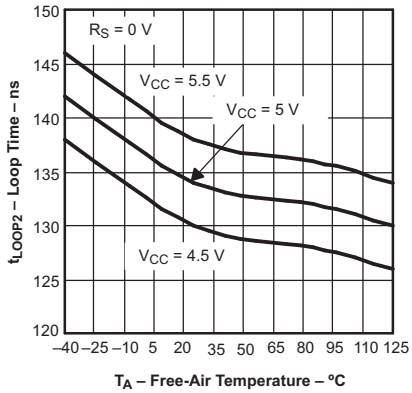

Figure 2. Dominant-to-Recessive Loop Delay vs Free-Air Temperature

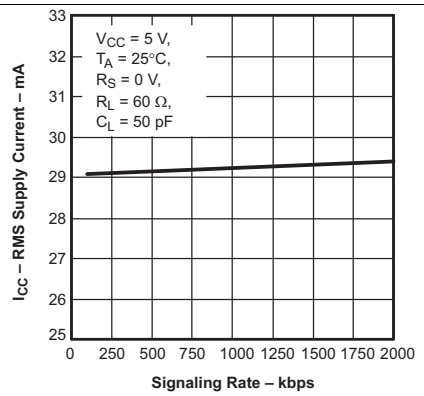

Figure 3. Supply Current (RMS) vs Signaling Rate

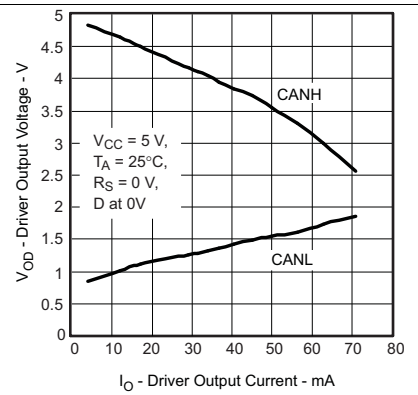

Figure 4. Driver Output Voltage vs Output Current

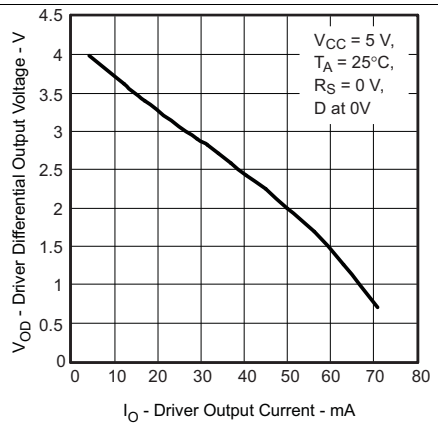

Figure 5. Driver Differential Output Voltage vs Output Current

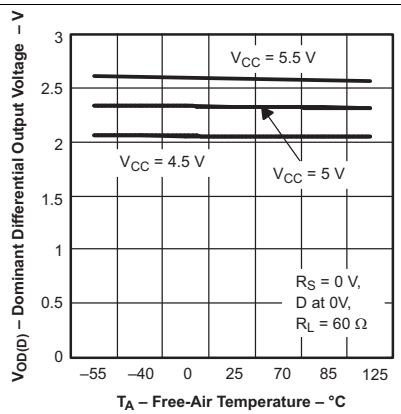

Figure 6. Dominant Differential Output Voltage vs free-Air Temperature

Typical Characteristics (continued)

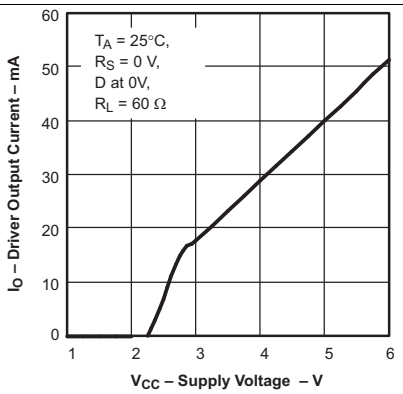

Figure 7. Driver Output Current vs Supply Voltage

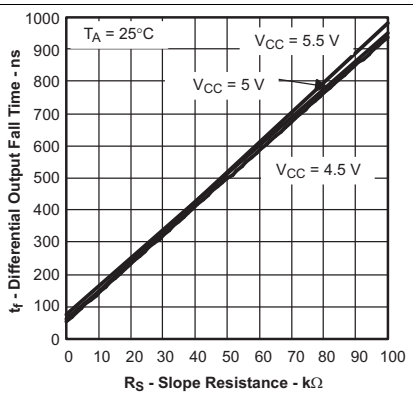

Figure 8. Differential Output Transition Time vs Slope Resistance (Rs)

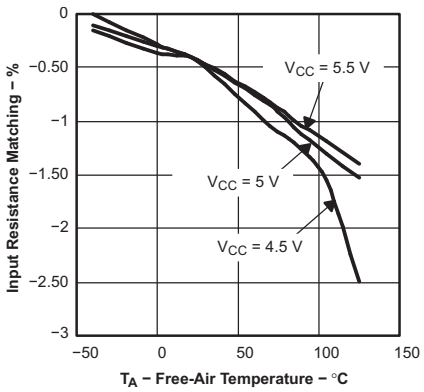

Figure 9. Input Resistance Matching vs Free-Air Temperature

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7 Parameter Measurement Information

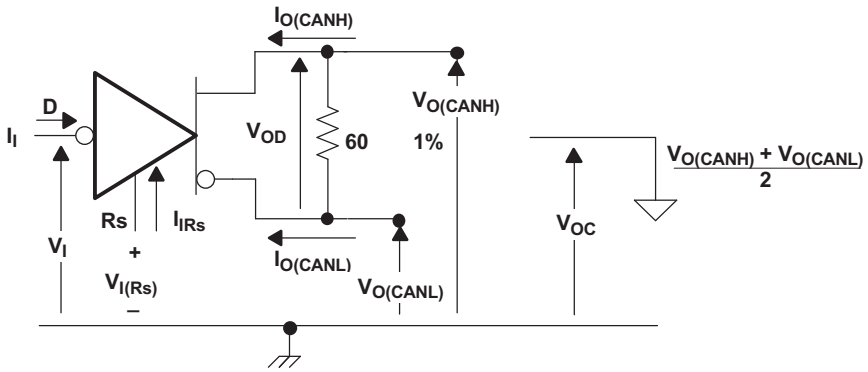


Figure 10. Driver Voltage, Current, and Test Definition

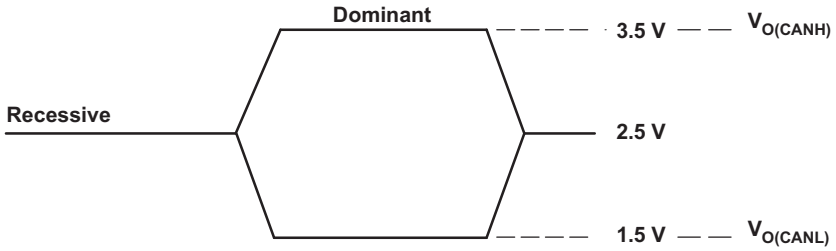


Figure 11. Bus Logic State Voltage Definitions

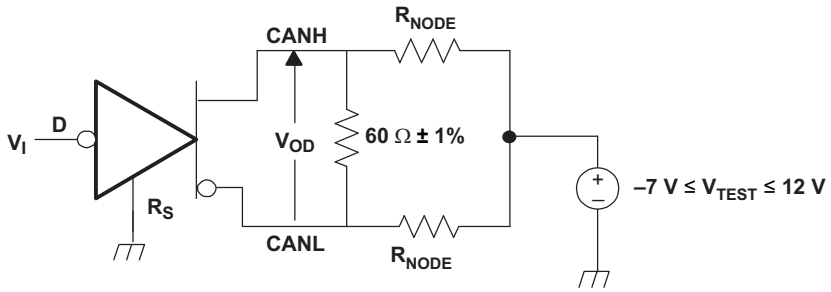


Figure 12. Driver V_{OD}

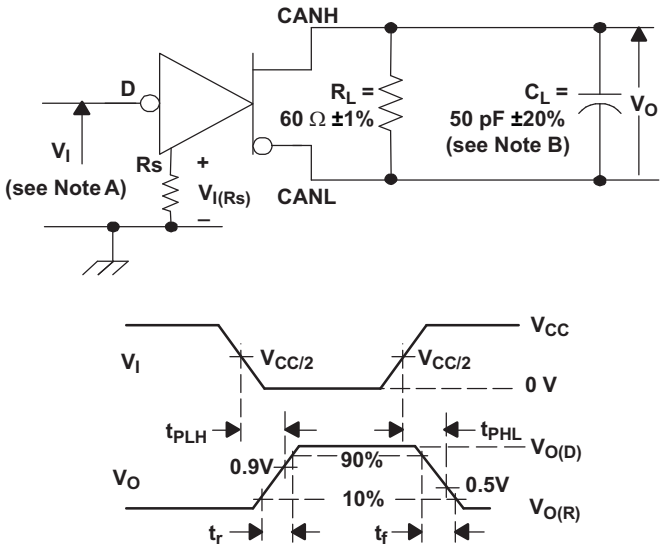


Figure 13. Driver Test Circuit and Voltage Waveforms

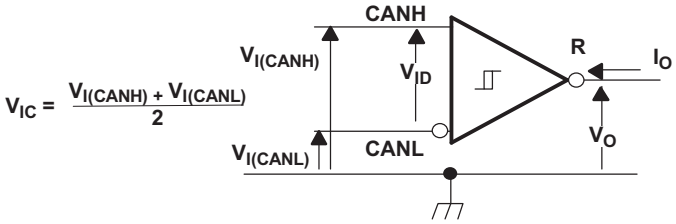
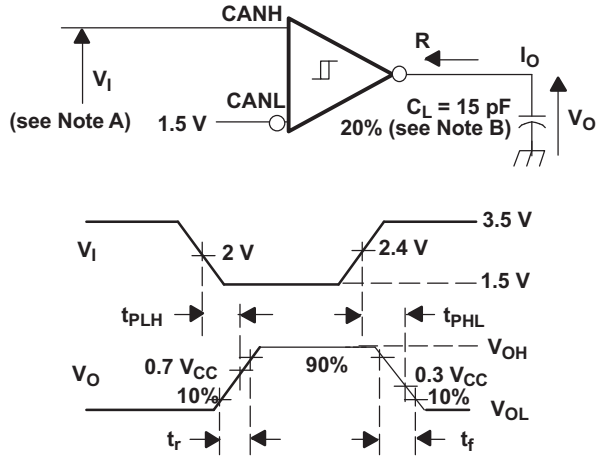


Figure 14. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 15. Receiver Test Circuit and Voltage Waveforms

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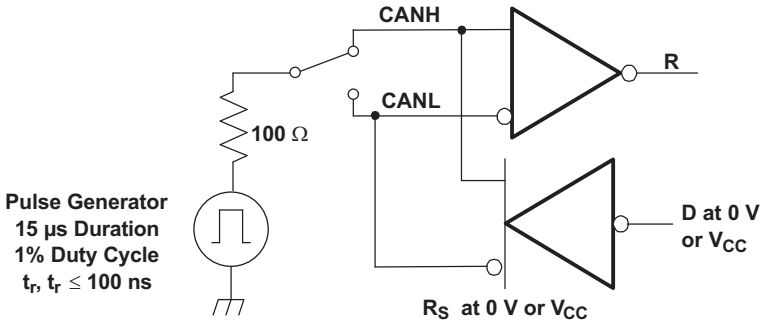


This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 16. Test Circuit, Transient Overvoltage Test

Table 1. Receiver Characteristics Over Common Mode Voltage

INPUT		DIFFERENTIAL INPUT	OUTPUT	
V_{CANH}	V_{CANL}	$\|V_{ID}\|$	R	
12 V	11.1 V	900 mV	L	V_{OL}
–6.1 V	–7 V	900 mV	L	
–1 V	–7 V	6 V	L	
12 V	6 V	6 V	L	
–6.5 V	–7 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–7 V	–1 V	6 V	H	
6 V	12 V	6 V	H	
open	open	X	H	

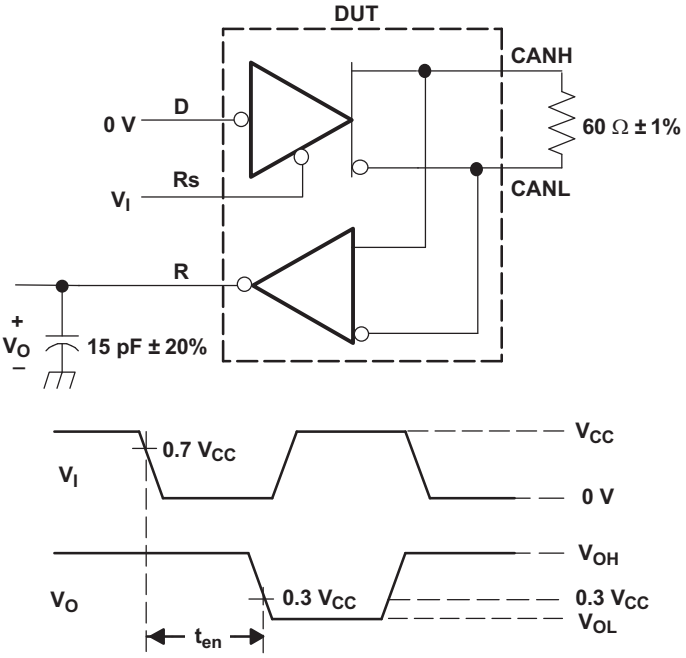
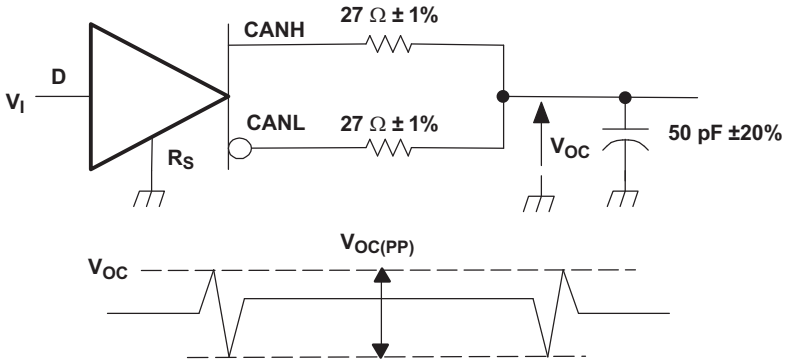


Figure 17. T_{en} Test Circuit and Voltage Waveforms



The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50 Ω.

Figure 18. Peak-to-Peak Common Mode Output Voltage

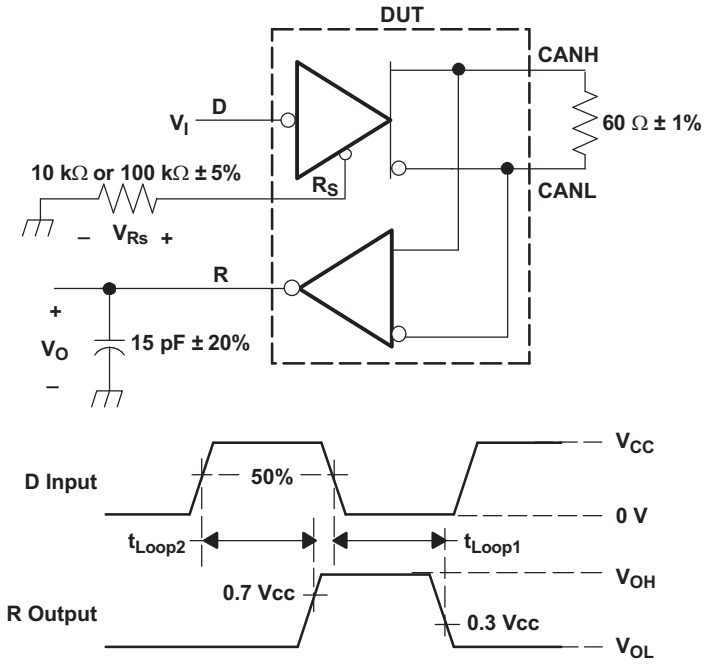


Figure 19. T_{LOOP} Test Circuit and Voltage Waveforms

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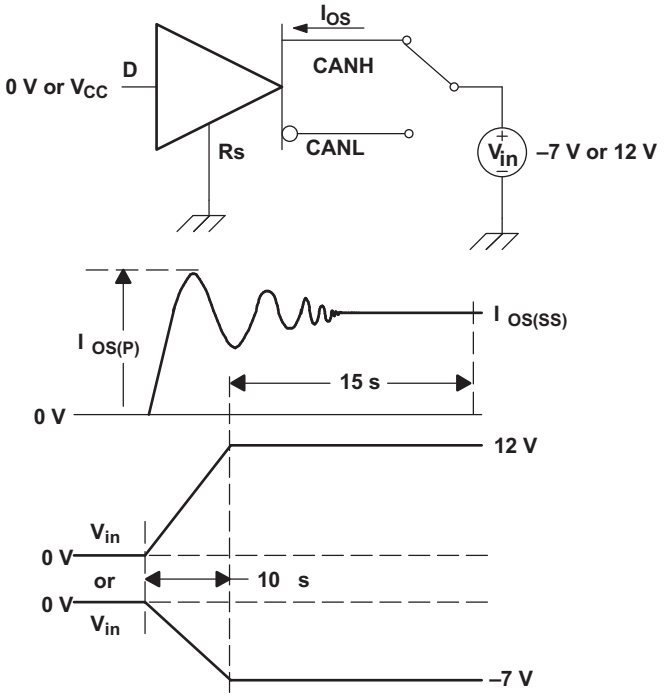
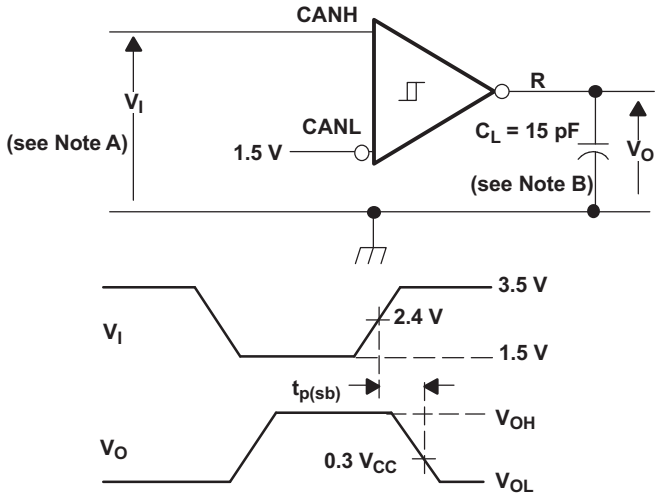


Figure 20. Driver Short-Circuit Test



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50 Ω.

B. CL includes instrumentation and fixture capacitance within ±20%.

Figure 21. Receiver Propagation Delay in Standby Test Circuit and Waveform

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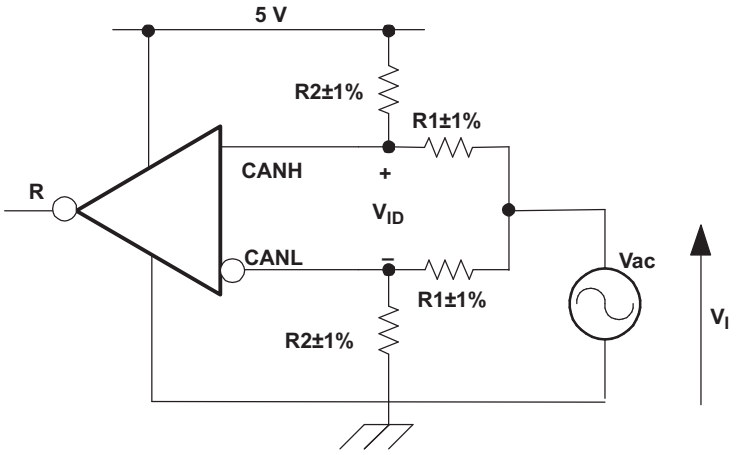

V_{ID}	R1	R2
500 mV	50	450
900 mV	50	227

A. All input pulses are supplied by a generator having the following characteristics: f_{IN} < 1.5 MHz, T_A = 25°C, V_{CC} = 5 V.

B. The receiver output should not change state during application of the common-mode input waveform.

Figure 22. Common-Mode Input Voltage Rejection Test

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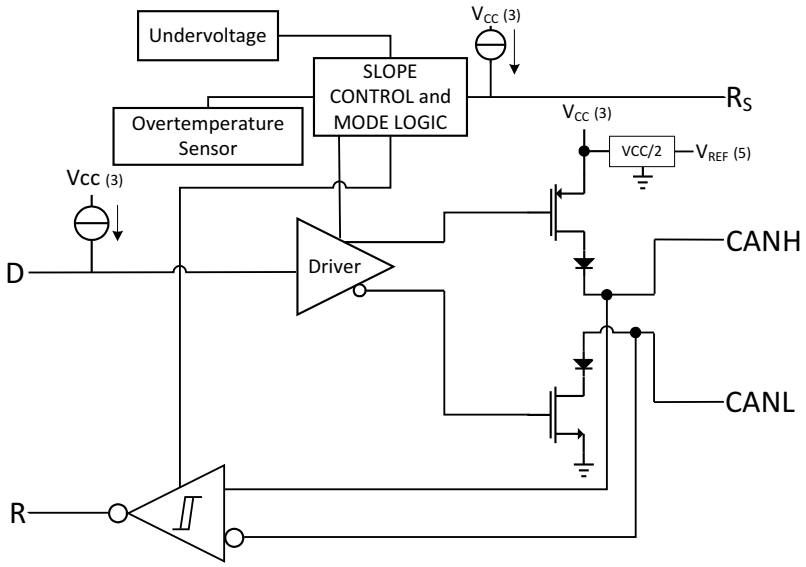
8 Detailed Description

8.1 Overview

The SNx5HVD251CAN bus transceiver is compatible with the ISO 11898-2 High Speed CAN (Controller Area Network) physical layer standard. It is design to interface between the differential bus lines in controller area network and the CAN protocol controller at data rates up to 1 Mbps.

8.2 Functional Block Diagram



8.3 Feature Description

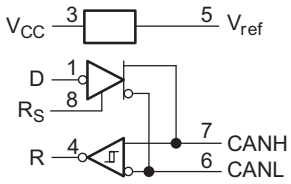


Figure 23. Function Diagram (Positive Logic)

8.3.1 Mode Control

R_S, Pin 8, selects one of three possible modes of operation: high-speed, slope control, or low-power mode.

8.3.2 High-Speed Mode

The high-speed mode of operation can be selected by setting R_S (Pin 8) low. High-speed allows the output to switch as fast as possible with no internal limitations on the output rise and fall slopes. The CAN bus driver and receiver are fully operational and the CAN communication is bi-directional. The driver is translating a digital input on D to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on R.

8.3.3 Slope Control Mode

The rise and fall slope of the SNx5HVD251 driver output can be adjusted by connecting a resistor from Rs (Pin 8) to ground (GND), or to a low-level input voltage as shown in Figure 24. The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value of 10 kΩ to achieve a ~15-V/µs slew rate, and up to 100 kΩ to achieve a ~2.0-V/µs slew rate. Figure 8 shows a plot of differential output transition time vs slope resistance from which the slew rate can be calculated.

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Feature Description (continued)

8.3.4 Low-Power Mode

If a high-level input (>0.75 V_{CC}) is applied to R_S (Pin 8), the circuit enters a low-current, listen only standby mode during which the driver is switched off and the receiver remains active. If using this mode to save system power while waiting for bus traffic, the local controller can monitor the R output pin for a falling edge which indicates that a dominant signal was driven onto the CAN bus. The local controller can then drive the R_S pin low to return to slope control mode or high-speed mode.

NOTE

Silent mode may be used to implement babbling idiot protection, to ensure that the driver does not disrupt the network during a local fault. Silent mode may also be used in redundant systems to select or de-select the redundant transceiver (driver) when needed.

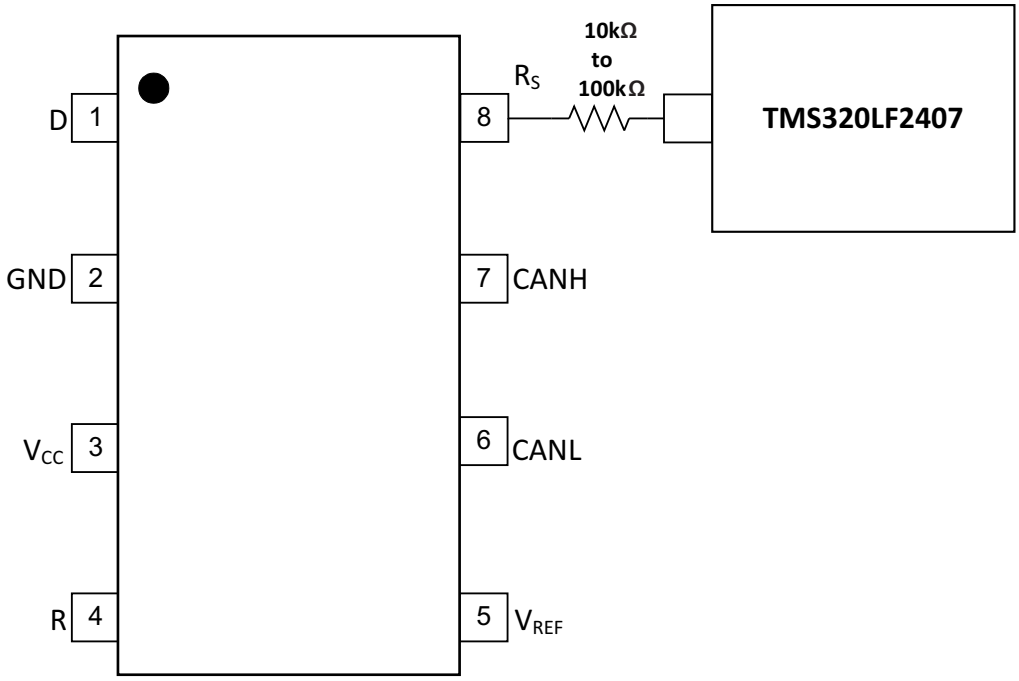

Figure 24. Slope Control

8.3.5 Thermal Shutdown

The SNx5HVD251 has a thermal shutdown feature that turns off the driver outputs when the junction temperature nears 165°C. This shutdown prevents catastrophic failure from bus shorts, but does not protect the circuit from possible damage. The user should strive to maintain recommended operating conditions and not exceed absolute-maximum ratings at all times. If an SNx5HVD251 is subjected to many, or long-duration faults that can put the device into thermal shutdown, it should be replaced.

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8.4 Device Functional Modes

Table 2. Driver

INPUTS	Voltage at R_S, V_{Rs}	OUTPUTS		BUS STATE
D		CANH	CANL	
L	V_{Rs} < 1.2 V	H	L	Dominant
H	V_{Rs} < 1.2 V	Z	Z	Recessive
Open	X	Z	Z	Recessive
X	V_{Rs} > 0.75 V_{CC}	Z	Z	Recessive
X	Open	Z	Z	Recessive

Table 3. Receiver

DIFFERENTIAL INPUTS [V_{ID} = V(CANH) - V(CANL)]	OUTPUT R(1)
V_{ID} ≥ 0.9 V	L
0.5 V < V_{ID} < 0.9 V	?
V_{ID} ≤ 0.5 V	H
Open	H

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

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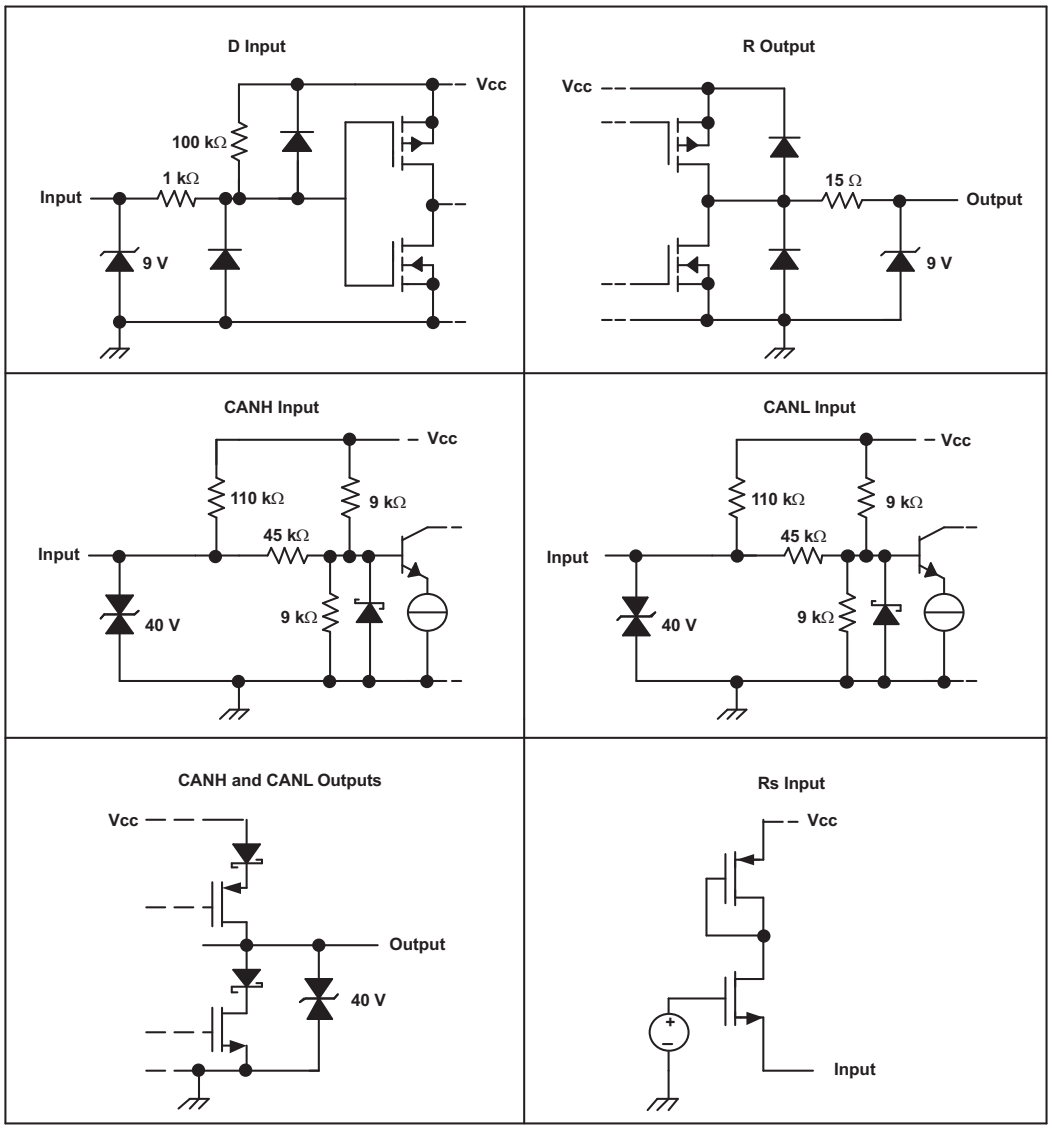

Figure 25. Equivalent Input and Output Schematic Diagrams

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The CAN bus has two states during powered operation of the device; dominant and recessive. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the D and R pin. A recessive bus state is when the bus is biased to $V_{CC}/2$ via the high-resistance internal resistors R_{IN} and R_{ID} of the receiver, corresponding to a logic high on the D and R pins. See Figure 26 and Figure 27.

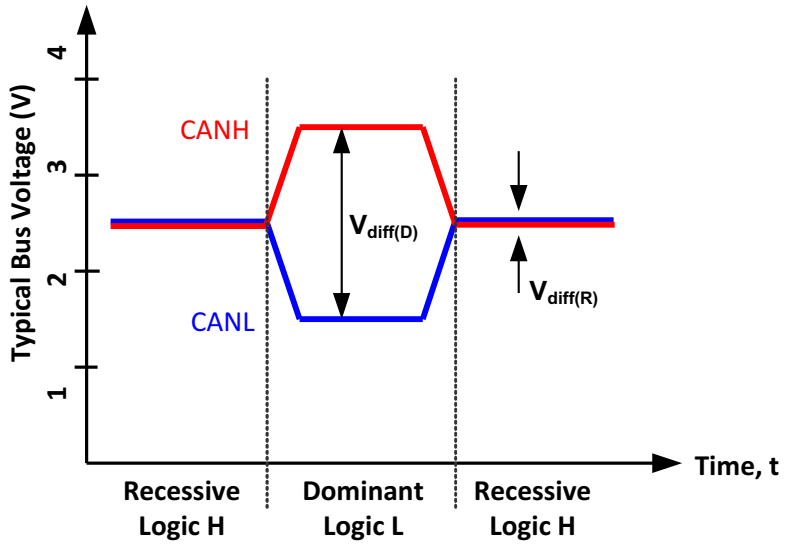

Figure 26. Bus States

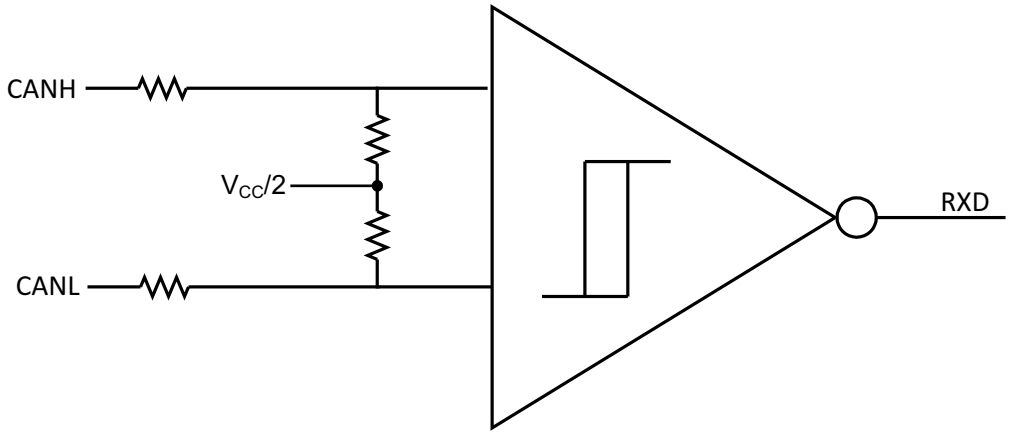

Figure 27. Simplified Recessive Common Mode Bias and Receiver

The HVD251 CAN transceiver is typically used in applications with a host microprocessor or FPGA that includes the link layer portion of the CAN protocol. The different nodes on the network are typically connected through the use of a 120-Ω characteristic impedance twisted pair cable with termination on both ends of the bus.

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Application Information (continued)

The basics of bus arbitration require that the receiver at the sending node designate the first bit as dominant or recessive after the initial wave of the first bit of a message travels to the most remote node on a network and back again. Typically, this *sample* is made at 75% of the bit width, and within this limitation, the maximum allowable signal distortion in a CAN network is determined by network electrical parameters.

Factors to be considered in network design include the 5 ns/m propagation delay of typical twisted-pair bus cable; signal amplitude loss due to the loss mechanisms of the cable; and the number, length, and spacing of drop-lines (stubs) on a network. Under strict analysis, variations among the different oscillators in a system must also be accounted for with adjustments in signaling rate and stub and bus length. Table 4 lists the maximum signaling rates achieved with the HVD251 in high-speed mode with several bus lengths of category-5, shielded twisted-pair (CAT 5 STP) cable.

Table 4. Maximum Signaling Rates for Various Cable Lengths

BUS LENGTH (m)	SIGNALING RATE (kbps)
30	1000
100	500
250	250
500	125
1000	62.5

The ISO 11898 standard specifies a maximum bus length of 40 meters and maximum stub length of 0.3 meters with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes on a bus. (Note: Non-standard application may come with a trade-off in signaling rate.) A bus with a large number of nodes requires a transceiver with high input impedance such as the HVD251.

The Standard specifies the interconnect to be a single twisted-pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Zo). Resistors equal to the characteristic impedance of the line terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines connect nodes to the bus and should be kept as short as possible to minimize signal reflections.

Connectors, while not specified by the ISO 11898 standard, should have as little effect as possible on standard operating parameters such as capacitive loading. Although unshielded cable is used in many applications, data transmission circuits employing CAN transceivers are usually used in applications requiring a rugged interconnection with a wide common-mode voltage range. Therefore, shielded cable is recommended in these electronically harsh environments, and when coupled with the –2-V to 7-V common-mode range of tolerable ground noise specified in the standard, helps to ensure data integrity. The HVD251 extends data integrity beyond that of the standard with an extended –7-V to 12-V range of common-mode operation.

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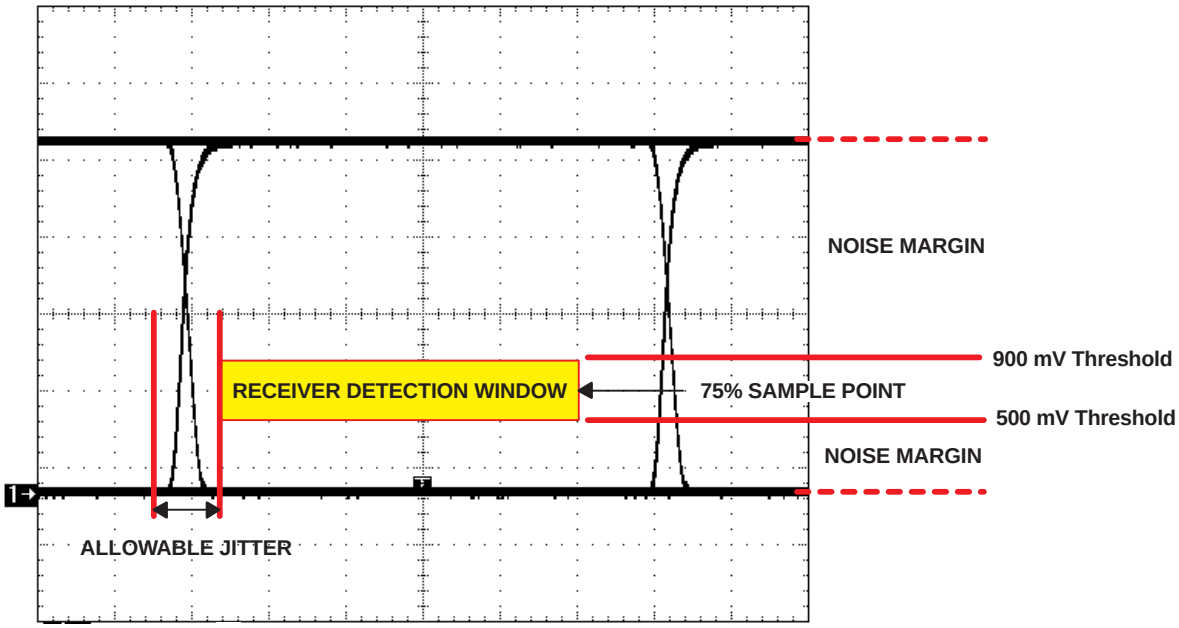

Figure 28. Typical CAN Differential Signal Eye-Pattern

An eye pattern is a useful tool for measuring overall signal quality. As displayed in Figure 28, the differential signal changes logic states in two places on the display, producing an *eye*. Instead of viewing only one logic crossing on the scope, an entire *bit* of data is brought into view. The resulting eye pattern includes all effects of systemic and random distortion, and displays the time during which a signal may be considered valid.

The height of the eye above or below the receiver threshold voltage level at the sampling point is the noise margin of the system. Jitter is typically measured at the differential voltage zero-crossing during the logic state transition of a signal. Note that jitter present at the receiver threshold voltage level is considered by some to be a more effective representation of the jitter at the input of a receiver.

As the sum of skew and noise increases, the eye closes and data is corrupted. Closing the width decreases the time available for accurate sampling, and lowering the height enters the 900-mV or 500-mV threshold of a receiver.

Different sources induce noise onto a signal. The more obvious noise sources are the components of a transmission circuit themselves; the signal transmitter, traces & cables, connectors, and the receiver. Beyond that, there is a termination dependency, cross-talk from clock traces and other proximity effects, V_{CC} and ground bounce, and electromagnetic interference from near-by electrical equipment.

The balanced receiver inputs of the HVD251 mitigate most sources of signal corruption, and when used with a quality shielded twisted-pair cable, help meet data integrity.

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9.2 Typical Application

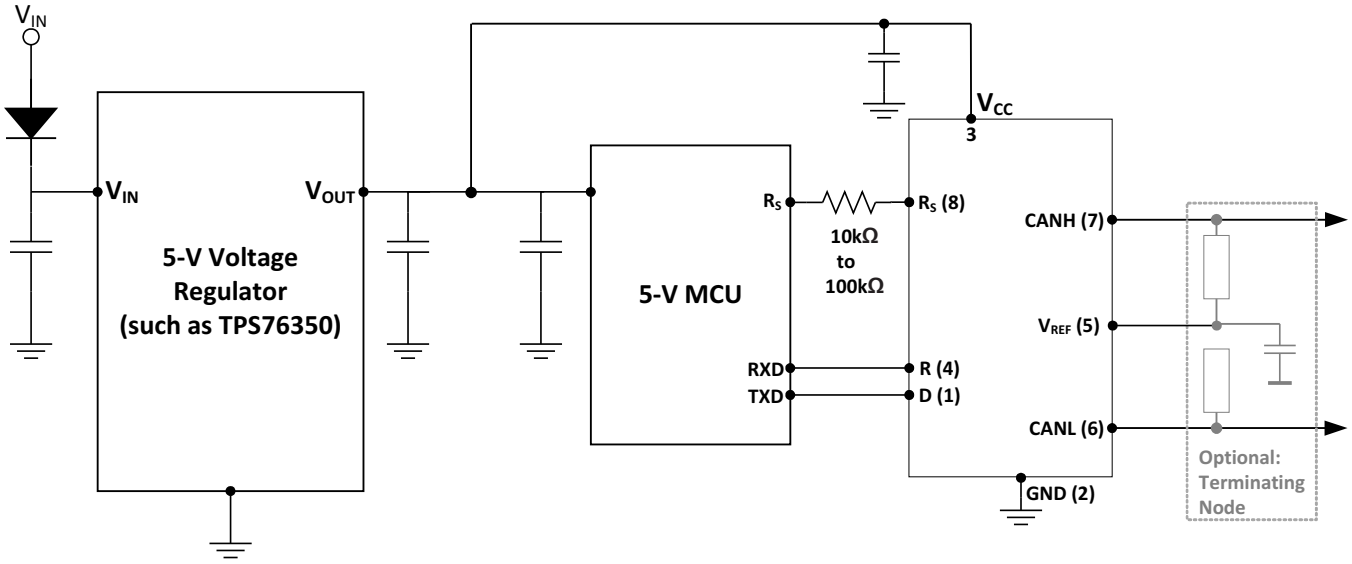

Figure 29. Typical Application Schematic

9.2.1 Design Requirements

9.2.1.1 Bus Loading, Length, and Number of Nodes

The ISO11898 Standard specifies up to 1-Mbps data rate, maximum bus length of 40 meters, maximum drop line (stub) length of 0.3 meters and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes to a bus. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898 standard. They have made system level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, CAN Kingdom, DeviceNet and NMEA200.

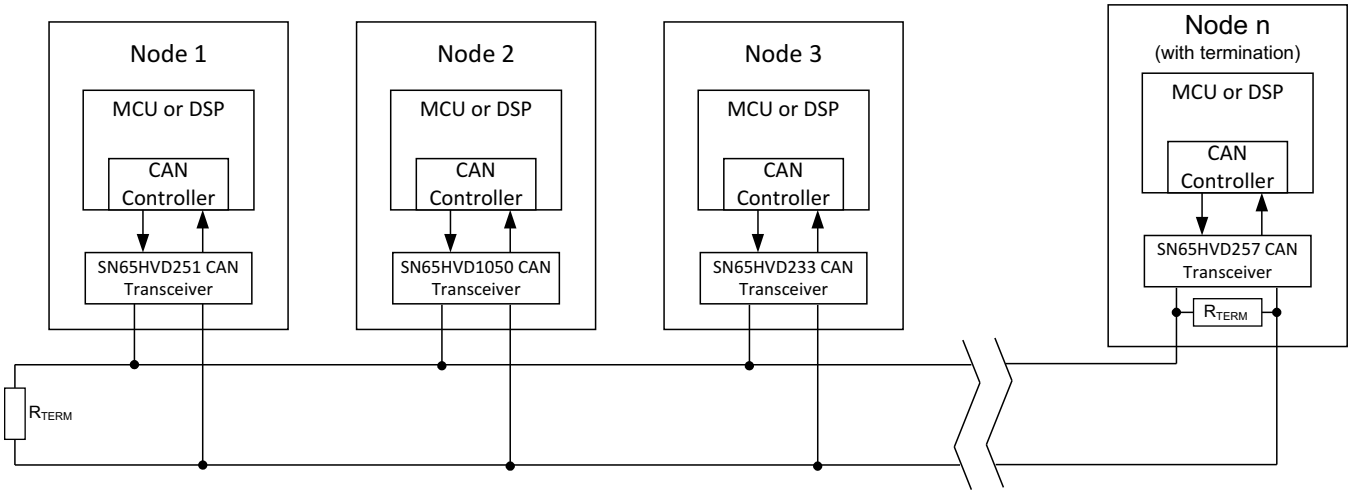

Figure 30. Typical CAN Bus

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Typical Application (continued)

A high number of nodes requires a transceiver with high input impedance and wide common mode range such as the SNx5HVD251 CAN transceiver. ISO11898-2 specifies the driver differential output with a 60-Ω load (two 120-Ω termination resistors in parallel) and the differential output must be greater than 1.5 V. The SNx5HVD251 devices are specified to meet the 1.5-V requirement with a 60-Ω load, and additionally specified with a differential output voltage minimum of 1.2 V across a common mode range of –2 V to 7 V via a 330-Ω coupling network. This network represents the bus loading of 120 SNx5HVD251 transceivers based on their minimum differential input resistance of 40 kΩ. Therefore, the SNx5HVD251 supports up to 120 transceivers on a single bus segment with margin to the 1.2-V minimum differential input voltage requirement at each node.

For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898 CAN standard.

9.2.2 Detailed Design Procedure

9.2.2.1 CAN Termination

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

Termination is typically a 120-Ω resistor at each end of the bus. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used (see Figure 30). Split termination utilizes two 60-Ω resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltages at the start and end of message transmissions.

Care should be taken when determining the power ratings of the termination resistors. A typical worst case fault condition is if the system power supply and ground were shorted across the termination resistance which would result in much higher current through the termination resistance than the CAN transceiver's current limit.

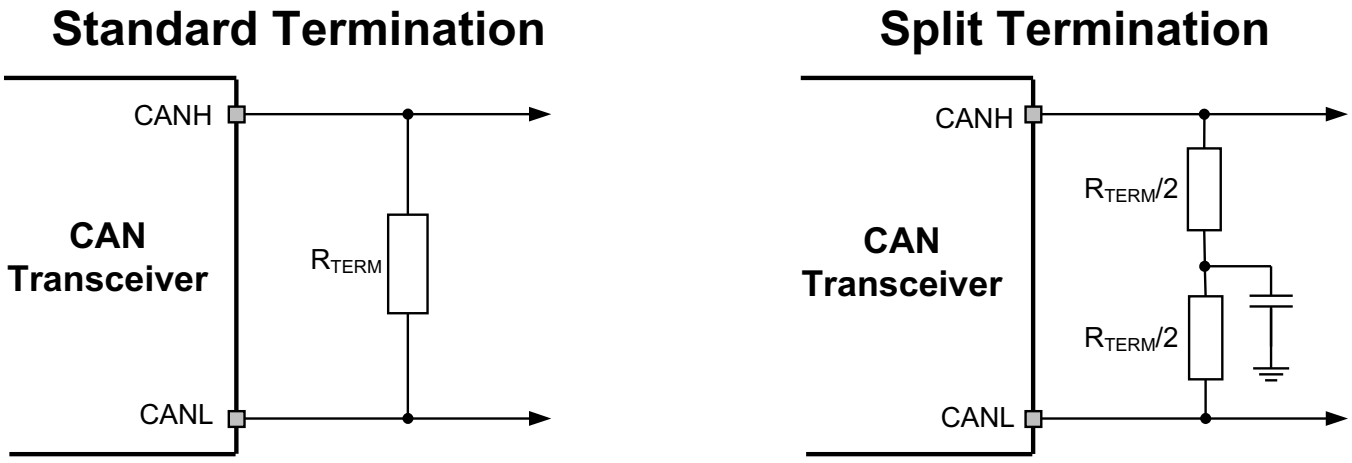

Figure 31. CAN Termination

Typical Application (continued)

9.2.2.2 Loop Propagation Delay

Transceiver loop delay is a measure of the overall device propagation delay, consisting of the delay from the driver input (D pin) to the differential outputs (CANH and CANL pins), plus the delay from the receiver inputs (CANH and CANL) to its output pin.

A typical loop delay for the SNx5HVD251 transceiver is displayed in Figure 32. This loop delay will increase as the slope of the driver output is slowed during slope control mode. This increased loop delay means that there is a tradeoff between the total bus length able to be used and the driver's output slope used via the slope control pin of the device. For example, the loop delay for a 10-kΩ resistor from the R_S pin to ground is ~100 ns, and the loop delay for a 100-kΩ resistor is ~500 ns. Therefore, if we use the following rule-of-thumb that the propagation delay of typical twisted pair bus cable is 5 ns/m, we can calculate an approximate cable length trade-off between normal high-speed mode and slope control mode with a 100-kΩ resistor. Using typical values, the loop delay for a recessive to dominant bit with R_S tied directly to ground is 60ns, and with a 100-kΩ resistor is 440 ns. At 5-ns/m of propagation delay, which you have to count in both directions the difference is 38 meters (440 – 60)/(2 × 5).

Another option to improving the electromagnetic emissions of the device besides slowing down the edge rates of the driver in slope control mode is using quality shielded bus cabling.

9.2.3 Application Curve

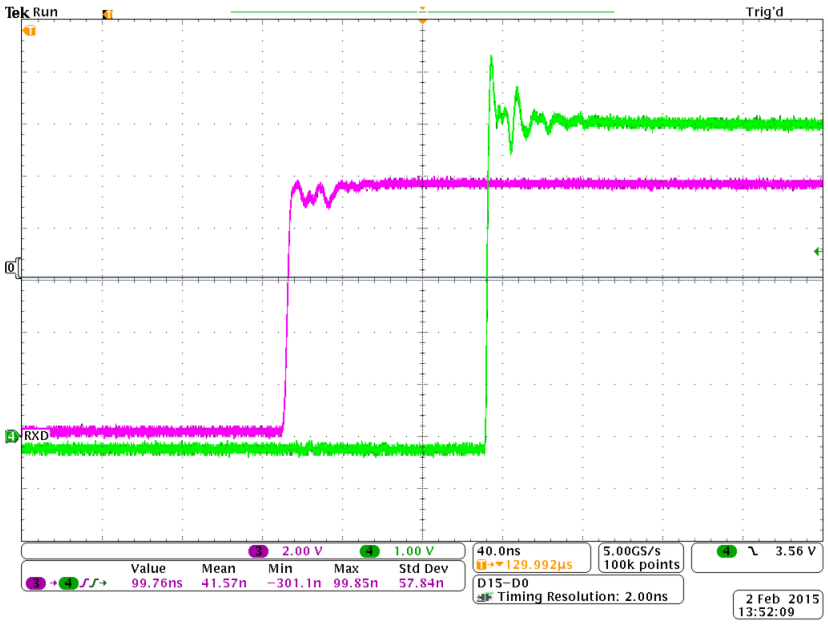

Figure 32. t_{LOOP} Delay

9.3 System Example

9.3.1 ISO 11898 Compliance of HVD251 5-V CAN Bus Transceiver

9.3.1.1 Introduction

The SNx5HVD251 CAN transceiver is a 5-V CAN transceiver that meets or exceeds the specification of the ISO 11898 standard for applications employing a controller area network.

9.3.1.2 Differential Signal

CAN is a differential bus where complementary signals are sent over two wires and the voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this voltage difference and outputs the bus state with a single ended logic level output signal.

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System Example (continued)

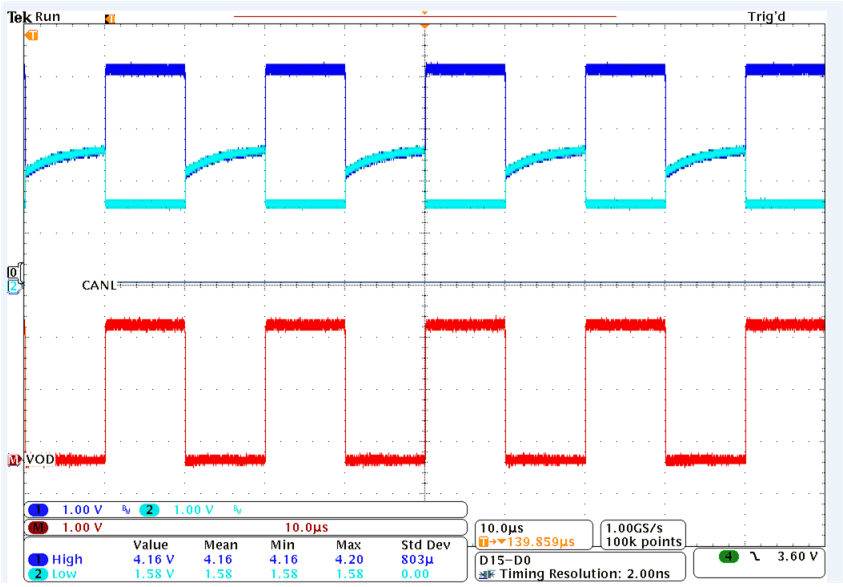

Figure 33. Differential Output Waveform

The CAN driver creates the differential voltage between CANH and CANL in the dominant state. The dominant differential output of the HVD251 is greater than 1.5 V and less than 3 V across a 60-Ω load as defined by the ISO 11898 standard. Figure 33 shows CANH, CANL, and the differential dominant state level for the SNx5HVD251.

A CAN receiver is required to output a recessive state when less than 500 mV of differential voltage exists on the bus, and a dominant state when more than 900 mV of differential voltage exists on the bus. The CAN receiver must do this with common-mode input voltages from –2 V to 7 V.

9.3.1.3 Common-Mode Signal

A common-mode signal is an average voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. Since the bias voltage of the recessive state of the device is dependent on V_{CC}, any noise present or variation of V_{CC} will have an effect on this bias voltage seen by the bus. The HVD251 CAN transceiver has the recessive bias voltage set to 0.5 × V_{CC} to comply with the ISO 11898-2 CAN standard.

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10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close as possible to the V_{CC} supply pins as possible. The TPS76350 is a linear voltage regulator suitable for the 5-V supply rail.

11 Layout

11.1 Layout Guidelines

In order for the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high frequency layout techniques must be applied during PCB design. On chip IEC ESD protection is good for laboratory and portable equipment but is usually not sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices at the bus connectors. Placement at the connector also prevents these harsh transient events from propagating further into the PCB and system.

Use V_{CC} and ground planes to provide low inductance.

NOTE

High frequency current follows the path of least inductance and not the path of least resistance.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.

An example placement of the Transient Voltage Suppression (TVS) device indicated as D1 (either bi-directional diode or varistor solution) and bus filter capacitors C5 and C7 are shown in Figure 34.

The bus transient protection and filtering components should be placed as close to the bus connector, J1, as possible. This prevents transients, ESD and noise from penetrating onto the board and disturbing other devices.

Bus termination: Figure 31 shows split termination. This is where the termination is split into two resistors, R5 and R6, with the center or split tap of the termination connected to ground via capacitor C6. Split termination provides common mode filtering for the bus. When termination is placed on the board instead of directly on the bus, care must be taken to ensure the terminating node is not removed from the bus as this will cause signal integrity issues if the bus is not properly terminated on both ends.

Bypass and bulk capacitors should be placed as close as possible to the supply pins of transceiver, examples C2, C3 (V_{CC}).

Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

To limit current of digital lines, serial resistors may be used. Examples are R1, R2, R3 and R4.

To filter noise on the digital IO lines, a capacitor may be used close to the input side of the IO as shown by C1 and C4.

Since the internal pull up and pull down biasing of the device is weak for floating pins, an external 1-kΩ to 10-kΩ pullup or pulldown resistor should be used to bias the state of the pin more strongly against noise during transient events.

Pin 1: If an open-drain host processor is used to drive the D pin of the device an external pullup resistor between 1 kΩ and 10 kΩ should be used to drive the recessive input state of the device.

Pin 5: is V_{REF} output voltage reference, if used, this pin should be tied to the common mode point of the split termination. If V_{REF} is not used, the pin can be left floating.

Pin 8: is shown assuming the mode pin, R_S, will be used. If the device will only be used in high-speed mode or slope control mode, R3 is not needed and the pads of C4 could be used for the pulldown resistor to GND.

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11.2 Layout Example

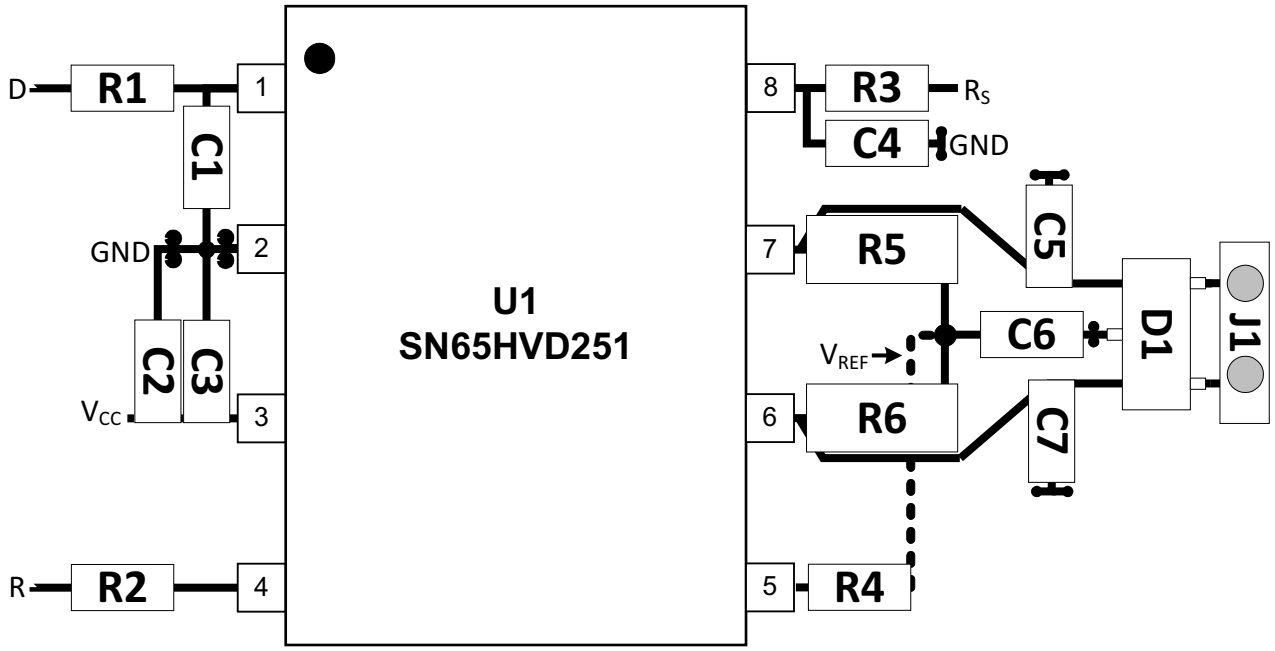

Figure 34. Layout Example Recommendation

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN55HVD251	Click here	Click here	Click here	Click here	Click here
SN65HVD251	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN55HVD251DRJR	Active	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	SN55 HVD251
SN55HVD251DRJR.A	Active	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	SN55 HVD251
SN55HVD251DRJRG4	Active	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	SN55 HVD251
SN55HVD251DRJRG4.A	Active	Production	SON (DRJ) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	SN55 HVD251
SN65HVD251DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP251
SN65HVD251DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP251
SN65HVD251DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP251
SN65HVD251P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	65HVD251
SN65HVD251P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	65HVD251
SN65HVD251PE4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	65HVD251

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65HVD251 :

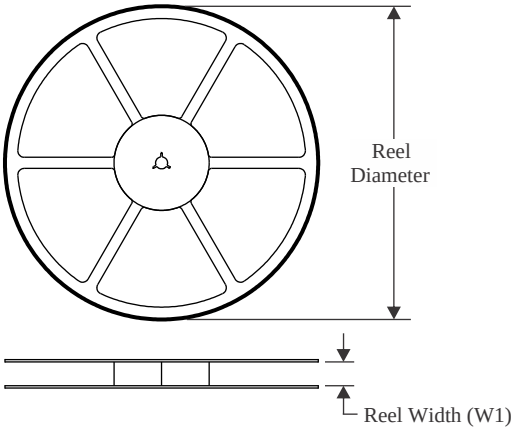
- Automotive : SN65HVD251-Q1

NOTE: Qualified Version Definitions:

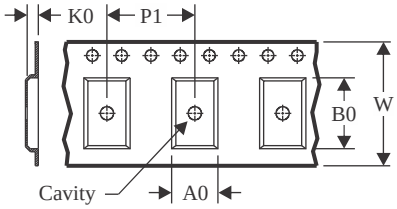
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

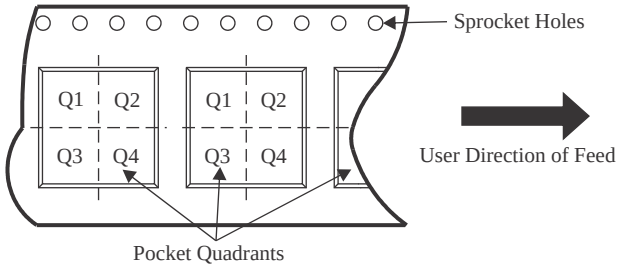


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

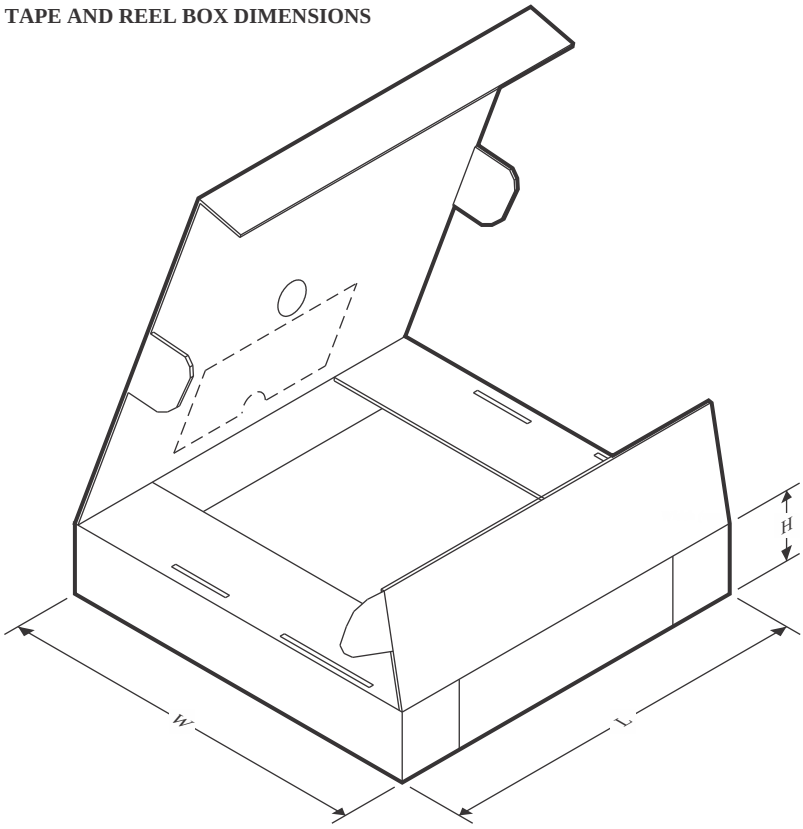
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN55HVD251DRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN55HVD251DRJRG4	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65HVD251DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

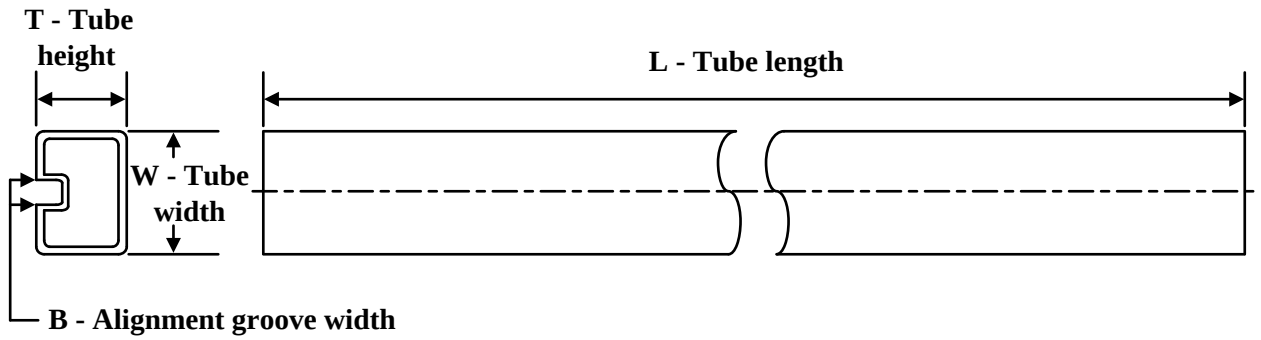
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN55HVD251DRJR	SON	DRJ	8	1000	213.0	191.0	35.0
SN55HVD251DRJRG4	SON	DRJ	8	1000	213.0	191.0	35.0
SN65HVD251DR	SOIC	D	8	2500	353.0	353.0	32.0

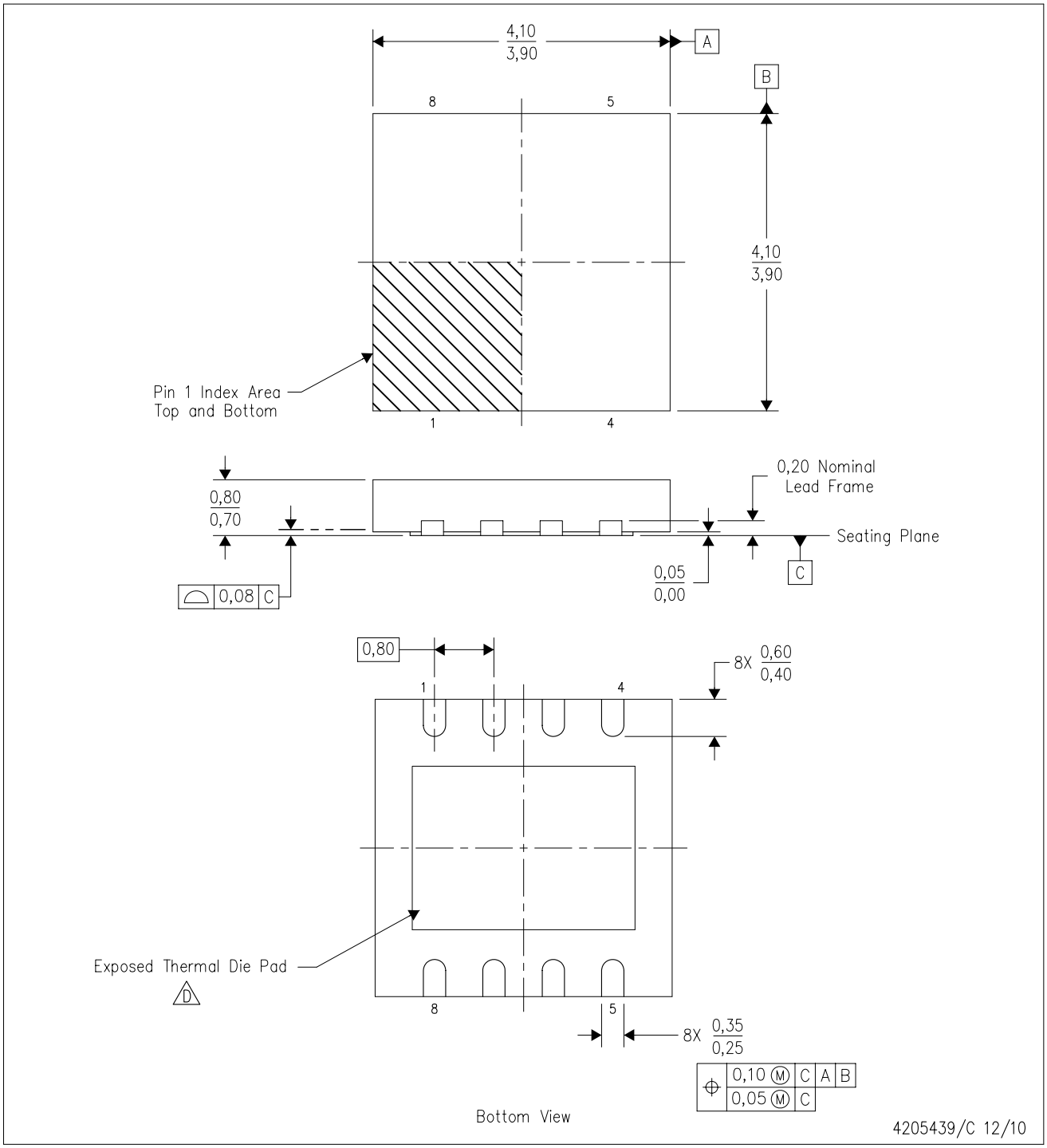
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD251P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD251P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD251PE4	P	PDIP	8	50	506	13.97	11230	4.32

DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–229 variation WGGB.

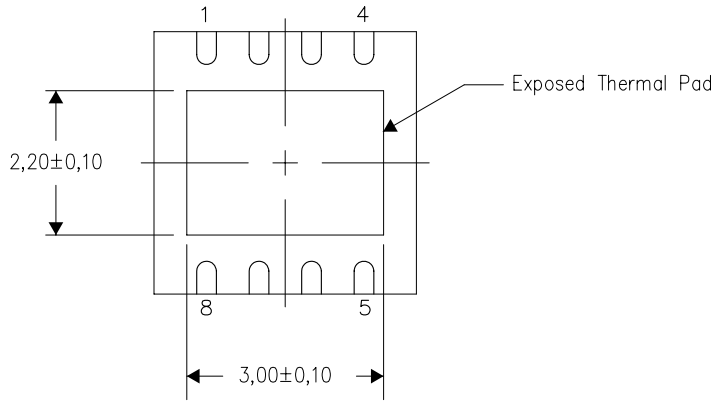
DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



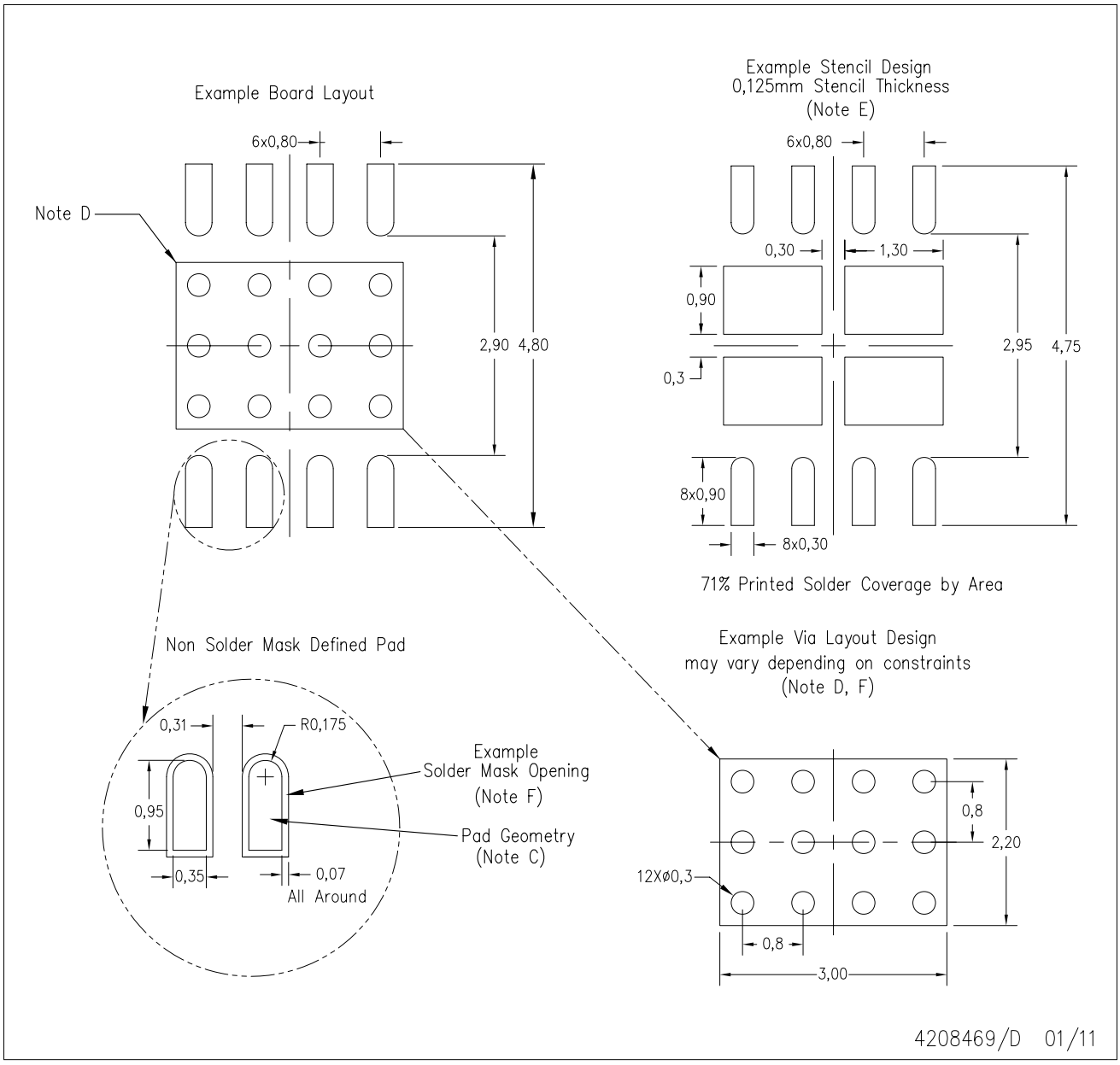
Bottom View

Exposed Thermal Pad Dimensions

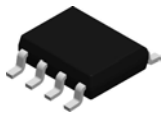
4206882/F 01/11

NOTE: All linear dimensions are in millimeters

DRJ (S–PWSON–N8) SMALL PACKAGE OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances and vias tenting recommendations for vias placed in the thermal pad.

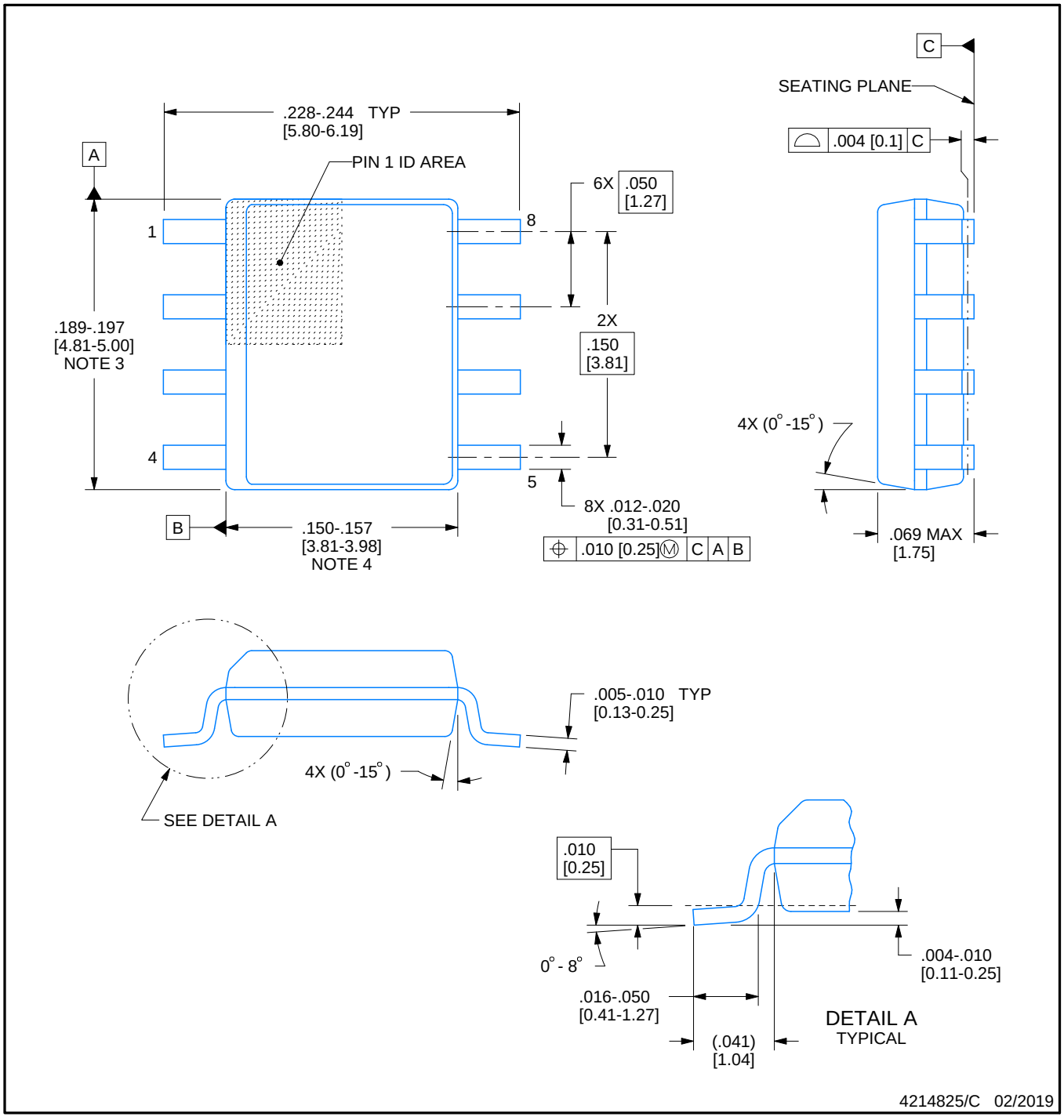


PACKAGE OUTLINE

D0008A

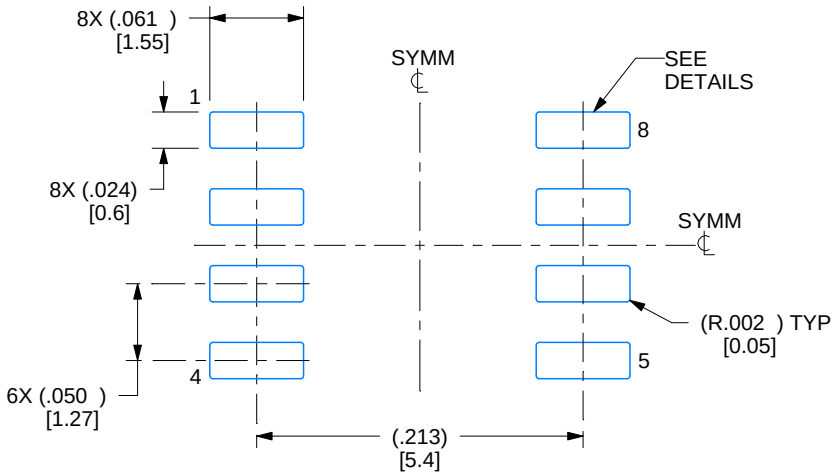
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

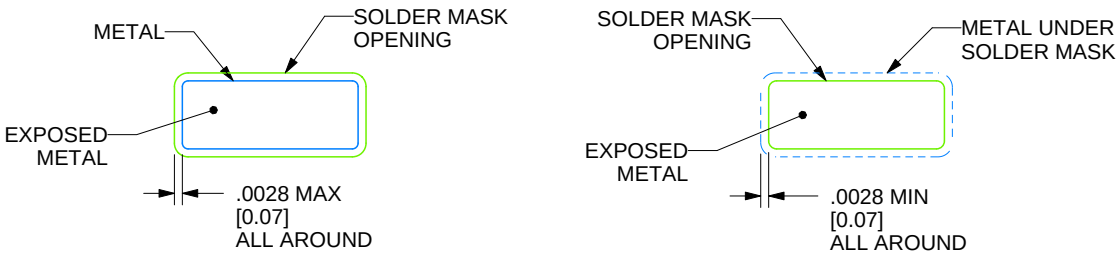


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

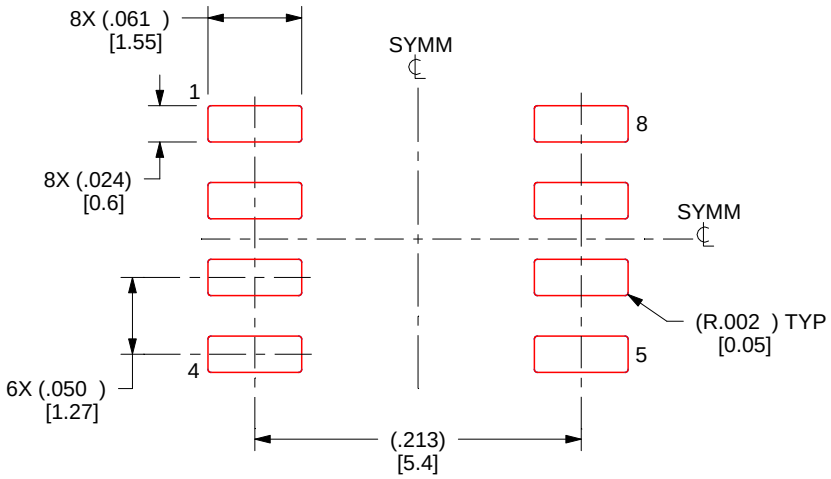
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



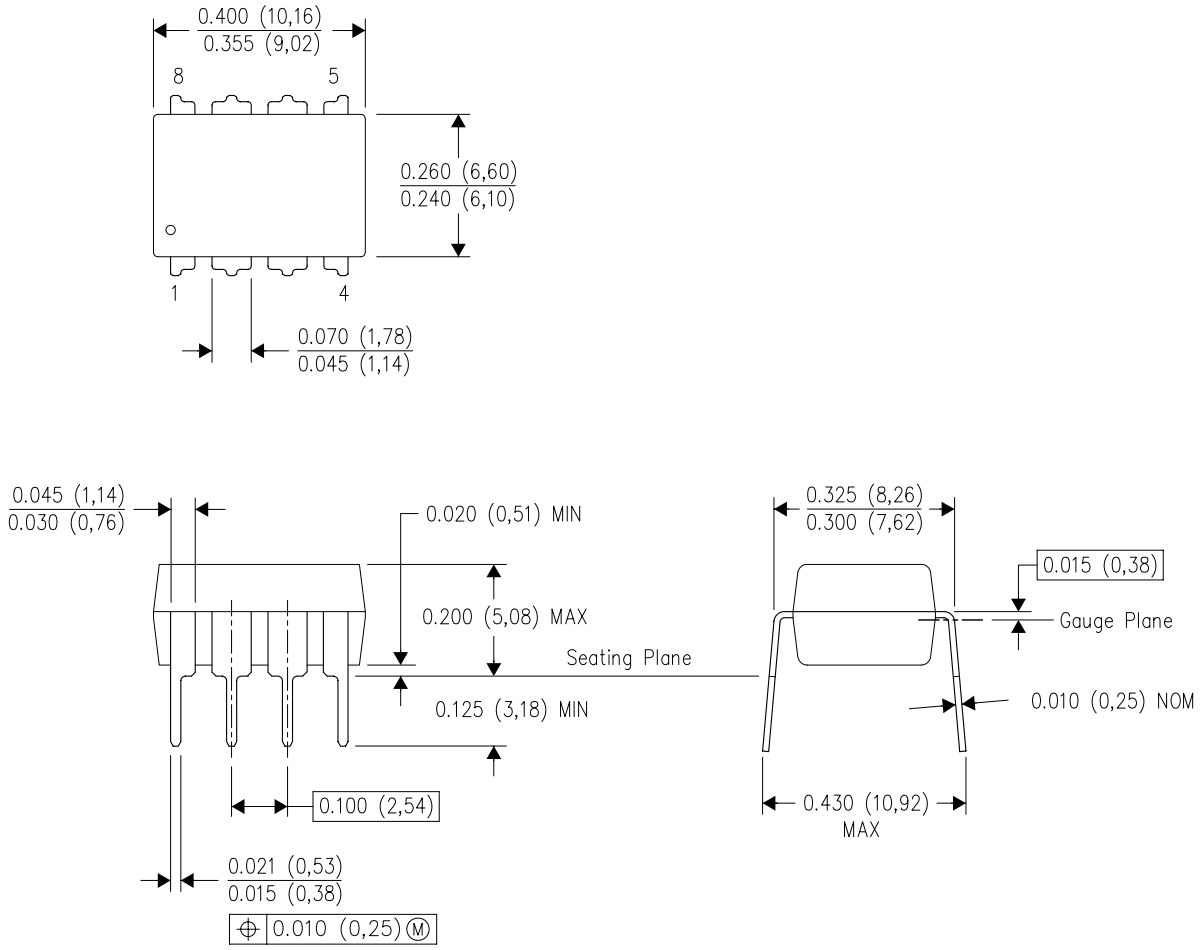
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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