



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The SN65HVDA540/SN65HVDA541 has an I/O supply voltage input pin (V_{IO} , pin 5) to ratiometrically level shift the digital logic input and output levels with respect to V_{IO} for compatibility with protocol controllers having I/O supply voltages between 3 V and 5.25 V. The V_{IO} supply also powers the low-power bus monitor and wake-up receiver of the SN65HVDA541 allowing the 5 V (V_{CC}) supply to be switched off for additional power savings at the system level during standby mode for either the SN65HVDA540 or SN65HVDA541. The 5 V (V_{CC}) supply needs to be reactivated by the local protocol controller at any time to resume high speed operation if it has been turned off for low-power standby operation. Both of the supply pins have undervoltage detection which place the device in standby mode to protect the bus during an undervoltage event on either the V_{CC} or V_{IO} supply pins. If V_{IO} is undervoltage the RXD pin is 3-statedn and the device does not pass any wake-up signals from the bus to the RXD pin.

STB (pin 8) provides for two different modes of operation: normal mode or low-power standby mode. The normal mode of operation is selected by applying a low logic level to STB. If a high logic level is applied to STB, the device enters standby mode (see Figure 1 and Figure 2). In standby mode, the SN65HVDA541 provides a wake-up receiver and monitor that remains active supplied via the V_{IO} pin so that V_{CC} may be removed allowing a system level reduction in standby current. A dominant signal on the bus longer than the wake-up signal time (t_{BUS}) is passed to the receiver output (RXD, pin 4) by the wake-up bus monitor circuit. The local protocol controller may then return the device to normal mode when the system needs to transmit or fully monitor the messages on the bus. If the bus has a fault condition where it is stuck dominant while the SN65HVDA541 is placed into standby mode, the device locks out the wake-up receiver output to RXD until the fault has been removed to prevent false wake-up signals in the system. Because the SN65HVDA540 does not have a low-power bus monitor and wake-up receiver, it provides a logic high output (recessive) on RXD while in standby mode.

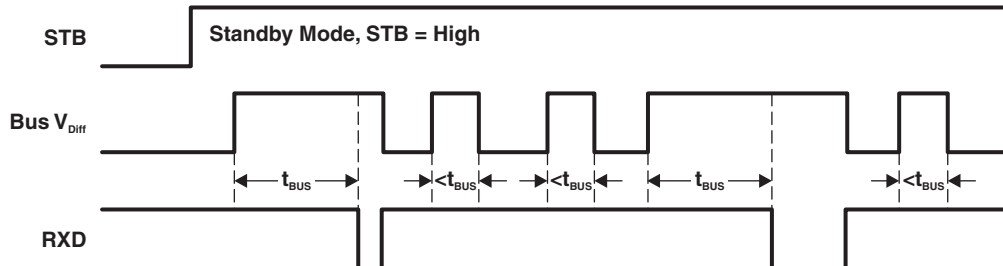


Figure 1. SN65HVDA541 Entering Standby Mode With Bus Recessive Condition

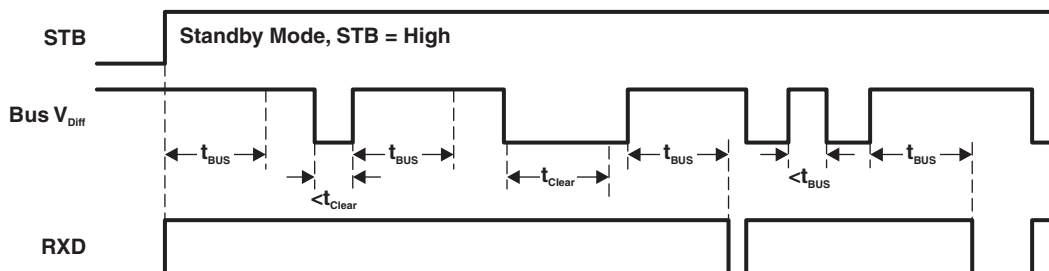
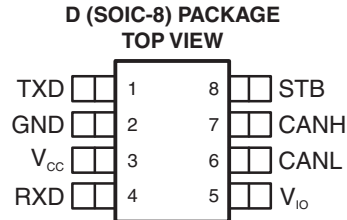


Figure 2. SN65HVDA541 Entering Standby Mode With Bus Dominant Condition

A dominant time-out circuit prevents the driver from blocking network communication in event of a hardware or software failure. The dominant time out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is reset by the next rising edge on TXD.



TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
TXD	1	I	CAN transmit data input (low for dominant bus state, high for recessive bus state)
GND	2	GND	Ground connection
V _{CC}	3	Supply	Transceiver 5-V supply voltage
RXD	4	O	CAN receive data output (low in dominant bus state, high in recessive bus state)
V _{IO}	5	Supply	Transceiver logic-level supply voltage
CANL	6	I/O	Low-level CAN bus line
CANH	7	I/O	High-level CAN bus line
STB	8	I	Standby mode select pin (active high)

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	SN65HVDA540QDR	A540Q
			SN65HVDA541QDR	A541Q

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

1.1	V _{CC}	Supply voltage range	–0.3 V to 6 V
1.2	V _{IO}	I/O supply voltage range	–0.3 V to 6 V
1.3		Voltage range at bus terminals (CANH, CANL)	–27 V to 40 V
1.4	I _O	Receiver output current	20 mA
1.5	V _I	Voltage input range (TXD, STB)	–0.3 V to 6 V and V _I ≤ V _{IO} + 0.3 V
1.6	T _J	Operating virtual-junction temperature range	–40°C to 150°C
1.7	T _{LEAD}	Lead temperature (soldering, 10 seconds)	260°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

ELECTROSTATIC DISCHARGE PROTECTION

PARAMETER		TEST CONDITIONS		VALUE
2.1	Electrostatic discharge	Human-Body Model ⁽¹⁾	Bus terminals (CANH, CANL) and GND ⁽²⁾	±12 kV
2.2			All pins	±4 kV
2.3		Charged-Device Model ⁽³⁾	All pins	±1 kV
2.4		Machine Model ⁽⁴⁾		±200 V

(1) Tested in accordance JEDEC Standard 22, Test Method A114-E

(2) Test method based upon JEDEC Standard 22 Test Method A114-E, CANH and CANL bus pins stressed with respect to each other and GND.

(3) Tested in accordance JEDEC Standard 22, Test Method C101

(4) Tested in accordance JEDEC Standard 22, Test Method A115-A

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT	
3.1	V _{CC}	Supply voltage	4.75	5.25	V	
3.2	V _{IO}	I/O supply voltage	3	5.25	V	
3.3	V _I or V _{IC}	Voltage at any bus terminal (separately or common mode)	-12	12	V	
3.4	V _{IH}	High-level input voltage	TXD, STB	0.7 × V _{IO}	V	
3.5	V _{IL}	Low-level input voltage	TXD, STB	0	0.3 × V _{IO}	V
3.6	V _{ID}	Differential input voltage, bus	Between CANH and CANL	-6	6	V
3.7	I _{OH}	High-level output current	RXD	-2		mA
3.8	I _{OL}	Low-level output current	RXD		2	mA
3.9	T _A	Operating ambient free-air temperature	See <i>Thermal Characteristics</i> table	-40	125	°C

SUPPLY CHARACTERISTICS

over recommended operating conditions, $T_J = -40^{\circ}\text{C}$ to 150°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
4.1	I_{CC}	5-V supply current	Standby mode	STB at V_{IO} , $V_{CC} = 5.25\text{ V}$, $V_{IO} = 3\text{ V}$, TXD at V_{IO} ⁽²⁾		5	μA	
4.2			Normal mode: Dominant	TXD at 0 V, 60- Ω load, STB at 0 V		50	70	mA
4.3			Normal mode: Recessive	TXD at V_{IO} , No load, STB at 0 V		6	10	
4.4	I_{IO}	I/O supply current	Standby mode	STB at V_{IO} , $V_{CC} = 5.25\text{ V}$ or 0 V, RXD floating, TXD at V_{IO}		7	15	μA
4.5			Normal mode (recessive or dominant)	STB at 0 V, $V_{CC} = 5.25\text{ V}$, RXD floating, TXD at 0 V or V_{IO}		75	300	
4.6	UV_{VCC}	Undervoltage detection on V_{CC} for forced standby mode			3.6		V	
4.7	$V_{HYS(UV_{VCC})}$	Hysteresis voltage for undervoltage detection on UV_{VCC} for standby mode			200		mV	
4.8	UV_{VIO}	Undervoltage detection on V_{IO} for forced standby mode			2.5		V	
4.9	$V_{HYS(UV_{VIO})}$	Hysteresis voltage for undervoltage detection on UV_{VIO} for forced standby mode			100		mV	

(1) All typical values are at 25°C and supply voltages of $V_{CC} = 5\text{ V}$ and $V_{IO} = 3.3\text{ V}$.

(2) The V_{CC} supply is not needed during standby mode so in the applicaiton I_{CC} in standby mode may be zero. If the V_{CC} supply remains, then I_{CC} is per specification with V_{CC} .

DEVICE SWITCHING CHARACTERISTICS

over recommended operating conditions, $T_J = -40^{\circ}\text{C}$ to 150°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
5.1	$t_{d(\text{LOOP1})}$	Total loop delay, driver input to receiver output, recessive to dominant	Figure 11, STB at 0 V	70		230	ns
5.2	$t_{d(\text{LOOP2})}$	Total loop delay, driver input to receiver output, dominant to recessive					

(1) All typical values are at 25°C and supply voltages of $V_{CC} = 5\text{ V}$ and $V_{IO} = 3.3\text{ V}$.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions, $T_J = -40^{\circ}\text{C}$ to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
6.1	$V_{O(D)}$ Bus output voltage (dominant)	CANH	$V_I = 0\text{ V}$, STB at 0 V , $R_L = 60\ \Omega$, See Figure 3 and Figure 4		2.9	4.5	V
6.2		CANL			0.8	1.75	
6.3	$V_{O(R)}$ Bus output voltage (recessive)	$V_I = V_{IO}$, $V_{IO} = 3\text{ V}$, STB at 0 V , $R_L = 60\ \Omega$, See Figure 3 and Figure 4	2	2.5	3	V	
6.4	V_O Bus output voltage (standby mode)	STB at V_{IO} , $R_L = 60\ \Omega$, See Figure 3 and Figure 4	-0.1		0.1	V	
6.5	$V_{OD(D)}$ Differential output voltage (dominant)	$V_I = 0\text{ V}$, $R_L = 60\ \Omega$, STB at 0 V , See Figure 3 , Figure 4 , and Figure 5			1.5	3	V
6.6		$V_I = 0\text{ V}$, $R_L = 45\ \Omega$, STB at 0 V , See Figure 3 , Figure 4 , and Figure 5			1.4	3	
6.7	$V_{OD(R)}$ Differential output voltage (recessive)	$V_I = 3\text{ V}$, STB at 0 V , $R_L = 60\ \Omega$, See Figure 3 and Figure 4	-0.012		0.012	V	
6.8		$V_I = 3\text{ V}$, STB at 0 V , No load			-0.5		0.05
6.9	V_{SYM} Output symmetry (dominant or recessive) ($V_{O(CANH)} + V_{O(CANL)}$)	STB at 0 V , $R_L = 60\ \Omega$, See Figure 15	$0.9 V_{CC}$	V_{CC}	$1.1 V_{CC}$	V	
6.10	$V_{OC(ss)}$ Steady-state common-mode output voltage	STB at 0 V , $R_L = 60\ \Omega$, See Figure 10	2	2.5	3	V	
6.11	$\Delta V_{OC(ss)}$ Change in steady-state common-mode output voltage				30	mV	
6.12	I_{IH} High-level input current, TXD input	TXD at V_{IO}	-2		2	μA	
6.13	I_{IL} Low-level input current, TXD input	TXD at 0 V	-100		-7	μA	
6.14	$I_{O(off)}$ Power-off TXD output current	$V_{CC} = 0\text{ V}$, $V_{IO} = 0\text{ V}$, TXD at 5.25 V			1	μA	
6.15	$I_{OS(ss)}$ Short-circuit steady-state output current	$V_{CANH} = -12\text{ V}$, CANL open, See Figure 13	-120	-85		mA	
6.16		$V_{CANH} = 12\text{ V}$, CANL open, See Figure 13			0.5		1
6.17		$V_{CANL} = -12\text{ V}$, CANH open, See Figure 13	-1	-0.6			
6.18		$V_{CANL} = 12\text{ V}$, CANH open, See Figure 13			75		120
6.19	C_O Output capacitance	See receiver input capacitance					

(1) All typical values are at 25°C and supply voltages of $V_{CC} = 5\text{ V}$ and $V_{IO} = 3.3\text{ V}$.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions, $T_J = -40^{\circ}\text{C}$ to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
7.1	t_{PLH} Propagation delay time, low-to-high level output	STB at 0 V , See Figure 6	65		120	ns
7.2	t_{PHL} Propagation delay time, high-to-low level output	STB at 0 V , See Figure 6	50		120	
7.3	t_r Differential output signal rise time	STB at 0 V , See Figure 6	25			
7.4	t_f Differential output signal fall time	STB at 0 V , See Figure 6	45			
7.5	t_{en} Enable time from standby mode to dominant	See Figure 9			10	μs
7.6	$t_{(dom)}$ Dominant time out	See Figure 12	300	400	700	μs

(1) All typical values are at 25°C and supply voltages of $V_{CC} = 5\text{ V}$ and $V_{IO} = 3.3\text{ V}$.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions, $T_J = -40^{\circ}\text{C}$ to 150°C (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
8.1	V_{IT+}	Positive-going input threshold voltage, normal mode	STB at 0 V, See Differential Input Voltage Threshold Test		800	900	mV
8.2	V_{IT-}	Negative-going input threshold voltage, normal mode	STB at 0 V, See Differential Input Voltage Threshold Test	500	650		mV
8.3	V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)		100	125		mV
8.4	V_{IT}	Input threshold voltage, standby mode (SN65HVDA541 only)	STB at V_{IO}	400		1150	mV
8.5	V_{OH}	High-level output voltage, RXD	$I_O = -2$ mA, See Figure 8	$0.8 \times V_{IO}$			V
8.6	V_{OL}	Low-level output voltage, RXD	$I_O = 2$ mA, See Figure 8			$0.2 \times V_{IO}$	V
8.7	$I_{I(off)}$	Power-off bus input current	CANH = CANL = 5 V, V_{CC} at 0 V, V_{IO} at 0 V, TXD at 0 V			3	μA
8.8	$I_{O(off)}$	Power-off RXD leakage current	V_{CC} at 0 V, V_{IO} at 0 V, RXD at 5.25 V			20	μA
8.9	C_I	Input capacitance to ground (CANH or CANL)	TXD at V_{IO} , V_{IO} at 3.3 V, $V_I = 0.4 \sin(4E6\pi t) + 2.5$ V	13			pF
8.10	C_{ID}	Differential input capacitance	TXD at V_{IO} , $V_{IO} = 3.3$ V, $V_I = 0.4 \sin(4E6\pi t)$	6			pF
8.11	R_{ID}	Differential input resistance	TXD at V_{IO} , $V_{IO} = 3.3$ V, STB at 0 V	29		80	k Ω
8.12	R_{IN}	Input resistance (CANH or CANL)	TXD at V_{IO} , $V_{IO} = 3.3$ V, STB at 0 V	14.5	25	40	k Ω
8.13	$R_{I(m)}$	Input resistance matching $[1 - (R_{IN(CANH)}/R_{IN(CANL)})] \times 100\%$	$V_{(CANH)} = V_{(CANL)}$	-3	0	3	%

(1) All typical values are at 25°C and supply voltages of $V_{CC} = 5$ V and $V_{IO} = 3.3$ V.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions, $T_J = -40^{\circ}\text{C}$ to 150°C (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
9.1	t_{PLH}	Propagation delay time, low-to-high-level output	STB at 0 V, See Figure 8		85	150	ns
9.2	t_{PHL}	Propagation delay time, high-to-low-level output			55	130	ns
9.3	t_r	Output signal rise time			8		ns
9.4	t_f	Output signal fall time			8		ns
9.5	t_{BUS}	Dominant time required on bus for wake-up from standby (SN65HVDA541 only)	STB at V_{IO} , See Figure 14	1.5		5	μs
9.6	t_{CLEAR}	Recessive time on the bus to clear the standby mode receiver output (RXD) if standby mode is entered while bus is dominant (SN65HVDA541 only)		1.5		5	μs

(1) All typical values are at 25°C and supply voltages of $V_{CC} = 5$ V and $V_{IO} = 3.3$ V.

STB PIN CHARACTERISTICS

over recommended operating conditions, $T_J = -40^{\circ}\text{C}$ to 150°C (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
10.1	I_{IH}	High-level input current	STB at V_{IO}			15	μA
10.2	I_{IL}	Low-level input current	STB at 0 V	-20			

(1) All typical values are at 25°C and supply voltages of $V_{CC} = 5$ V and $V_{IO} = 3.3$ V.

THERMAL CHARACTERISTICS

over recommended operating conditions, $T_J = -40^{\circ}\text{C}$ to 150°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
11.1	θ_{JA}	Junction-to-air thermal resistance ⁽¹⁾	Low-K thermal resistance ⁽²⁾		140		$^{\circ}\text{C}/\text{W}$
11.2			High-K thermal resistance ⁽²⁾		109		
11.3	θ_{JB}	Junction-to-board thermal resistance			50		$^{\circ}\text{C}/\text{W}$
11.4	θ_{JC}	Junction-to-case thermal resistance			56		$^{\circ}\text{C}/\text{W}$
11.5	P_D	Average power dissipation	$V_{CC} = 5\text{ V}$, $V_{IO} = 3.3\text{ V}$, $T_J = 27^{\circ}\text{C}$, $R_L = 60\ \Omega$, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF		112		mW
11.6			$V_{CC} = 5.5\text{ V}$, $V_{IO} = 3.3\text{ V}$, $T_J = 130^{\circ}\text{C}$, $R_L = 45\ \Omega$, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF			170	
11.7	Thermal shutdown temperature				185		$^{\circ}\text{C}$

- (1) The junction temperature (T_J) is calculated using the following $T_J = T_A + (P_D \times \theta_{JA})$
(2) Tested in accordance with the Low-K (EIA/JESD51-3) or High-K (EIA/JESD51-7) thermal metric definitions for leaded surface-mount packages.

OPERATING MODE SELECTION

V_{CC}	V_{IO}	STB ⁽¹⁾	BUS STATE	RXD STATE
$V_{CC} \geq UV_{VCC}$	$V_{IO} \geq UV_{VIO}$	L	Normal Mode	Mirrors bus state
$V_{CC} \geq UV_{VCC}$	$V_{IO} \geq UV_{VIO}$	H	Standby Mode	Mirrors bus state via wake-up filter ⁽²⁾
$V_{CC} \leq UV_{VCC}$	$V_{IO} \geq UV_{VIO}$	X	Standby Mode (Forced)	Mirrors bus state via wake-up filter ⁽²⁾
$V_{CC} \geq UV_{VCC}$	$V_{IO} \leq UV_{VIO}$	X	Standby Mode (Forced) ⁽³⁾	3-state

- (1) H = high level, L = low level, X = irrelevant
(2) SN65HVDA541 only. SN65HVDA540 RXD state is recessive.
(3) When V_{IO} is undervoltage, the device is forced into standby mode with respect to the CAN bus since there is not a valid digital reference to determine the digital I/O states or power the wake-up receiver.

FUNCTION TABLES

DRIVER

INPUTS		OUTPUTS		BUS STATE
TXD ⁽¹⁾	STB ⁽¹⁾	CANH ⁽¹⁾	CANL ⁽¹⁾	
L	L	H	L	DOMINANT
H	L	Z	Z	RECESSIVE
Open	L	Z	Z	RECESSIVE
X	H or Open	Y	Y	RECESSIVE

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Y = weak pull down to GND, Z = high impedance

RECEIVER

DIFFERENTIAL INPUTS $V_{ID} = V(\text{CANH}) - V(\text{CANL})$	STB ⁽¹⁾	OUTPUT RXD ⁽¹⁾		BUS STATE
X	H or Open	SN65HVDA540 ⁽²⁾	H	X
$V_{ID} \geq 1.15 \text{ V}$		SN65HVDA541 ⁽³⁾	L	DOMINANT
$0.4 \text{ V} < V_{ID} < 1.15 \text{ V}$?	?
$V_{ID} \leq 0.4 \text{ V}$			H	RECESSIVE
$V_{ID} \geq 0.9 \text{ V}$	L	L		DOMINANT
$0.5 \text{ V} < V_{ID} < 0.9 \text{ V}$	L	?		?
$V_{ID} \leq 0.5 \text{ V}$	L	H		RECESSIVE
Open	X	H		RECESSIVE

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Y = weak pull down to GND, Z = high impedance

(2) While STB is high (standby mode) the RXD output of the SN65HVDA540 is always high (recessive) because it has no wake-up receiver

(3) While STB is high (standby mode) the RXD output of the SN65HVDA541 functions according to the levels above and the wake-up conditions shown in Figure 1 and Figure 2.

PARAMETER MEASUREMENT INFORMATION

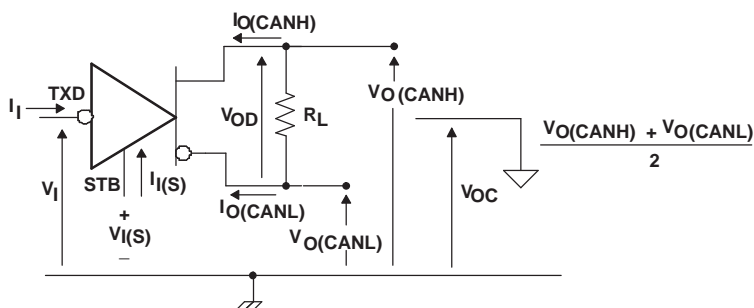


Figure 3. Driver Voltage, Current, and Test Definition

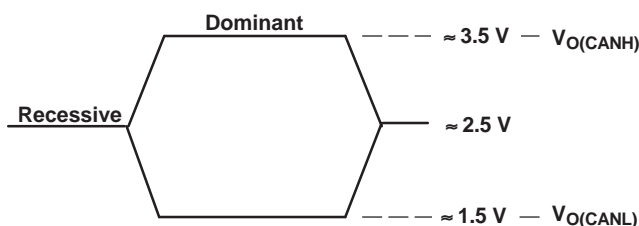


Figure 4. Bus Logic-State Voltage Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

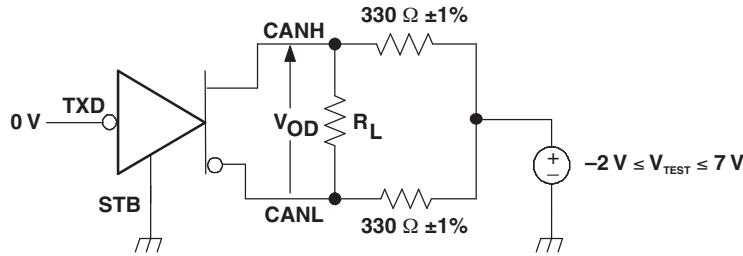
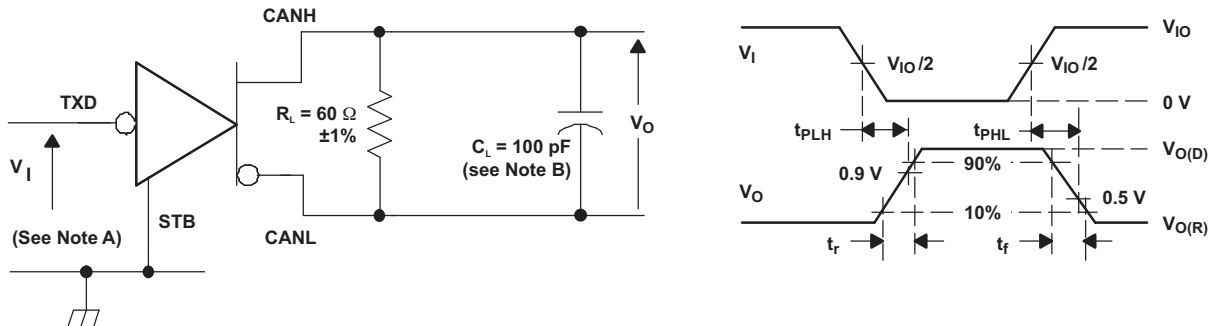


Figure 5. Driver V_{OD} Test Circuit



- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 125$ kHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- B. C_L includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 6. Driver Test Circuit and Voltage Waveforms

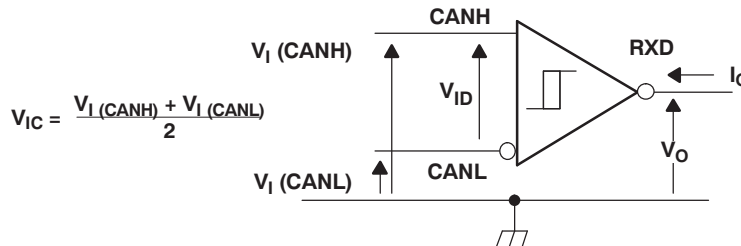
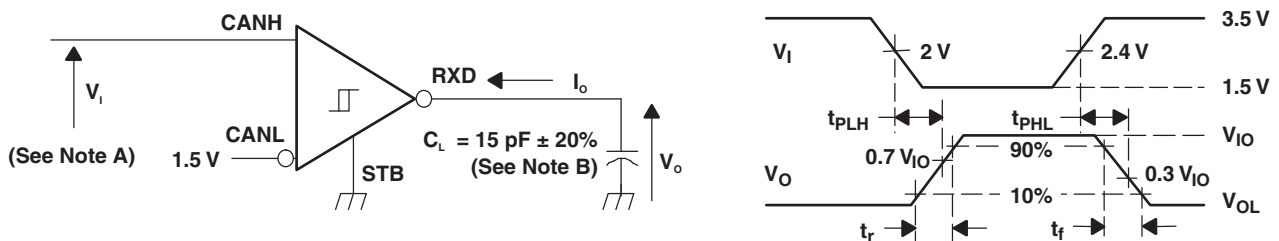


Figure 7. Receiver Voltage and Current Definitions

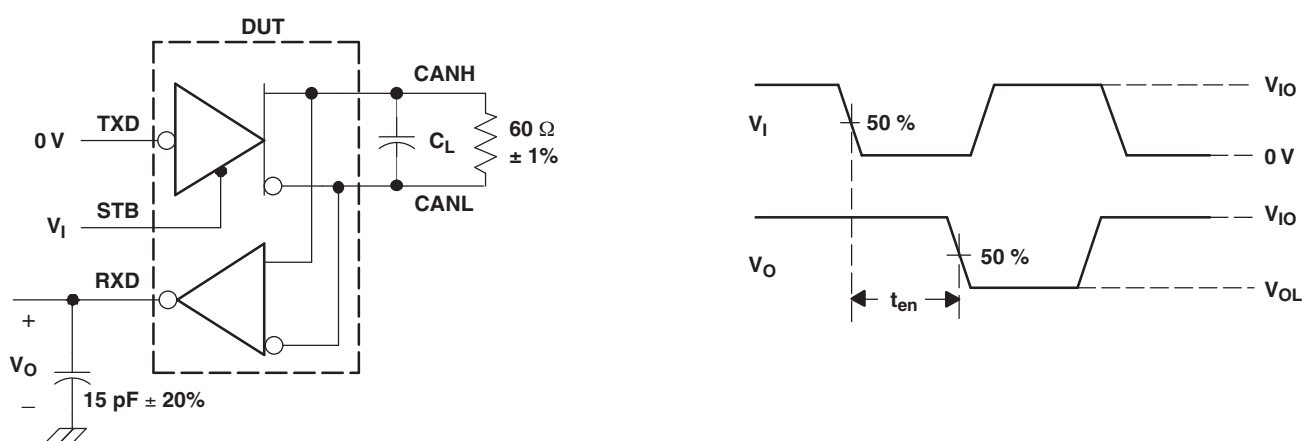


- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 125$ kHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- B. C_L includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 8. Receiver Test Circuit and Voltage Waveforms

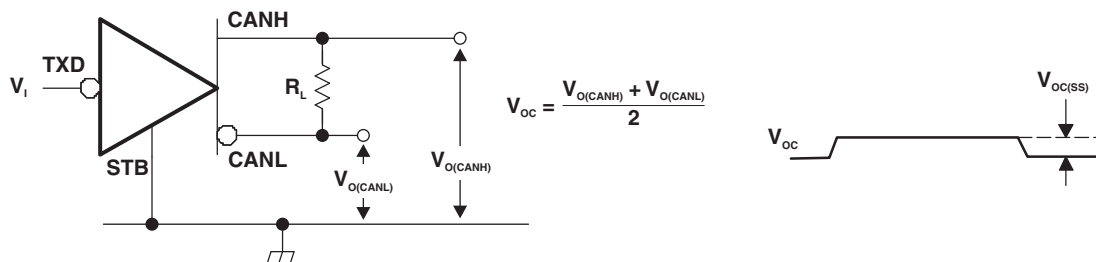
Differential Input Voltage Threshold Test

INPUT			OUTPUT
V_{CANH}	V_{CANL}	$ V_{ID} $	R
-11.1 V	-12 V	900 mV	L
12 V	11.1 V	900 mV	L
-6 V	-12 V	6 V	L
12 V	6 V	6 V	L
-11.5 V	-12 V	500 mV	H
12 V	11.5 V	500 mV	H
-12 V	-6 V	6 V	H
6 V	12 V	6 V	H
Open	Open	X	H



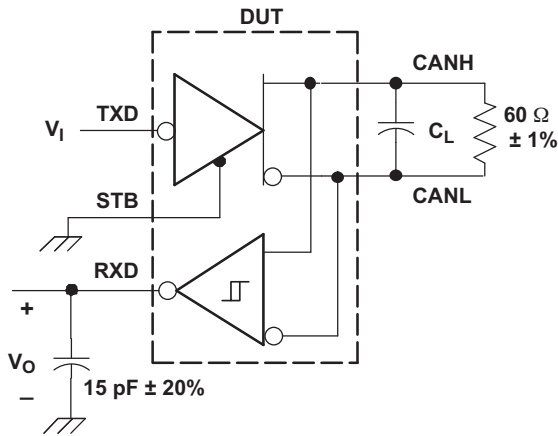
- A. $C_L = 100$ pF includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns. Pulse Repetition Rate (PRR) = 25 kHz, 50% duty cycle.

Figure 9. t_{en} Test Circuit and Waveforms



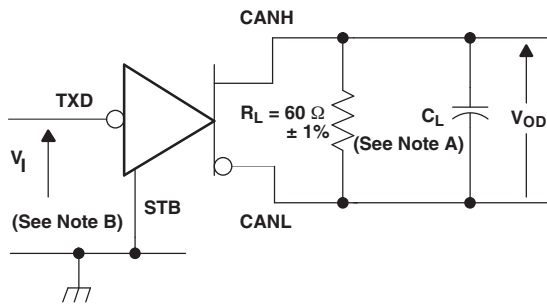
- A. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 10. Common-Mode Output Voltage Test and Waveforms



- A. $C_L = 100 \text{ pF}$ includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or $t_f \leq 6 \text{ ns}$. Pulse Repetition Rate (PRR) = 125 kHz , 50% duty cycle.

Figure 11. t_{LOOP} Test Circuit and Waveform



- A. $C_L = 100 \text{ pF}$ includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or $t_f \leq 6 \text{ ns}$. Pulse Repetition Rate (PRR) = 500 Hz , 50% duty cycle.

Figure 12. Dominant Time-Out Test Circuit and Waveforms

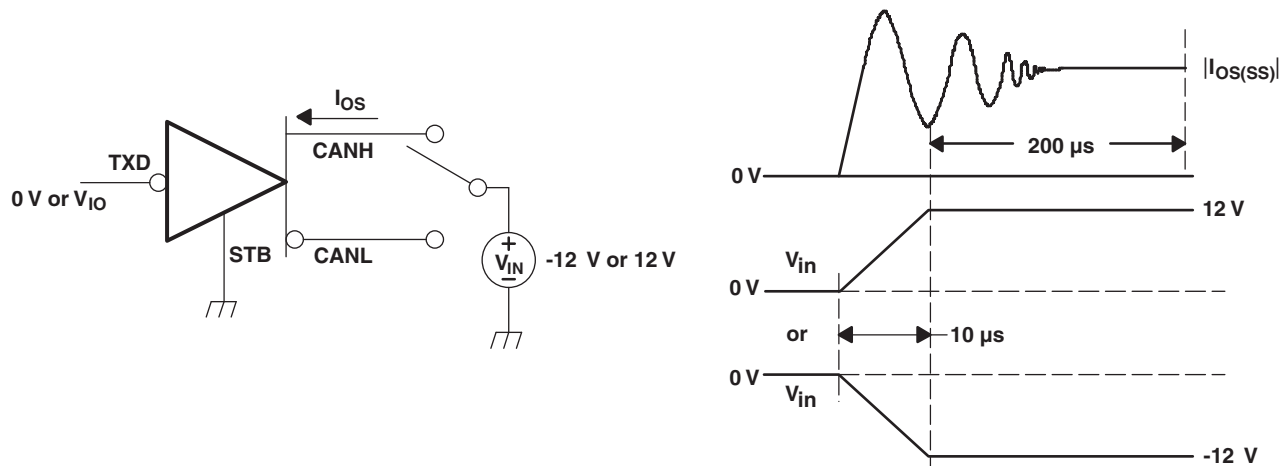
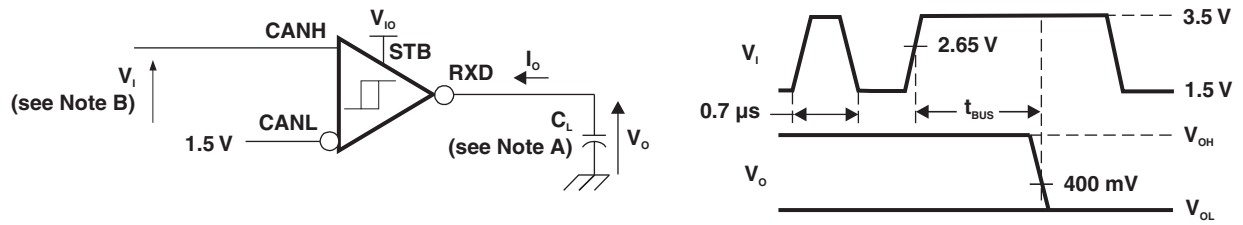
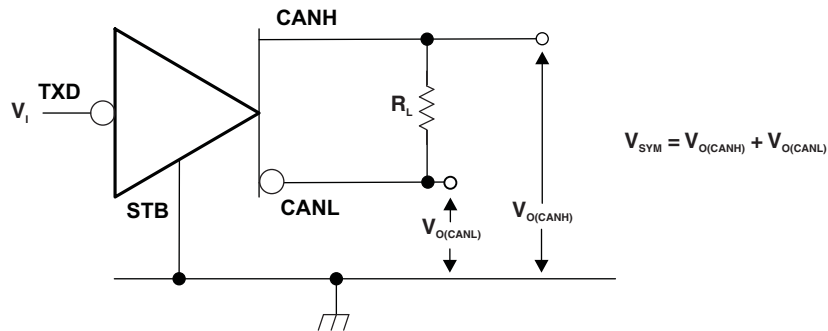


Figure 13. Driver Short-Circuit Current Test and Waveforms



- A. $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. For V_I bit width $\leq 0.7 \text{ } \mu\text{s}$, $V_O = V_{OH}$. For V_I bit width $\geq 5 \text{ } \mu\text{s}$, $V_O = V_{OL}$. V_I input pulses are supplied from a generator with the following characteristics: $t_r/t_f < 6 \text{ ns}$.

Figure 14. t_{BUS} Test Circuit and Waveforms



- A. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: $t_r/t_f \leq 6 \text{ ns}$, Pulse Repetition Rate (PRR) = 250 kHz , 50% duty cycle.

Figure 15. Driver Output Symmetry Test Circuit

APPLICATION INFORMATION

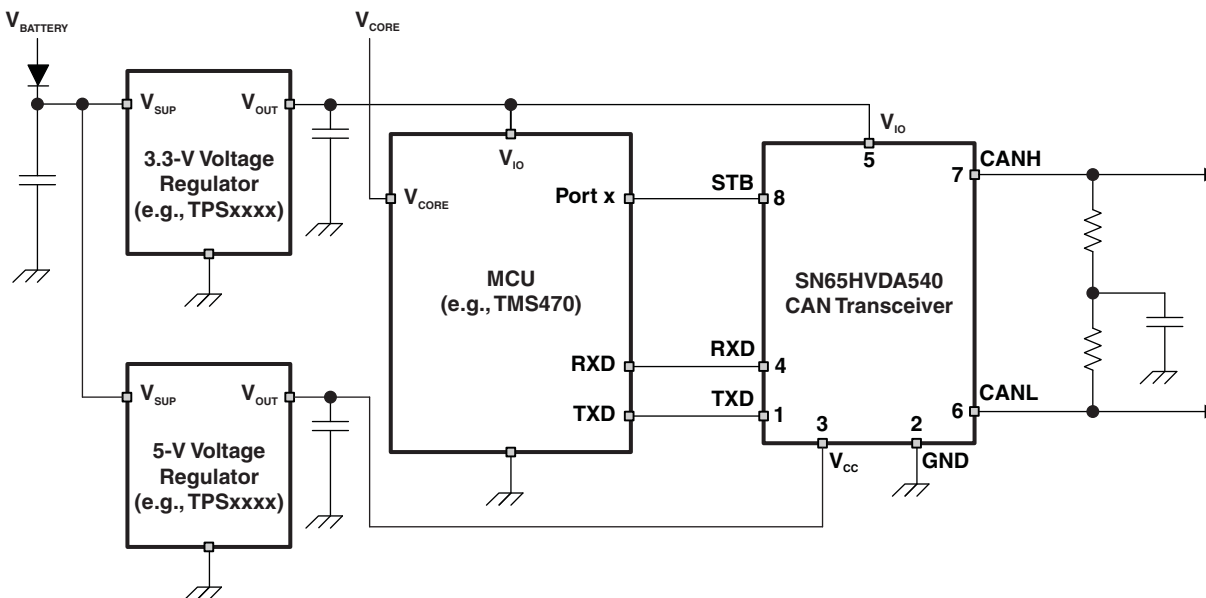


Figure 16. Typical Application Using 3.3 V I/O voltage level

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVDA540QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A540Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN65HVDA540 :

- Automotive: [SN65HVDA540-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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