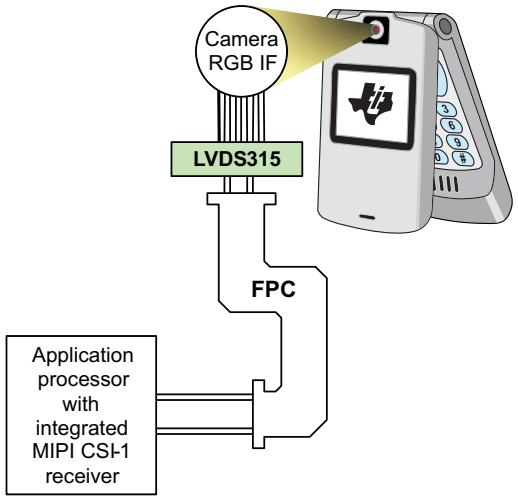
SN65LVDS315 Camera Parallel RGB to MIPI CSI-1 Serial Converter

1 Features

- MIPI CSI-1 and SMIA CCP Support
- Connects Directly to OMAP CSI Interface
- 4×4 mm QFN Package
- ESD Rating >3 kV (HBM) Camera Input Ports and >2 kV (HBM) All Other Ports
- Pixel Clock Range 3.5–27 MHz
- Three Operating Modes to Conserve Power
  - Active Mode VGA Camera 30 fps: 7 mA
  - Typical Shutdown and Standby: 0.5 µA
  - Operating Temperature Range –40°C to 85°C
  - Input Data Voltage Range From 1.8 V to 3.3 V
- EMI

2 Applications

- Camera to Host Controller (e.g. OMAP2420, OMAP2430, OMAP3430)
- Mobile Phones and Smart Phones



3 Description

The SN65LVDS315 is a camera serializer that converts 8-bit parallel camera data into MIPI-CSI1 or SMIA CCP compliant serial signals.

The device converts the parallel 8-bit data to two sub-low-voltage differential signaling (SubLVDS) serial data and clock output. Meanwhile the serialized data is presented on the differential serial data output DOUT with a differential clock signal on output CLK. Where The frequency of CLK is 8x DCLK input pixel clock rate.

The SN65LVDS315 supports three power modes (Shutdown, standby and active) to conserve power.

All CMOS inputs offer failsafe operation to protect the input from damage during power up and to avoid current flow into the device inputs during power up. The core supply of the SN65LVDS315 is 1.8 V. To provide greater flexibility, the camera data inputs support a supply range from 1.8 V to 3.3 V and the device is characterized for operation over ambient air temperatures of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LVDS315	VQFN (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (September 2012) to Revision G — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Replaced Dissipation Ratings with Thermal Information ... 1

Changes from Revision E (August 2012) to Revision F — **Page**

- deleted $\Delta V_{OCM(SS)}$ and $V_{OCM(PP)}$ From the OUTPUT ELECTRICAL CHARACTERISTICS ... 8
- Changed the RECEIVER TERMINATION REQUIREMENT section ... 27

Changes from Revision D (February 2012) to Revision E — **Page**

- Added the RECEIVER TERMINATION REQUIREMENT section ... 27

Changes from Revision C (June 2001) to Revision D — **Page**

- Changed Feature From: Pixel Clock Range 3.5–26 MHz To: Pixel Clock Range 3.5–27 MHz ... 1
- Chnaged the pin function for FSEL From: FSEL=1: DCLK input frequencies from 7.0 MHz to 26 MHz are supported To: FSEL=1: DCLK input frequencies from 7.0 MHz to 27 MHz are supported ... 5
- Changed Data clock frequency for FSEL = 1 in the ROC table From: MAX = 26 MHz To: MAX = 27 MHz ... 6
- Changed the ROC table section MODE, TXEN, FSEL To: MODE, TXEN ... 6
- Added section FSEL to the ROC table ... 6
- Changed the TYPICAL APPLICATION FREQUENCIES section. From: The SN65LVDS315 in display mode supports pixel clock frequencies from 7 MHz to 26 MHz To: The SN65LVDS315 in display mode supports pixel clock frequencies from 7 MHz to 27 MHz ... 30

Changes from Revision B (November 2008) to Revision C **Page**

- Changed Figure 17: Note E - From: "Time between HS falling and HS rising edge" To: "Time between VS falling and VS rising edge 18
- Changed the Acquire Mode (PLL Approaches Lock) section. From: "HS low-to-high" To: VS low-to-high and From "MODE is set low"; To: "MODE is set high" 24
- Changed text in the VGA CAMERA APPLICATION section From: The pixel clock rate is 11 MHz, assuming ≠10% blanking overhead. To: The pixel clock rate is 11 MHz, assuming ≈20% blanking overhead 28

Changes from Revision A (March 2008) to Revision B **Page**

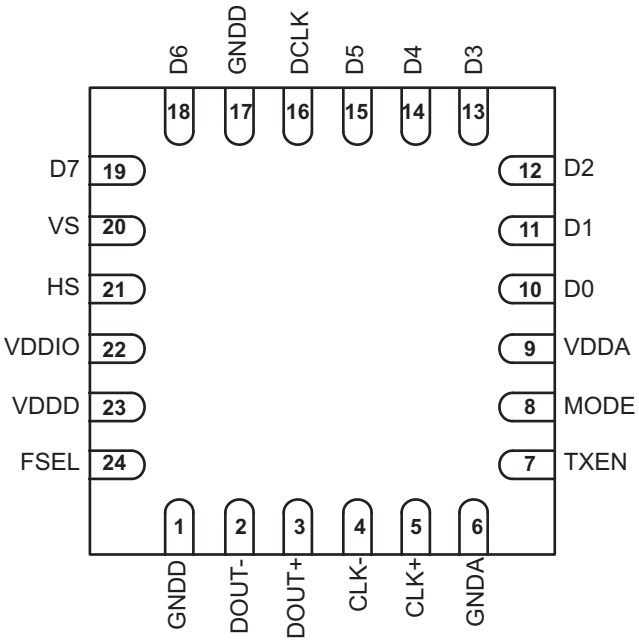
- Changed the Absoulute Maximum Ratings table - Voltage range at any input terminal value From: –0.5 to 2.175 To: –0.5 to VDDIO + 0.5V..... 5

Changes from Original (December 2007) to Revision A **Page**

- Changed the document from: Product Preview To: Production 1

5 Pin Configuration and Functions

24-Pin 0.5-mm Pitch QFN (Top View)



Pin Functions

PIN			DESCRIPTION
NO.	NAME	TYPE	
2, 3,	DOUT+, DOUT–	SubLVDS out	SubLVDS data link CSI-1 compliant (active during normal operation; high-impedance during power down or standby) DOUT is valid on the rising edge of CLK+.
4, 5,	CLK+, CLK–		SubLVDS clock output (CSI-1 Mode 0 compliant)
10, 11, 12, 13, 14, 15, 18, 19	D0–D7	CMOS in(1)	Data inputs (8) for pixel data; These inputs are sampled on the falling DCLK edge; inputs incorporate bus hold Note: D[7:0] states are latched into the SN65LVDS315 on the falling DCLK input edge
20	VS		Vertical Sync (also called frame sync); Data input (high active). This input is sampled on every falling DCLK edge Input incorporates bus hold
21	HS		Horizontal Sync (also called line sync); Data input (high active). This input is sampled on every falling DCLK edge Input incorporates bus hold
16	DCLK		Data input Clock; DCLK represents the camera pixel clock. All 8 pixel bits as well as VS and HS are latched into the device on the falling edge of DCLK (falling edge clocking) Input incorporates bus hold

(1) These inputs are referenced to the VDDIO supply rail and support a voltage range of 1.65 V to 3.6 V

Pin Functions (continued)

PIN			DESCRIPTION
NO.	NAME	TYPE	
7	TXEN	CMOS in(2)	Disables the subLVDS Drivers and turns off the PLL putting device in Shutdown mode 1 – Transmitter enabled 0 – Transmitter disabled (shutdown) **Note:** TXEN input incorporates glitch-suppression logic to avoid device malfunction on short input spikes. It is necessary to pull TXEN high for longer than 10 µs to enable the transmitter. It is necessary to pull the TXEN input low for longer than 10 µs to disable the transmitter. At power up, the transmitter is enabled immediately if TXEN = 1 and disabled if TXEN = 0. Do not leave TXEN floating.
24	FSEL		Frequency Select FSEL=0: DCLK input frequencies from 3.5 MHz to 13 MHz are supported FSEL=1: DCLK input frequencies from 7.0 MHz to 27 MHz are supported Do not leave FSEL floating.
8	MODE		The mode pin enables line counting to generate proper EOF signalling in case VS and HS do not reset during the same DCLK cycle (0-line counter disable; 1-counter enabled). The impact of the MODE pin setting is described in detail in the *VS and HS Timing to Generate the Correct Control Signals* section. If you are unsure about the proper setting of the MODE input, it is recommended to set MODE=high. Do not leave the MODE input floating.
22	VDDIO	Power Supply(3)	IO Supply Voltage for inputs D[0:7], HS, VS, and DCLK, (1.8 V up to 3.3 V)
23	VDDD		Digital supply voltage (1.8 V only)
17	GNDD		Supply Ground for VDDIO and VDDD
9	VDDA		PLL and SubLVDS I/O supply voltage (1.8 V only)
6	GNDA		PLL and SubLVDS Ground

(2) These inputs can tolerate an input voltage up to 3.6 V while the actual input threshold from logic low to logic high is at 0.9 V nominal; This allows driving these inputs from a 1.8 V or 3.3 V GPIO independent of the camera supply voltage.
(3) In a multilayer PCB, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Supply voltage range(2)	V_{DDIO}	–0.3	4	V
	V_{DDD}, V_{DDA}	–0.3	2.175	V
Voltage range at any output terminal		–0.5	2.175	V
Voltage range at any input terminal		–0.5	V_{DDIO} + 0.5	V
Continuous power dissipation		See *Thermal Information*		

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute maximum- rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND pins.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model(1) (All pins)	–3	3	kV
		Charged device model(2) (All pins)	–500	500	V
		Machine model(3) (All pins)	–200	200	

(1) In accordance with JEDEC Standard 22, Test Method A114-A.
(2) In accordance with JEDEC Standard 22, Test Method C101.
(3) In accordance with JEDEC Standard 22, Test Method A115-A

6.3 Recommended Operating Conditions

Unused single-ended inputs must be held high or low to prevent them from floating.

			MIN	NOM	MAX	UNIT
V_{DDIO} V_{DDD} V_{DDA}	Supply voltage		1.65 1.65 1.65	 1.8 1.8	3.6 1.95 1.95	V
$V_{DDn(PP)}$	Supply voltage noise magnitude	$f(V_{DDn(PP)})$ = 1 Hz to 2 GHz (test set-up see Figure 13)			100	mV
f_{DCLK}	Data clock frequency	FSEL = 0, See Figure 16, Figure 17, Figure 18	3.5		13	MHz
		FSEL = 1, See Figure 16, Figure 17, Figure 18	7		27	
		Standby mode (1)			500	kHz
$t_H \times f_{DCLK}$	DCLK Input duty cycle		0.35		0.65	
T_A	Operating free-air temperature		–40		85	°C
$t_{jit(per)DCLK}$	DCLK RMS period jitter (2)	Measured on DCLK input			5	ps-rms
$t_{jit(TJ)DCLK}$	DCLK total jitter (3)				$0.05/f_{DCLK}$	s
$t_{jit(CC)DCLK}$	DCLK peak cycle to cycle jitter (4)				$0.02/f_{DCLK}$	s
Icount	Number of active video lines (5)	MODE = V_{IH}; count the number of HS↓ transitions within one frame	1		2046	
t_{hblank}	Horizontal blanking time		4			UI (1/DCLK)
t_{vblank}	Vertical blanking time		8			UI (1/DCLK)
DCLK, D[0:1], VS, HS						
V_{IH}	High-level input voltage	See Figure 7	$0.7\times V_{DDIO}$		V_{DDIO}	V
V_{IL}	Low-level input voltage	See Figure 7	0		$0.3\times V_{DDIO}$	V
t_{DS}	Data set up time prior to ↑↓ DCLK	See Figure 8	2.0			ns
t_{DH}	Data hold time after ↑↓ DCLK	See Figure 8	2.0			ns
MODE, TXEN						
V_{IH}	High-level input voltage	See Figure 7	$0.7\times V_{DDA}$		3.6	V
V_{IL}	Low-level input voltage	See Figure 7	0		$0.3\times V_{DDA}$	V
FSEL						
V_{IH}	High-level input voltage	See Figure 7	$0.7\times V_{DDD}$		3.6	V
V_{IL}	Low-level input voltage	See Figure 7	0		$0.3\times V_{DDD}$	V

(1) DCLK input frequencies lower than 500 kHz will force the SN65LVDS315 into standby mode. Input frequencies between 500 kHz and 3 MHz might activate the SN65LVDS315. Input frequencies beyond 3MHz will activate the SN65LVDS315.
(2) Period jitter is the deviation in cycle time of a signal with respect to the ideal period over a random sample of 100,000 cycles.
(3) Total jitter reflects the maximum jitter amplitude observed over a time period of 10^{12} data bits. It is often derived by adding all deterministic jitter components (ps peak-to-peak values) and the geometric sum of all random components (ps-rms values × 14.069 for 10–12 bit error rate)
(4) Cycle-to-cycle jitter is the variation in cycle time of a signal between adjacent cycles over a random sample of 1,000 adjacent cycle pairs.
(5) For a VGA resolution of 640x480, Icount would be 480

6.4 Thermal Information

THERMAL METRIC (1)		SN65LVDS315 RGE 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	16.1	
ψ_{JT}	Junction-to-top characterization parameter	0.9	
ψ_{JB}	Junction-to-board characterization parameter	16.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Device Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{DD}	Supply current	V_{DDIO} = V_{DDD} = V_{DDA}, $R_{L(CLK)}$ = $R_{L(D0)}$ = 100 Ω, V_{IH}=V_{DDIO}, V_{IL}=0V, TXEN and MODE at V_{DDD}, typical blanking power test pattern. See Table 1	FSEL = V_{IL}, f_{DCLK} = 3.5 MHz		4.8		mA
			FSEL = V_{IL}, f_{DCLK} = 11 MHz		7.6		
			FSEL = V_{IH}, f_{DCLK} = 11 MHz		5.9		
			FSEL = V_{IH}, f_{DCLK} = 26 MHz		9.6		
		V_{DDIO} = V_{DDD} = V_{DDA}, $R_{L(CLK)}$ = $R_{L(D0)}$ = 100 Ω, V_{IH}=V_{DDIO}, V_{IL}=0V, TXEN and MODE at V_{DDD}, Alternating (worst-case) 1010 serial bit pattern. See Table 2	FSEL = V_{IL}, f_{DCLK} = 3.5 MHz		5.7	8.1	
			FSEL = V_{IL}, f_{DCLK} = 11 MHz		8.9	11.2	
			FSEL = V_{IH}, f_{DCLK} = 11 MHz		7.2	9.5	
			FSEL = V_{IH}, f_{DCLK} = 26 MHz		11.3	13.3	
		Standby mode (TXEN at V_{DD})	V_{DDIO} = V_{DDD} = V_{DDA}, $R_{L(CLK)}$ = $R_{L(D0)}$ = 100 Ω, V_{IH}=V_{DDIO}, V_{IL}=0 V, TXEN and MODE at V_{DDD}, All inputs held static high (V_{IH}) or static low (V_{IL})		0.2	10	µA
		Shutdown mode (TXEN at GND)			0.2	10	
		Standby mode (TXEN at V_{DD})	V_{DDIO} = V_{DDD} = V_{DDA}, $R_{L(CLK)}$ = $R_{L(D0)}$ = 100 Ω, V_{IH}=V_{DDIO}, V_{IL}=0 V, TXEN and Mode = V_{IL}; D[7:0] VS, HS, and DCLK left open		0.02	10	
		Shutdown mode (TXEN at GND)			0.03	5	
P_D	Device power dissipation	V_{DDx} = 1.8 V, T_A = 25°C	f_{DCLK} = 3.5 MHz			10.8	mW
			f_{DCLK} = 11 MHz			17.7	
			f_{DCLK} = 26 MHz			21.2	
		V_{DDx} = 1.95 V, T_A = –40°C	f_{DCLK} = 3.5 MHz			15.7	
			f_{DCLK} = 26 MHz			26.0	

(1) All typical values are at 25°C and with 1.8 V supply unless otherwise noted.

6.6 Output Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
subLVDS OUTPUTS (DOUT+, DOUT–, CLK+, and CLK–)						
$V_{OCM}(SS)$	Steady-state common-mode output voltage	See Figure 7, Output load see Figure 11	0.8	0.925	1.0	V
$\|V_{OD}\|$	Differential output voltage magnitude $\|V_{DOUT+} - V_{DOUT-}\|$, $\|V_{CLK+} - V_{CLK-}\|$		100	170	250	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage between logic states		–10		10	mV
ZOD	Differential small-signal output impedance	TXEN at VDD	5			kΩ
I_{OSD}	Differential short-circuit output current	V_{OD} = 0 V; f_{DCLK} = 26 MHz		1	10	mA
I_{OZ}	High-impedance state output current	V_O = 0 V or V_{DD}(max), TXEN at GND	–3		3	µA

(1) All typical values are at 25°C and with 1.8V supply unless otherwise noted.

6.7 Input Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Dx, VS, HS, DCLK						
$I_{IL(hold)}$	Bus hold input current(2)	V_{DDIO} = 1.65 V and V_{DDIO} = 3.6 V	15		100	µA
$I_{IH(hold)}$	Bus hold input current(3)	V_{DDIO} = 1.65 V and V_{DDIO} = 3.6 V	–15		–100	µA
C_{IN}	Input capacitance			1.5		pF
MODE, TXEN, FSEL						
I_{IL}	High-level input current	V_{IH} = 0.7 V_{DDD}, See Figure 7	–200	–0.7	200	nA
I_{IH}	Low-level input current	V_{IL} = 0.3 V_{DDD}, See Figure 7	–200	0.5	200	nA
C_{IN}	Input capacitance	V_I = TBD		1.5		pF

(1) All typical values are at 25°C and with 1.8 V supply unless otherwise noted.
(2) $I_{IL(hold)}$ is the input current the bus-hold input stage is able to source to maintain a low logic level; The bus-hold current becomes minimal as the input approaches GND. $I_{IL(hold)}$ is the least amount of current a camera output must source to overcome the bus hold and force a high signal.
(3) $I_{IH(hold)}$ is the input current the bus-hold input stage is able to source to maintain a high logic level. The bus-hold current becomes minimal as the input approaches V_{DDIO}. $I_{IL(hold)}$ is the least amount of current a camera output must be able source to overcome the bus hold and switch to a low signal.

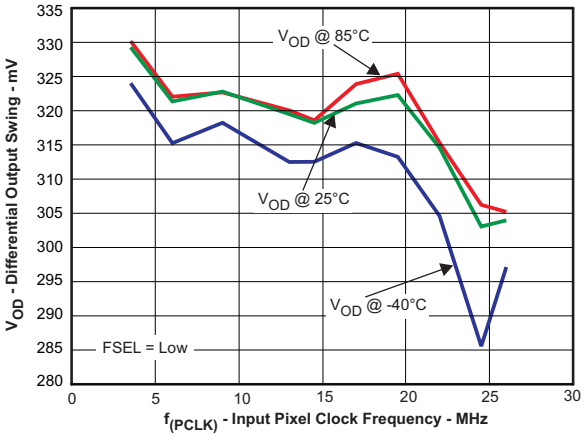
6.8 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_r	20%-to-80% differential output signal rise time	f_{DCLK}=3.5 MHz, See Figure 10 and Figure 11		360	460	730	ps
t_f	20%-to-80% differential output signal fall time	f_{DCLK}=3.5 MHz, See Figure 10 and Figure 11		360	460	730	ps
$t_{s(DOUT)}$	Setup time DOUT valid before CLK+ rising edge	See Figure 9	FSEL = 0, f_{DCLK} = 13 MHz FSEL = 1, f_{DCLK} = 26 MHz	3.327 1.163	4.2 1.8		ns
$t_{h(DOUT)}$	Hold time DOUT valid before CLK+ ringing edge		FSEL = 0, f_{DCLK} = 13 MHz FSEL = 1, f_{DCLK} = 26 MHz	4.627 2.463	5.4 3.0		ns
$t_{pd(L)}$	Propagation delay time, input to serial output (data latency)	TXEN at V_{DDD}, V_{IH} = V_{DDD}, V_{IL}=GND, R_L = 100 Ω, See Figure 12		4.5/f_{DCLK}	4.7/f_{DCLK}	5.5/f_{DCLK}	
t_H x f_{CLKO}	Output CLK duty cycle			0.45	0.50	0.55	
t_{GS}	TXEN glitch suppression pulse width(2)	V_{IH} = V_{DDD}, V_{IL}=GND, TXEN toggles between V_{IL} and V_{IH}, See Figure 14		3.8		10	µs
t_{pwnup}	Enable time from power down (↑TXEN)	MODE at V_{DD}; time from TXEDN pulled high to CLK and DOUT outputs enabled and transmit valid data; See Figure 14		100	100µs + 2×VS↑		µs
t_{pwrdn}	Disable time from active mode (↓TXEN)	TXEN is pulled low during transmit mode; time measurement until output becomes disabled and PLL is shutdown; See Figure 14				11	µs
t_{wakup}	Enable time from standby (↑↓DCLK)	TXEN and MODE at V_{DD}; device in standby; time measurement from DCLK starts switching to CLK and DOUT enabled and transmit valid data; See Figure 15		100	100µs + 2×VS↑		µs
t_{sleep}	Disable time from standby (DCLK stopping)	TXEN at V_{DD}; device in transmitting; time measurement from DCLK input signal stops starts until CLK + DOUT outputs becomes disabled and PLL is shutdown, See Figure 15			<8/f_{DCLK}	100	µs

(1) All typical values are at 25°C and with 1.8 V supply unless otherwise noted.
(2) The TXEN input incorporates glitch-suppression circuitry to disregard short input pulses. t_{GS} is the duration of either a high-to-low or low-to-high transition that is suppressed.

6.9 Typical Characteristics



FSEL = Low

Figure 1. Differential Output Swing V_{OD} as a Function DCLK Input Frequency vs

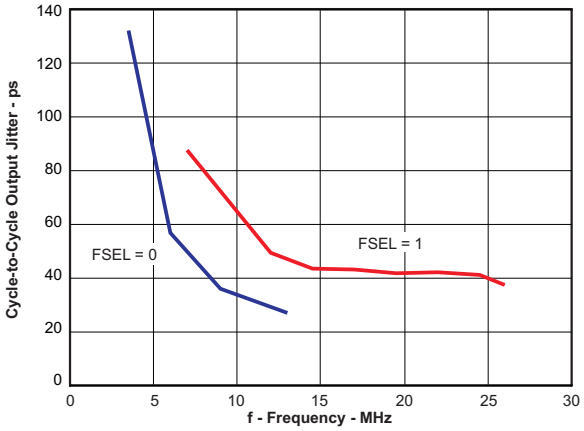


Figure 2. Cycle-to-Cycle Output Jitter

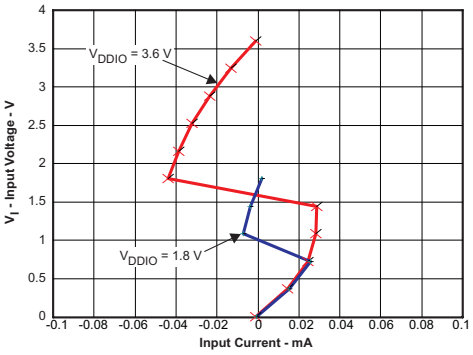


Figure 3. Bus Hold Leakage Current

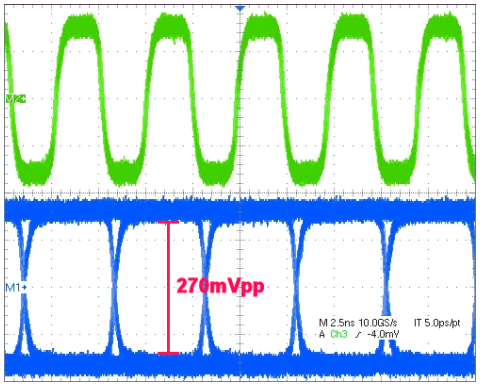
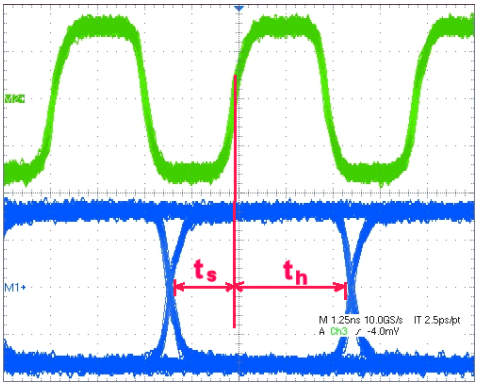
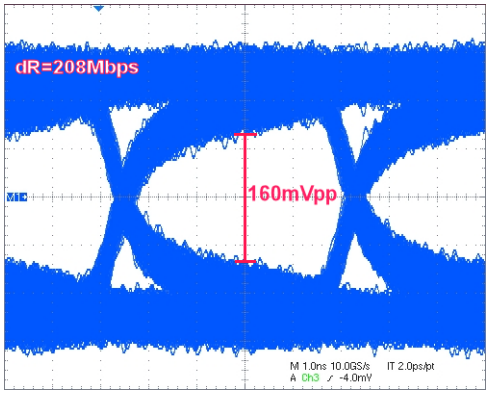


Figure 4. SN65LVDS315 Output Data and Clock Signal at 208 mbps (Maximum Speed)



The asymmetrical setup and hold time is optimized to meet OMAP processor input timing.

Figure 5. SN65LVDS315 Output Data and Clock Signal at 208 mbps



Through pcb interconnect of 80-inch of FR4 at 208Mbps

Figure 6. SN65LVDS315 Output Clock and Data

7 Parameter Measurement Information

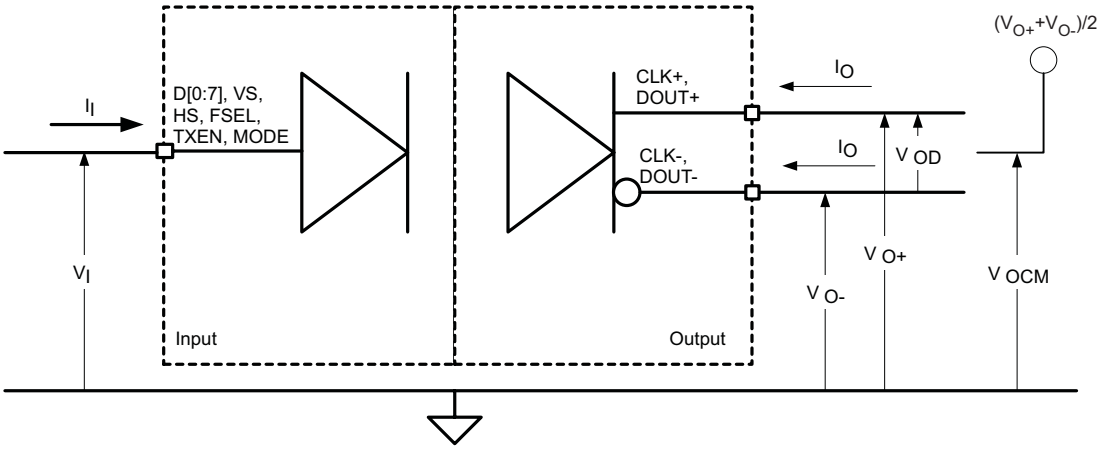


Figure 7. I/O Voltage and Current Definition

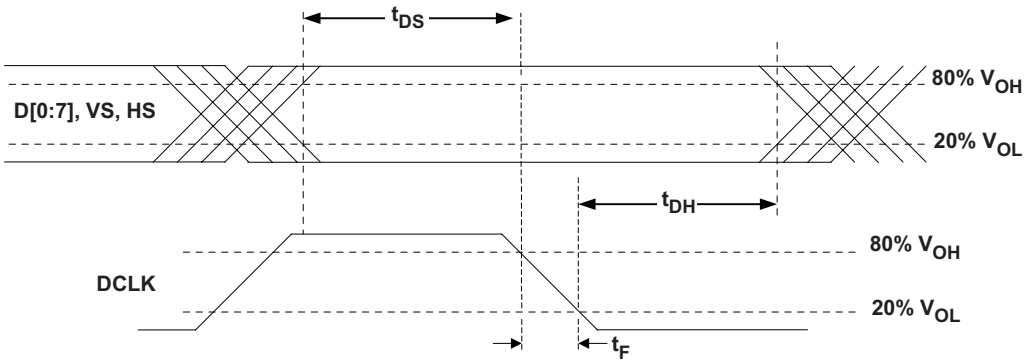


Figure 8. Input Signal Setup and Hold Time Definition T_{DS} And T_{DH}

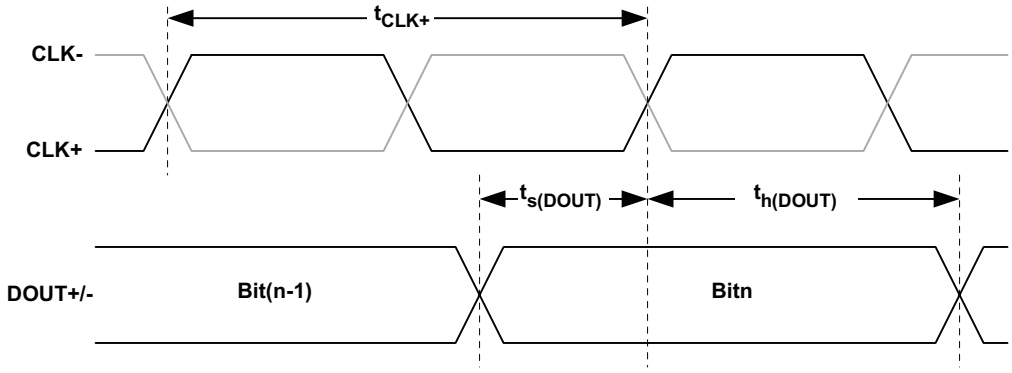


Figure 9. Output Signal Setup and Hold Time Definition $T_{s(DOUT)}$ And $T_{h(DOUT)}$

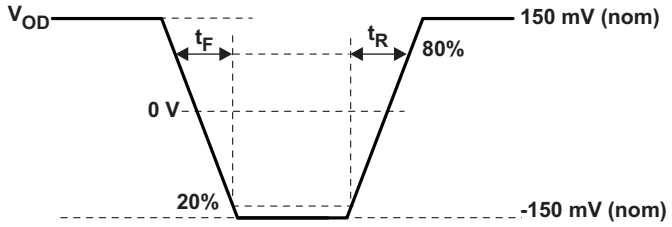
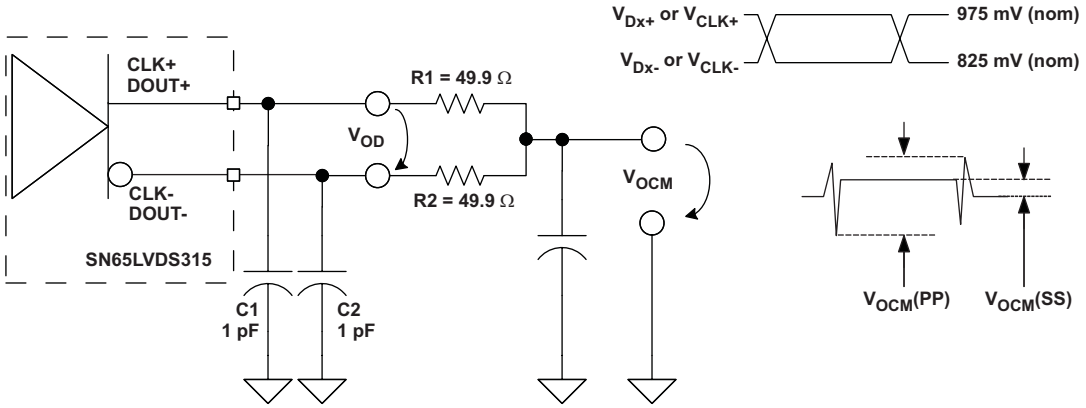


Figure 10. Rise and Fall Time Definition



NOTES:
A. 88 MHz output test pattern on CLK output and 44 MHz output test pattern on DOUT; this is achieved by:
1. MODE = 0
2. f_{PCLK} = 11 MHz
3. Inputs D0 = D2 = D4 = D6 = VDDIO and D1 = D3 = D5 = D7 = GND
4. Toggle VS↑, HS↑, HS↓, VS↓, VS↑, HS↑, HS↓, VS↓, VS↑, HS↑

B. C1 and C2 include instrumentation and Fixture capacitance; +/- 20%
C. R1 and R2 tolerance +/- 1%
D. The measurement of V_{OCM}(PP) and V_{OC}(SS) are taken with test equipment bandwidth > 1 GHz

Figure 11. Driver Output Voltage Test Circuit and Definitions

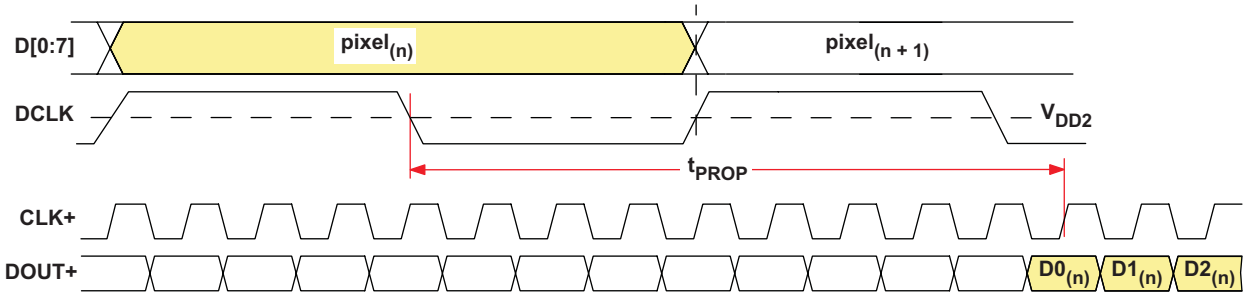


Figure 12. TPD(L) Propagation Delay Input to Output

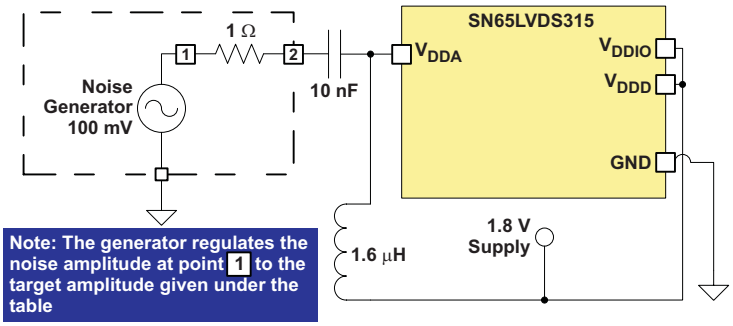


Figure 13. Power Supply Noise Test Set-Up

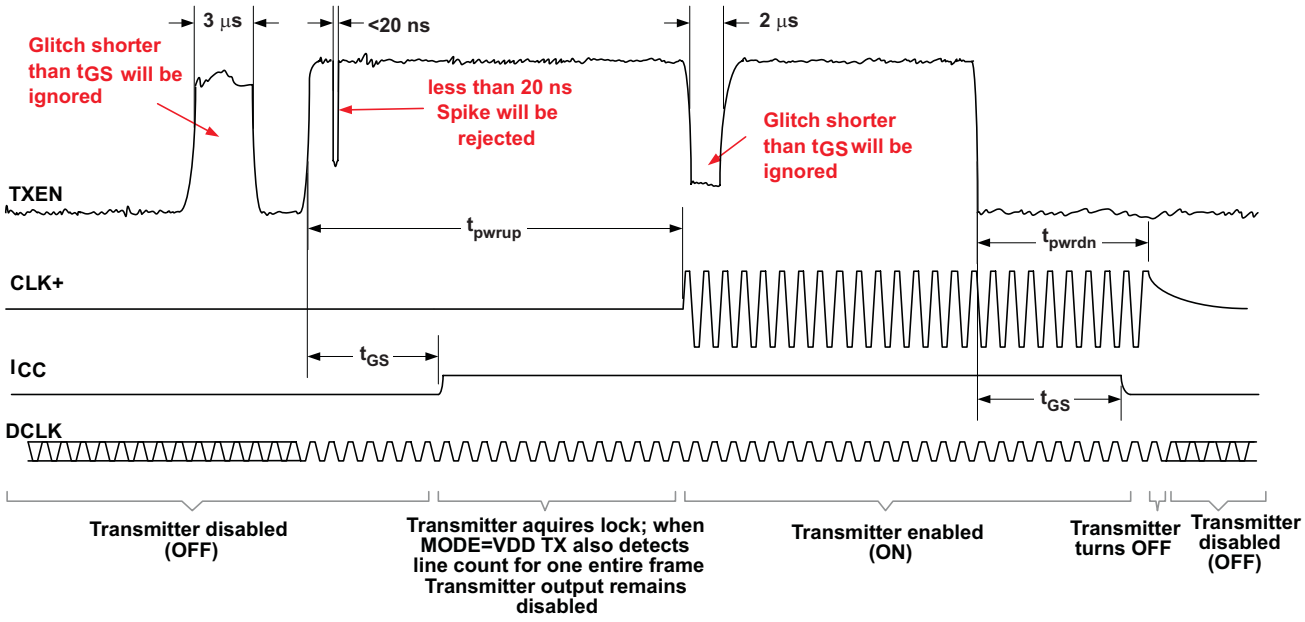


Figure 14. Glitch Suppression Enable/Disable Time

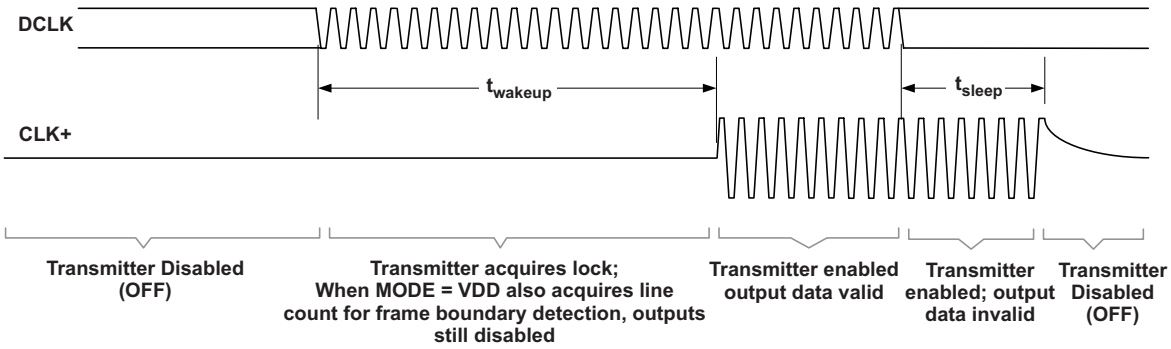


Figure 15. Standby Detection

7.1 Typical Blanking Power Consumption Test Pattern

During blanking VS is low, and the SN65LVDS315 data output DOUT presents a high signal. The typical power consumption test patterns during the blanking time consists of one data word. The pattern repeats itself throughout the entire measurement.

Table 1. Typical IC Power Consumption Test During Blanking

WORD	TEST PATTERN		
	D[7:0]	VS	HS
1	0x00	0	x

7.2 Maximum Power Consumption Test Pattern

The maximum (or worst-case) power consumption of the SN65LVDS315 is tested using an alternating 1010 test pattern. The pattern repeats itself throughout the entire measurement.

Table 2. Worst Case IC Power Consumption Test Pattern 1

WORD	TEST PATTERN		
	D[7:0]	VS	HS
1	0x00	1	1
2	0xFF	1	1

7.3 Jitter Performance

The jitter performance of the SN65LVDS315 is tested using a pattern that stresses the interconnect, particularly to test for ISI. The test pattern uses very long run lengths of consecutive bits. The pattern incorporates very high and low data rates, and maximizes switching noise. The pattern is self-repeating for the duration of the test.

Table 3. Jitter Test Pattern

WORD	TEST PATTERN		
	D[7:0]	VS	HS
1	0x00	1	1
2	0x00	1	1
3	0x00	1	1
4	0x01	1	1
5	0x03	1	1
6	0x07	1	1
7	0x18	1	1
8	0xE7	1	1
9	0x35	1	1
10	0x02	1	1
11	0x54	1	1
12	0xA5	1	1
13	0xAD	1	1
14	0x55	1	1
15	0xA6	1	1
16	0xA6	1	1
17	0x55	1	1
18	0x55	1	1
19	0xAA	1	1
20	0x52	1	1
21	0x5A	1	1
22	0xAB	1	1
23	0xFD	1	1
24	0xCA	1	1
25	0x18	1	1
26	0xE7	1	1
27	0xF8	1	1
28	0xFC	1	1
29	0xFE	1	1
30	0xFF	1	1
31	0xFF	1	1
32	0xFF	1	1

8 Detailed Description

8.1 Overview

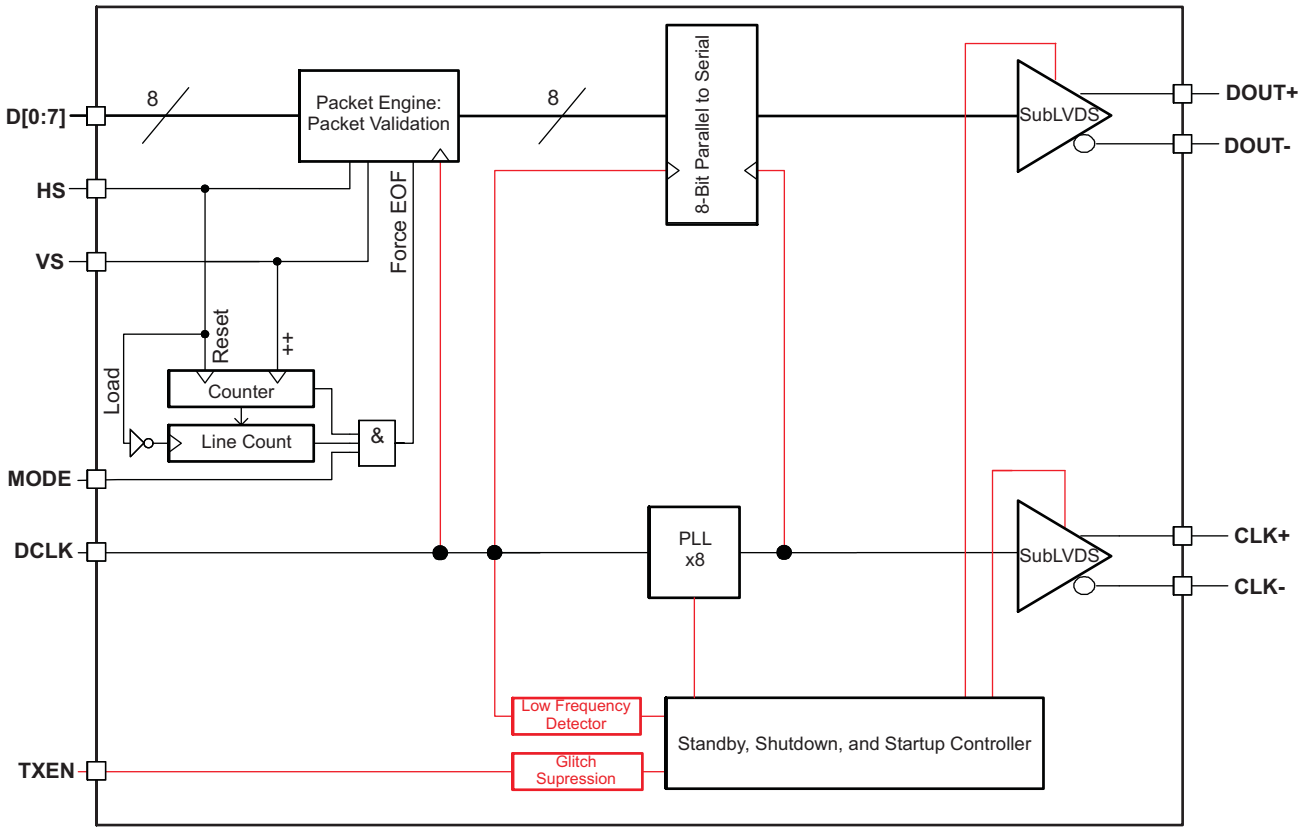
The SN65LVDS315 is a camera serializer that converts 8-bit parallel camera data into MIPI-CSI1 or SMIA CCP compliant serial signals.

The parallel data is latched in with the pixel clock input DCLK on the falling clock edge (D0 :D7), and the control inputs VS and HS are used to determine line and frame synchronization. According the state of HS and VS, the SN65LVDS315 shall generate a synchronization code (Start of frame SOF, End Of Frame EOF, Start Of Line SOL and End Of Line EOL) which will be included into the streaming data. Subsequently The latched data are serialized and transmitted by the SubLVDS driver (could be either input data or synchronization code). And the frequency of the differential output clock is eight times the input pixel clock rate.

The SN65LVDS315 has implemented an extra control for each frame size. If the MODE pin is high, then the device shall generate an EOF synchronization code when the number of transmitted lines belonging to the same frame reach the maximum allowed, in order to avoid a frame overflow.

The SN65LVDS315 supports three power modes (shutdown, standby and active) to conserve power. The TXEN input may be used to put the SN65LVDS315 in a shutdown mode. The SN65LVDS315 enters an active standby mode if the input clock, DCLK, stops. This minimizes power consumption without the need for controlling an external pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Frame Counter Size

The maximum size of *frame_count* is limited to 2046 lines. Transmitting more than 2046 active lines within one frame causes an error if MODE is held high.

Feature Description (continued)

8.3.2 Data Formats

The SN65LVDS315 supports the transfer of following data formats:

Table 4. Supported Data Formats

DATA TYPE	ABBR.	COMMENT
YUV 422 image data	YUV422	D[0:7] inputs are used as data inputs; The host processor must be configured to receive YUV 422 data; the SN65LVDS315 is transparent to these data formats (no special configuration required); The camera sensor must provide a UYVY output data sequence (e.g. U1,Y1,V1,Y2,U2,Y3,V3,Y4,U3,Y5...)
YUV 420 image data	YUV420	D[0:7] inputs are used as data inputs; The host processor must be configured to receive YUV 420 data; the SN65LVDS315 is transparent to these data formats (no special configuration required); The camera sensor must provide an odd/even (or UYY.../ VYY...) output data sequence (e.g. odd like U1,Y1,Y2,U3,Y3,Y4,... followed by an even line V1,Y1,Y2,V3,Y3,Y4,...)
RGB 888 image data	RGB888	D[0:7] inputs are used as data inputs; The host processor must be configured to receive RGB888 data; the SN65LVDS315 is transparent to these data formats (no special configuration required); The camera sensor must provide an output data sequence of B1,G1,R1,B2,G2,R2,...
RGB 565 image data	RGB565	This data format can only be supported if the camera sensor outputs a 16-bit data format (two output bytes of 8-bit each) with the following format: First byte: B[0:4] and G[0:2] (G2 is MSB on device input D7) Second byte: G[3:5] and R[0:4] (R4 is MSB on device input D7)
Raw bayer, 8-bit image data	RAW8	D[0:7] inputs are used as data inputs; The host processor must be configured to receive RAW8 data; The camera line length should be a multiple of 4 pixel; the SN65LVDS315 is transparent to these data formats (no special configuration required); The camera sensor must provide an output data sequence of P1,P2,P3,P4,,...

Following data formats are not supported by the SN65LVDS315:

- RGB 444 image data
- Raw Bayer 6-bit image data
- Raw Bayer 7-bit image data
- Raw Bayer 10-bit image data
- Raw Bayer 12-bit image data
- JPEG 8-bit data

8.3.3 Parallel Input Port Timing Information

The parallel input data must comply with the following signal timing:

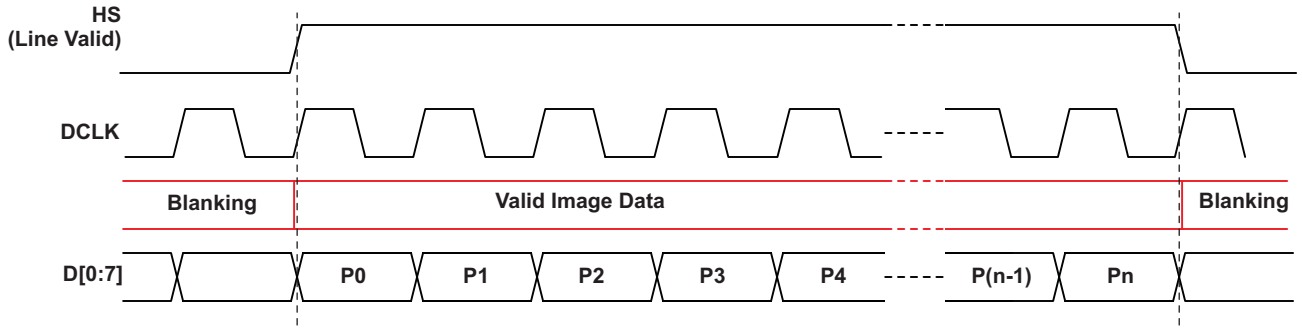
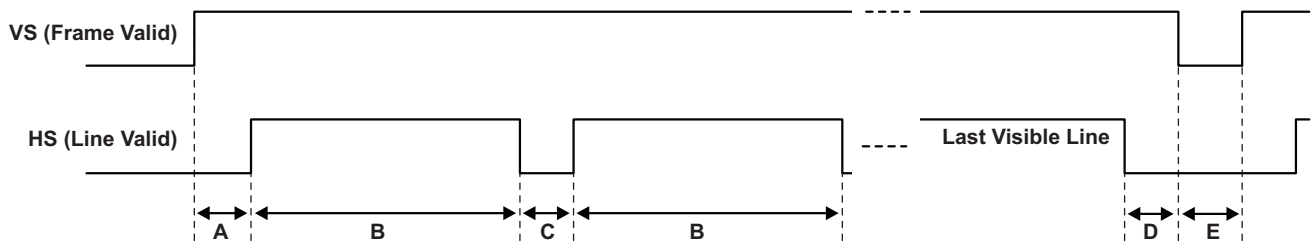


Figure 16. Parallel Input Timing Diagram

The relationship between frame sync and line sync shall be the following:



A - Time between VS and HS rising edge:	$0 \le t_A$
B - Number of pixel in active line:	$0 \le t_B$
C - Horizonal line blanking:	$8x1/f_{DCLK} \le t_C$
D - Time between VS and HS falling edge:	$0 \le t_D$
E - Time between VS falling and VS rising edge:	if MODE = high or $t_D = 0$: $8x1/f_{DCLK} \le t_E$
	if MODE = low or $t_D > 0$: $12x1/f_{DCLK} \le t_E$

Figure 17. VS and HS Timing Diagram

8.3.4 MIPI CSI-1 / CCP2-Class 0 Interface

When MODE is held low, the SN65LVDS315 provides a MIPI CSI-1 compliant serial output. The output data on DOUT is set on each falling edge of the differential clock signal, CLK. The CSI-1/CCP2 receiver should latch the data in on the rising CLK edge. The clock signal is free running (and not gated as optional in the CCP2 spec). The data format is bytewise (8-bit boundary) with the least significant bit (LSB) sent first. When nothing is being transferred (e.g. during blanking), DOUT remains high, except during power shutdown.

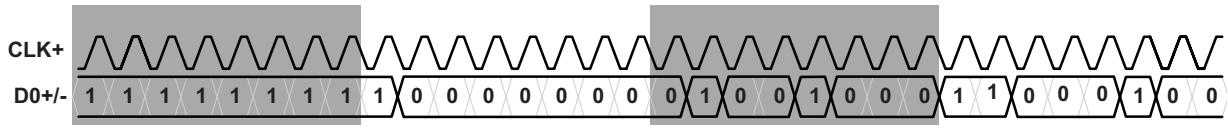


Figure 18. Data and Clock Output in CSI-1/CCP2 Camera Mode Class-0 Transferring a Data Sequence of 0XFF011223H

8.3.5 Frame Structure and Synchronization Codes

Camera images are transferred in frames. Each frame contains one camera image. Each frame consists of a number of lines. A frame is always larger than the number of visible lines. The non-visible lines within a frame are called frame blanking. Frame blanking must be signaled on the SN65LVDS315 parallel input via a low VS signal. Each line within a frame has an invisible area as well — this area is called line blanking, and is indicated with a low HS signal. The CSI-1/CCP2-compliant output only transmits visible pixels within each frame. During line and frame blanking (also called horizontal and vertical blanking), the data output is set high. To indicate the line start, line end, frame start, and frame end, the SN65LVDS315 transmits synchronization codes.

Four synchronization codes are generated and embedded in the serial bit-stream:

Start Of Line Code	SOL=0xFF00:0000	This code identifies the start of a new line SOL; It is received for every line, except for the first line, which starts with a FSC
End Of Line Code	EOL=0xFF00:0001	This code identifies the end of a line EOL; It is received for every line, except for the last line, which ends with a FEC
Start of Frame Code	SOF=0xFF00:0002	This code identifies the start of a new frame SOF
End of Frame Code	EOF=0xFF00:0003	This code identifies the end of the last line and the end of the current frame EOF

Every synchronization code is transmitted byte-wise least significant bit (LSB) first. For example, the code 0xFF00:0002 transmitted from the image sensor corresponds to the following bit stream: 11111111 – 00000000 – 00000000 – 01000000.

Every default code starts with a set of eight 1s and sixteen 0s that are never received in pixel data (as having eight 1s and sixteen 0s is not allowed in pixel data).

8.3.6 Preventing Wrong Synchronization

To avoid actual pixel data from being erroneously interpreted as a control command, the SN65LVDS315 incorporates bit manipulation. If the SN65LVDS315 parallel input detects a bit sequence of eight 1s followed by sixteen 0s, it replaces the LSB of the 0x00 parallel input word with a one instead of a zero (so the actual pixel value will be adjusted from 0x00 to 0x01). Here are a few examples:

input code on DIN: 0xFF.00.00 — serial output sequence on D0: 0xFF.00.01

input code on DIN: 0xFE.01.00.00 — serial output sequence on D0: 0xFE.01.01.00

D[7:0] parallel input Code				**serial output code before correction**			
Byte 1	**Byte 2**	**Byte 3**	**Byte 4**				
MSB—LSB	**MSB—LSB**	**MSB—LSB**	**MSB—LSB**	**---time----------→**			
11111111	00000000	00000000	**xxxxxxxx**	11111111	00000000	00000000	xxxxxxxx
1111111**x**	00000001	00000000	**xxxxxxx**0	x1111111	10000000	00000000	0xxxxxxx
111111**xx**	00000011	00000000	**xxxxxx**00	xx111111	11000000	00000000	00xxxxxx
11111**xxx**	00000111	00000000	**xxxxx**000	xxx11111	11100000	00000000	000xxxxx
1111**xxxx**	00001111	00000000	**xxxx**0000	xxxx1111	11110000	00000000	0000xxxx
111**xxxxx**	00011111	00000000	**xxx**00000	xxxxx111	11111000	00000000	00000xxx
11**xxxxxx**	00111111	00000000	**xx**000000	xxxxxx11	11111100	00000000	000000xx
1**xxxxxxx**	01111111	00000000	**x**0000000	xxxxxxx1	11111110	00000000	0000000x
↓↓				↓↓			
D[7:0] parallel input Code (corrected)				serial output code **after** correction			
Byte 1	Byte 2	Byte 3	Byte 4				
MSB—LSB	MSB—LSB	MSB—LSB	MSB—LSB	---time----------→			
11111111	00000000	0000000**1**	**xxxxxxxx**	11111111	00000000	1**0000000**	xxxxxxxx
1111111 **x**	00000001	0000000**1**	**xxxxxxx**0	x1111111	10000000	1**0000000**	0xxxxxxx
111111**xx**	00000011	0000000**1**	**xxxxxx**00	xx111111	11000000	1**0000000**	00xxxxxx
11111**xxx**	00000111	0000000**1**	**xxxxx**000	xxx11111	11100000	1**0000000**	000xxxxx
1111**xxxx**	00001111	0000000**1**	**xxxx**0000	xxxx1111	11110000	1**0000000**	0000xxxx
111**xxxxx**	00011111	0000000**1**	**xxx**00000	xxxxx111	11111000	1**0000000**	00000xxx
11**xxxxxx**	00111111	0000000**1**	**xx**000000	xxxxxx11	11111100	1**0000000**	000000xx
1**xxxxxxx**	01111111	0000000**1**	**x**0000000	xxxxxxx1	11111110	1**0000000**	0000000x

8.3.7 Frame Structure

The next two graphs show the construction and transmission of a frame:

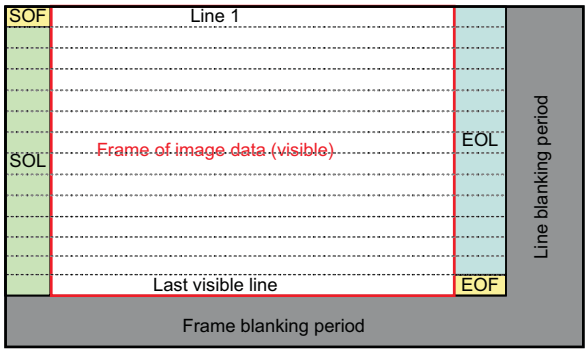


Figure 19. Frame Structure

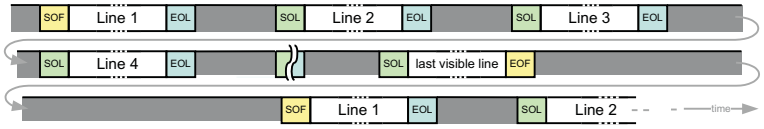


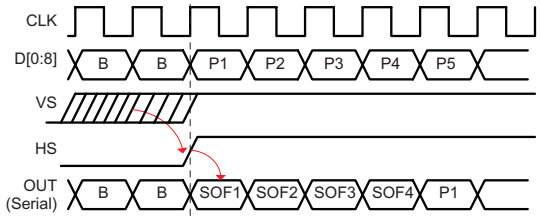
Figure 20. Data and Clock Output in CSI-1 / CCP2 Camera Mode Class-0 Transferring a Data Sequence of 0XFF011223H

8.3.8 VS and HS Timing to Generate the Correct Control Signals

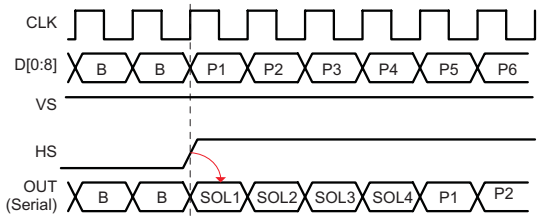
The VS and HS timing received from camera sensors varies. The SN65LVDS315 responds in the following way:

Frame Start and Line Start

Frame start is indicated by a VS transition from low to high. The rising edge on HS following the VS high transition or occurring simultaneously with VS indicates the first valid data line and initiates the transmission of SOF.

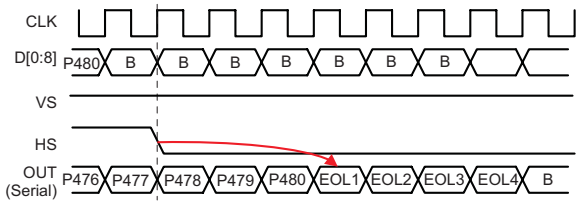


Any additional rising edge on HS initiates transmission of SOL until VS is de-asserted to low.

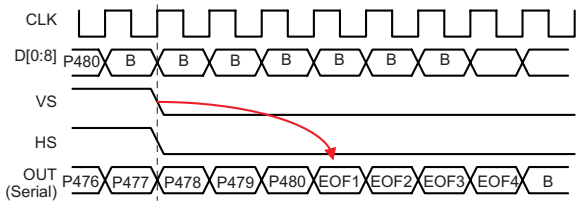


Line End and Frame End

A falling edge of HS indicates the end of a valid line, causing the SN65LVDS315 to transmit the EOL data word.



If HS and VS are set low with the same DCLK cycle, the device will transmit EOF instead of EOL.



Ideally, the VS and HS falling edge occur during the same clock period. In such case, the MODE input can be kept low (MODE=0), and the response of the SN65LVDS315 output to the parallel input data looks like the following:

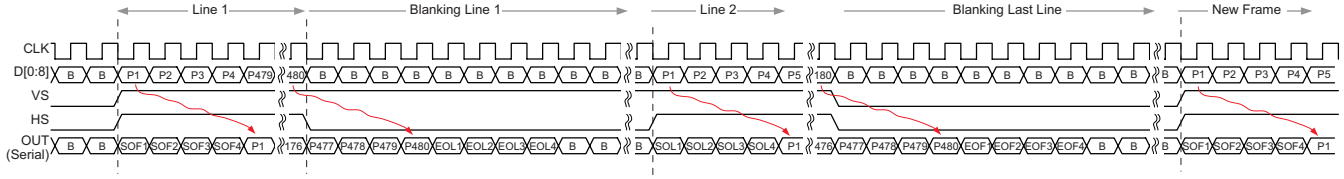
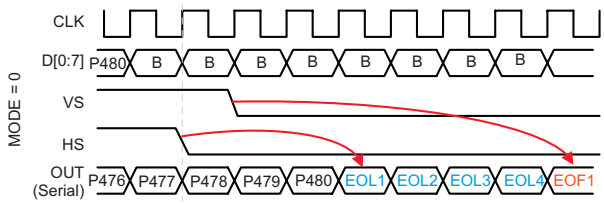
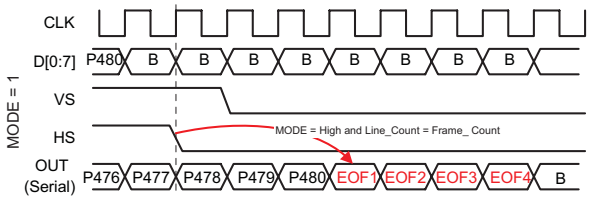


Figure 21. VS and HS Timing

Caution: Some camera sensors generate a frame sync (VS) signal that lasts longer than the HS of the last visible line. In such case, and with **MODE = low**, the SN65LVDS315 transmits EOL during the last HS low transition and transmits EOF when VS transitions low. If the CSI-1 receiver can tolerate receiving EOL followed by EOF, it is recommended to keep the MODE input pin set to low.



If the CSI-1 receiver cannot tolerate reception of an EOL packet followed by an EOF packet, the SN65LVDS315 can also be configured in a mode that allows it to predict the number of visible lines and generate an EOF packet at the proper time. A high level on the the **MODE input** enables a line counter within the SN65LVDS315 that counts every HS rising edge while VS is high. The OMAP processors require the MODE signal to be set high.



The counter value is stored into register *frame_count* when VS transitions low and the counter is reset to zero. When the counter reaches the value stored in *frame_count*, an EOF packet is transmitted instead of the EOL packet. As long as the active number of lines remains constant, this implementation ensures proper transmission of EOF.

If, however, the camera sensor changes the number of transmitted lines during active transmission, the EOF will not be generated properly for that particular frame.

If the number of lines transmitted by the camera sensor increases, an EOF will be sent too early. All active lines following EOF are then ignored during this particular frame. Blanking will be signaled instead. The *frame_count* register will be updated at the end of the frame in order to properly transmit the next frame.

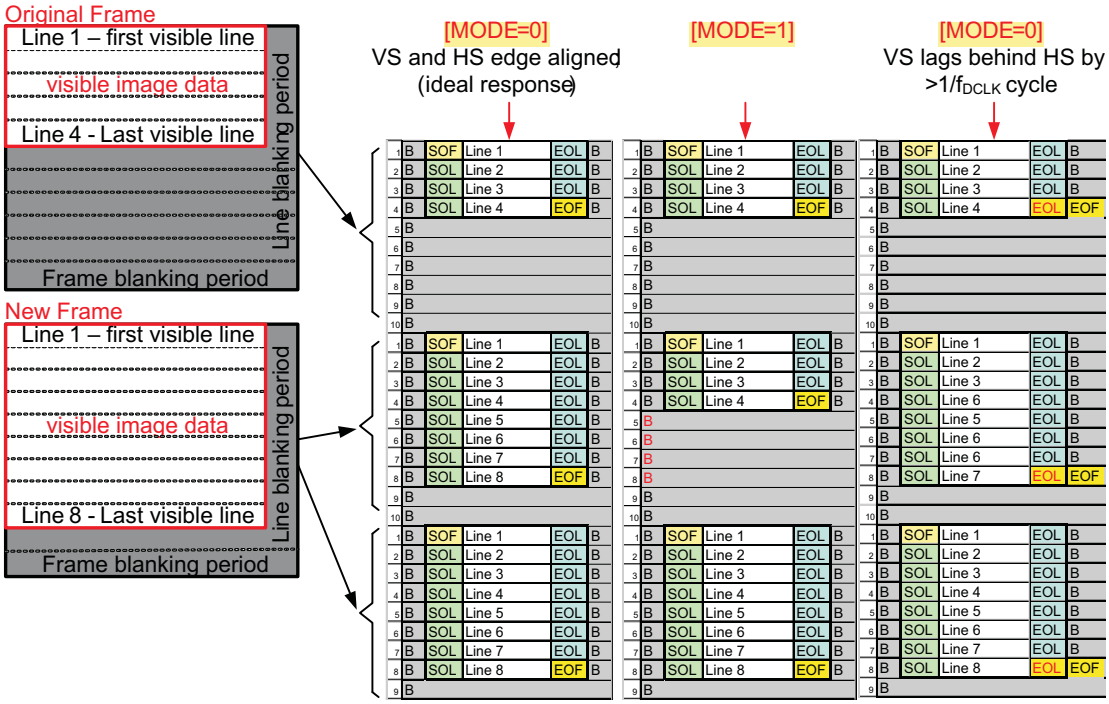


Figure 22. MODE Implementation Example 1

If the number of lines transmitted by the camera sensor decreases, EOL will be sent improperly after the last camera line. When VS is detected low, the EOF command will follow.

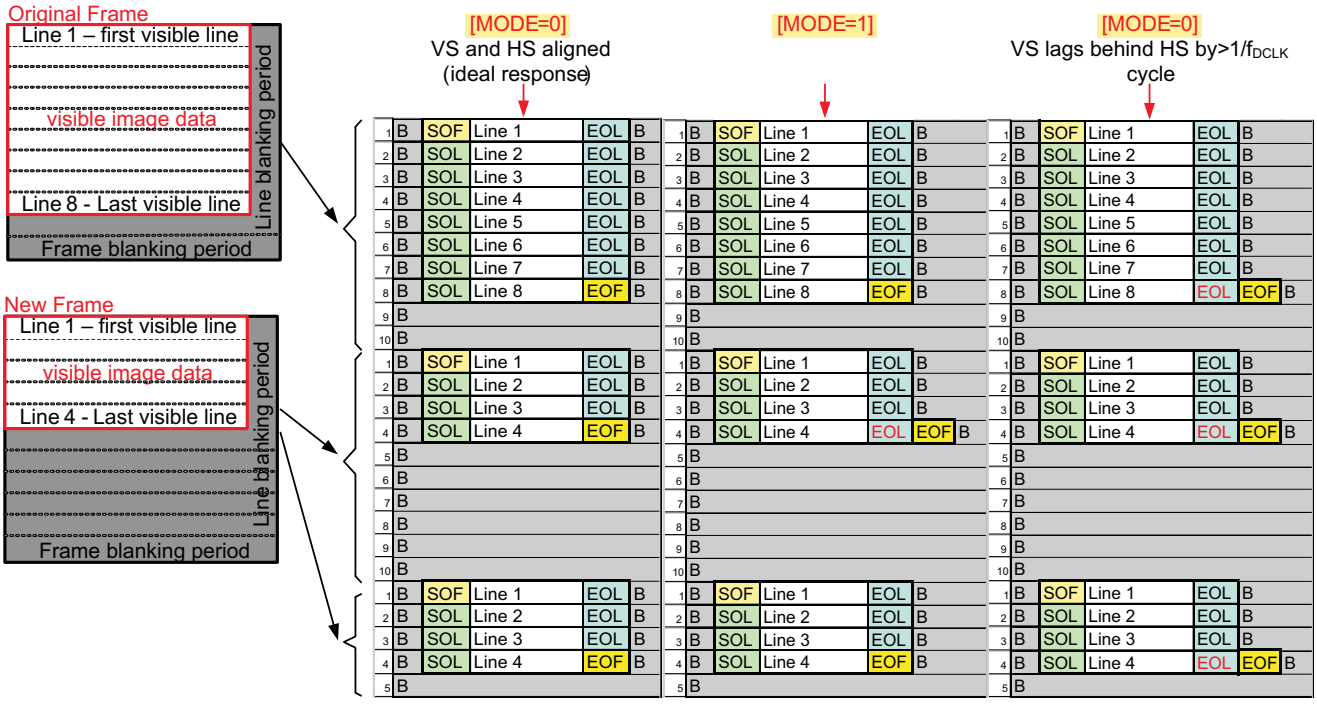


Figure 23. MODE Implementation Example 2

8.4 Device Functional Modes

8.4.1 Powerdown Modes

The SN65LVDS315 transmitter has two power-down modes to facilitate efficient power management.

8.4.1.1 Shutdown Mode

The SN65LVDS315 enters shutdown mode when the TXEN terminal is asserted low. This turns off all transmitter circuitry, including the CMOS input, PLL, serializer, and SubLVDS transmitter output stage. All outputs are high impedance. Current consumption in shutdown mode is nearly zero.

8.4.1.2 Standby Mode

The SN65LVDS315 enters the standby mode if TXEN is high and the DCLK input signal frequency is less than 500 kHz. All circuitry except the DCLK input monitor is shut down, and all outputs enter the high-impedance state. The current consumption in standby mode is low. When the DCLK input signal is completely stopped, the IDD current consumption is minimized.

NOTE

Leaving the TXEN, FSEL or MODE input floating (left open) allows leakage currents to flow from V_{DD} to GND. To prevent excessive leakage current, a CMOS gate must be kept at a valid logic level, either high (above V_{IH} min) or low (below V_{IL} min). This can be achieved by applying an external voltage or ground to these inputs. Inputs Dx, VS, HS, and DCLK incorporate bus hold, and can be left floating or tied high or low. Switching inputs also causes increased leakage currents. Only if no input signal is switching will the I_{DD} current be at its minimum.

8.4.2 Active Modes

When TXEN is high and the DCLK input clock frequency is higher than 3 MHz, the SN65LVDS315 enters the active mode. Current consumption in the active mode depends on operating frequency and the number of data transitions in the data payload.

8.4.2.1 Acquire Mode (PLL Approaches Lock)

The PLL is enabled and attempts to lock to the input clock. All outputs remain in the high-impedance state. First, the PLL monitor waits until it detects stable PLL operation. If MODE is set low, the digital core will wait for one VS low-to-high transition (new frame start) before the device switches from the acquire mode to the transmit mode. This ensures that the outputs turn on when a new image frame is transmitted by the camera sensor. If MODE is set high, the digital core will wait for two (instead of one) VS low-to-high transitions before the device switches from the acquire mode to the transmit mode. This not only ensures that the device waits for a new camera frame, but also allows the internal SN65LVDS315 counter to be initiated with the proper line count. For proper device operation, the pixel-clock frequency (f_{DCLK}) must fall within the valid f_{DCLK} range specified under recommended operating conditions. If the pixel clock frequency is higher than 3 MHz but lower than f_{DCLK}(min), the SN65LVDS315 PLL is enabled. Under such conditions, it is possible for the PLL to lock temporarily to the pixel clock, causing the PLL monitor to release the device into transmit mode. If this happens, the PLL may or may not be properly locked to the pixel clock input, potentially causing data errors, frequency oscillation, and PLL deadlock (loss of VCO oscillation).

8.4.2.2 Transmit Mode

After the PLL achieves lock, the device enters the normal transmit mode. The CLK and DOUT terminals output CSI-1 compliant serial data.

8.4.3 Status Detect and Operating Modes Flow Diagram

The SN65LVDS315 switches between the power saving and active modes in the following way:

Device Functional Modes (continued)

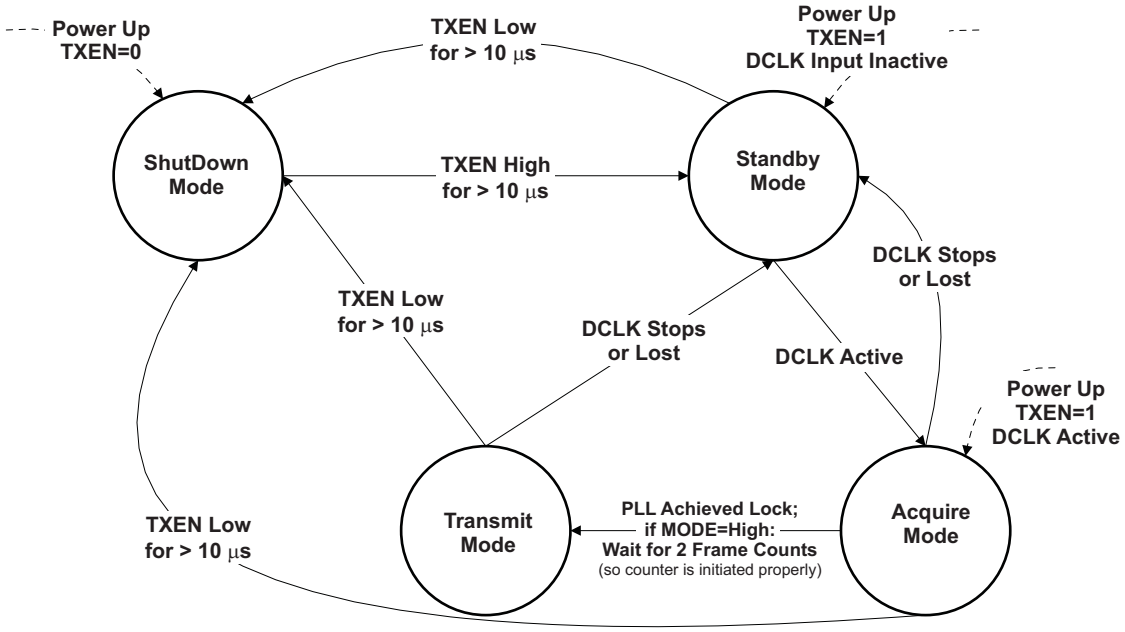


Figure 24. Status Detect and Operating Modes Flow Diagram

Table 5. Status Detect and Operating Modes Descriptions

MODE	CHARACTERISTICS	CONDITIONS
Shutdown Mode	Least amount of power consumption (most circuitry turned off); All outputs high impedance.	TXEN is low for longer than 10 µs (1) (2)
Standby Mode	Low power consumption (only clock activity circuit active; PLL is disabled to conserve power); all outputs are high impedance.	TXEN is high for longer than 10 µs; DCLK input signal is missing or inactive. (2)
Acquire Mode	PLL tries to achieve lock; if MODE is high, initiate line counter (to place EOF at proper position); All outputs are high impedance.	TXEN is high; DCLK input monitor detected input activity.
Transmit Mode	Data transfer (normal operation); transmitter serializes data and transmits data on serial output.	TXEN is high and PLL is locked to the incoming clock.

(1) In Shutdown Mode, all SN65LVDS315 internal switching circuits (e.g., PLL, serializer, etc.) are turned off to minimize power consumption. The input stage of any input pin remains active.
(2) Leaving inputs unconnected can cause random noise to toggle the input stage and potentially harm the device. All CMOS inputs without an internal bus hold (e.g. FSEL, TXEN, MODE) must be tied to a valid logic level during shutdown or standby Mode.

Table 6. Mode Transition Use Cases

MODE TRANSITION	USE CASE	TRANSITION SPECIFICS
Shutdown -> Standby	Set TXEN high to enable transmitter	1. TXEN high > 10 µs 2. Transmitter enters Standby mode a. All outputs are in high-impedance state. b. Transmitter turns on clock input monitor
Standby-> Acquire	DCLK input activity detected	1. DCLK input monitor detects clock input activity; 2. Outputs remain in high-impedance state. 3. PLL circuit is enabled

Table 6. Mode Transition Use Cases (continued)

MODE TRANSITION	USE CASE	TRANSITION SPECIFICS
Acquire -> Transmit	Device is ready to transfer data	1. PLL is active and approaches lock 2. PLL achieves lock within t_{wakeup} 3. Parallel data input latches into shift register. 4. Data input patterns are monitored and the line counter is initialized 5. CLK output turns on 6. DOUT turns on and sends out first serial data bit.
Transmit -> Standby	Request transmitter to enter standby mode by stopping DCLK	1. DCLK Input monitor detects missing DCLK. 2. Transmitter indicates standby, putting all outputs into high-impedance state. 3. PLL shuts down. 4. DCLK activity input monitor remains active.
Transmit/Standby -> Shutdown	Turn off transmitter by pulling TXEN low	1. TXEN pulled low for > t_{pwrdn}. 2. Transmitter indicates standby by switching output CLK+ and CLK– into high-impedance state. 3. Transmitter drives DOUT into high-impedance state. 4. Most IC circuitry is shut down for least power consumption.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The typical application for the SN65LVDS315 is the video streaming, where the device communicates the image sensor and the video processor, the SN65LVDS315 takes the video data from the image sensor in parallel format, then it serializes and sends this information in MIPI CSI-1.

9.1.1 Receiver Termination Requirement

The SN65LVDS315 outputs two differential lanes that must be specially terminated near the CSI-1 receiver device. As shown in Figure 25, place two resistors and one capacitor in each lane (within ±20% to the values shown). There are two possible implementations, based on whether the termination inside the receiver device can be disabled. If it can be disabled, place the components as close to the receiver as possible. This RC filter is a requirement that adds stability to the common mode voltage.

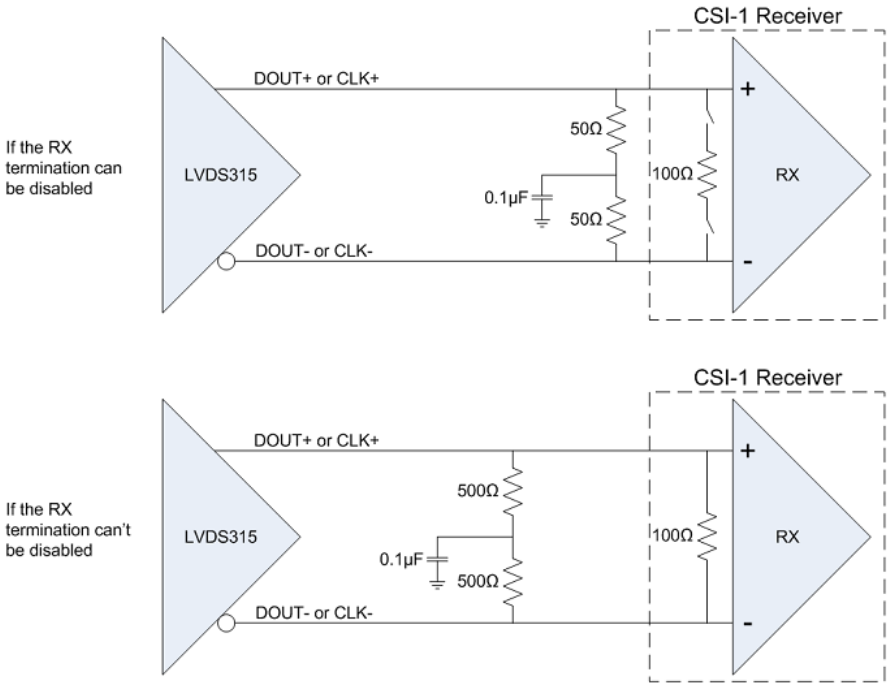


Figure 25. CSI-1 Receiver Device Termination

9.1.2 Preventing Control Inputs From Increased Leakage Currents

To ensure the lowest possible leakage current during standby or power down, all inputs must be held static. Any kind of input switching will cause increased leakage current. Hold inputs TXEN and MODE either at V_{IH} or V_{IL}. The LVDS315 incorporates a bus-hold feature on the D[0:7] inputs, DCLK, VS, and HS. This feature ensures that the input-stage leakage current is minimized during times when the camera output is in a high impedance state. Inputs with the bus-hold feature can be left open without the need of an external pullup or pulldown. This feature minimizes the power consumption of standby and power down modes in particular.

Application Information (continued)

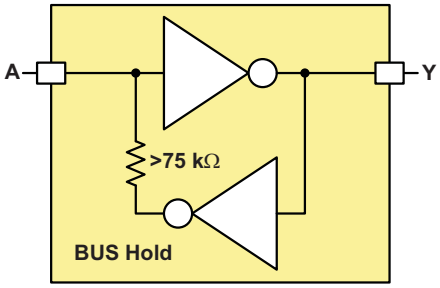


Figure 26. Bus-Hold Circuit

9.2 Typical Application

9.2.1 VGA Camera Application

Figure 27 shows a possible implementation of a 10-Mpixel camera transfer with 30Hz frame refresh rate. The SN65LVDS315 interfaces to the OMAP2420, a TI application processor with integrated CSI receiver. The pixel clock rate is 11 MHz, assuming ≈20% blanking overhead. The application assumes 8-bit color resolution.

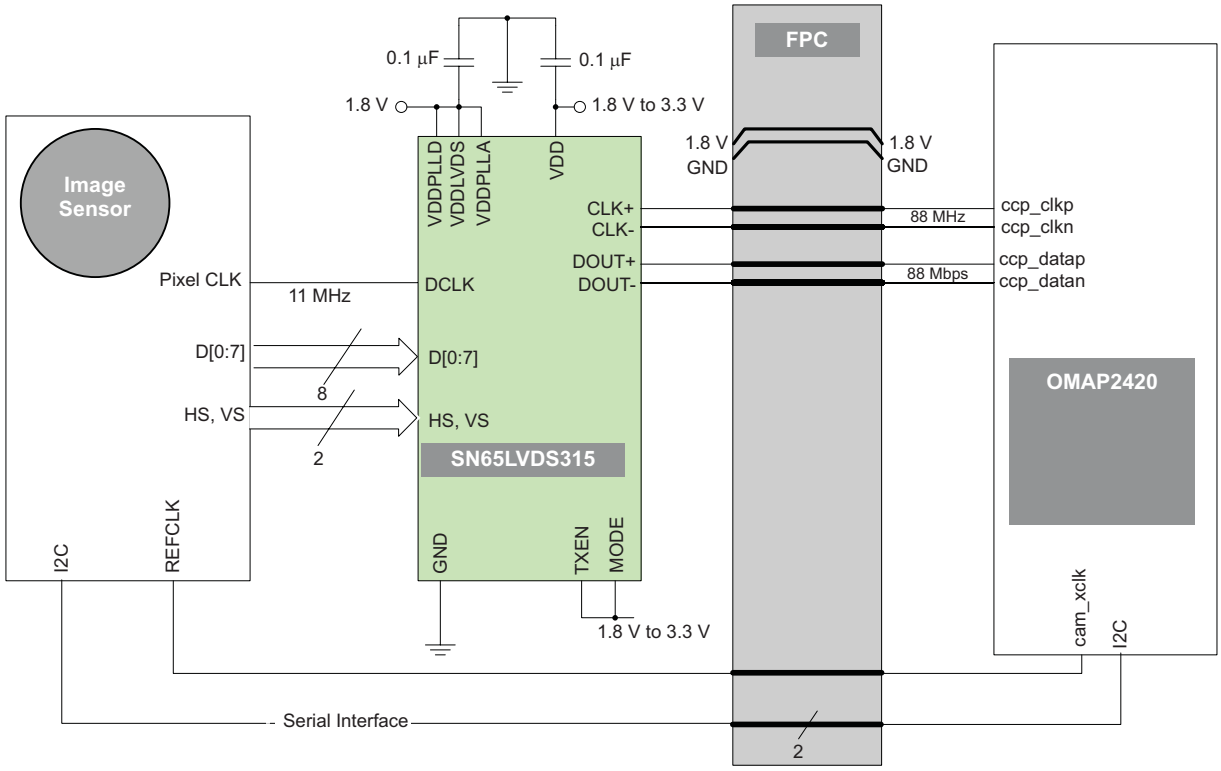


Figure 27. Typical VGA Display Application

Typical Application (continued)

9.2.1.1 Design Requirements

PARAMETERS	VALUE
VDD supply voltage	1.8 V to 3.3 V
VDDPLLD, VDDPLLA & VDDLVDS supply voltage	1.8 V
Input frequency	3.5 to 27 MHz (fixed to 11 MHz)
8-bit parallel input data	YUV422, YUV420, RGB888, RGB565 & RAW8
Input clock period jitter	5 ps-rms

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Calculation Example: VGA Camera Sensor

The following calculation shows an example for a VGA camera with following parameter:

display resolution: 640 x 480
frame refresh rate: 30 fps

vertical visible pixel: 480 lines
vertical blanking: 10 lines

horizontal visible pixel: 640 columns
horizontal blanking: 5 columns

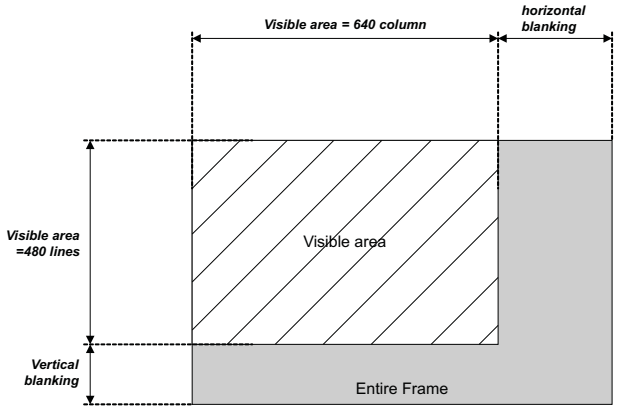


Figure 28. VGA - Full Frame Composition

Calculation of the total number of pixel and Blanking overhead:

visible area pixel count: 640 x 480 = 307,200 pixel
total frame pixel count: (640+5) x (480+10) = 316,050 pixel
blanking overhead: (316,050–307,200) div 307,200 = 2.8%

The application requires following serial link parameters:

pixel clk frequency: f_{DCLK} = 316.050 x 30 Hz = 9.5 MHz
DOUT serial data rate: dR = f_{DCLK} x8 = 76 Mbps
CLK output clock rate: f_{CLK} = f(dR) = 76 MHz

9.2.1.2.2 Typical Application Frequencies

The SN65LVDS315 in display mode supports pixel clock frequencies from 7 MHz to 27 MHz (which translates to DCLK frequencies of 56 MHz to 208 MHz). Table 7 provides a few typical display resolution examples. Table 7 also shows the assumed blanking overhead, which often times is smaller in the final application, resulting in a lower data rate.

9.2.1.2.2.1 8-Bit Camera Application

Table 7. Typical Application Data Rates And Serial Lane Usage

DISPLAY SCREEN RESOLUTION	VISIBLE PIXEL COUNT	CONTROL OVERHEAD	FRAME REFRESH RATE	DCLK PIXEL CLOCK FREQUENCY [MHz]	DATA RATE ON D0 WITH LS=0	f(CLK)
640x480 (VGA)	307,200	14%	10 Hz	3.5 MHz	28 Mbps	28 MHz
640x480 (VGA)	307,200	2%	15 Hz	4.7 MHz	38 Mbps	38 MHz
640x480 (VGA)	307,200	10%	30 Hz	10.1 MHz	81 Mbps	81 MHz
3 Mpixel	3,000,000	10%	7 Hz	23.1 MHz	185 Mbps	185 MHz
4 Mpixel	4,000,000	10%	5 Hz	22.0 MHz	176 Mbps	176 MHz
5 Mpixel	5,000,000	10%	4 Hz	22.0 MHz	176 Mbps	176 MHz
6 Mpixel	6,000,000	10%	3 Hz	19.8 MHz	158 Mbps	158 MHz
8 Mpixel	8,000,000	10%	2 Hz	17.6 MHz	141 Mbps	141 MHz
10 Mpixel	10,000,000	10%	2 Hz	22.0 MHz	176 Mbps	176 MHz
12 Mpixel	12,000,000	10%	2 Hz	25.1 MHz	201 Mbps	201 MHz

9.2.1.3 Application Curve

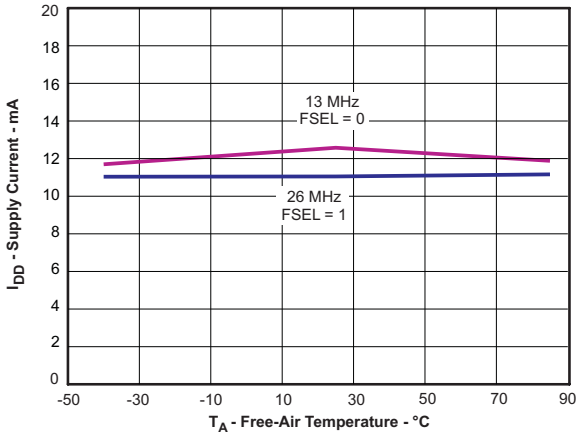


Figure 29. Supply Current I_{DD} Overtemperature

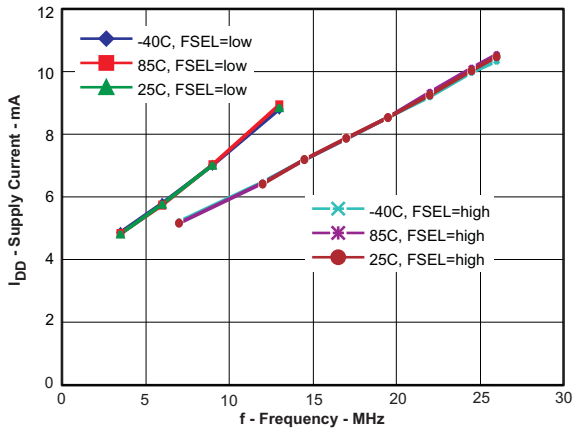


Figure 30. Supply Current I_{DD} Over PCLK Frequency

10 Power Supply Recommendations

The SN65LVDS315 was designed to operate reliably in a constricted environment with other digital switching ICs. In cell phone designs, the SN65LVDS315 often shares a power supply with various other ICs. The SN65LVDS315 can operate with power supply noise as specified in *Recommended Operating Conditions*. To minimize the power supply noise floor, provide good decoupling near the SN65LVDS315 power pins. The use of four ceramic capacitors (two 0.01 µF and two 0.1 µF) provides good performance. At the very least, it is recommended to install one 0.1 µF and one 0.01 µF capacitor near the SN65LVDS315. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and IC power inputs pins must be minimized. Placing the capacitor underneath the SN65LVDS315 on the bottom of the pcb is often a good choice.

11 Layout

11.1 Layout Guidelines

- Use 45 degree bends (chamfered corners), instead of right-angle (90°) bends. Right-angle bends increase the effective trace width, which changes the differential trace impedance creating large discontinuities. A 45° bends is seen as a smaller discontinuity.
- Place passive components within the signal path, such as source-matching resistors or ac-coupling capacitors, next to each other. Routing as in case a) creates wider trace spacing than in b), the resulting discontinuity, however, is limited to a far narrower area.
- When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below.
- Avoid metal layers and traces underneath or between the pads off the DisplayPort connectors for better impedance matching. Otherwise they will cause the differential impedance to drop below 75 Ω and fail the board during TDR testing.
- Use solid power and ground planes for 100 Ω impedance control and minimum power noise.
- For a multilayer PCB, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.
- For 100 Ω differential impedance, use the smallest trace spacing possible, which is usually specified by the PCB vendor.
- Keep the trace length as short as possible to minimize attenuation.
- Place bulk capacitors (for example, 10 µF) close to power sources, such as voltage regulators or where the power is supplied to the PCB.

11.2 Layout Example

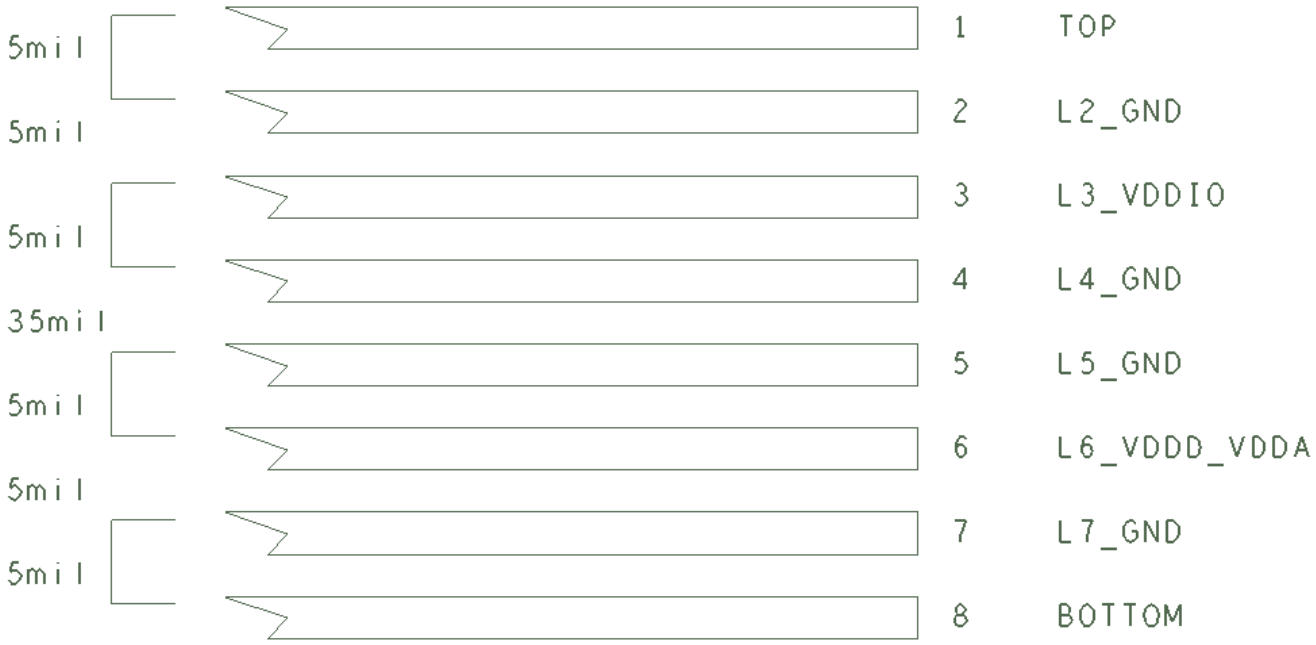


Figure 31. 8-Layers PCB Example

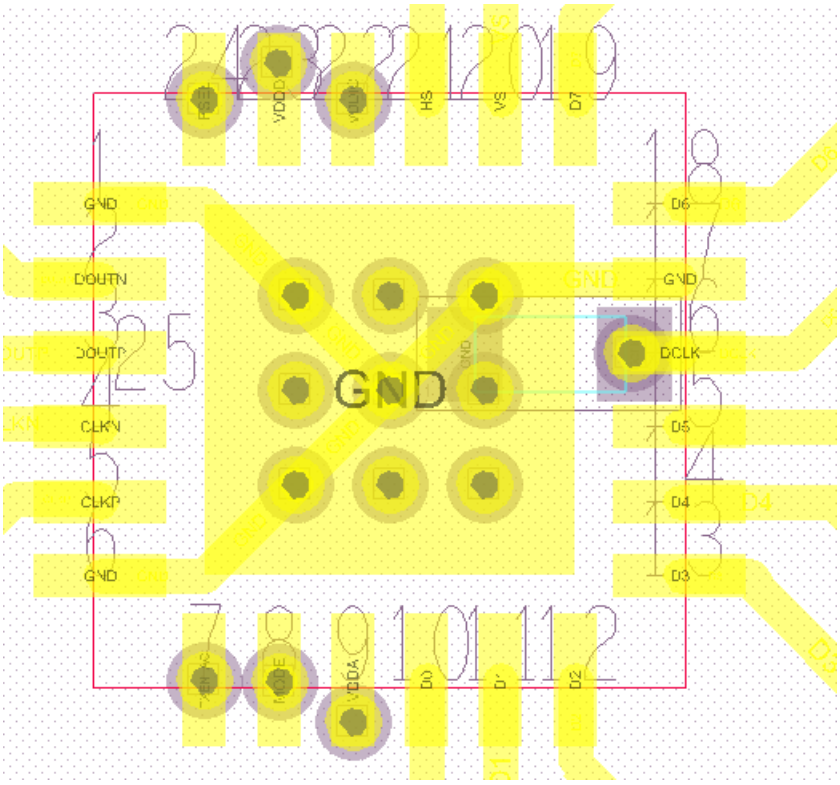


Figure 32. Footprint Example

Layout Example (continued)

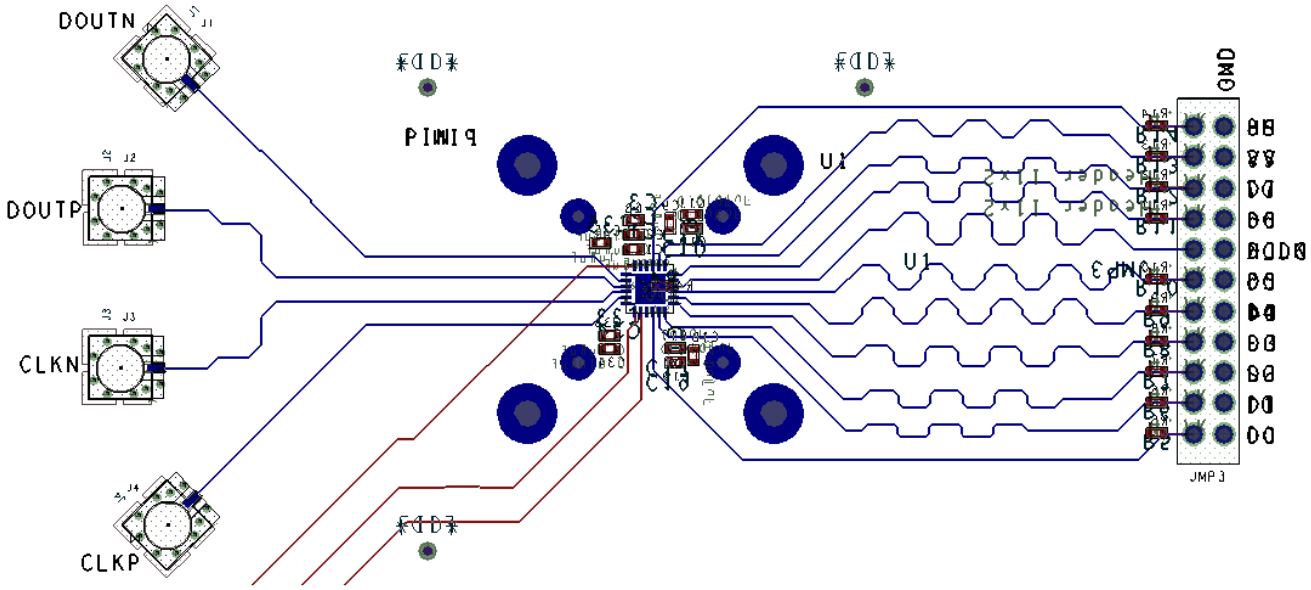


Figure 33. PCB Routing Example

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS315RGER	Active	Production	VQFN (RGE) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVDS315
SN65LVDS315RGER.A	Active	Production	VQFN (RGE) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVDS315
SN65LVDS315RGERG4	Active	Production	VQFN (RGE) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVDS315
SN65LVDS315RGERG4.A	Active	Production	VQFN (RGE) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVDS315
SN65LVDS315RGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVDS315
SN65LVDS315RGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVDS315

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

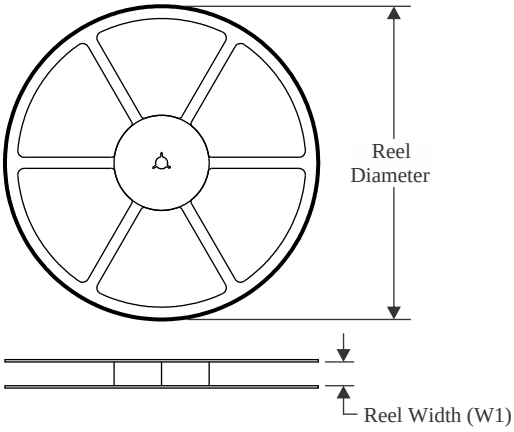
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

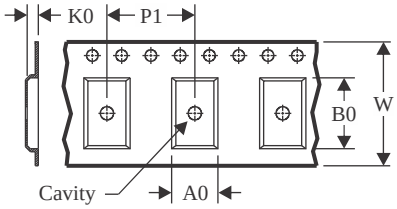
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

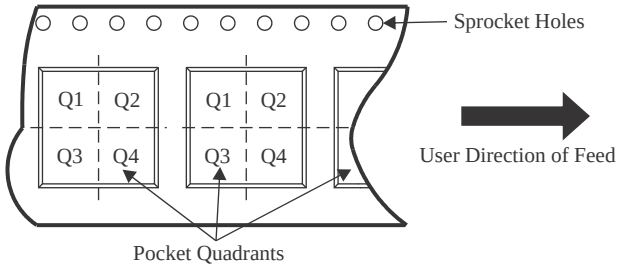


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

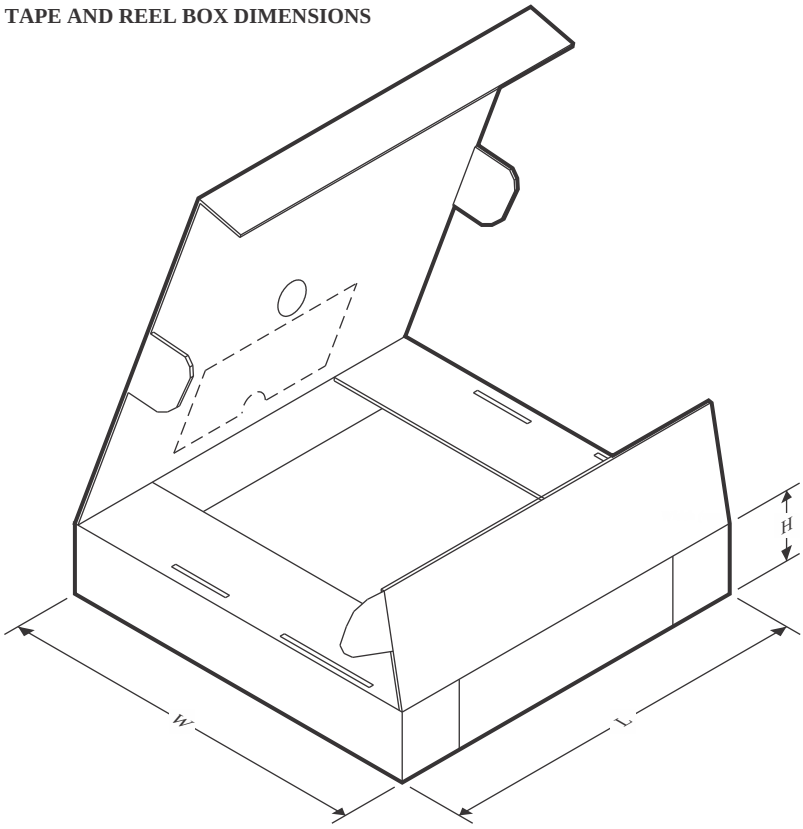
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS315RGER	VQFN	RGE	24	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65LVDS315RGERG4	VQFN	RGE	24	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65LVDS315RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



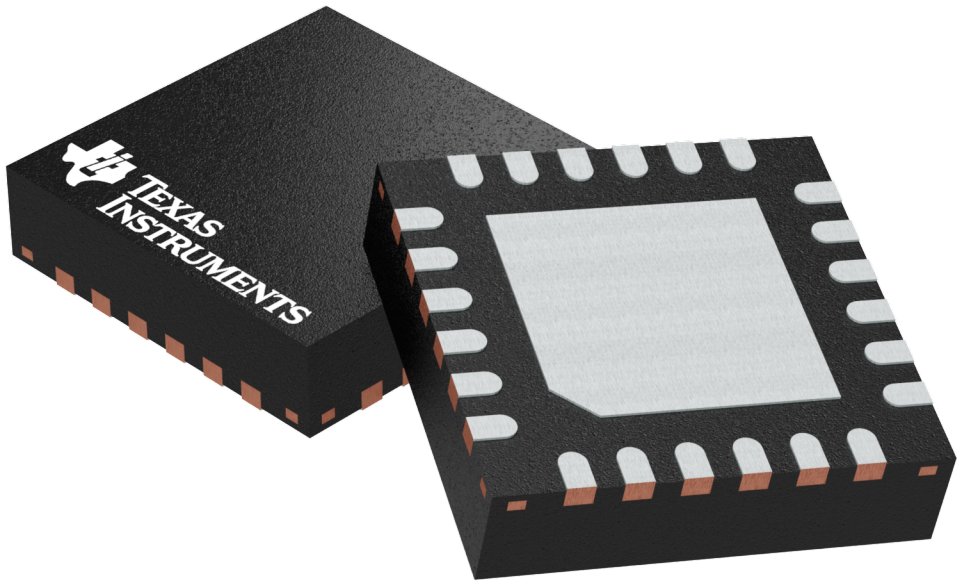
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS315RGER	VQFN	RGE	24	2500	353.0	353.0	32.0
SN65LVDS315RGERG4	VQFN	RGE	24	2500	353.0	353.0	32.0
SN65LVDS315RGET	VQFN	RGE	24	250	213.0	191.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

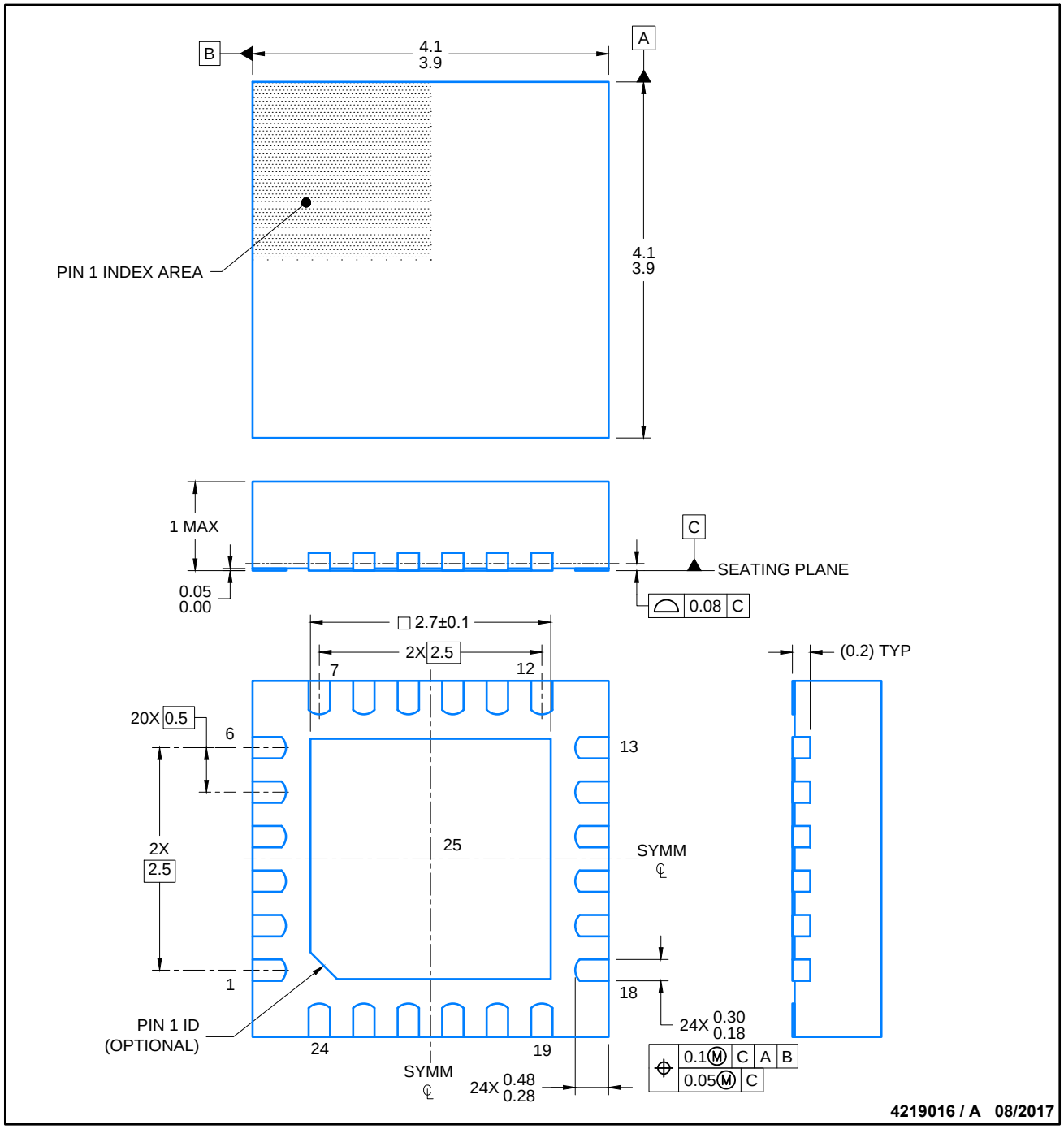
4204104/H

PACKAGE OUTLINE

RGE0024H

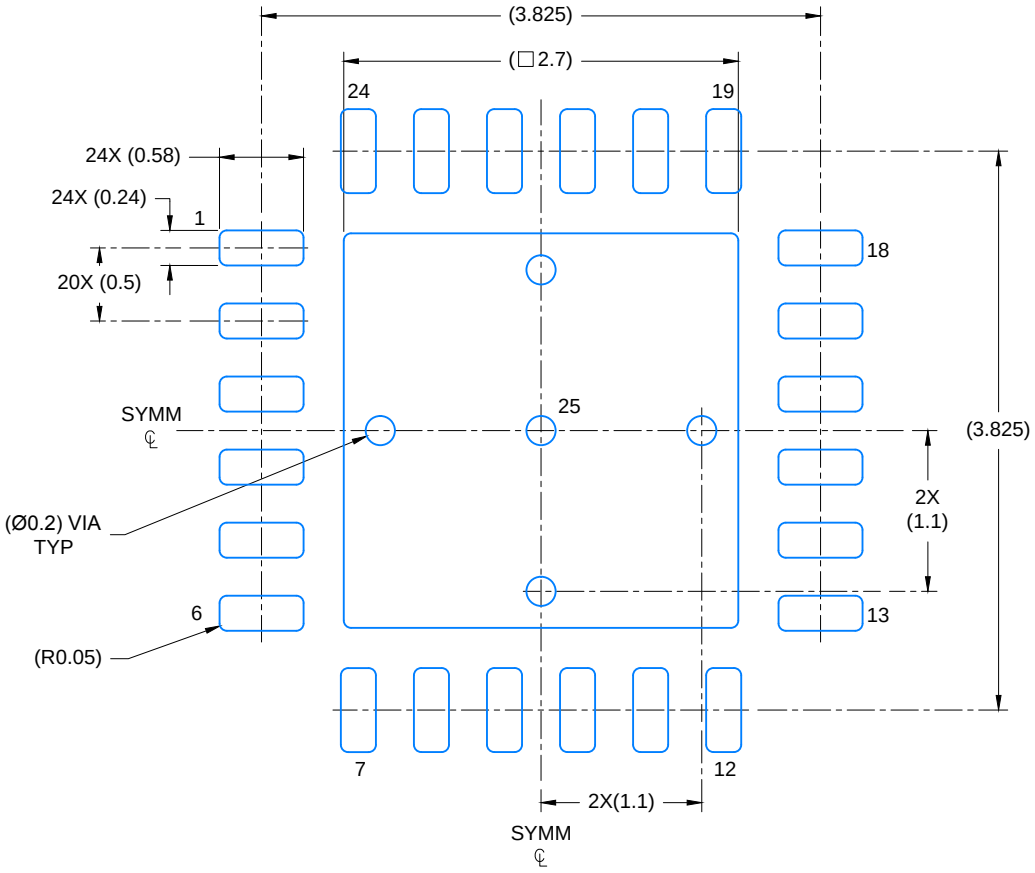
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



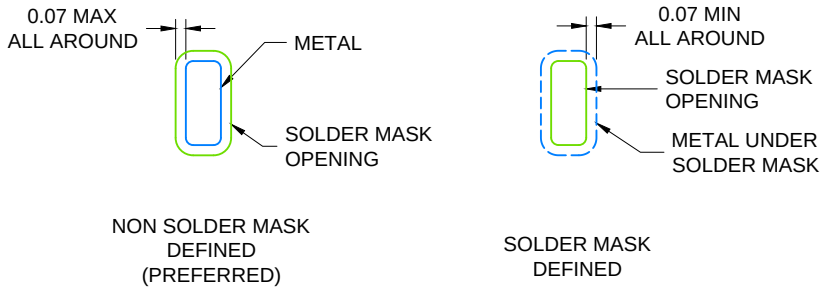
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

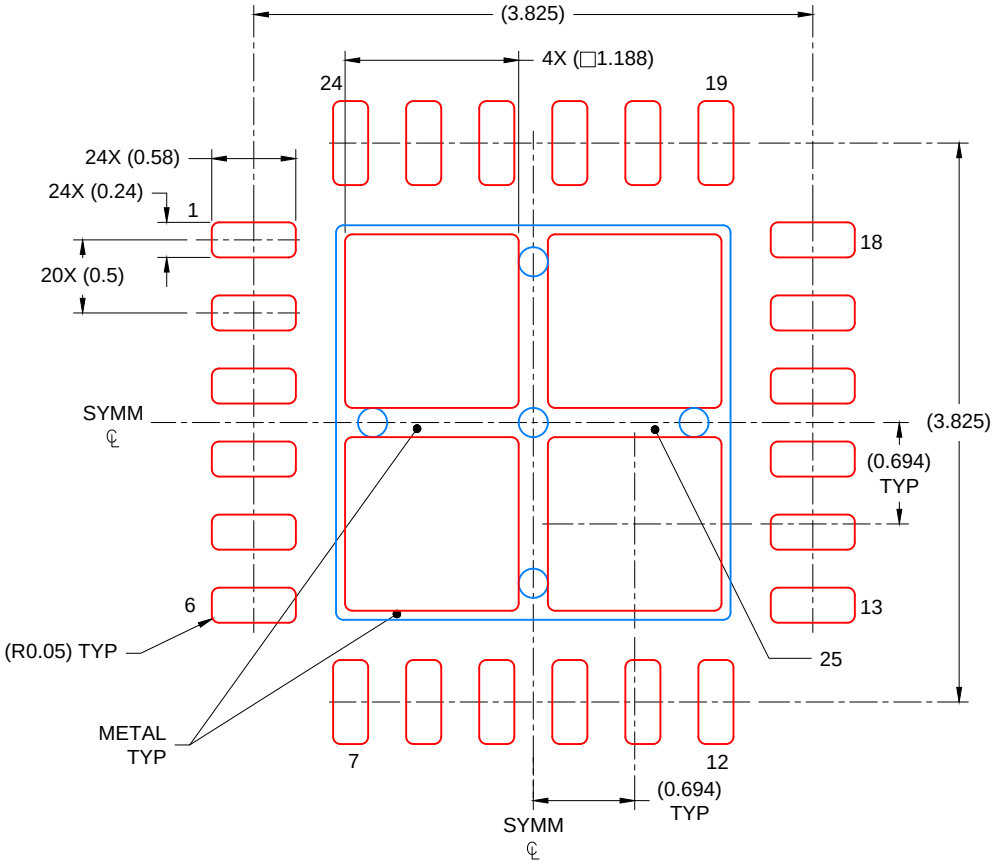


SOLDER MASK DETAILS

4219016 / A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219016 / A 08/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025