

SN54ABT162245, SN74ABT162245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS239F – MARCH 1993 – REVISED JUNE 2004

- Members of the Texas Instruments Widebus™ Family
- A-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- I_{off} Supports Partial-Power-Down Mode Operation
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

description/ordering information

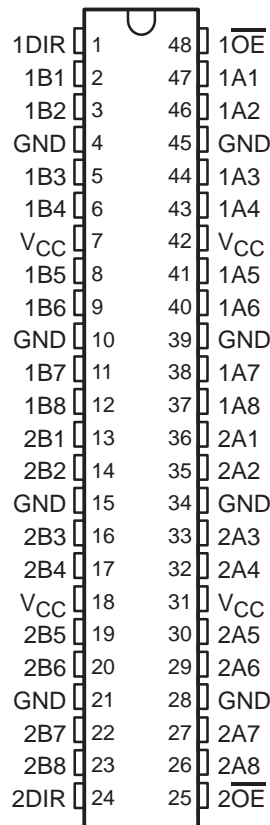
The 'ABT162245 devices are 16-bit noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses effectively are isolated.

The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

SN54ABT162245 . . . WD PACKAGE
SN74ABT162245 . . . DGG OR DL PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74ABT162245DL	ABT162245
		Tape and reel	SN74ABT162245DLR	
	TSSOP – DGG	Tape and reel	SN74ABT162245DGGR	ABT162245
–55°C to 125°C	CFP – WD	Tube	SNJ54ABT162245WD	SNJ54ABT162245WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54ABT162245, SN74ABT162245
16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS239F – MARCH 1993 – REVISED JUNE 2004

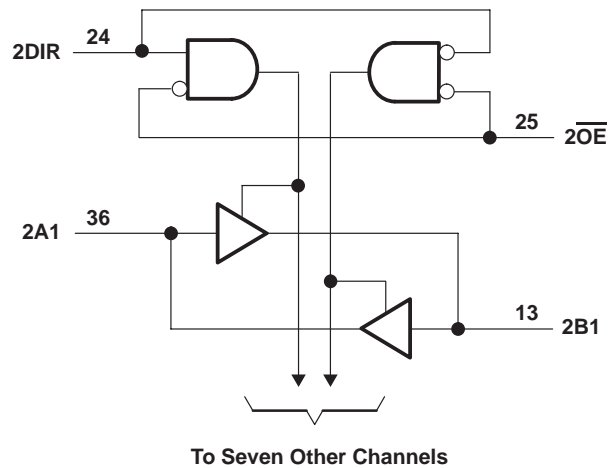
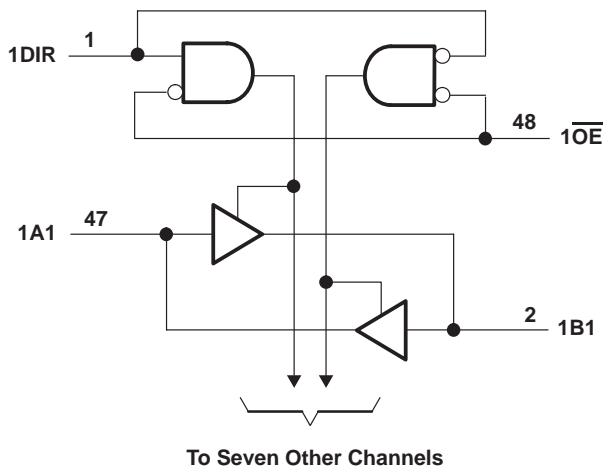
description/ordering information (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT162245 (B port)	96 mA
SN74ABT162245 (B port)	128 mA
SN54/74ABT162245 (A port)	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	70°C/W
DL package	63°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54ABT162245, SN74ABT162245
16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS239F – MARCH 1993 – REVISED JUNE 2004

recommended operating conditions (see Note 3)

		SN54ABT162245		SN74ABT162245		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	B port		-24	-32	mA
		A port		-3	-12	
I _{OL}	Low-level output current	B port		48	64	mA
		A port		12	12	
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ABT162245, SN74ABT162245

16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS239F – MARCH 1993 – REVISED JUNE 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			SN54ABT162245		SN74ABT162245		UNIT	
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA				-1.2				-1.2	V	
V _{OH}	A port	V _{CC} = 5 V, I _{OH} = -1 mA	3.8			2.5			2.5	V	
		V _{CC} = 4.5 V	I _{OH} = -1 mA	3.3			3				3
			I _{OH} = -3 mA	3.1			3				3.1
	B port	V _{CC} = 5 V	I _{OH} = -12 mA	2.6*							2.6
			I _{OH} = -3 mA	3			3				3
		V _{CC} = 4.5 V	I _{OH} = -3 mA	2.5			2.5				2.5
V _{OL}	A port	V _{CC} = 4.5 V	I _{OL} = 12 mA			0.8			0.8	V	
			B port	I _{OL} = 48 mA			0.45				0.45
				I _{OL} = 64 mA			0.55*				0.55
V _{hys}				100					mV		
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND				±1			±1	μA	
	A or B ports					±20			±20		
I _{OZH} §	V _{CC} = 5.5 V, V _O = 2.7 V				10			10	10	μA	
I _{OZL} §	V _{CC} = 5.5 V, V _O = 0.5 V				-10			-10	-10	μA	
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V				±100				±100	μA	
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V		Outputs high		50			50	50	μA	
I _O ¶	A port	V _{CC} = 5.5 V, V _O = 2.5 V	-25	-50	-100‡	-25	-90	-25	-100	mA	
	B port		-50	-100	-180	-50	-180	-50	-180		
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		2			2	2	mA	
			Outputs low		32			32	32		
			Outputs disabled		2			2	2		2
ΔI _{CC} #	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled		1			2	2	mA	
			Outputs disabled		0.05			1	0.05		
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5			1.5	1.5		
C _i	V _I = 2.5 V or 0.5 V				3				pF		
C _{io}	V _O = 2.5 V or 0.5 V				6				pF		

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ This limit applies only to the SN74ABT162245.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.



SN54ABT162245, SN74ABT162245
16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS239F – MARCH 1993 – REVISED JUNE 2004

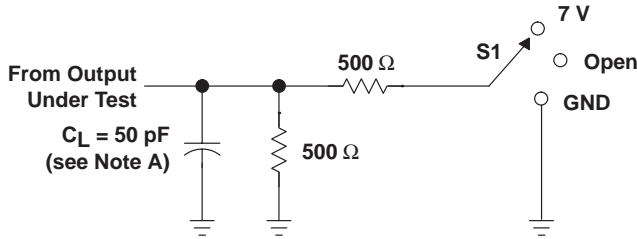
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABT162245		SN74ABT162245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	2.2	3.4	1	4.1	1	3.9	ns
t_{PHL}			1	2.3	3.7	1	4.4	1	4.2	
t_{PLH}	B	A	1	2.7	4.1	1	4.9	1	4.6	ns
t_{PHL}			1.5	3.1	4.6	1.5	5.2	1.5	5.1	
t_{PZH}	\overline{OE}	B	1	3.6	5.2	1	6.4	1	6.3	ns
t_{PZL}			1	3.7	5.4	1	6.5	1	6.4	
t_{PHZ}	\overline{OE}	B	2	4.4	5.8	2	6.4	2	6.3	ns
t_{PLZ}			1.5	3.3	4.7	1.5	5.6	1.5	5.2	
t_{PZH}	\overline{OE}	A	1.5	4.1	6	1.5	7.2	1.5	7.1	ns
t_{PZL}			1.5	4.3	6.1	1.5	7.3	1.5	7	
t_{PHZ}	\overline{OE}	A	2	4.5	6.1	2	6.8	2	6.6	ns
t_{PLZ}			1.5	3.7	5.1	1.5	6.1	1.5	5.7	

SN54ABT162245, SN74ABT162245
16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

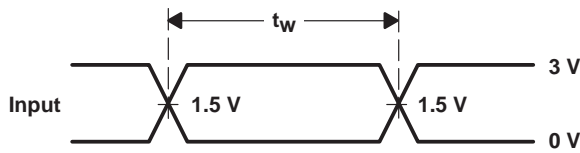
SCBS239F – MARCH 1993 – REVISED JUNE 2004

PARAMETER MEASUREMENT INFORMATION

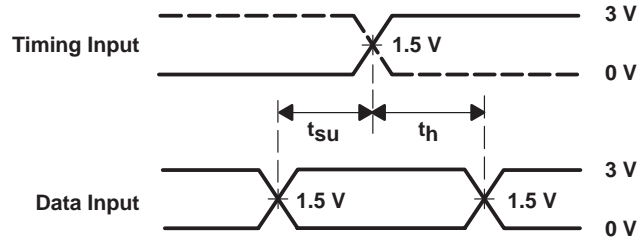


LOAD CIRCUIT

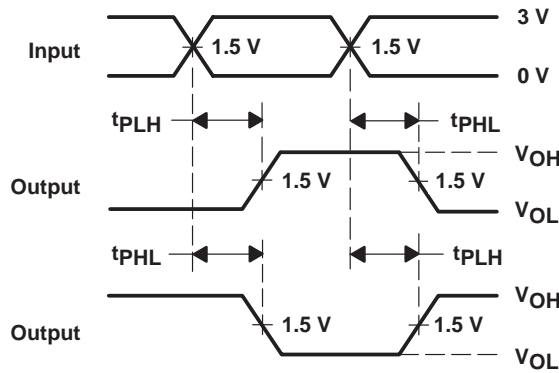
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



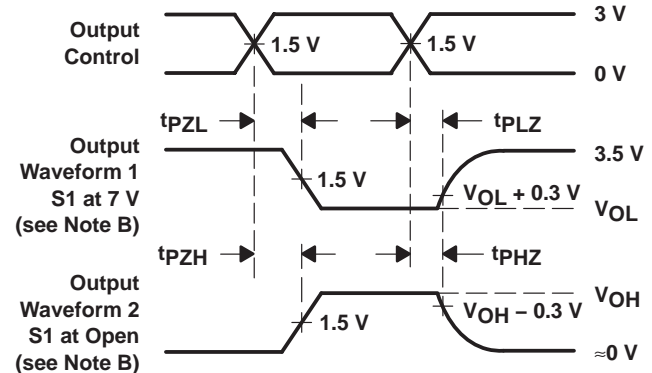
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9677401QXA	Active	Production	CFP (WD) 48	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9677401QX A SNJ54ABT162245 WD
74ABT162245DLRG4	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162245
SN74ABT162245DGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162245
SN74ABT162245DL	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162245
SN74ABT162245DLR	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162245
SNJ54ABT162245WD	Active	Production	CFP (WD) 48	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9677401QX A SNJ54ABT162245 WD

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ABT162245, SN74ABT162245 :

- Catalog : [SN74ABT162245](#)
- Military : [SN54ABT162245](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT162245DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ABT162245DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

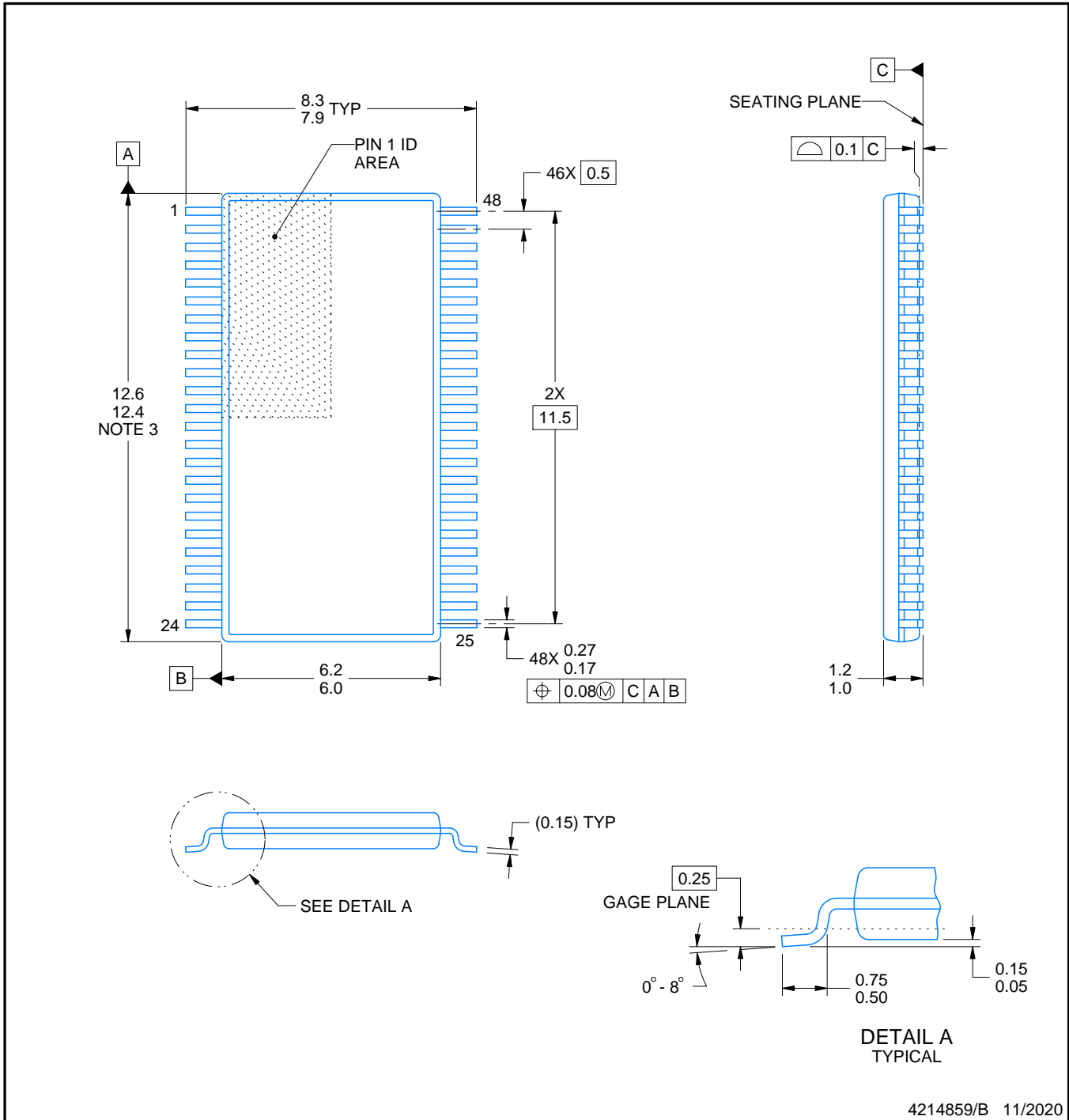
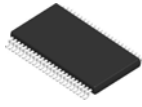

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT162245DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ABT162245DLR	SSOP	DL	48	1000	367.0	367.0	55.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT162245DL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74ABT162245DLG4	DL	SSOP	48	25	473.7	14.24	5110	7.87



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

- Publication IPC-7351 may have alternate designs.
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

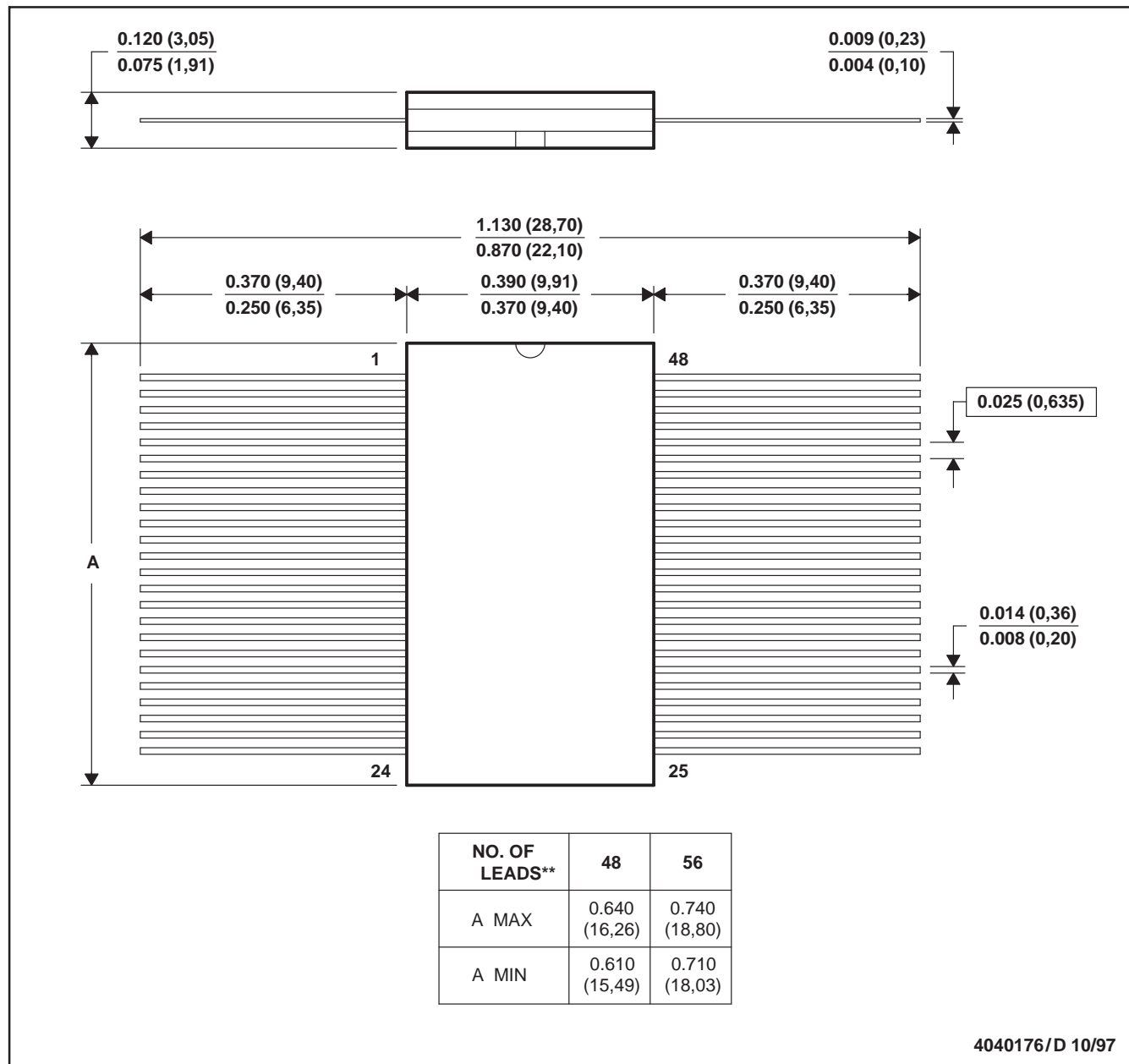


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
 GDFP1-F56 and JEDEC MO-146AB

MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated