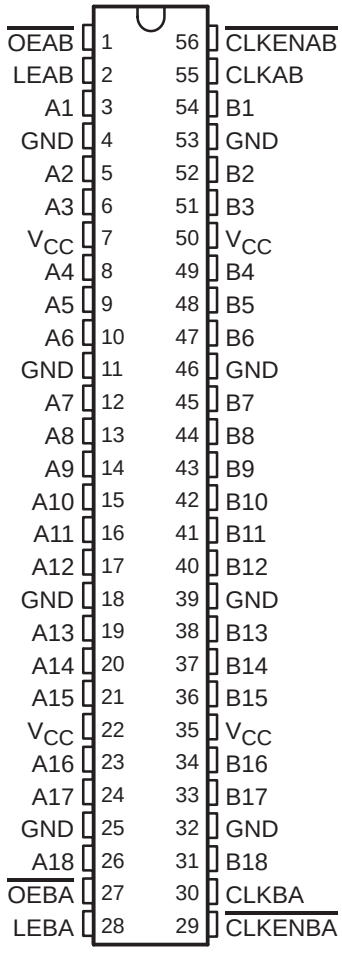
- **Members of the Texas Instruments *Widebus*™ Family**
- **B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT162601 . . . WD PACKAGE
SN74ABT162601 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs.

For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

The B-port outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

description (continued)

The SN54ABT162601 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT162601 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

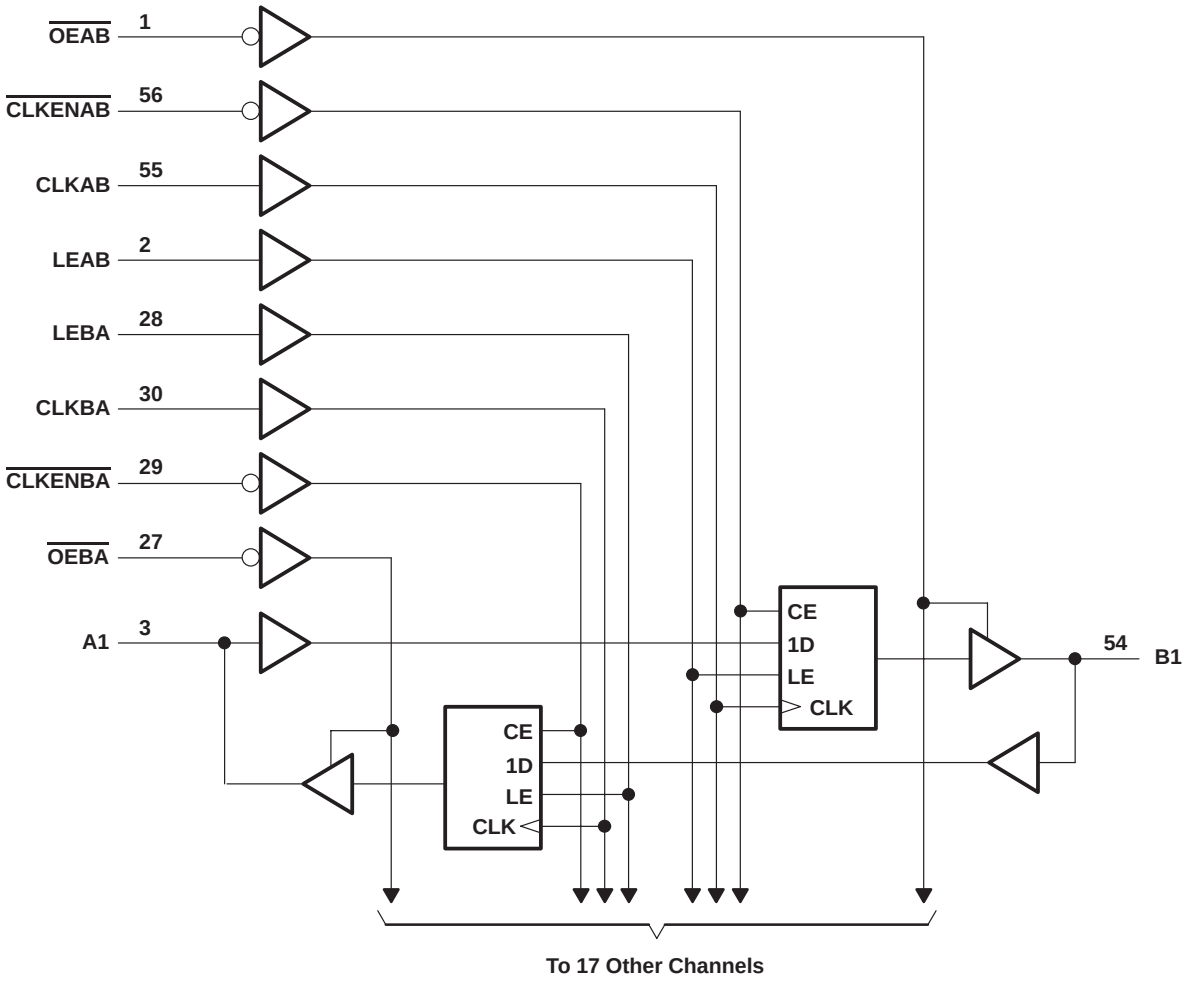
INPUTS					OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
H	L	L	X	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0‡
L	L	L	H	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, CLKBA, and $\overline{\text{CLKENBA}}$.

‡ Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT162601 (A port) . . . . . 96 mA
SN74ABT162601 (A port) . . . . . 128 mA
B port . . . . . 30 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –18 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . . 81°C/W
DL package . . . . . 74°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			SN54ABT162601		SN74ABT162601		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	A port		–24		–32	mA
		B port		–12		–12	
I_{OL}	Low-level output current	A port		48		64	mA
		B port		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused inputs of the devices must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application note, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A = 25°C			SN54ABT162601		SN74ABT162601		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2		–1.2		–1.2	V
V_{OH}	A port	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5			2.5		2.5		V
		V_{CC} = 5 V,	I_{OH} = –3 mA	3			3		3		
		V_{CC} = 4.5 V	I_{OH} = –24 mA	2			2				
			I_{OH} = –32 mA	2*					2		
	B port	V_{CC} = 4.5 V,	I_{OH} = –1 mA	3.35			3.3		3.35		
		V_{CC} = 5 V,	I_{OH} = –1 mA	3.85			3.8		3.85		
		V_{CC} = 4.5 V	I_{OH} = –3 mA	3.1			3		3.1		
			I_{OH} = –12 mA	2.6					2.6		
V_{OL}	A port	V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55		0.55			V
			I_{OL} = 64 mA			0.55*				0.55	
	B port	V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.8		0.8		0.8	
V_{hys}					100						mV
I_I	Control inputs	V_{CC} = 0 to 5.5 V, V_I = V_{CC} or GND				±1		±1		±1	µA
	A or B ports	V_{CC} = 2.1 V to 5.5 V, V_I = V_{CC} or GND				±20		±20		±20	
I_{OZPU}		V_{CC} = 0 to 2.1 V, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50		±50**		±50	µA
I_{OZPD}		V_{CC} = 2.1 V to 0, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50		±50**		±50	µA
I_{OZH}‡		V_{CC} = 2.1 V to 5.5 V, V_O = 2.7 V, $\overline{OE}$ ≥ 2 V				10		10		10	µA
I_{OZL}‡		V_{CC} = 2.1 V to 5.5 V, V_O = 0.5 V, $\overline{OE}$ ≥ 2 V				–10		–10		–10	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V			±100*				±100	µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	A port	V_{CC} = 5.5 V,	V_O = 2.5 V	–50	–100	–180	–50	–180	–50	–180	mA
	B port			–25	–55	–100	–25	–100	–25	–100	
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			3		3		3	mA
			Outputs low			36		36		36	
			Outputs disabled			3		3		3	
ΔI_{CC}¶		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				50		50		50	µA
C_i	Control inputs	V_I = 2.5 V or 0.5 V			3						pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V			9						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
** On products compliant to MIL-PRF-38535, this parameter is not production tested.
† All typical values are at V_{CC} = 5 V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

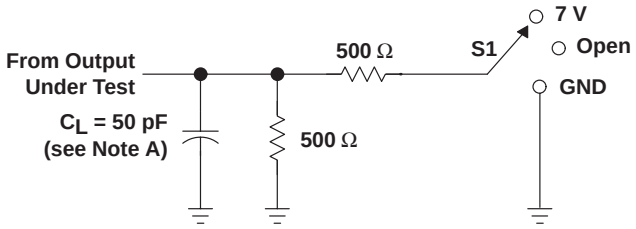
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(see Figure 1)

				SN54ABT162601		SN74ABT162601		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			0	150	0	150	MHz
t_w	Pulse duration	LEAB or LEBA high		2.5		2.5		ns
		CLKAB or CLKBA high or low		3.3		3		
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑		4.8		4.3		ns
		A before LEAB↓ or B before LEBA↓	CLK high	2.5		2.5		
			CLK low	1.2		1		
		CLKEN before CLK↑		2.7		2.7		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑		0.5		0		ns
		A after LEAB↓ or B after LEBA↓		2		0.5		
		CLKEN after CLK↑		0.5		0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

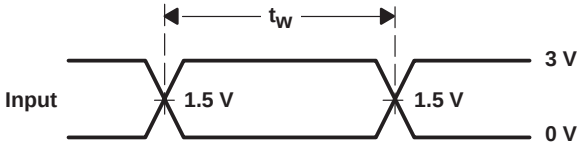
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT162601		SN74ABT162601		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	A	B	1.5	2.8	4	1.5	5.1	1.5	4.8	ns
t_{PHL}			2	3.7	5.2	2	6.1	2	5.7	
t_{PLH}	B	A	1	2.5	3.6	1	4.5	1	4	ns
t_{PHL}			2	3.3	4.5	2	5.1	2	4.9	
t_{PLH}	LEBA	A	2	3.3	4.5	2	5.6	2	5	ns
t_{PHL}			2	3.6	4.7	2	5.4	2	5	
t_{PLH}	LEAB	B	2	3.4	4.8	2	6.1	2	5.6	ns
t_{PHL}			2	3.8	5.2	2	6.4	2	5.9	
t_{PLH}	CLKBA	A	1.5	3.1	4.7	1.5	5.4	1.5	5.3	ns
t_{PHL}			1.5	3.1	4.3	1.5	5.2	1.5	5	
t_{PLH}	CLKAB	B	1.5	3.3	4.7	1.5	6	1.5	5.5	ns
t_{PHL}			1.5	3.5	4.8	1.5	5.8	1.5	5.3	
t_{PZH}	$\overline{OEBA}$	A	2	3.5	4.6	2	5.5	2	5.1	ns
t_{PZL}			2	3.7	4.7	2	5.8	2	5.4	
t_{PZH}	$\overline{OEAB}$	B	2	3.8	5.3	1.5	6.6	2	6.1	ns
t_{PZL}			2	3.6	5.1	2	6.2	2	5.7	
t_{PHZ}	$\overline{OEBA}$	A	2	3.6	5.4	1.4	6.6	2	6.2	ns
t_{PLZ}			1.5	3.2	4.7	1.5	5.8	1.5	5.4	
t_{PHZ}	$\overline{OEAB}$	B	2	3.4	4.8	1.4	5.6	2	5.4	ns
t_{PLZ}			1.5	3.2	4.5	1.5	5.7	1.5	5.2	

PARAMETER MEASUREMENT INFORMATION

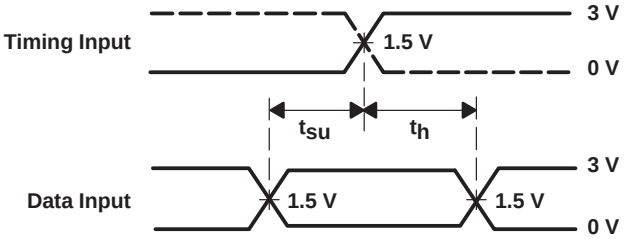


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

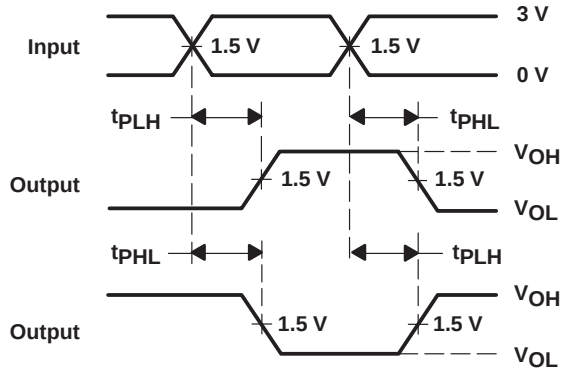
LOAD CIRCUIT



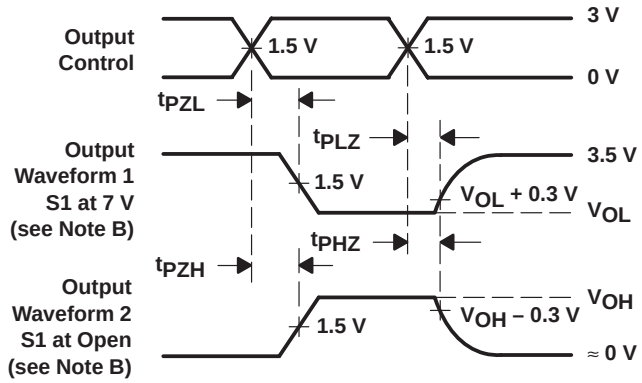
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ABT162601DGGR	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162601
SN74ABT162601DGGR.B	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162601
SN74ABT162601DLR	Active	Production	SSOP (DL) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162601
SN74ABT162601DLR.B	Active	Production	SSOP (DL) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162601

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

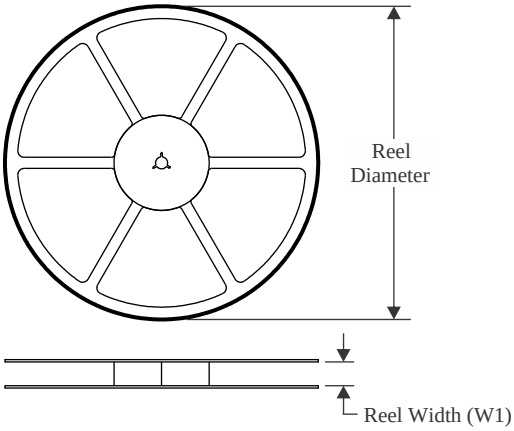
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

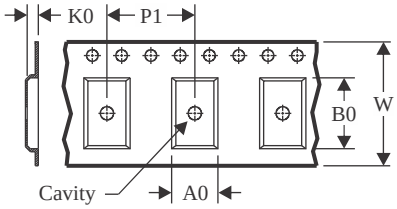
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

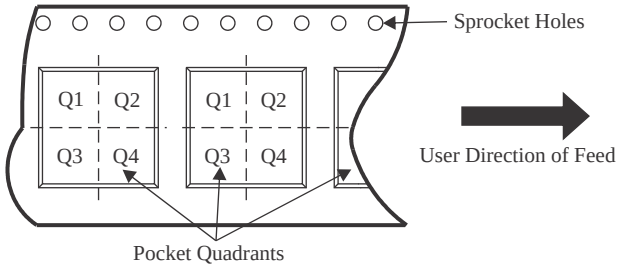


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

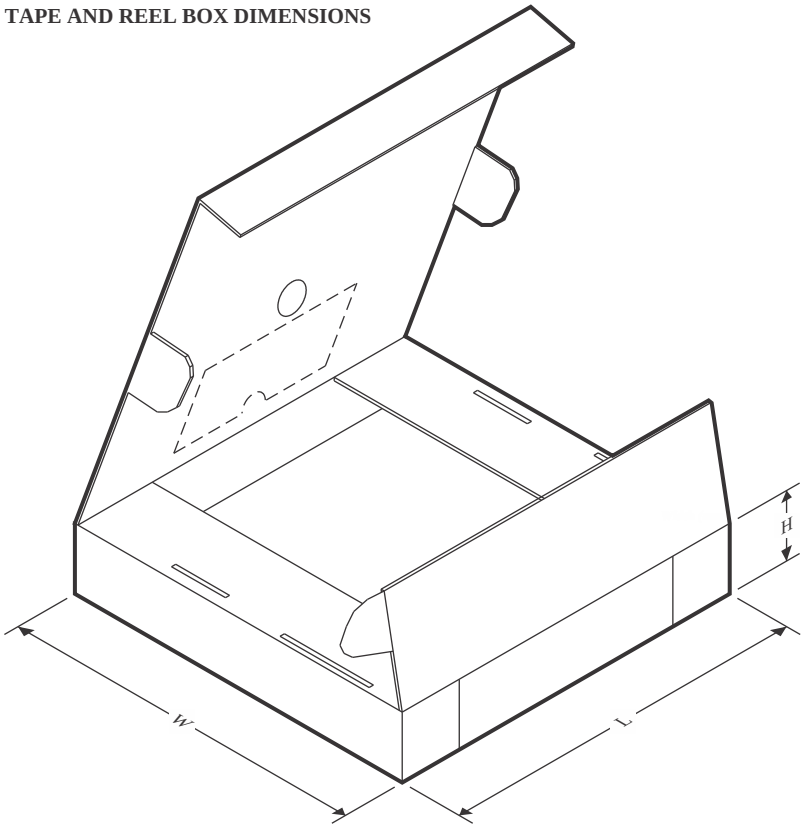
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT162601DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74ABT162601DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

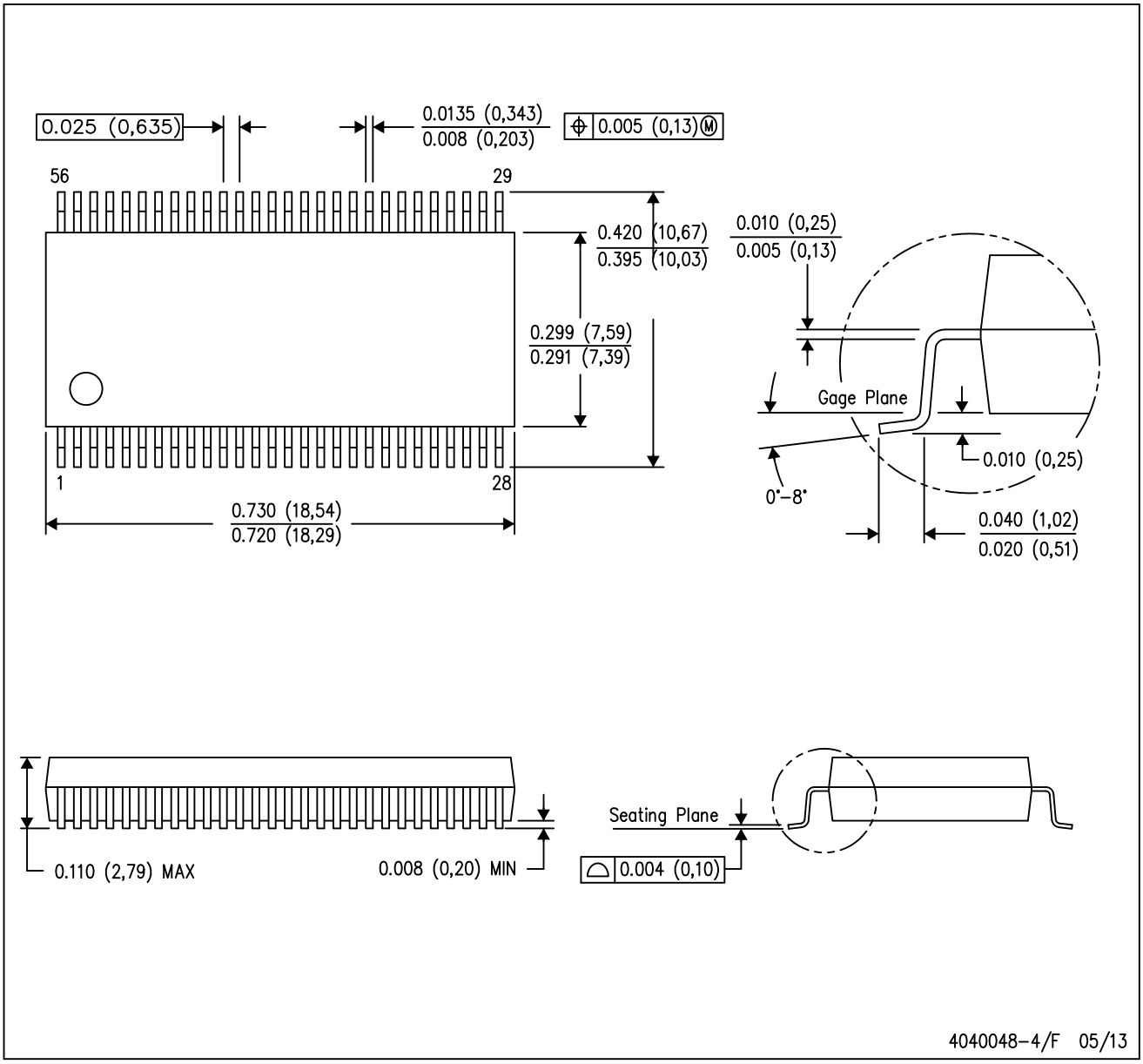
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT162601DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74ABT162601DLR	SSOP	DL	56	1000	356.0	356.0	53.0

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

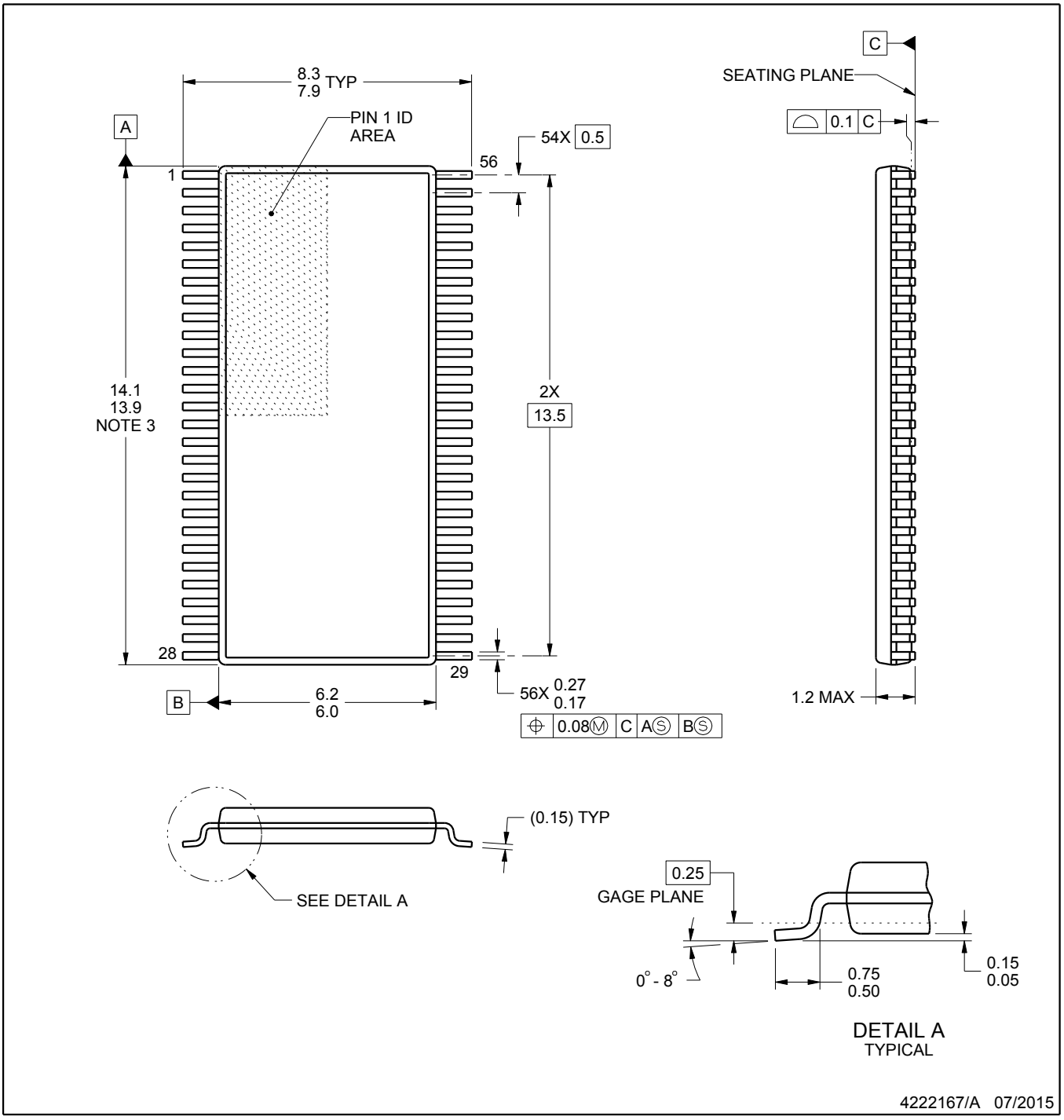
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DGG0056A

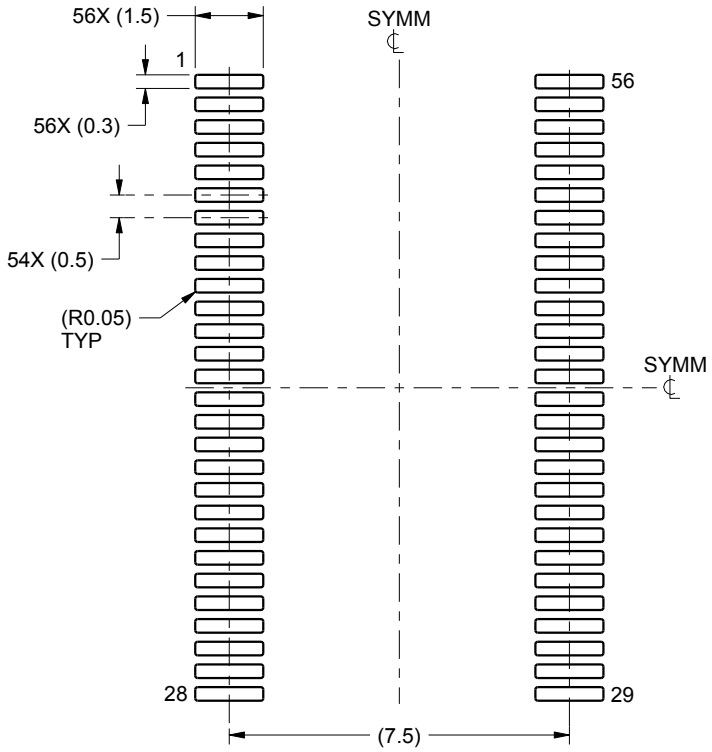
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

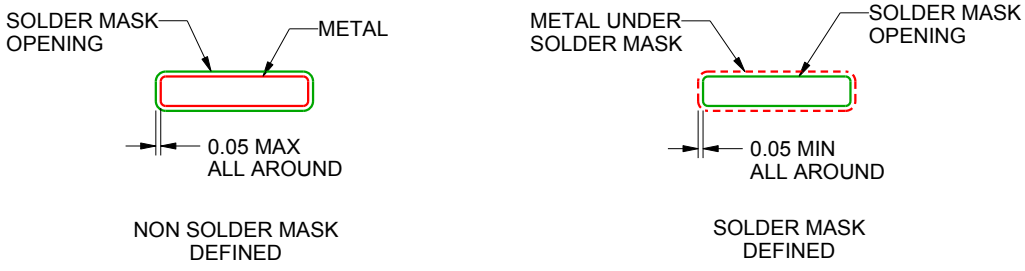


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

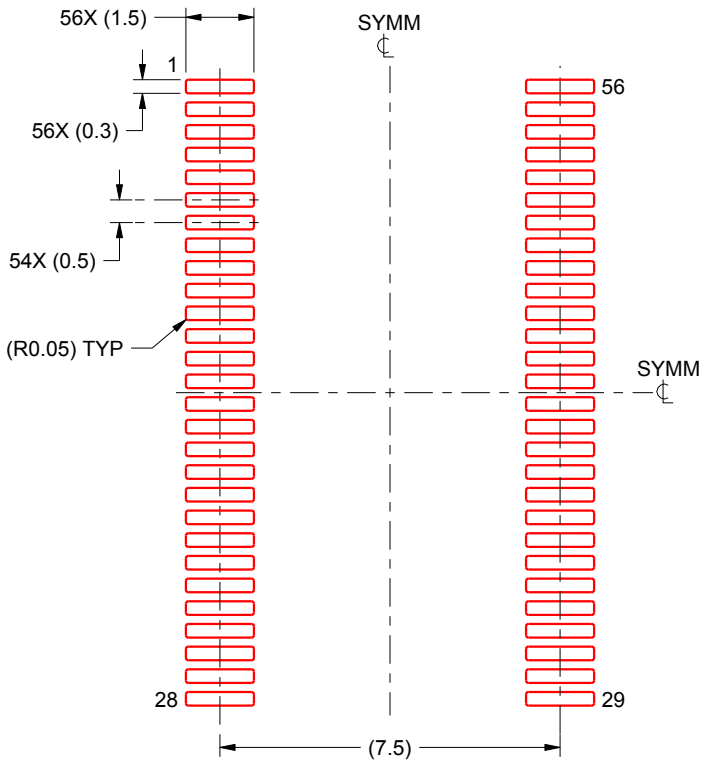


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025