

SN54ABT620, SN74ABT620 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS113D – FEBRUARY 1991 – REVISED APRIL 1998

- State-of-the-Art *EPIC-II^B*™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Plastic (N) and Ceramic (J) DIPs

description

These octal bus transceivers provide for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing. The 'ABT620 devices provide inverted data at the outputs.

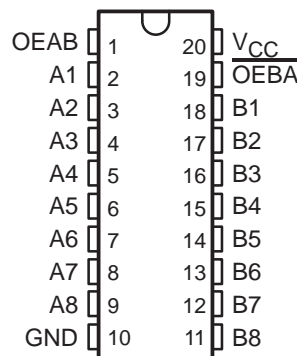
These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic levels at the output-enable (OEAB and $\overline{\text{OEBA}}$) inputs.

The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. When both OEAB and $\overline{\text{OEBA}}$ are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 total) remain at their last states. In this way, each output reinforces its input in this configuration.

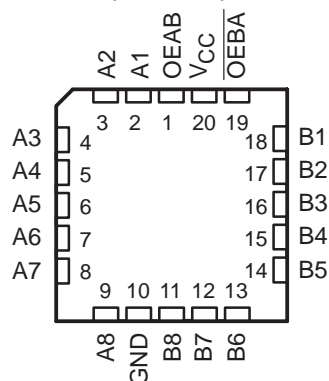
To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN54ABT620 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT620 is characterized for operation from -40°C to 85°C .

SN54ABT620 . . . J PACKAGE
SN74ABT620 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT620 . . . FK PACKAGE
(TOP VIEW)



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 **TEXAS
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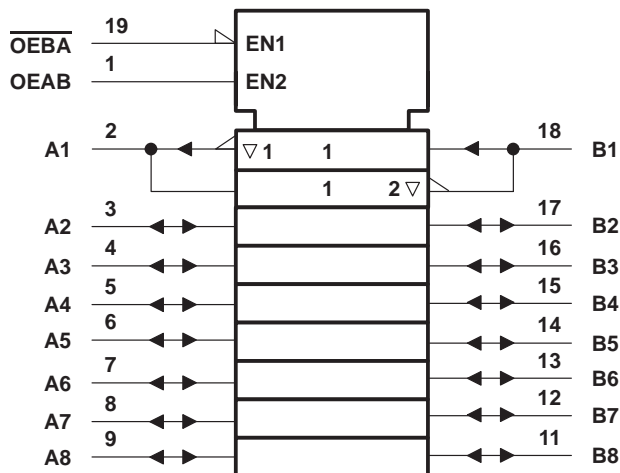
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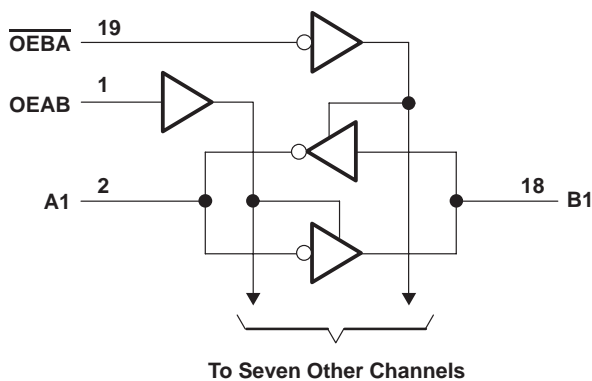
FUNCTION TABLE

INPUTS		OPERATION
OEBA	OEAB	
L	L	\overline{B} data to A bus
L	H	\overline{B} data to A bus, A data to B bus
H	L	Isolation
H	H	\overline{A} data to B bus

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT620	96 mA
SN74ABT620	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	115°C/W
DW package	97°C/W
N package	67°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions (see Note 3)

		SN54ABT620		SN74ABT620		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		5	5	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused pins (control or I/O) of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			SN54ABT620		SN74ABT620		UNIT		
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX			
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA		-1.2			-1.2		-1.2		V		
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.5			2.5		2.5		V		
	V _{CC} = 5 V, I _{OH} = -3 mA		3			3		3				
	V _{CC} = 4.5 V	I _{OH} = -24 mA	2			2						
I _{OH} = -32 mA		2*					2					
V _{OL}	V _{CC} = 4.5 V		I _{OL} = 48 mA			0.55		0.55		V		
			I _{OL} = 64 mA			0.55*			0.55			
V _{hys}			100							mV		
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND	±1			±1		±1		μA		
	A or B ports		±100			±100		±100				
I _{OZH} ‡	V _{CC} = 5.5 V, V _O = 2.7 V		50			50		50		μA		
I _{OZL} ‡	V _{CC} = 5.5 V, V _O = 0.5 V		-50			-50		-50		μA		
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		μA		
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V		Outputs high			50		50		μA		
I _O §	V _{CC} = 5.5 V, V _O = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA		
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high			5		250		250		μA
			Outputs low			24		30		30		mA
			Outputs disabled			0.5		250		250		μA
ΔI _{CC} ¶	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled			1.5		1.5		1.5		mA
			Outputs disabled			0.05		0.05		0.05		
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1.5			1.5		1.5			
C _i	Control inputs	V _I = 2.5 V or 0.5 V		4							pF	
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V		7							pF	

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C		SN54ABT620		SN74ABT620		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	4.1	1		1	4.8	ns
t_{PHL}			1	4.3	1		1	4.8	
t_{PZH}	\overline{OEBA}	A	1.3	4.6	1.3		1.3	5.5	ns
t_{PZL}			1	6.1	1		1	7.1	
t_{PHZ}	\overline{OEBA}	A	2	6.3	2		2	7	ns
t_{PLZ}			1.4	5.4	1.4		1.4	5.8	
t_{PZH}	OEAB	B	1.6	6.2	1.6		1.6	6.8	ns
t_{PZL}			2	5.9	2		2	6.4	
t_{PHZ}	OEAB	B	1.2	5.6	1.2		1.2	6.5	ns
t_{PLZ}			1.1	4.7	1.1		1.1	5.6	

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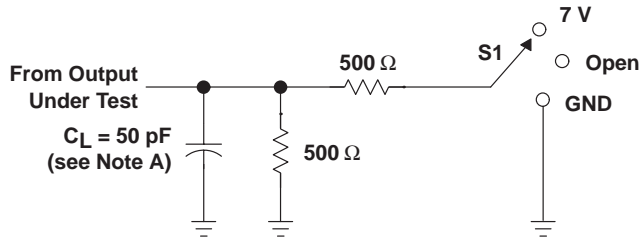


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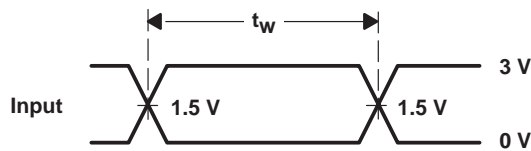
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PARAMETER MEASUREMENT INFORMATION

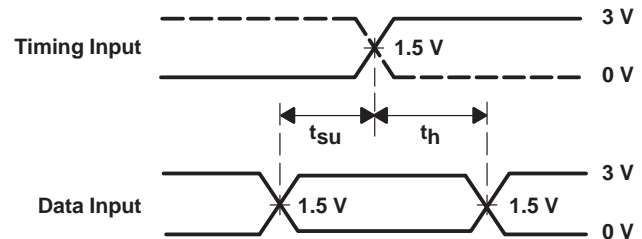


LOAD CIRCUIT

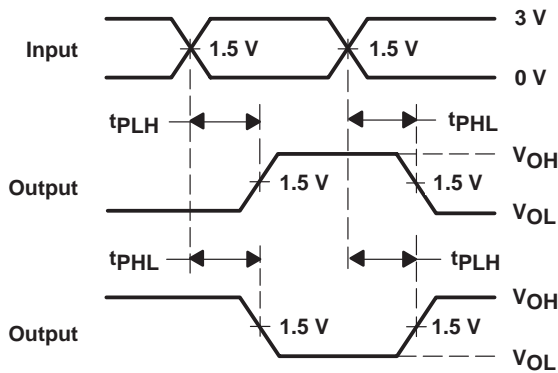
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



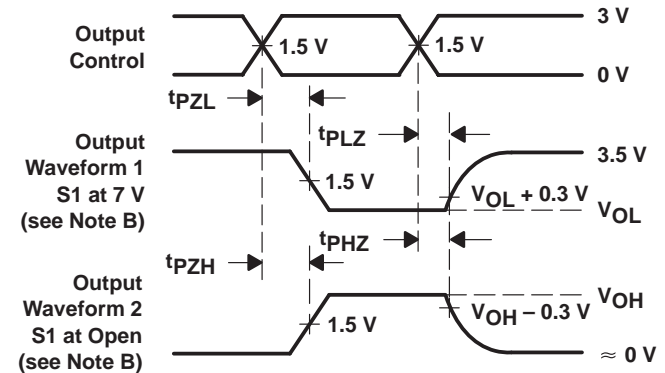
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT620DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT620	Samples
SN74ABT620N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74ABT620N	Samples
SN74ABT620NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT620	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT620NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT620NSR	SO	NS	20	2000	367.0	367.0	45.0

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