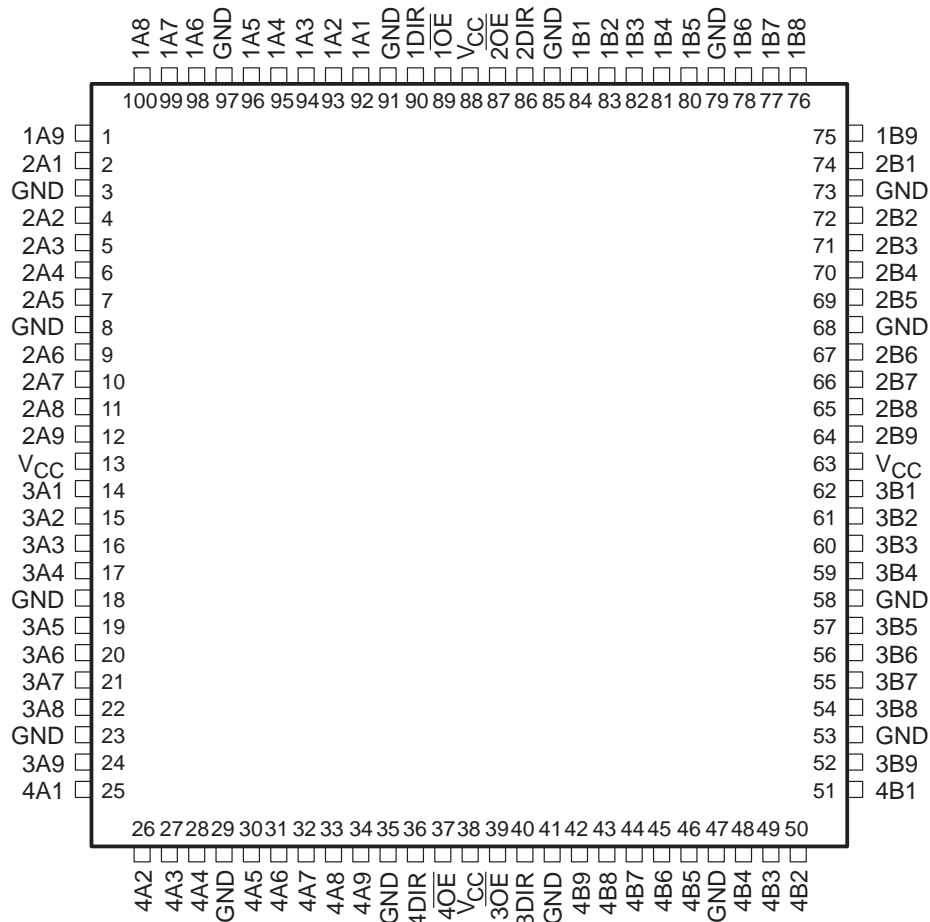


SN54ABTH32245, SN74ABTH32245 36-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS228G – JUNE 1992 – REVISED MAY 1997

- Members of the Texas Instruments *Widebus+*™ Family
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Released as DSCC SMD 5962-9557701NXD
- PZ Package Qualified for Military Per MIL-PRF-38535 (QML)
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include 100-Pin Plastic Thin Quad Flat (PZ) Package With 14×14 -mm Body Using 0.5-mm Lead Pitch and Space-Saving 100-Pin Ceramic Quad Flat (HS) Package†

'ABTH32245 . . . PZ PACKAGE
(TOP VIEW)



† The HS package is not production released.



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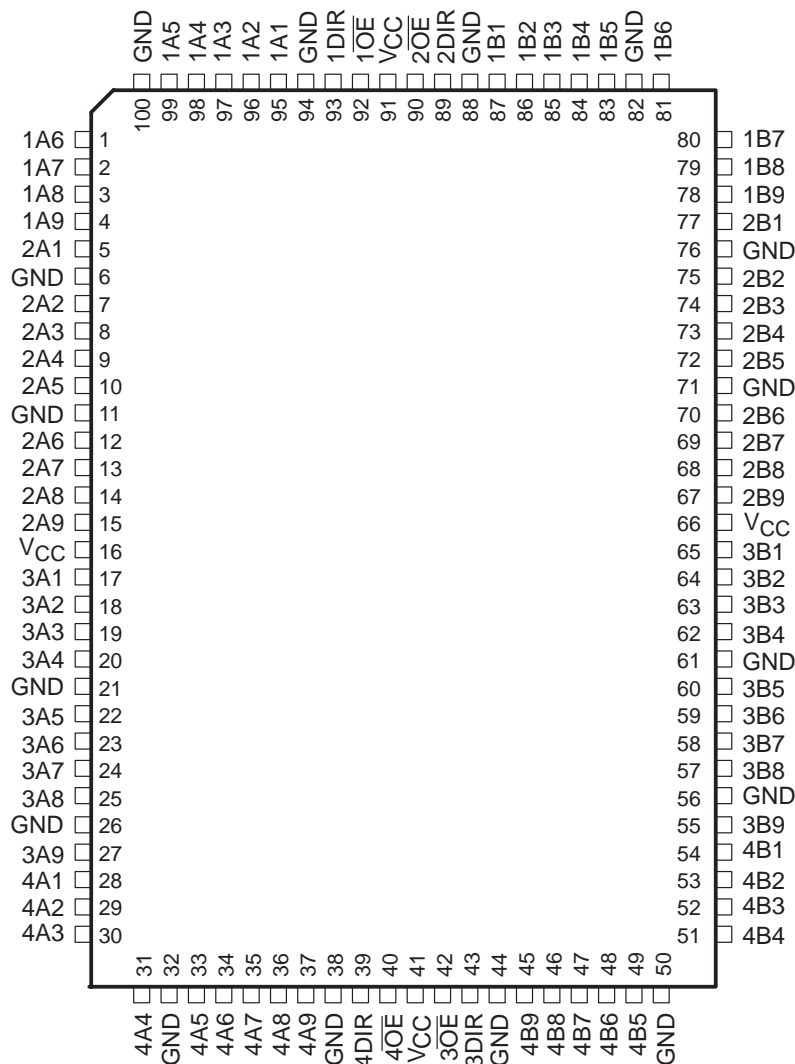
SN54ABTH32245, SN74ABTH32245

36-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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SN54ABTH32245 . . . HS PACKAGE†
(TOP VIEW)



† For HS package availability, please contact the factory or your local TI Field Sales Office.

description

The 'ABTH32245 are 36-bit (quad 9-bit) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as four 9-bit transceivers, two 18-bit transceivers, or one 36-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) inputs. The output-enable (\overline{OE}) inputs can be used to disable the device so that the buses are effectively isolated.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.



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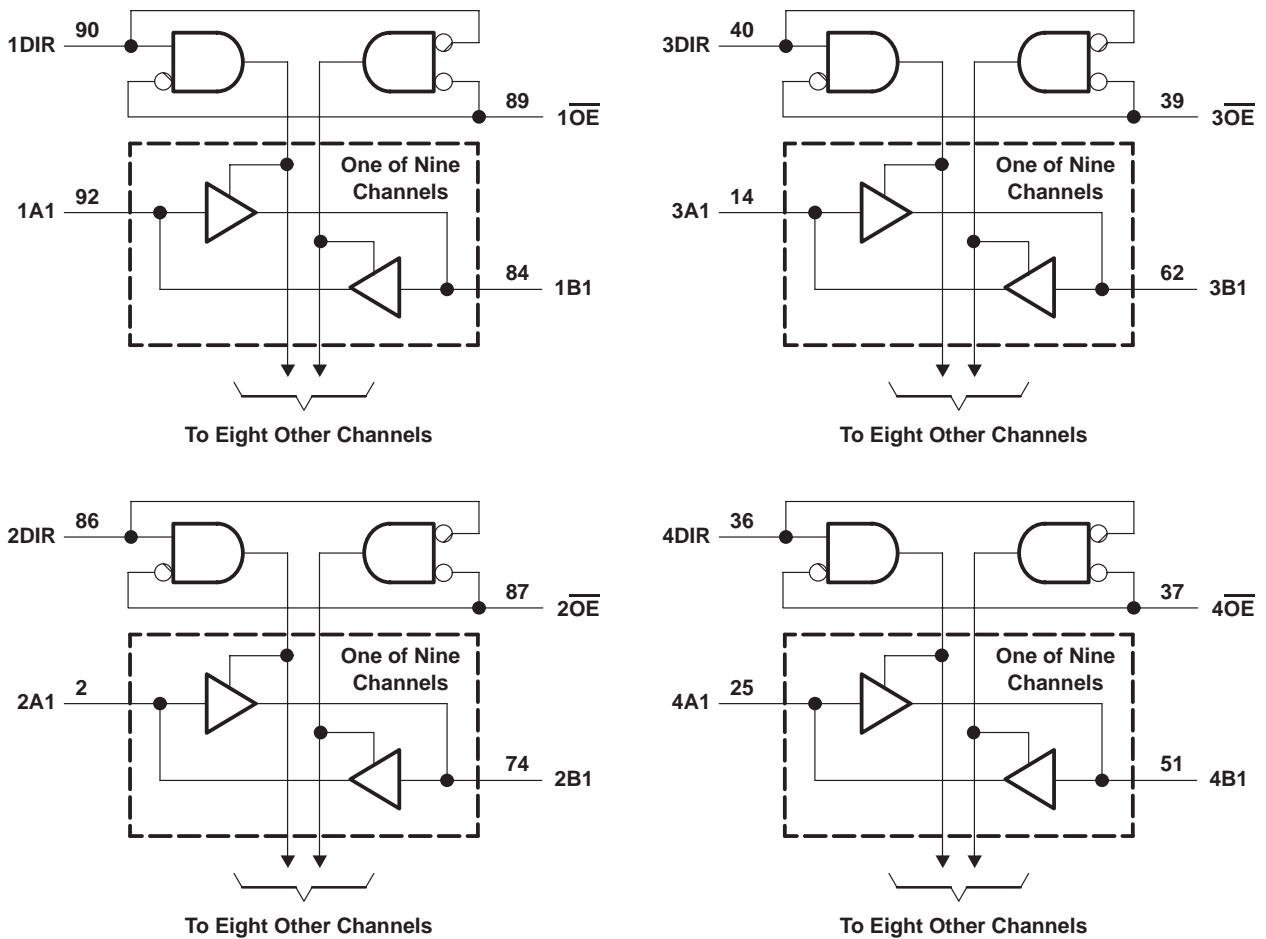
description (continued)

The SN54ABTH32245 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABTH32245 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 9-bit section)

INPUTS		OPERATION
$\overline{\text{OE}}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



Pin numbers shown are for the PZ package.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABTH32245	96 mA
SN74ABTH32245	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): PZ package	50°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

		SN54ABTH32245		SN74ABTH32245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
	Outputs enabled					
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μ s/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused control pins must be held high or low to prevent them from floating.



SN54ABTH32245, SN74ABTH32245
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ABTH32245			SN74ABTH32245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA		-1.2			-1.2			V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = -3 mA		2.5			2.5			V
		V _{CC} = 5 V, I _{OH} = -3 mA		3			3			
		V _{CC} = 4.5 V, I _{OH} = -24 mA		2			2			
V _{OL}		V _{CC} = 4.5 V, I _{OL} = 48 mA		0.55			0.55			V
				I _{OL} = 64 mA					0.55	
V _{hys}				100			100			mV
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND					±1			μA
	A or B ports	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND					±20			
	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND		±1						μA
	A or B ports	V _{CC} = 5.5 V, V _I = V _{CC} or GND		±20						
I _I (hold)	A or B ports	V _{CC} = 4.5 V, V _I = 0.8 V		100			100			μA
		V _{CC} = 4.5 V, V _I = 2 V		-100			-100			
I _{OZPU} ‡		V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$		±50			±50			μA
I _{OZPD} ‡		V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$		±50			±50			μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V					±100			μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V, Outputs high		50			50			μA
I _O §		V _{CC} = 5.5 V, V _O = 2.5 V		-50	-100	-180	-50	-100	-180	mA
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND		Outputs high			3			mA
				Outputs low			20			
				Outputs disabled			2			
ΔI _{CC} ¶		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1			1			mA
C _i	Control inputs	V _I = 2.5 V or 0.5 V		3.5			3.5			pF
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V		9.5			9.5			pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This parameter is specified by characterization.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C#			SN54ABTH32245		SN74ABTH32245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	1.7	3.2	4.4	1	5.3	1.7	5	ns
t _{PHL}			1.7	3.3	4.6	1	5.3	1.7	5.2	
t _{PZH}	\overline{OE}	B or A	1.6	4.2	6.1	1	7.6	1.6	7.3	ns
t _{PZL}			2.7	5.2	7	1.5	8.2	2.7	8.1	
t _{PHZ}	\overline{OE}	B or A	1.3	3.9	6.1	0.8	6.7	1.3	6.5	ns
t _{PLZ}			2	4.4	6.6	1	7.2	2	6.9	

These limits apply only to the SN74ABTH32245



SN54ABTH32245, SN74ABTH32245
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PARAMETER MEASUREMENT INFORMATION

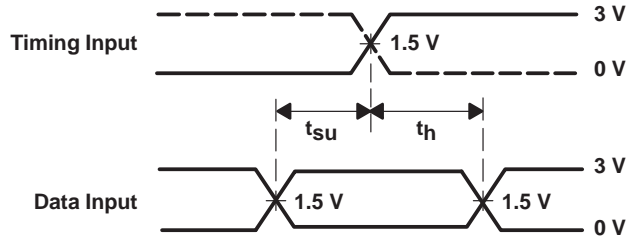


LOAD CIRCUIT

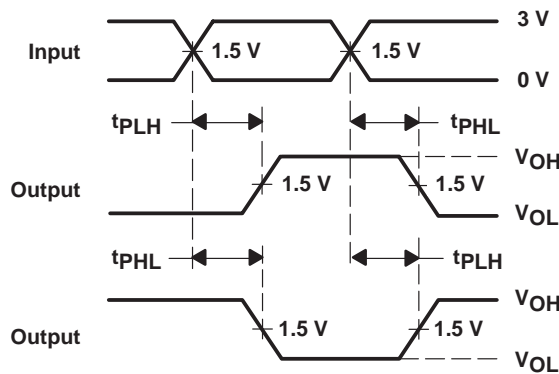
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



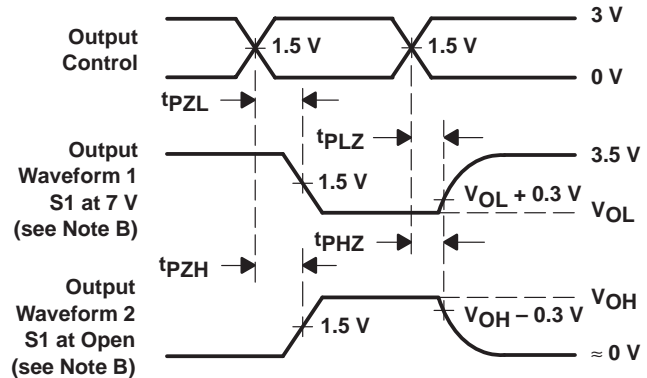
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9557701NXD	Active	Production	LQFP (PZ) 100	90 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	9557701NXD ABTH32245
SN74ABTH32245PZ	Active	Production	LQFP (PZ) 100	90 JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABTH32245

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54ABTH32245, SN74ABTH32245 :

- Catalog : [SN74ABTH32245](#)
- Military : [SN54ABTH32245](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TRAY

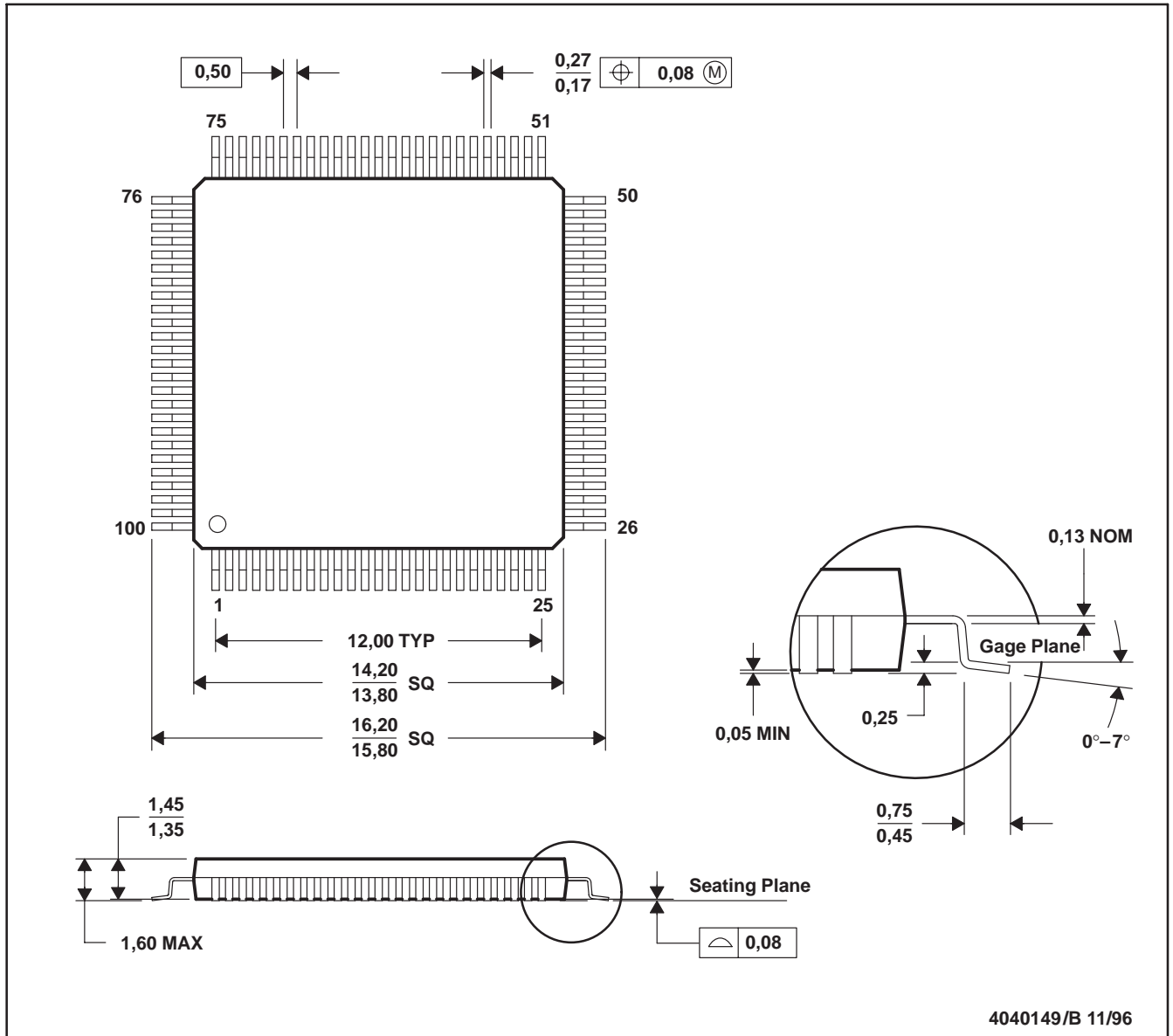

Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
5962-9557701NXD	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
5962-9557701NXD.Z	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
SN74ABTH32245PZ	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
SN74ABTH32245PZ.Z	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45

PZ (S-PQFP-G100)

PLASTIC QUAD FLATPACK

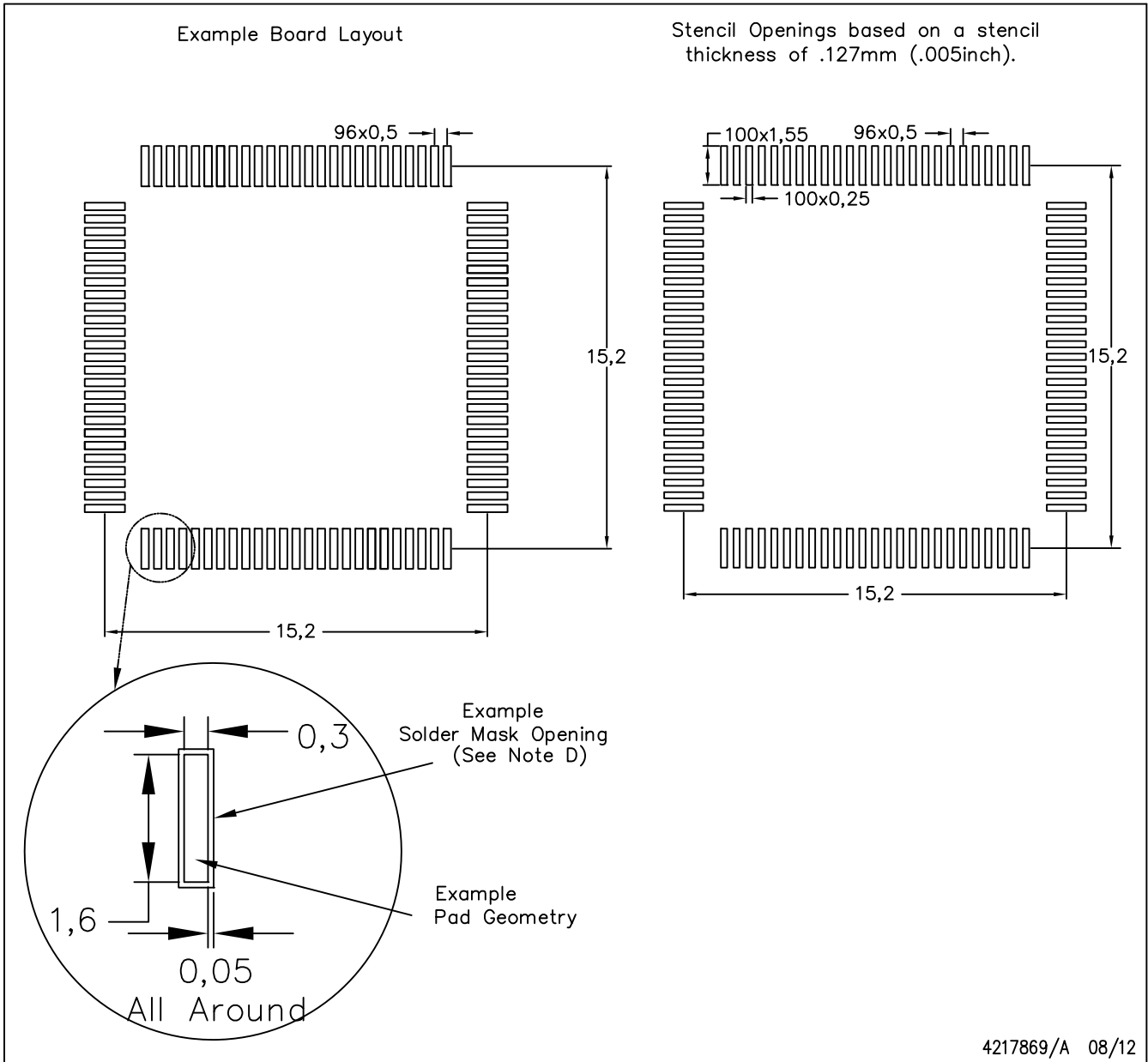


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- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

PZ (S-PQFP-G100)

PLASTIC QUAD FLAT PACK



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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