

## SN74AHC1G00 Single 2-Input Positive-NAND Gate

### 1 Features

- Operating range: 2 V to 5.5 V
- Maximum  $t_{pd}$  of 6.5 ns at 5 V
- Low power consumption: maximum  $I_{CC}$  of 10  $\mu$ A
- $\pm 8$ -mA output drive at 5 V
- Schmitt trigger action at all inputs makes the circuit tolerant for slower input rise and fall time
- Latch-up performance exceeds 250 mA per JESD 17

### 2 Applications

- [Enable or disable a digital signal](#)
- [Controlling an indicator LED](#)
- [Translation between communication modules and system controllers](#)

### 3 Description

The SN74AHC1G00 performs the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

#### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE <sup>(2)</sup>
SN74AHC1G00	DBV (SOT-23, 5)	2.9 mm x 2.8 mm	2.9 mm x 1.6 mm
	DCK (SC-70, 5)	2 mm x 2.1 mm	2 mm x 1.25 mm
	DRL (SOT, 5)	1.6 mm x 1.6 mm	1.6 mm x 1.2 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) The package size (length x width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)



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## 4 Pin Configuration and Functions

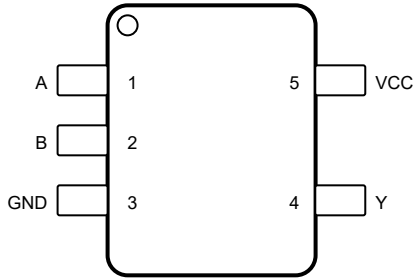


Figure 4-1. DBV Package 5-Pin SOT-23 Top View

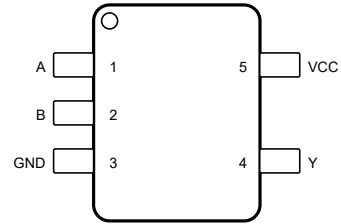


Figure 4-2. DCK Package 5-Pin SC70 Top View

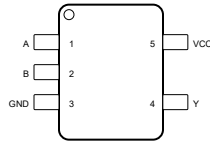


Figure 4-3. DRL Package 5-Pin SOT Top View

Table 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	A	I	A input
2	B	I	B input
3	GND	—	Ground
4	Y	O	Output
5	V <sub>CC</sub>	—	Power

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		-0.5	7	V
V <sub>I</sub> <sup>(2)</sup>	Input voltage		-0.5	7	V
V <sub>O</sub> <sup>(2)</sup>	Output voltage		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	(V <sub>I</sub> < 0)		-20	mA
I <sub>OK</sub>	Output clamp current	(V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )		±20	mA
I <sub>O</sub>	Continuous output current	(V <sub>O</sub> = 0 to V <sub>CC</sub> )		±25	mA
	Continuous current through V <sub>CC</sub> or GND			±50	mA
T <sub>J</sub>	Maximum junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		V
		V <sub>CC</sub> = 3 V	2.1		
		V <sub>CC</sub> = 5.5 V	3.85		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5	V
		V <sub>CC</sub> = 3 V		0.9	
		V <sub>CC</sub> = 5.5 V		1.65	
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		-50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V		-4	
		V <sub>CC</sub> = 5 V ± 0.5 V		-8	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50	μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V		4	
		V <sub>CC</sub> = 5 V ± 0.5 V		8	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V		100	ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V		20	

### 5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
T <sub>A</sub>	Operating free-air temperature	-40	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74AHC1G00			UNIT	
	DBV (SOT-23)	DCK (SC70)	DRL (SOT)		
	5 PINS	5 PINS	5 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	278	289.2	256	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	180.5	205.8	130	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	184.4	176.2	152	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	115.4	117.6	9.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	183.4	175.1	152	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bot) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

### 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER <sup>(1)</sup>	TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OH</sub> High level output voltage	I <sub>OH</sub> = -50 μA	T <sub>A</sub> = 25°C	2 V	1.9	2		V
		T <sub>A</sub> = -40°C to +85°C		1.9			
		T <sub>A</sub> = -40°C to +125°C		1.9			
		T <sub>A</sub> = 25°C	3 V	2.9	3		
		T <sub>A</sub> = -40°C to +85°C		2.9			
		T <sub>A</sub> = -40°C to +125°C		2.9			
		T <sub>A</sub> = 25°C	4.5 V	4.4	4.5		
		T <sub>A</sub> = -40°C to +85°C		4.4			
		T <sub>A</sub> = -40°C to +125°C		4.4			
	I <sub>OH</sub> = -4 mA	T <sub>A</sub> = 25°C	3 V	2.58			
		T <sub>A</sub> = -40°C to +85°C		2.48			
		T <sub>A</sub> = -40°C to +125°C		2.48			
	I <sub>OH</sub> = -8 mA	T <sub>A</sub> = 25°C	4.5 V	3.94			
		T <sub>A</sub> = -40°C to +85°C		3.8			
		T <sub>A</sub> = -40°C to +125°C		3.8			

## 5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER <sup>(1)</sup>		TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 50 μA	T <sub>A</sub> = 25°C	2 V			0.1	V
			T <sub>A</sub> = –40°C to +85°C				0.1	
			T <sub>A</sub> = –40°C to +125°C				0.1	
			T <sub>A</sub> = 25°C	3 V			0.1	
			T <sub>A</sub> = –40°C to +85°C				0.1	
			T <sub>A</sub> = –40°C to +125°C				0.1	
			T <sub>A</sub> = 25°C	4.5 V			0.1	
			T <sub>A</sub> = –40°C to +85°C				0.1	
			T <sub>A</sub> = –40°C to +125°C				0.1	
		I <sub>OL</sub> = 4 mA	T <sub>A</sub> = 25°C	3 V			0.36	
			T <sub>A</sub> = –40°C to +85°C				0.44	
			T <sub>A</sub> = –40°C to +125°C				0.44	
I <sub>OL</sub> = 8 mA	T <sub>A</sub> = 25°C	4.5 V			0.36			
	T <sub>A</sub> = –40°C to +85°C				0.44			
	T <sub>A</sub> = –40°C to +125°C				0.44			
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = 5.5 V or GND	T <sub>A</sub> = 25°C	0 V to 5.5 V			±0.1	μA
			T <sub>A</sub> = –40°C to +85°C				±1	
			T <sub>A</sub> = –40°C to +125°C				±1	
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	T <sub>A</sub> = 25°C	5.5 V			1	μA
			T <sub>A</sub> = –40°C to +85°C				10	
			T <sub>A</sub> = –40°C to +125°C				10	
C <sub>i</sub>	Input Capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND	T <sub>A</sub> = 25°C	5 V		2	10	pF
			T <sub>A</sub> = –40°C to +85°C				10	
			T <sub>A</sub> = –40°C to +125°C				10	

(1) Recommended T<sub>A</sub> = –40°C to +125°C

## 5.6 Switching Characteristics: V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T <sub>A</sub> <sup>(1)</sup>	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF	25°C		5.5	7.9	ns
				–40°C to +85°C	1		9.5	
				–40°C to +125°C	1		10.5	
25°C					5.5	7.9		
–40°C to +85°C				1		9.5		
–40°C to +125°C				1		10.5		
t <sub>PHL</sub>	A or B	Y	C <sub>L</sub> = 50 pF	25°C		8	11.4	ns
				–40°C to +85°C	1		13	
				–40°C to +125°C	1		14	
25°C					8	11.4		
–40°C to +85°C				1		13		
–40°C to +125°C				1		14		

(1) Recommended T<sub>A</sub> = –40°C to +125°C

### 5.7 Switching Characteristics: $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	$T_A$ (1)	MIN	TYP	MAX	UNIT
$t_{PLH}$	A or B	Y	$C_L = 15\text{ pF}$	25°C	3.7	5.5	ns	
				-40°C to +85°C	1	6.5		
				-40°C to +125°C	1	7		
$t_{PHL}$	A or B	Y	$C_L = 15\text{ pF}$	25°C	3.7	5.5	ns	
				-40°C to +85°C	1	6.5		
				-40°C to +125°C	1	7		
$t_{PLH}$	A or B	Y	$C_L = 50\text{ pF}$	25°C	5.2	7.5	ns	
				-40°C to +85°C	1	6.5		
				-40°C to +125°C	1	9		
$t_{PHL}$	A or B	Y	$C_L = 50\text{ pF}$	25°C	5.2	7.5	ns	
				-40°C to +85°C	1	6.5		
				-40°C to +125°C	1	9		

(1) Recommended  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$

### 5.8 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$		9.5		pF

### 5.9 Typical Characteristics

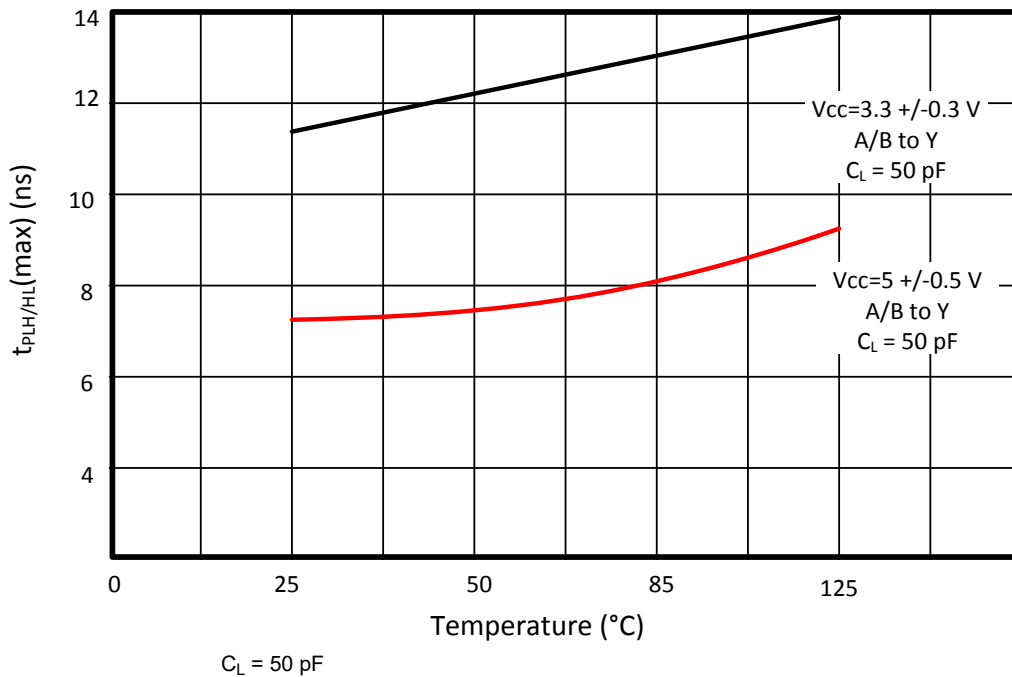
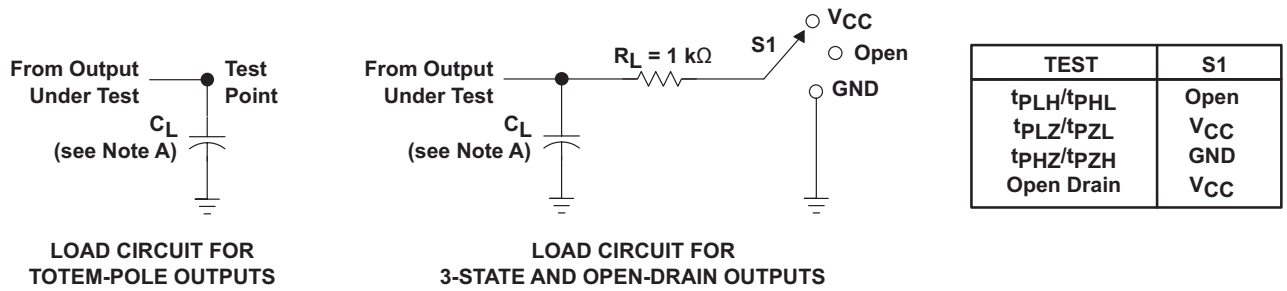


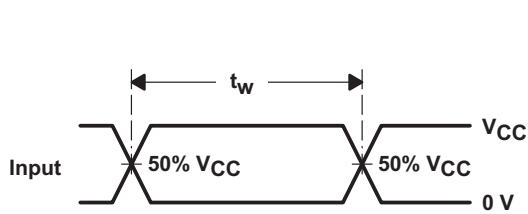
Figure 5-1. Propagation Delay vs Temperature

## 6 Parameter Measurement information

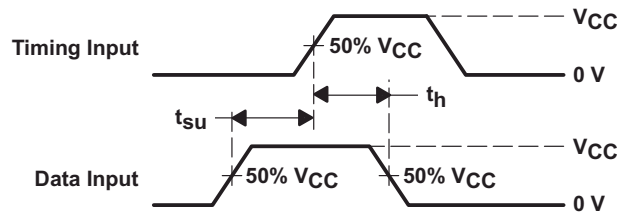


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

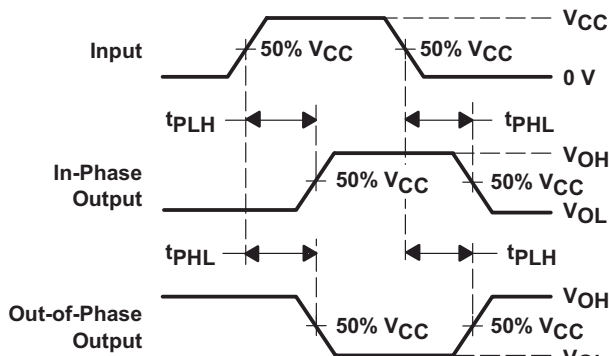
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



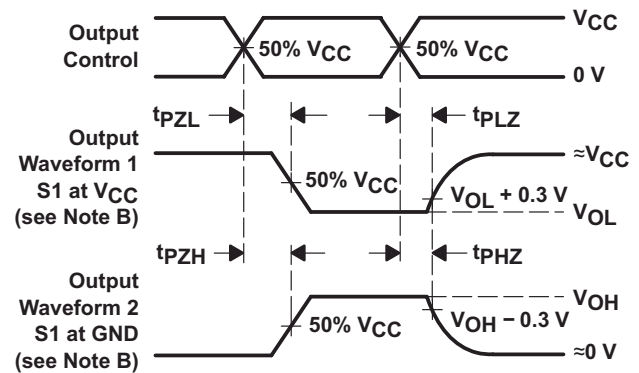
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms



## 7 Detailed Description

### 7.1 Overview

The SN74AHC1G00 device performs the NAND Boolean function  $Y = \overline{A \times B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic. The device has a wide operating range of  $V_{CC}$  from 2 V to 5 V.

### 7.2 Functional Block Diagram



**Figure 7-1. Logic Diagram (Positive Logic)**

### 7.3 Feature Description

The SN74AHC1G00 device has wide operating voltage range for logic system from 2 V to 5 V. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low power consumption of 10- $\mu$ A (maximum) makes this device a good choice for portable and battery power-sensitive applications. The Schmitt trigger action on all inputs have noise rejection capabilities.

### 7.4 Device Functional Modes

**Table 7-1. Function Table**

INPUTS <sup>(1)</sup>		OUTPUT <sup>(2)</sup>
A	B	Y
H	H	L
L	X	H
X	L	H

- (1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care  
 (2) H = Driving High, L = Driving Low, Z = High Impedance State

## 8 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 8.1 Typical Application

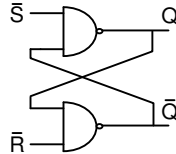


Figure 8-1. Typical Application

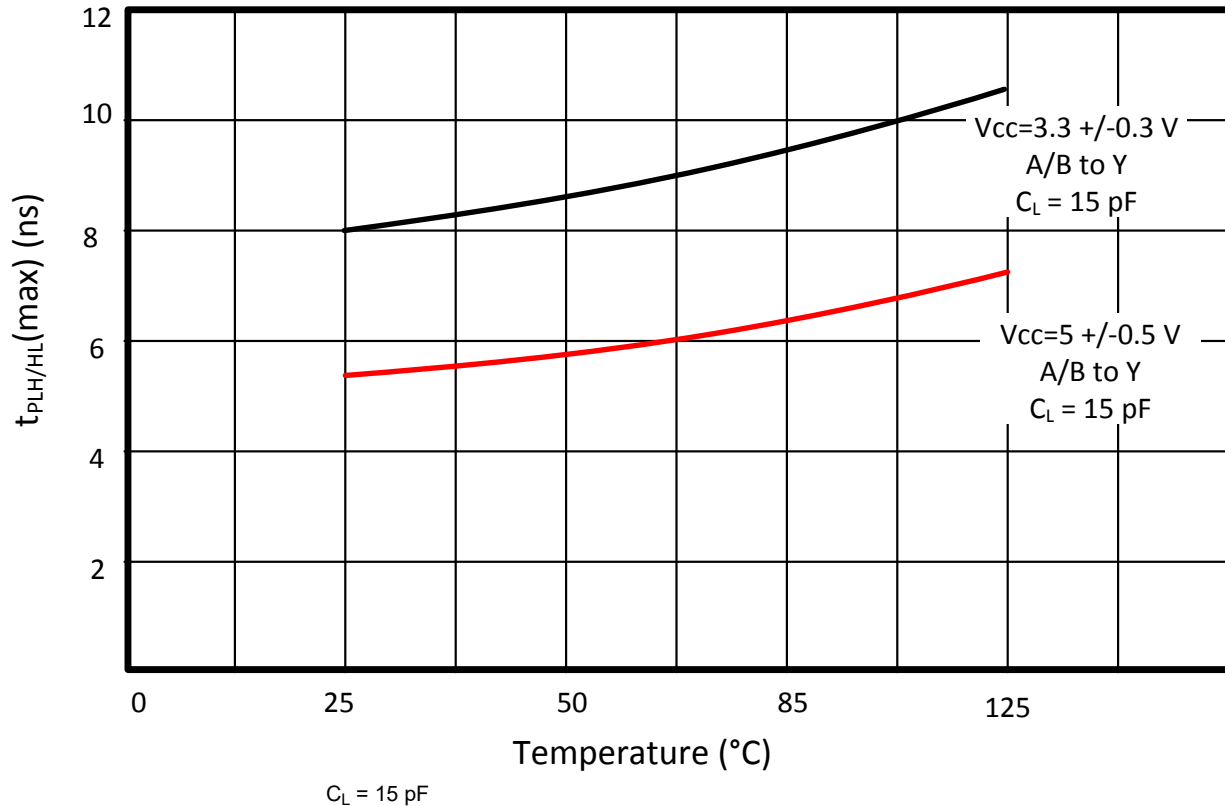
#### 8.1.1 Design Requirements

This SN74AHC1G00 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads. Routing and load conditions must be considered to prevent ringing.

#### 8.1.2 Detailed Design Procedure

- Recommended input conditions:
  - Specified high and low levels. See  $V_{IH}$  and  $V_{IL}$  in [Section 5.3](#).
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
- Recommended output conditions:
  - Load currents must not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

### 8.1.3 Application Curve



**Figure 8-2. Propagation Delay vs Temperature**

### 8.2 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Section 5.3](#).

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- $\mu$ F capacitor; if there are multiple  $V_{CC}$  terminals, then TI recommends a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

## 8.3 Layout

### 8.3.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float.

In many cases, functions or parts of functions of digital logic devices are unused. For example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. The following are the rules must be observed under all circumstances.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the outputs section of the part when asserted. This does not disable the input section of the input and output, so they also cannot float when disabled.

### 8.3.2 Layout Example

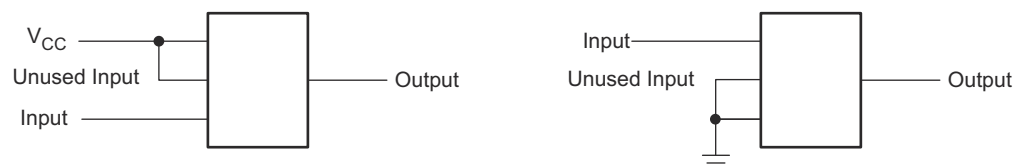


Figure 8-3. Layout Recommendation

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Introduction to Logic application report](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision P (October 2023) to Revision Q (January 2024)</b>	<b>Page</b>
• Updated thermal values for DBV package from R $\theta$ JA = 240 to 278, R $\theta$ JC(top) = 174.5 to 180.5, R $\theta$ JB = 73.7 to 184.4, $\Psi$ JT = 54.9 to 115.4, $\Psi$ JB = 60.1 to 183.4, R $\theta$ JC(bot) = N/A, all values in °C/W .....	5

<b>Changes from Revision O (April 2016) to Revision P (October 2023)</b>	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated thermal values for DCK package from R $\theta$ JA = 276.53 to 289.2, R $\theta$ JC(top) = 118.5 to 205.8, R $\theta$ JB = 62.8 to 176.2, $\Psi$ JT = 6.7 to 117.6, $\Psi$ JB = 62.1 to 175.1, R $\theta$ JC(bot) = N/A, all values in °C/W .....	5

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC1G00DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(35XH, 3BSF, A003, A00G, A00J, A00L, A00S)	Samples
SN74AHC1G00DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A00G	Samples
SN74AHC1G00DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125	(A003, A00G, A00J, A00S)	
SN74AHC1G00DCK3	ACTIVE	SC70	DCK	5	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 125	AA3	Samples
SN74AHC1G00DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	(1QP, AA3, AAG, AAJ, AAL, AAS)	Samples
SN74AHC1G00DCKRE4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA3	Samples
SN74AHC1G00DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA3	Samples
SN74AHC1G00DCKT	OBSOLETE	SC70	DCK	5		TBD	Call TI	Call TI	-40 to 125	(AA3, AAG, AAJ, AAS)	
SN74AHC1G00DCKTG4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA3	Samples
SN74AHC1G00DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(AAB, AAS)	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74AHC1G00 :**

- Automotive : [SN74AHC1G00-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G00DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G00DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G00DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74AHC1G00DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G00DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G00DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G00DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G00DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G00DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74AHC1G00DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G00DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G00DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0

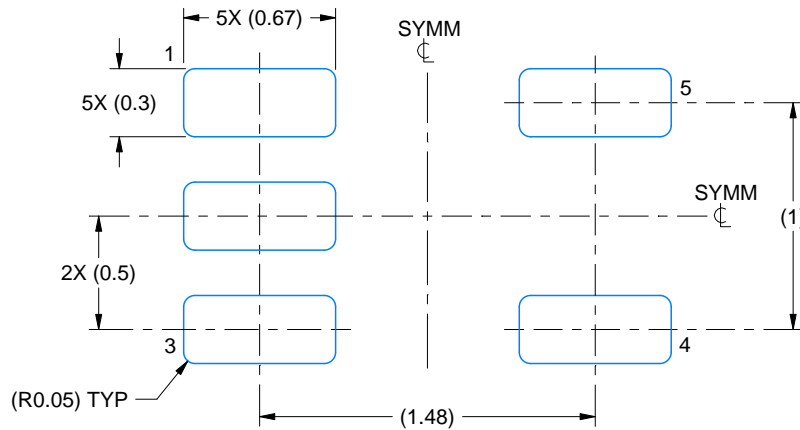


# EXAMPLE BOARD LAYOUT

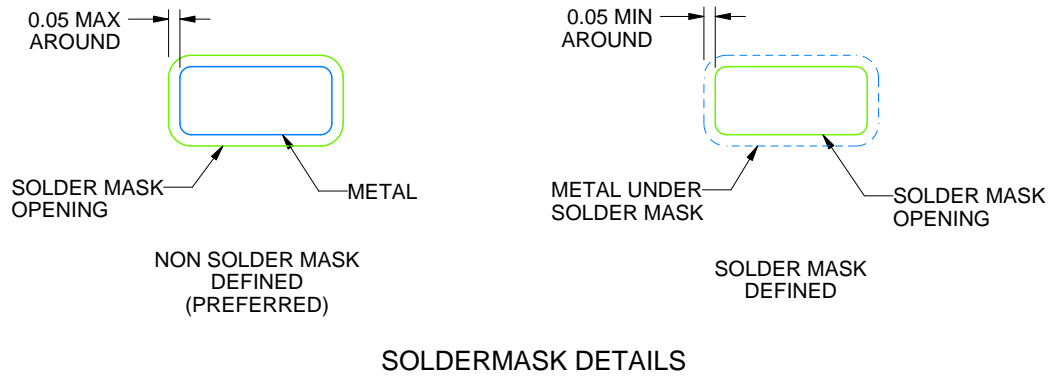
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

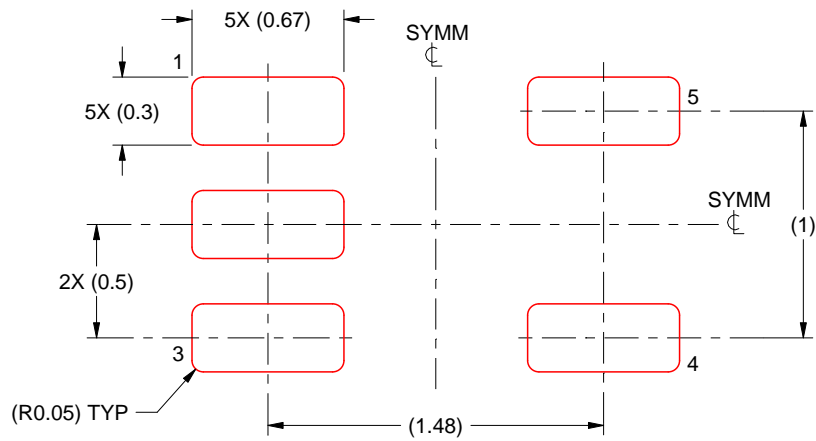
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

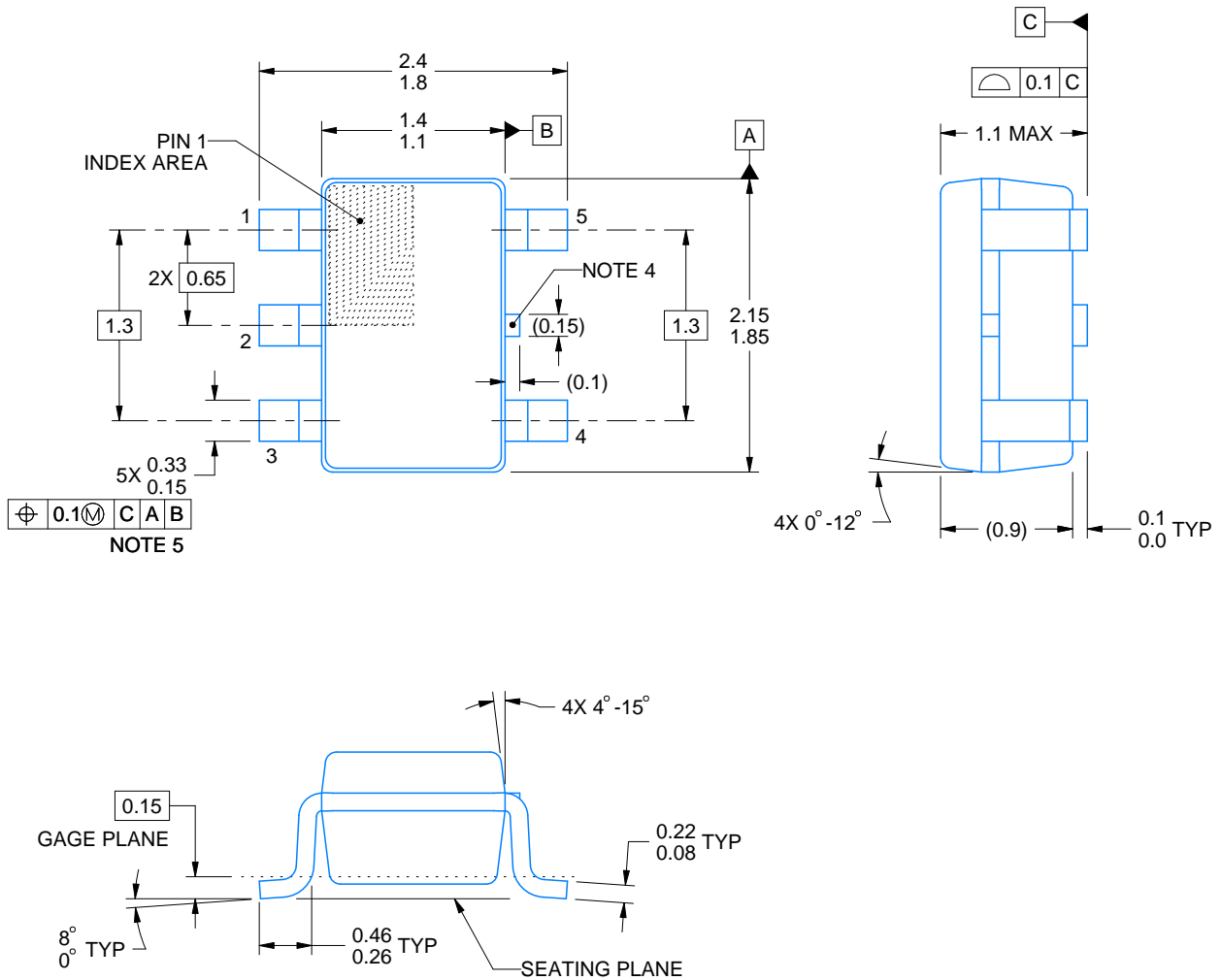
# DCK0005A



# PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE: 18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.





# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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