These edge-triggered multivibrators feature output pulse-duration control by three methods. In the first method, the \( \overline{A} \) input is low, and the \( B \) input goes high. In the second method, the \( B \) input is high, and the \( \overline{A} \) input goes low. In the third method, the \( \overline{A} \) input is low, the \( B \) input is high, and the clear (CLR) input goes high.

The output pulse duration is programmed by selecting external resistance and capacitance values. The external timing capacitor must be connected between \( C_{\text{ext}} \) and \( R_{\text{ext}}/C_{\text{ext}} \) (positive) and an external resistor connected between \( R_{\text{ext}}/C_{\text{ext}} \) and \( V_{CC} \). To obtain variable pulse durations, connect an external variable resistance between \( R_{\text{ext}}/C_{\text{ext}} \) and \( V_{CC} \). The output pulse duration also can be reduced by taking CLR low.

### ORDERING INFORMATION

<table>
<thead>
<tr>
<th>( T_A )</th>
<th>PACKAGE†</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>D, DB, DG, N, OR PW PACKAGE</td>
<td>SN74AHCT123A . . . J OR W PACKAGE</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PDIP – N</td>
<td>SN74AHCT123AN</td>
<td>SN74AHCT123AN</td>
</tr>
<tr>
<td></td>
<td>SOIC – D</td>
<td>SN74AHCT123AD</td>
<td>AHCT123A</td>
</tr>
<tr>
<td></td>
<td>SSOP – DB</td>
<td>SN74AHCT123ADR</td>
<td></td>
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<td></td>
<td>TSSOP – PW</td>
<td>SN74AHCT123APWR</td>
<td>HB123A</td>
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<td></td>
<td>TVSOP – DGV</td>
<td>SN74AHCT123ADGVR</td>
<td>HB123A</td>
</tr>
<tr>
<td></td>
<td>CDIP – J</td>
<td>SNJ54AHCT123AJ</td>
<td>SNJ54AHCT123AJ</td>
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<td></td>
<td>CFP – W</td>
<td>SNJ54AHCT123AW</td>
<td>SNJ54AHCT123AW</td>
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<tr>
<td></td>
<td>LCCC – FK</td>
<td>SNJ54AHCT123AFK</td>
<td>SNJ54AHCT123AFK</td>
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<td>SN74AHCT123DR</td>
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<td>SN74AHCT123AR</td>
<td></td>
</tr>
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<td></td>
<td></td>
<td>SNJ54AHCT123AR</td>
<td></td>
</tr>
</tbody>
</table>

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The \( \overline{A} \), \( B \), and \( CLR \) inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active (\( \overline{A} \)) or high-level-active (\( B \)) input. Pulse duration can be reduced by taking \( CLR \) low. \( CLR \) input can be used to override \( \overline{A} \) or \( B \) inputs. The input/output timing diagram illustrates pulse control by retriggering the inputs and early clearing.

The variance in output pulse duration from device to device typically is less than \( \pm 0.5\% \) for given external timing components. An example of this distribution for the 'AHCT123A is shown in Figure 10. Variations in output pulse duration versus supply voltage and temperature are shown in Figure 6.

During power up, \( Q \) outputs are in the low state, and \( \overline{Q} \) outputs are in the high state. The outputs are glitch free, without applying a reset pulse.

For additional application information on multivibrators, see the application report, *Designing With the SN74AHC123A and SN74AHCT123A*, literature number SCLA014.

### FUNCTION TABLE

(Each multivibrator)

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>A</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>H</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>↓</td>
</tr>
<tr>
<td>↑</td>
<td>L</td>
</tr>
</tbody>
</table>

†These outputs are based on the assumption that the indicated steady-state conditions at the \( \overline{A} \) and \( B \) inputs have been set up long enough to complete any pulse started before the setup.

### Logic Diagram, Each Multivibrator (Positive Logic)

![Logic Diagram](image-url)
absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

- Supply voltage range, $V_{CC}$ (see Note 1) .......................................................... $-0.5 \, \text{V} \text{ to } 7 \, \text{V}$
- Input voltage range, $V_I$ (see Note 2) ................................................................. $-0.5 \, \text{V} \text{ to } 7 \, \text{V}$
- Output voltage range, $V_O$ (see Note 1) ............................................................... $-0.5 \, \text{V} \text{ to } V_{CC} + 0.5 \, \text{V}$
- Input clamp current, $I_{IK}$ ($V_I < 0$) ................................................................. $-20 \, \text{mA}$
- Output clamp current, $I_{OK}$ ($V_O < 0 \text{ or } V_O > V_{CC}$) ........................................ $\pm20 \, \text{mA}$
- Continuous output current, $I_O$ ($V_O = 0 \text{ to } V_{CC}$) ........................................ $\pm25 \, \text{mA}$
- Continuous current through $V_{CC}$ or GND ......................................................... $\pm50 \, \text{mA}$
- Package thermal impedance, $\theta_{JA}$ (see Note 3): D package ................................ $73^\circ\text{C/W}$
- .................................................. DB package ........................................ $82^\circ\text{C/W}$
- .................................................. DGV package ...................................... $120^\circ\text{C/W}$
- .................................................. N package ........................................ $67^\circ\text{C/W}$
- .................................................. PW package ...................................... $108^\circ\text{C/W}$
- Storage temperature range, $T_{stg}$ ........................................................................ $-65^\circ\text{C} \text{ to } 150^\circ\text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to the network ground terminal.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
**SN54AHCT123A, SN74AHCT123A**  
**DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS**  

**SCLS420G – JUNE 1998 – REVISED APRIL 2003**  

---

### recommended operating conditions (see Note 4)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SN54AHCT123A</th>
<th>SN74AHCT123A</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>MIN  MAX</td>
<td>MIN  MAX</td>
</tr>
<tr>
<td>IOL</td>
<td>0.8  0.8 V</td>
<td>0.8  0.8 V</td>
</tr>
<tr>
<td>VIl</td>
<td>–8  –8 mA</td>
<td>–8  –8 mA</td>
</tr>
<tr>
<td>VO</td>
<td>0  V CC</td>
<td>0  V CC</td>
</tr>
<tr>
<td>VOH</td>
<td>4.4  4.5 V</td>
<td>4.4  4.5 V</td>
</tr>
<tr>
<td>VOI</td>
<td>3.94  3.8 V</td>
<td>3.86  3.8 V</td>
</tr>
<tr>
<td>Rext</td>
<td>1k  1k Ω</td>
<td>1k  1k Ω</td>
</tr>
<tr>
<td>TA</td>
<td>–55  125 °C</td>
<td>–40  85 °C</td>
</tr>
</tbody>
</table>

**NOTE 4:** Unused Rext/Cext terminals should be left unconnected. All remaining unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

---

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>VCC</th>
<th>T A  = 25°C</th>
<th>SN54AHCT123A</th>
<th>SN74AHCT123A</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOH</td>
<td>IOH = –50 μA</td>
<td>4.5 V</td>
<td>4.4  4.5 V</td>
<td>4.4  4.4 V</td>
<td>4.4  4.4 V</td>
<td>V</td>
</tr>
<tr>
<td>VOL</td>
<td>IOL = 50 μA</td>
<td>4.5 V</td>
<td>0.1  0.1 V</td>
<td>0.1  0.1 V</td>
<td>0.1  0.1 V</td>
<td>V</td>
</tr>
<tr>
<td>Rext/Cext</td>
<td>Vl = VCC or GND</td>
<td>5.5 V</td>
<td>±0.25  ±0.25 V</td>
<td>±0.25  ±0.25 V</td>
<td>±0.25  ±0.25 V</td>
<td>V</td>
</tr>
<tr>
<td>ICC</td>
<td>VI = VCC or GND</td>
<td>5 V</td>
<td>4  40 μA</td>
<td>4  40 μA</td>
<td>4  40 μA</td>
<td>μA</td>
</tr>
<tr>
<td>ICC</td>
<td>VI = 0.5 V CC</td>
<td>5.5 V</td>
<td>560  750 μA</td>
<td>975  975 μA</td>
<td>975  975 μA</td>
<td>μA</td>
</tr>
<tr>
<td>AICC</td>
<td>One input at 3.4 V</td>
<td>5.5 V</td>
<td>1.35  1.5 mA</td>
<td>1.35  1.5 mA</td>
<td>1.35  1.5 mA</td>
<td>mA</td>
</tr>
<tr>
<td>Ci</td>
<td>VI = VCC or GND</td>
<td>5 V</td>
<td>1.9  10 pF</td>
<td>10  10 pF</td>
<td>10  10 pF</td>
<td>pF</td>
</tr>
</tbody>
</table>

* On products compliant to MIL-PRF-38535, this parameter is not production tested at VCC = 0 V.
† This test is performed with the terminal in the off-state condition.
‡ This is the change in supply current for each input at one of the specified TTL voltage levels rather than 0 V or VCC.

---

### timing requirements over recommended operating free-air temperature range, VCC = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

<table>
<thead>
<tr>
<th>TEST CONDITIONS</th>
<th>T A  = 25°C</th>
<th>SN54AHCT123A</th>
<th>SN74AHCT123A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tw</td>
<td>50  50 ns</td>
<td>50  50 ns</td>
<td>50  50 ns</td>
</tr>
<tr>
<td>Tr</td>
<td>50  50 ns</td>
<td>50  50 ns</td>
<td>50  50 ns</td>
</tr>
</tbody>
</table>

§ See retriggering data in the application information section.
switching characteristics over recommended operating free-air temperature range, 
\( V_{CC} = 5 \, \text{V} \pm 0.5 \, \text{V} \) (unless otherwise noted) (see Figure 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
<th>( T_A = 25^\circ \text{C} )</th>
<th>SN54AHCT123A</th>
<th>SN74AHCT123A</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPLH</td>
<td>A or B</td>
<td>Q or ( \overline{Q} )</td>
<td>( C_L = 15 , \text{pF} )</td>
<td>5.3* 10*</td>
<td>1* 13*</td>
<td>1 11</td>
<td>ns</td>
</tr>
<tr>
<td>tPLH</td>
<td>CLR</td>
<td>Q or ( \overline{Q} )</td>
<td>( C_L = 15 , \text{pF} )</td>
<td>7.7* 12*</td>
<td>1* 15*</td>
<td>1 13</td>
<td>ns</td>
</tr>
<tr>
<td>tPLH</td>
<td>CLR trigger</td>
<td>Q or ( \overline{Q} )</td>
<td>( C_L = 15 , \text{pF} )</td>
<td>8* 13*</td>
<td>1* 16*</td>
<td>1 14</td>
<td>ns</td>
</tr>
<tr>
<td>tPLH</td>
<td>A or B</td>
<td>Q or ( \overline{Q} )</td>
<td>( C_L = 50 , \text{pF} )</td>
<td>6.8 11</td>
<td>1 14</td>
<td>1 12</td>
<td>ns</td>
</tr>
<tr>
<td>tPLH</td>
<td>CLR</td>
<td>Q or ( \overline{Q} )</td>
<td>( C_L = 50 , \text{pF} )</td>
<td>9.2 13</td>
<td>1 16</td>
<td>1 14</td>
<td>ns</td>
</tr>
<tr>
<td>tPLH</td>
<td>CLR trigger</td>
<td>Q or ( \overline{Q} )</td>
<td>( C_L = 50 , \text{pF} )</td>
<td>9.5 14</td>
<td>1 17</td>
<td>1 15</td>
<td>ns</td>
</tr>
</tbody>
</table>

\( t_w^\dagger \) | Q or \( \overline{Q} \) | \( C_L = 50 \, \text{pF}, \) \( C_{ext} = 28 \, \text{pF}, R_{ext} = 2 \, \text{k}\Omega \) | 133 200 | 240 | 240 | ns |
| \( t_w^\dagger \) | Q or \( \overline{Q} \) | \( C_L = 50 \, \text{pF}, \) \( C_{ext} = 0.01 \, \text{\mu F}, R_{ext} = 10 \, \text{k}\Omega \) | 90 100 110 | 90 110 90 | 110 | \mu s |
| \( \Delta t_w^\ddagger \) | Q or \( \overline{Q} \) | \( C_L = 50 \, \text{pF}, \) \( C_{ext} = 0.1 \, \text{\mu F}, R_{ext} = 10 \, \text{k}\Omega \) | 0.9 1 1.1 | 0.9 1.1 0.9 | 1.1 | ms |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† \( t_w \) = Pulse duration at Q and \( \overline{Q} \) outputs
‡ \( \Delta t_w \) = Output pulse-duration variation (Q and \( \overline{Q} \)) between circuits in same package

**operating characteristics, \( V_{CC} = 5 \, \text{V}, \ T_A = 25^\circ \text{C} \)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TYP</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{pd} )</td>
<td>Power dissipation capacitance</td>
<td>No load</td>
<td>29</td>
</tr>
</tbody>
</table>
PARAMETER MEASUREMENT INFORMATION

NOTES: A. C\textsubscript{L} includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: Z\textsubscript{O} = 50 \, \Omega, t\textsubscript{r} = 3 \, ns, t\textsubscript{f} = 3 \, ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms
APPLICATION INFORMATION

cautions in use

To prevent malfunctions due to noise, connect a high-frequency capacitor between VCC and GND, and keep the wiring between the external components and Cext and Rext/Cext terminals as short as possible.

power-down considerations

Large values of Cext may cause problems when powering down the ‘AHCT123A devices because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from VCC through the protection diodes at pin 2 or pin 14. Current through the input protection diodes must be limited to 30 mA; therefore, the turn-off time of the VCC power supply must not be faster than \( t = \frac{VCC \times Cext}{30 \text{ mA}} \). For example, if \( VCC = 5 \text{ V} \) and \( Cext = 15 \text{ pF} \), the VCC supply must turn off no faster than \( t = \frac{(5 \text{ V}) \times (15 \text{ pF})}{30 \text{ mA}} = 2.5 \text{ ns} \). Usually, this is not a problem because power supplies are heavily filtered and cannot discharge at this rate. When a more rapid decrease of VCC to zero occurs, the ‘AHCT123A devices may sustain damage. To avoid this possibility, use external clamping diodes.

output pulse duration

The output pulse duration, \( t_w \), is determined primarily by the values of the external capacitance (\( C_T \)) and timing resistance (\( R_T \)). The timing components are connected as shown in Figure 2.

![Figure 2. Timing-Component Connections](image)

The pulse duration is given by:

\[
t_w = K \times R_T \times C_T
\]

if \( C_T \geq 1000 \text{ pF} \), \( K = 1.0 \) or

if \( C_T < 1000 \text{ pF} \), \( K \) can be determined from Figure 5

where:

\( t_w = \) pulse duration in ns

\( R_T = \) external timing resistance in kΩ

\( C_T = \) external capacitance in pF

\( K = \) multiplier factor

Equation 1 and Figure 3 can be used to determine values for pulse duration, external resistance, and external capacitance.
APPLICATION INFORMATION

detriggering data

The minimum input retriggering time \( t_{\text{MIR}} \) is the minimum time required after the initial signal before retriggering the input. After \( t_{\text{MIR}} \), the device retriggers the output. Experimentally, it also can be shown that to retrigger the output pulse, the two adjacent input signals should be \( t_{\text{MIR}} \) apart, where \( t_{\text{MIR}} = 0.30 \times t_{w} \). The retrigger pulse duration is calculated as shown in Figure 3.

\[
\begin{align*}
  t_{\text{RT}} &= t_{w} + t_{\text{PLH}} = (K \times R_T \times C_T) + t_{\text{PLH}} \\
  \text{Where:} & \\
  t_{\text{MIR}} &= \text{Minimum Input Retriggering Time} \\
  t_{\text{PLH}} &= \text{Propagation Delay} \\
  t_{\text{RT}} &= \text{Retrigger Time} \\
  t_{w} &= \text{Output Pulse Duration Before Retriggering}
\end{align*}
\]

Figure 3. Retrigger Pulse Duration

The minimum value from the end of the input pulse to the beginning of the retriggered output should be approximately 15 ns to ensure a retriggered output (see Figure 4).

\[
\begin{align*}
  t_{\text{MRT}} &= \text{Minimum Time Between the End of the Second Input Pulse and the Beginning of the Retriggered Output} \\
  t_{\text{MRT}} &= 15 \text{ ns}
\end{align*}
\]

Figure 4. Input/Output Requirements
APPLICATION INFORMATION†

Figure 5. Output Pulse Duration vs External Timing Capacitance

Figure 6. Variations in Output Pulse Duration vs Temperature

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.
APPLICATION INFORMATION†

**MINIMUM TRIGGER TIME**

**vs**

**VCC CHARACTERISTICS**

![Figure 7](image)

**OUTPUT PULSE-DURATION CONSTANT**

**vs**

**SUPPLY VOLTAGE**

![Figure 8](image)

**EXTERNAL CAPACITANCE**

**vs**

**MULTIPLIER FACTOR**

![Figure 9](image)

**DISTRIBUTION OF UNITS**

**vs**

**OUTPUT PULSE DURATION**

![Figure 10](image)

†Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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<tbody>
<tr>
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<td>ACTIVE</td>
<td>LCCC</td>
<td>FK</td>
<td>20</td>
<td>1</td>
<td>TBD</td>
<td>POST-PLATE</td>
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<td>5962-9861601Q2A</td>
<td>Samples</td>
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<tr>
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<td>CDIP</td>
<td>J</td>
<td>16</td>
<td>1</td>
<td>TBD</td>
<td>A42</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>5962-9861601QE</td>
<td>Samples</td>
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<tr>
<td>5962-9861601QFA</td>
<td>ACTIVE</td>
<td>CFP</td>
<td>W</td>
<td>16</td>
<td>1</td>
<td>TBD</td>
<td>A42</td>
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<td>5962-9861601QF</td>
<td>Samples</td>
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<td>SN74AHCT123AD</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>AHCT123A</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74AHCT123ADBR</td>
<td>ACTIVE</td>
<td>SSOP</td>
<td>DB</td>
<td>16</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>HB123A</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74AHCT123ADGVR</td>
<td>ACTIVE</td>
<td>TVSOP</td>
<td>DGV</td>
<td>16</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>HB123A</td>
<td>Samples</td>
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<tr>
<td>SN74AHCT123ADR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>AHCT123A</td>
<td>Samples</td>
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<td>PDIP</td>
<td>N</td>
<td>16</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>-40 to 85</td>
<td>SN74AHCT123AN</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74AHCT123APWR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>HB123A</td>
<td>Samples</td>
</tr>
<tr>
<td>SNJ54AHCT123AFK</td>
<td>ACTIVE</td>
<td>LCCC</td>
<td>FK</td>
<td>20</td>
<td>1</td>
<td>TBD</td>
<td>POST-PLATE</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>5962-9861601Q2A</td>
<td>Samples</td>
</tr>
<tr>
<td>SNJ54AHCT123AJ</td>
<td>ACTIVE</td>
<td>CDIP</td>
<td>J</td>
<td>16</td>
<td>1</td>
<td>TBD</td>
<td>A42</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>5962-9861601QE</td>
<td>Samples</td>
</tr>
<tr>
<td>SNJ54AHCT123AW</td>
<td>ACTIVE</td>
<td>CFP</td>
<td>W</td>
<td>16</td>
<td>1</td>
<td>TBD</td>
<td>A42</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>5962-9861601QF</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHCT123A, SN74AHCT123A:

- Catalog: SN74AHCT123A
- Military: SN54AHCT123A

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
Military - QML certified for Military and Defense Applications
TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W  (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74AHCT123ADGVR</td>
<td>TVSOP</td>
<td>DGV</td>
<td>16</td>
<td>2000</td>
<td>330.0</td>
<td>12.4</td>
<td>6.8</td>
<td>4.0</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>SN74AHCT123ADR</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>330.0</td>
<td>16.4</td>
<td>6.5</td>
<td>10.3</td>
<td>2.1</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>SN74AHCT123 APWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>2000</td>
<td>330.0</td>
<td>12.4</td>
<td>6.9</td>
<td>5.6</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*

** TAPE DIMENSIONS **

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

** REEL DIMENSIONS **

- Reel Diameter
- Reel Width W1

** QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE **

- Q1
- Q2
- Q3
- Q4

- Sprocket Holes
- User Direction of Feed

- Pocket Quadrants

[www.ti.com 20-Dec-2018]
### TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74AHCT123ADGVR</td>
<td>TVSOP</td>
<td>DGV</td>
<td>16</td>
<td>2000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>SN74AHCT123ADR</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>333.2</td>
<td>345.9</td>
<td>28.6</td>
</tr>
<tr>
<td>SN74AHCT123APWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>2000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
**NOTES:**

A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS-004
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AC.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
   14/16/20/56 Pins – MO-194
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16
J (R-GDIP-T**)  
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE

<table>
<thead>
<tr>
<th>PINS **</th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.300 (7.62)</td>
<td>0.300 (7.62)</td>
<td>0.300 (7.62)</td>
<td>0.300 (7.62)</td>
</tr>
<tr>
<td>B MAX</td>
<td>0.785 (19.94)</td>
<td>.840 (21.34)</td>
<td>.960 (24.38)</td>
<td>1.060 (26.92)</td>
</tr>
<tr>
<td>B MIN</td>
<td>——</td>
<td>——</td>
<td>——</td>
<td>——</td>
</tr>
<tr>
<td>C MAX</td>
<td>0.300 (7.62)</td>
<td>0.300 (7.62)</td>
<td>0.310 (7.87)</td>
<td>0.300 (7.62)</td>
</tr>
<tr>
<td>C MIN</td>
<td>0.245 (6.22)</td>
<td>0.245 (6.22)</td>
<td>0.220 (5.59)</td>
<td>0.245 (6.22)</td>
</tr>
</tbody>
</table>

NOTES:  
A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
D. Falls within JEDEC MO-150

<table>
<thead>
<tr>
<th>DIM</th>
<th>14</th>
<th>16</th>
<th>20</th>
<th>24</th>
<th>28</th>
<th>30</th>
<th>38</th>
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</thead>
<tbody>
<tr>
<td>A MAX</td>
<td>6.50</td>
<td>6.50</td>
<td>7.50</td>
<td>8.50</td>
<td>10.50</td>
<td>10.50</td>
<td>12.90</td>
</tr>
<tr>
<td>A MIN</td>
<td>5.90</td>
<td>5.90</td>
<td>6.90</td>
<td>7.90</td>
<td>9.90</td>
<td>9.90</td>
<td>12.30</td>
</tr>
</tbody>
</table>
**N (R—PDIP—T**)**

**PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN

<table>
<thead>
<tr>
<th>DIM</th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>A MAX</td>
<td>0.775 (19.69)</td>
<td>0.775 (19.69)</td>
<td>0.920 (23.37)</td>
<td>1.060 (26.92)</td>
</tr>
<tr>
<td>A MIN</td>
<td>0.745 (18.92)</td>
<td>0.745 (18.92)</td>
<td>0.850 (21.59)</td>
<td>0.940 (23.88)</td>
</tr>
</tbody>
</table>

MS—001 VARIATION

A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS—001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

14/18 Pin Only
20 Pin vendor option

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