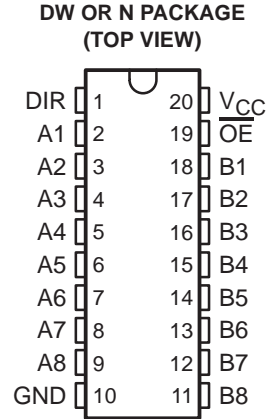


# SN74ALS1640A, SN74ALS1645A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDAS246B – DECEMBER 1982 – REVISED FEBRUARY 1997

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Lower-Power Versions of SN74ALS640B and SN74ALS645A
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs



## description

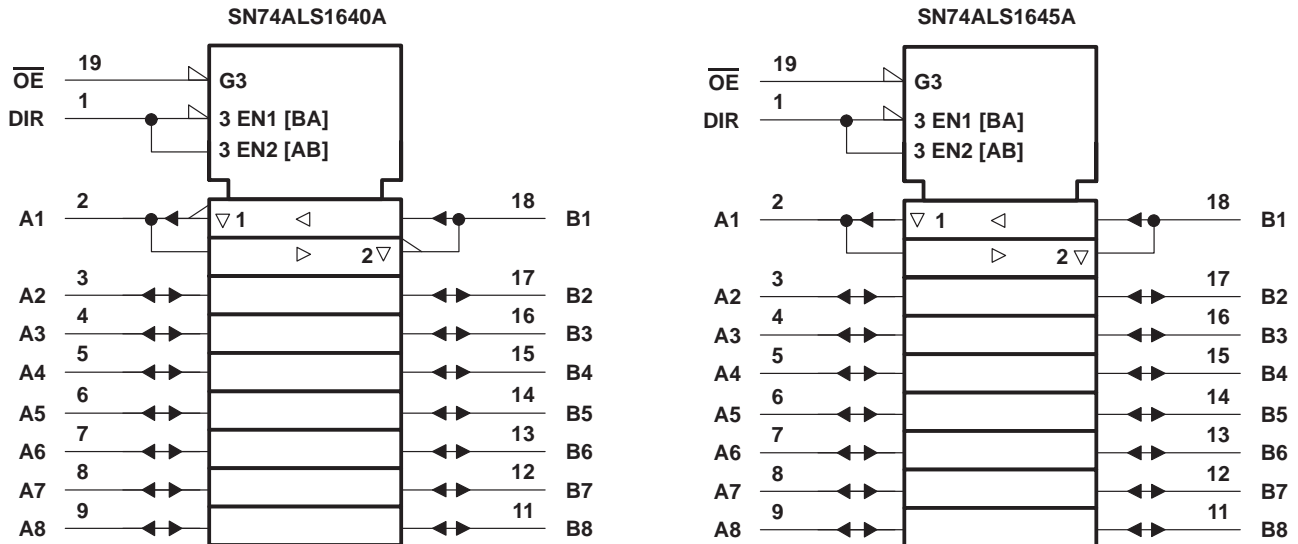
These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated. The SN74ALS1640A features inverting logic, while the SN74ALS1645A features noninverting logic.

The SN74ALS1640A and SN74ALS1645A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		OPERATION	
$\overline{OE}$	DIR	SN74ALS1640A	SN74ALS1645A
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

## logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

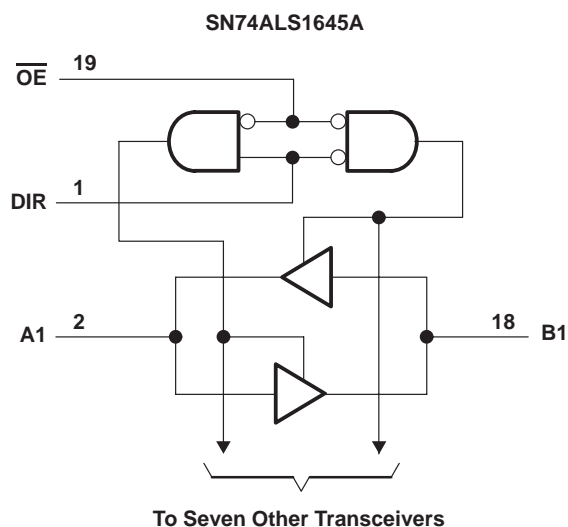
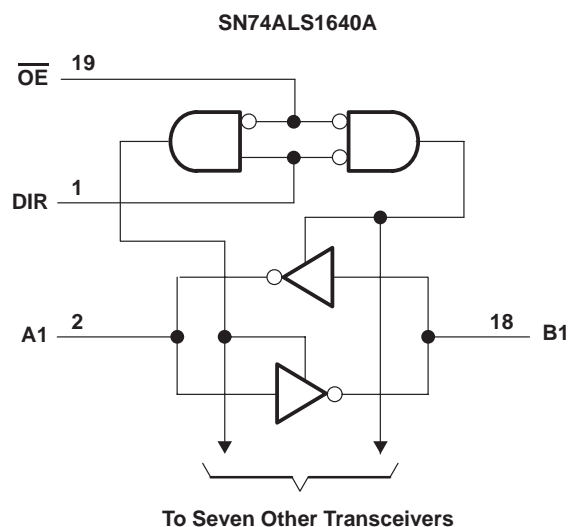
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# SN74ALS1640A, SN74ALS1645A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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## logic diagrams (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ : All inputs .....	7 V
I/O ports .....	5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 1): DW package .....	97°C/W
N package .....	67°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions

		SN74ALS1640A SN74ALS1645A			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current			-15	mA
$I_{OL}$	Low-level output current			16	mA
$T_A$	Operating free-air temperature	0	70		°C

# SN74ALS1640A, SN74ALS1645A OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	SN74ALS1640A SN74ALS1645A		UNIT
			MIN	TYP†	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$	-1.5		V
$V_{OH}$		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$	$V_{CC}-2$		V
		$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$	2.4	3.2	
		$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -15\text{ mA}$	2		
$V_{OL}$		$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 8\text{ mA}$	0.25	0.4	V
		$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 16\text{ mA}$	0.35	0.5	
$I_I$	Control inputs	$V_{CC} = 5.5\text{ V}$	$V_I = 7\text{ V}$		mA
	A or B ports		$V_I = 5.5\text{ V}$		
$I_{IH}$	Control inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$	20		$\mu\text{A}$
	A or B ports‡		20		
$I_{IL}$	Control inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$	-0.1		mA
	A or B ports‡		-0.1		
$I_O§$		$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	-30	-112	mA
$I_{CC}$	SN74ALS1640A	$V_{CC} = 5.5\text{ V}$	18	32	mA
	SN74ALS1645A	$V_{CC} = 5.5\text{ V}$	25	38	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current,  $I_{OS}$ .

## switching characteristics (see Figure 1)

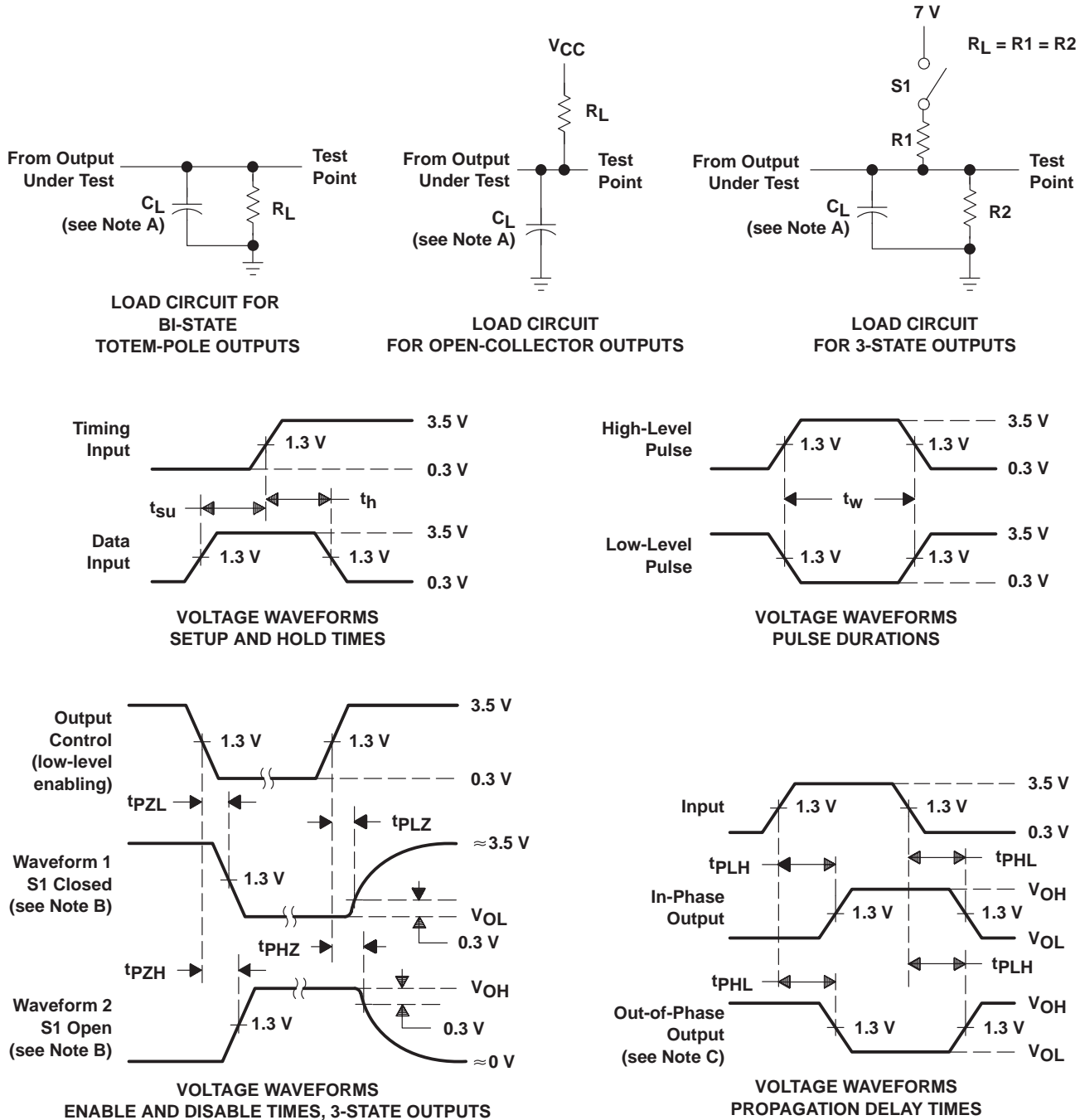
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_1 = 500\ \Omega$ , $R_2 = 500\ \Omega$ , $T_A = \text{MIN to MAX}\ddagger$				UNIT
			SN74ALS1640A		SN74ALS1645A		
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	4	15	2	13	ns
$t_{PHL}$			2	10	2	13	
$t_{PZH}$	$\overline{OE}$	A or B	5	20	8	25	ns
$t_{PZL}$			5	22	8	25	
$t_{PHZ}$	$\overline{OE}$	A or B	2	10	2	12	ns
$t_{PLZ}$			5	13	3	18	

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN74ALS1640A, SN74ALS1645A**  
**OCTAL BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

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**PARAMETER MEASUREMENT INFORMATION**  
**SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS1645AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS1645AN	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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