

SN54ALS191A, SN74ALS191A SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

SDAS210C – DECEMBER 1982 – REVISED JULY 1996

- Single Down/Up Count-Control Line
- Look-Ahead Circuitry Enhances Speed of Cascaded Counters
- Fully Synchronous in Count Modes
- Asynchronously Presetable With Load Control
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

The 'ALS191A are synchronous 4-bit reversible up/down binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

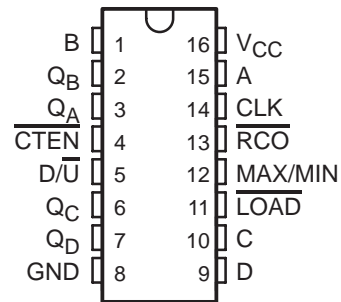
The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock (CLK) input if the count enable ($\overline{\text{CTEN}}$) input is low. A high at $\overline{\text{CTEN}}$ inhibits counting. The direction of the count is determined by the level of the down/up ($\overline{\text{D/U}}$) input. When $\overline{\text{D/U}}$ is low, the counter counts up, and when $\overline{\text{D/U}}$ is high, the counter counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{\text{CTEN}}$ and $\overline{\text{D/U}}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter is dictated solely by the conditions meeting the stable setup and hold times.

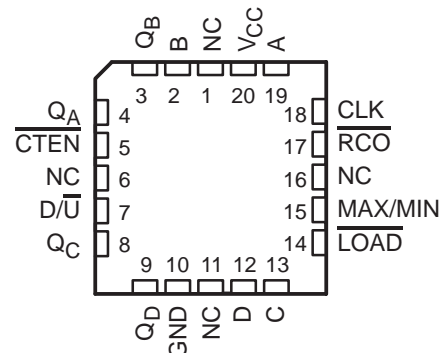
These counters are fully programmable. Each output can be preset to either level by placing a low on the $\overline{\text{LOAD}}$ input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

CLK, $\overline{\text{D/U}}$, and $\overline{\text{LOAD}}$ are buffered to lower the drive requirement, which significantly reduces the loading on (current required by) clock drivers, for long parallel words.

SN54ALS191A . . . J PACKAGE
SN74ALS191A . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS191A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN54ALS191A, SN74ALS191A SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS

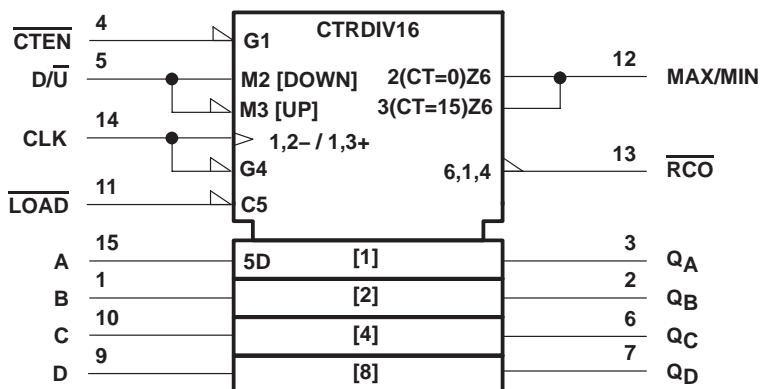
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description (continued)

Two outputs are available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is minimum (0) counting down or maximum (15) counting up. The ripple-clock output (\overline{RCO}) produces a low-level output pulse under those same conditions, but only while the clock input is low. The counter easily can be cascaded by feeding the ripple-clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count (MAX/MIN) output can be used to accomplish look ahead for high-speed operation.

The SN54ALS191A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS191A is characterized for operation from 0°C to 70°C .

logic symbol†

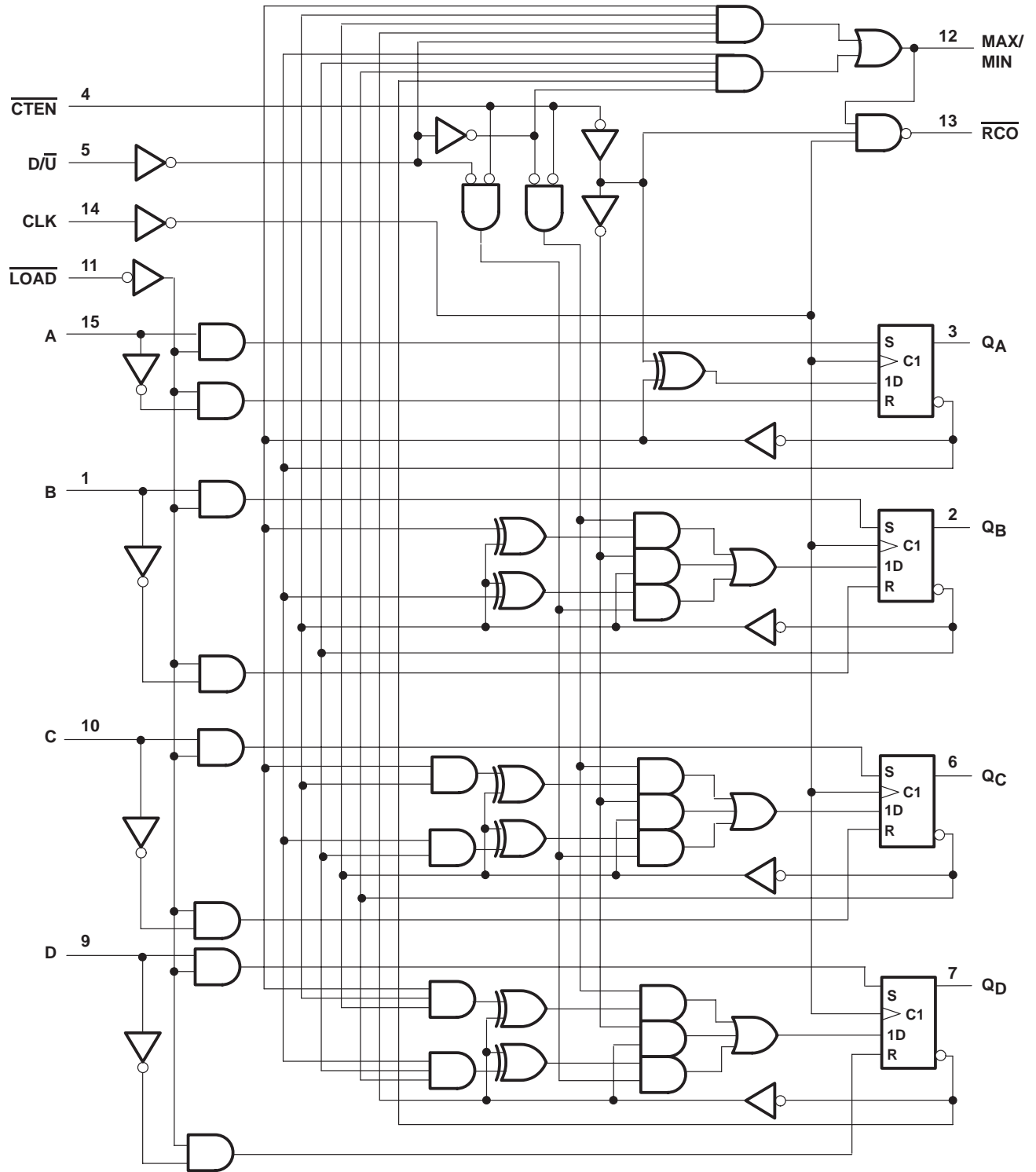


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

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logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.



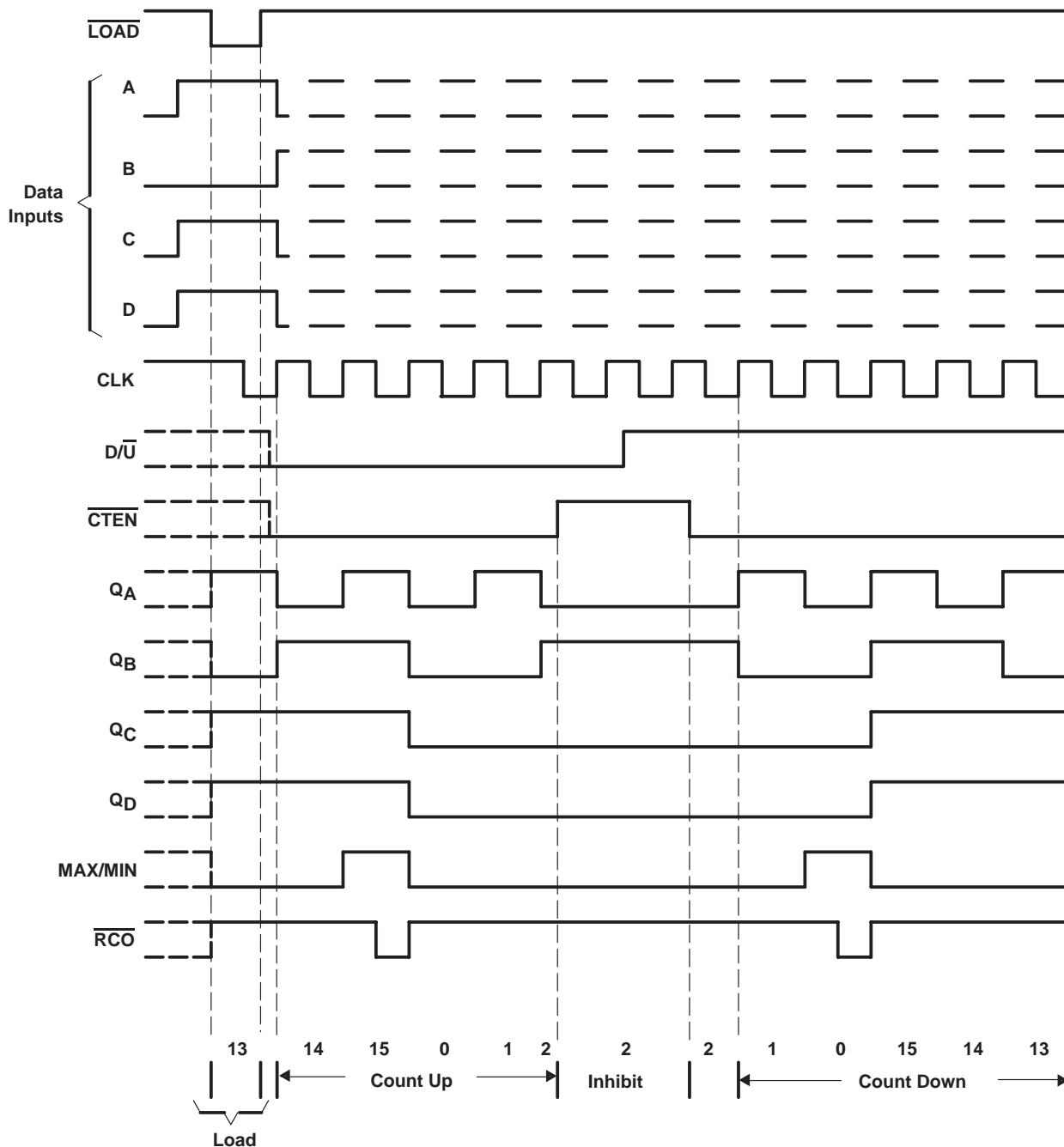
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typical load, count, and inhibit sequences

The following sequence is illustrated below:

1. Load (preset) to binary 13
2. Count up to 14, 15 (maximum), 0, 1, and 2
3. Inhibit
4. Count down to 1, 0 (minimum), 15, 14, and 13



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN54ALS191A	–55°C to 125°C
SN74ALS191A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS191A			SN74ALS191A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			4			8	mA
f_{clock}	Clock frequency	0		20	0		30	MHz
t_w	Pulse duration	CLK high or low		20	16.5		ns	
		LOAD low		25	20			
t_{su}	Setup time	Data before $\overline{LOAD}\uparrow$		25	20		ns	
		\overline{CTEN} before $CLK\uparrow$		45	20			
		D/\overline{U} before $CLK\uparrow$		30	20			
		\overline{LOAD} inactive before $CLK\uparrow$		20	20			
t_h	Hold time	Data after $\overline{LOAD}\uparrow$		5	5		ns	
		\overline{CTEN} after $CLK\uparrow$		0	0			
		D/\overline{U} after $CLK\uparrow$		0	0			
T_A	Operating free-air temperature	–55		125	0		70	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS191A		SN74ALS191A		UNIT
			MIN	TYP†	MAX	MIN	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA		-1.5		-1.5		V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} - 2		V _{CC} - 2		V
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 4 mA	0.25	0.4	0.25	0.4	
		I _{OL} = 8 mA			0.35	0.5	
I _I	V _{CC} = 5.5 V, V _I = 7 V		0.2		0.1		mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V		20		20		μA
I _{IL}	CTEN or CLK	V _{CC} = 5.5 V, V _I = 0.4 V	-0.2		-0.2		mA
	All others		-0.2		-0.1		
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V		-20	-112	-30	-112	mA
I _{CC}	V _{CC} = 5.5 V, All inputs at 0		12	22	12	22	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (OUTPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54ALS191A		SN74ALS191A		
			MIN	MAX	MIN	MAX	
f _{max}			20		30	MHz	
t _{PLH}	LOAD	Any Q	7	37	7	30	ns
t _{PHL}			8	34	8	30	
t _{PLH}	A, B, C, D	Any Q	3	25	3	21	ns
t _{PHL}			4	25	4	21	
t _{PLH}	CLK	RCO	5	24	5	20	ns
t _{PHL}			5	25	5	20	
t _{PLH}	CLK	Any Q	3	26	3	18	ns
t _{PHL}			3	22	3	18	
t _{PLH}	CLK	MAX/MIN	8	37	8	31	ns
t _{PHL}			8	34	8	31	
t _{PLH}	D \bar{U}	RCO	8	45	8	37	ns
t _{PHL}			10	36	10	28	
t _{PLH}	D \bar{U}	MAX/MIN	8	35	8	25	ns
t _{PHL}			8	30	8	25	
t _{PLH}	CTEN	RCO	4	21	4	18	ns
t _{PHL}			4	23	4	18	

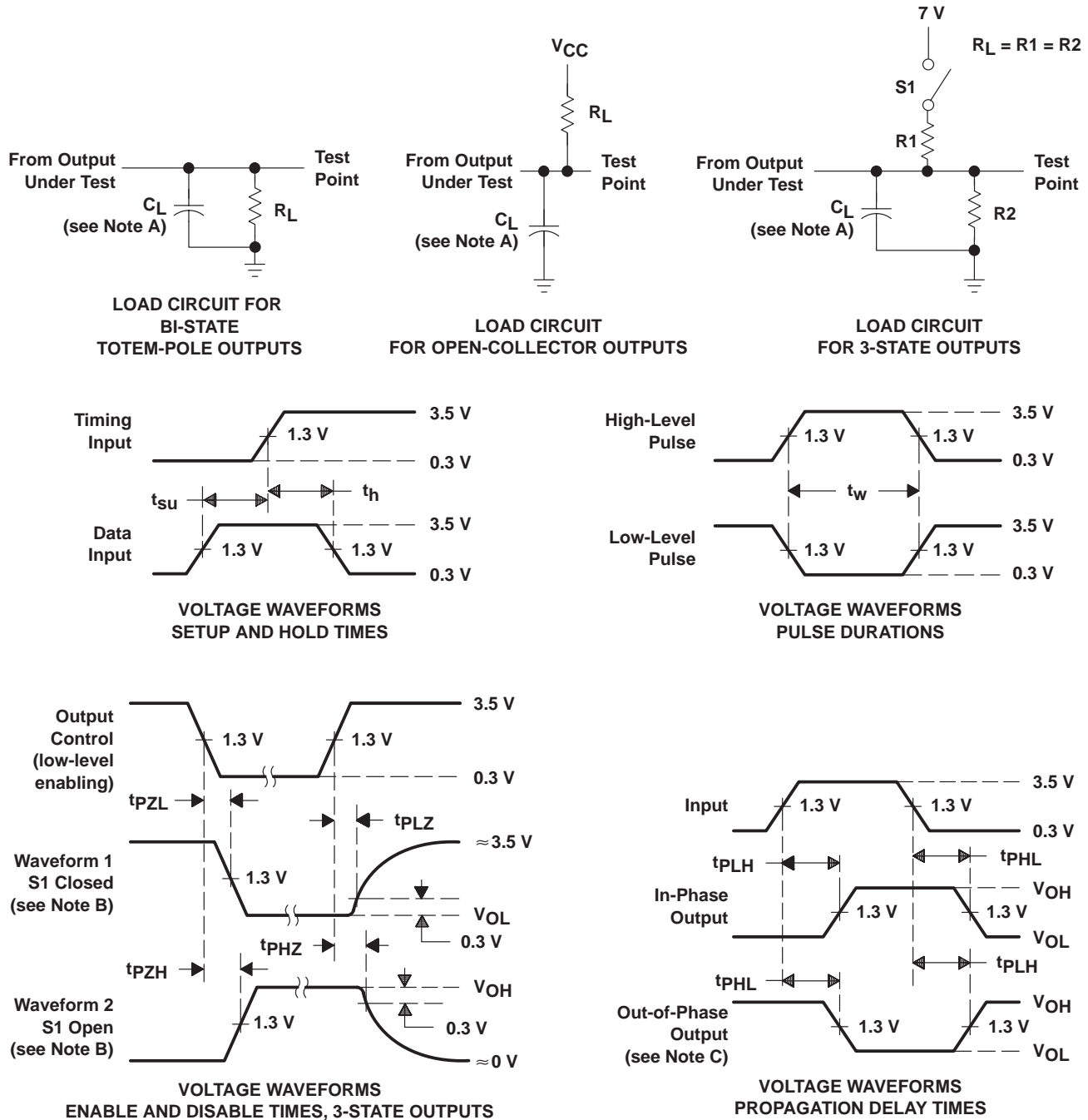
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-86840012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 86840012A SNJ54ALS 191AFK	Samples
5962-8684001EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8684001EA SNJ54ALS191AJ	Samples
5962-8684001FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8684001FA SNJ54ALS191AW	Samples
SN74ALS191AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS191A	Samples
SN74ALS191ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS191A	Samples
SN74ALS191ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS191A	Samples
SN74ALS191AN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS191AN	Samples
SN74ALS191ANE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS191AN	Samples
SNJ54ALS191AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 86840012A SNJ54ALS 191AFK	Samples
SNJ54ALS191AJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8684001EA SNJ54ALS191AJ	Samples
SNJ54ALS191AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8684001FA SNJ54ALS191AW	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ALS191A, SN74ALS191A :

● Catalog: [SN74ALS191A](#)

● Military: [SN54ALS191A](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS191ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS191ADR	SOIC	D	16	2500	333.2	345.9	28.6

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

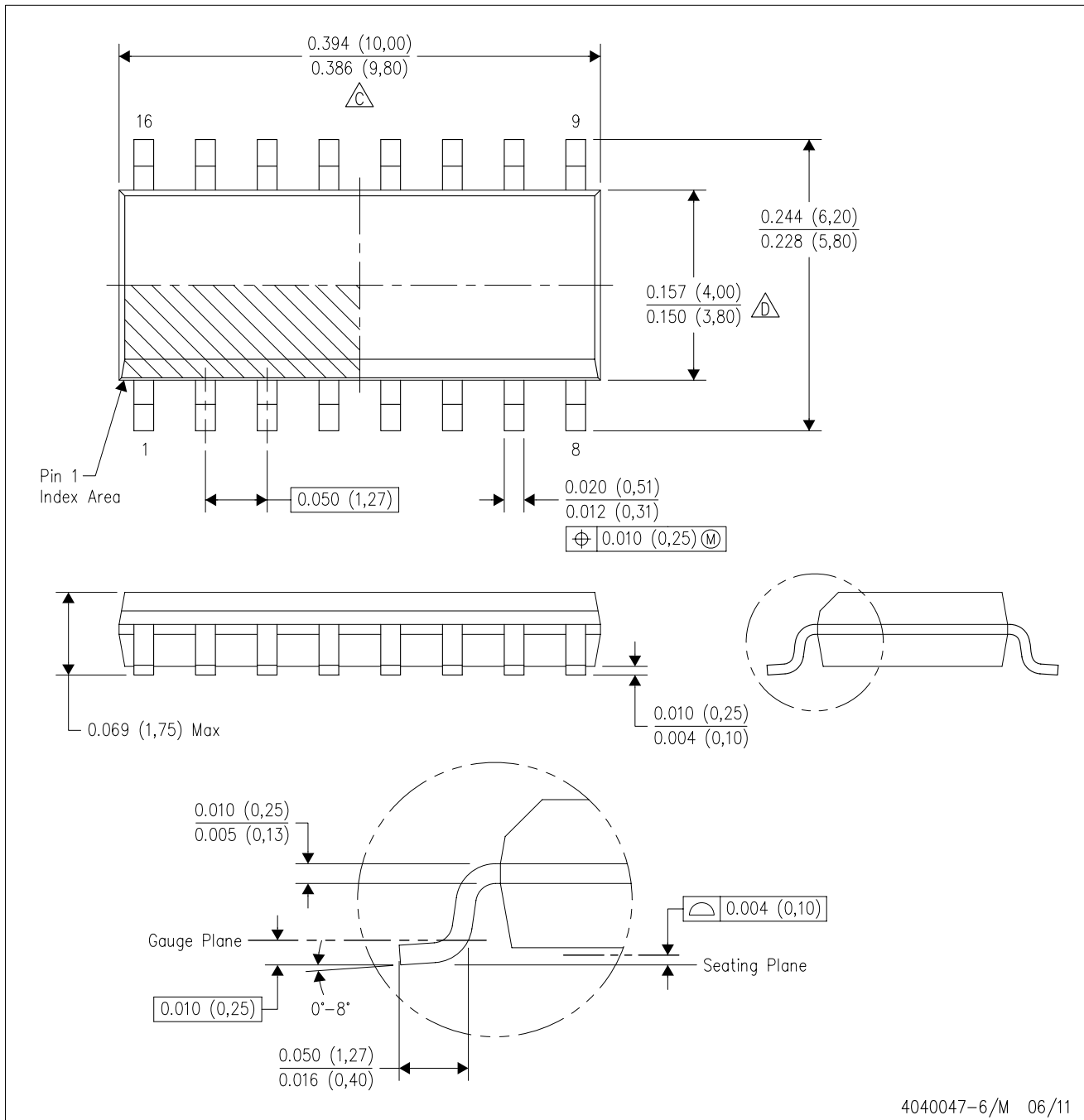


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

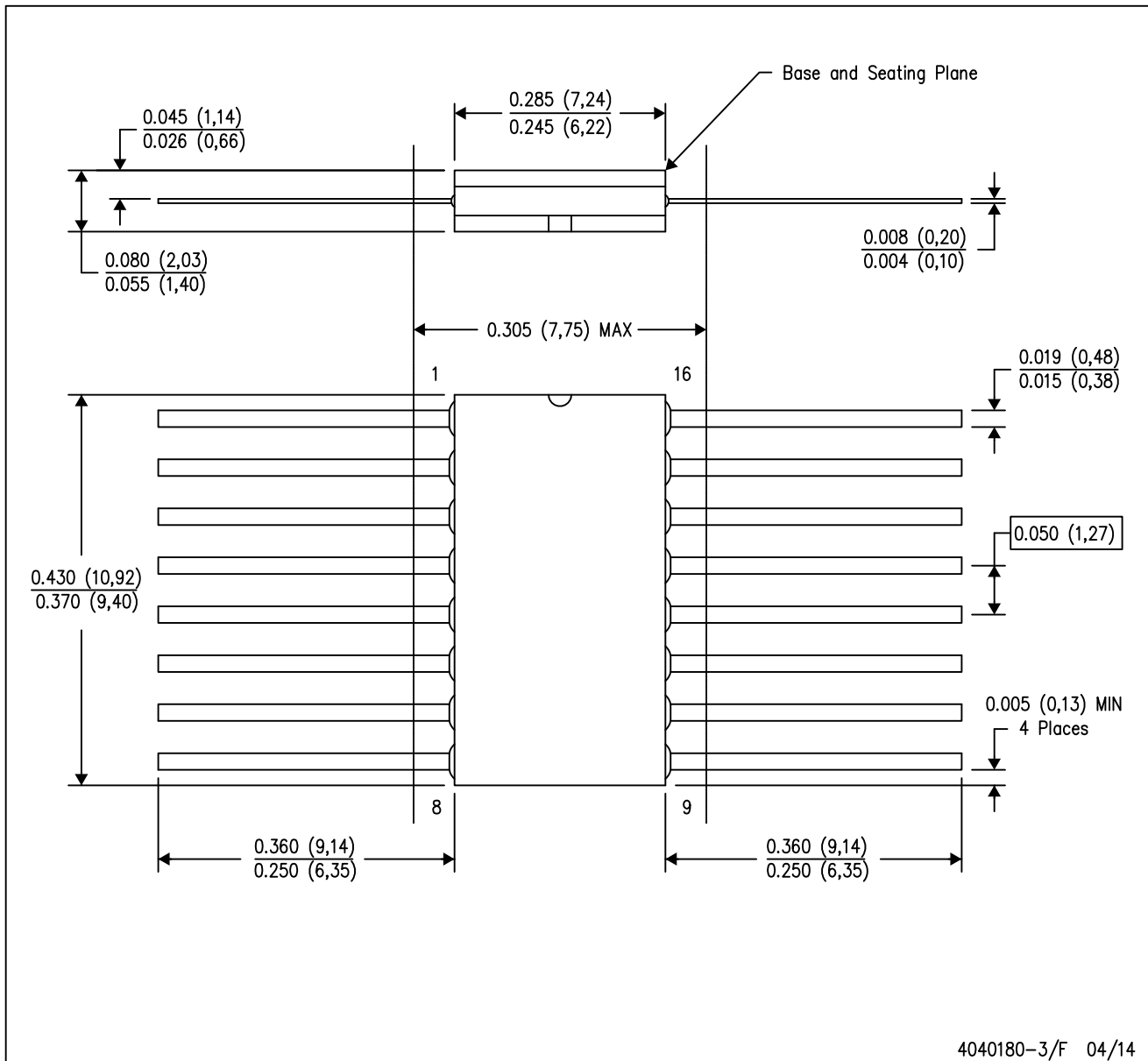


4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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