

# SN54ALS193A, SN74ALS193A SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS WITH DUAL CLOCK AND CLEAR

SDAS211C – DECEMBER 1982 – REVISED JULY 1996

- Look-Ahead Circuitry Enhances Cascaded Counters
- Fully Synchronous in Count Modes
- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

The 'ALS193A are synchronous, reversible, 4-bit up/down binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count/clock (UP or DOWN) input. The direction of the count is determined by which count input is pulsed while the other count input is high.

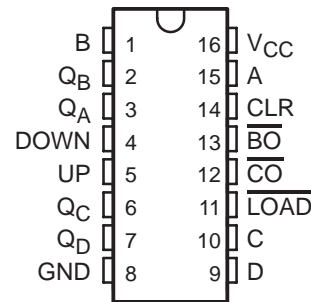
All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load (LOAD) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A high level applied to the clear (CLR) input forces all outputs to the low level. The clear function is independent of the count and LOAD inputs. The UP, DOWN, and LOAD inputs are buffered to lower the drive requirement, which significantly reduces the loading on, or current required by, clock drivers, etc., for long parallel words.

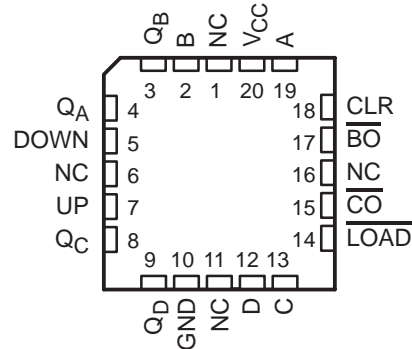
These counters are designed to be cascaded without the need for external circuitry. The borrow ( $\overline{BO}$ ) output produces a low-level pulse while the count is zero (all Q outputs low) and the DOWN input is low. Similarly, the carry ( $\overline{CO}$ ) output produces a low-level pulse while the count is 9 or 15 (all Q outputs high) and the UP input is low. The counters can then be easily cascaded by feeding  $\overline{BO}$  and  $\overline{CO}$  to the count-down and count-up inputs, respectively, of the succeeding counter.

The SN54ALS193A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS193A is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS193A . . . J PACKAGE  
SN74ALS193A . . . D OR N PACKAGE  
(TOP VIEW)



SN54ALS193A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection



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**TEXAS  
INSTRUMENTS**

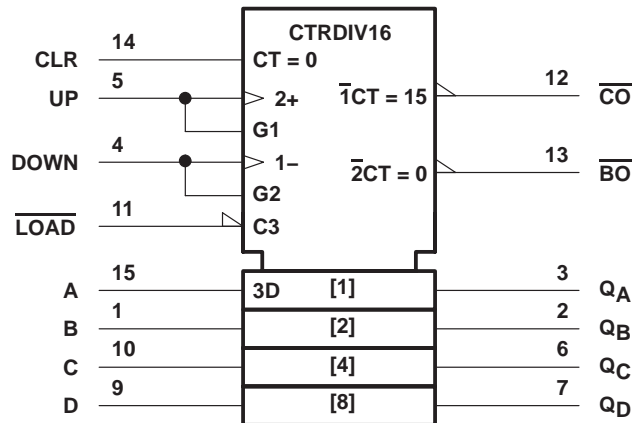
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## logic symbol†

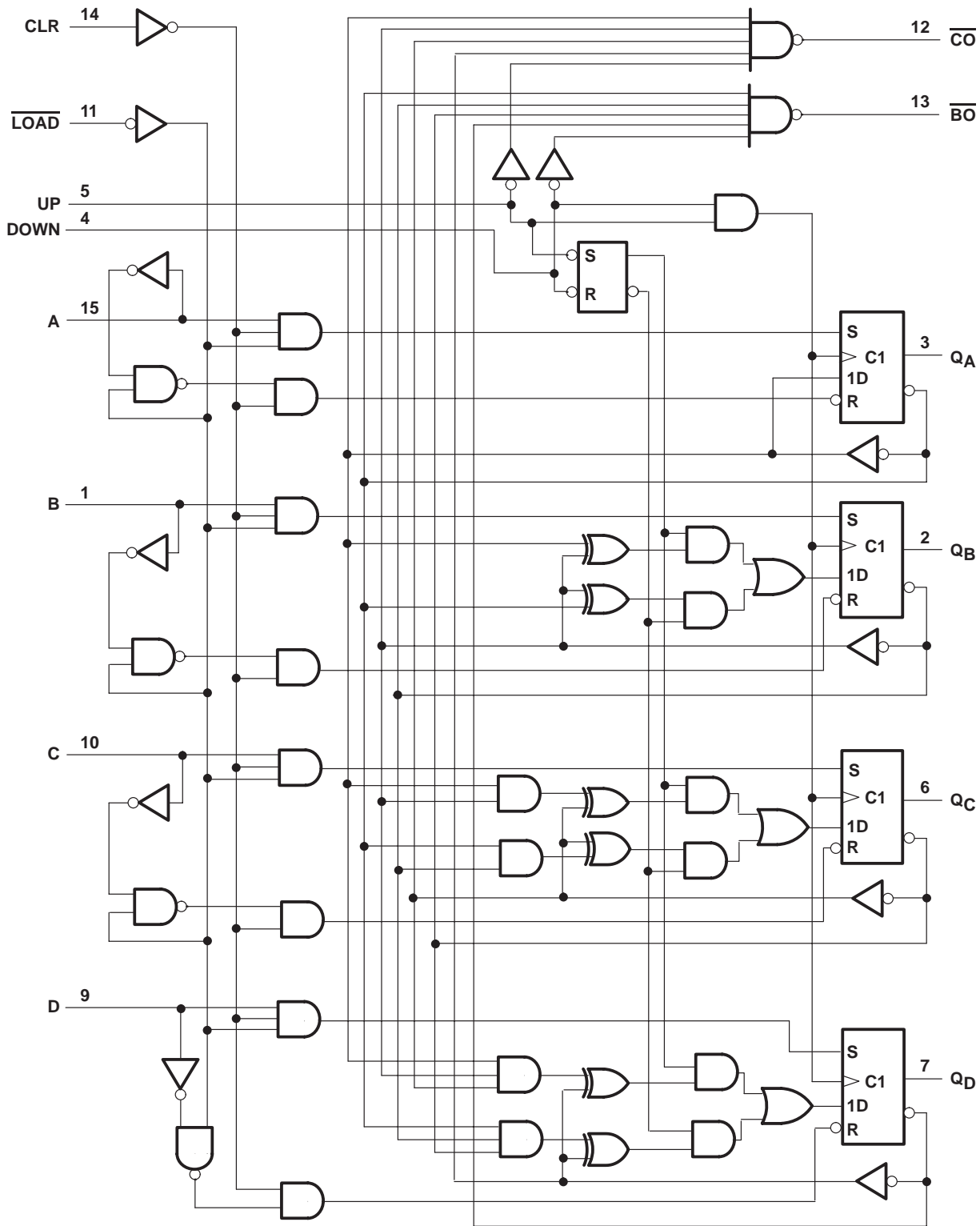


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

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logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.



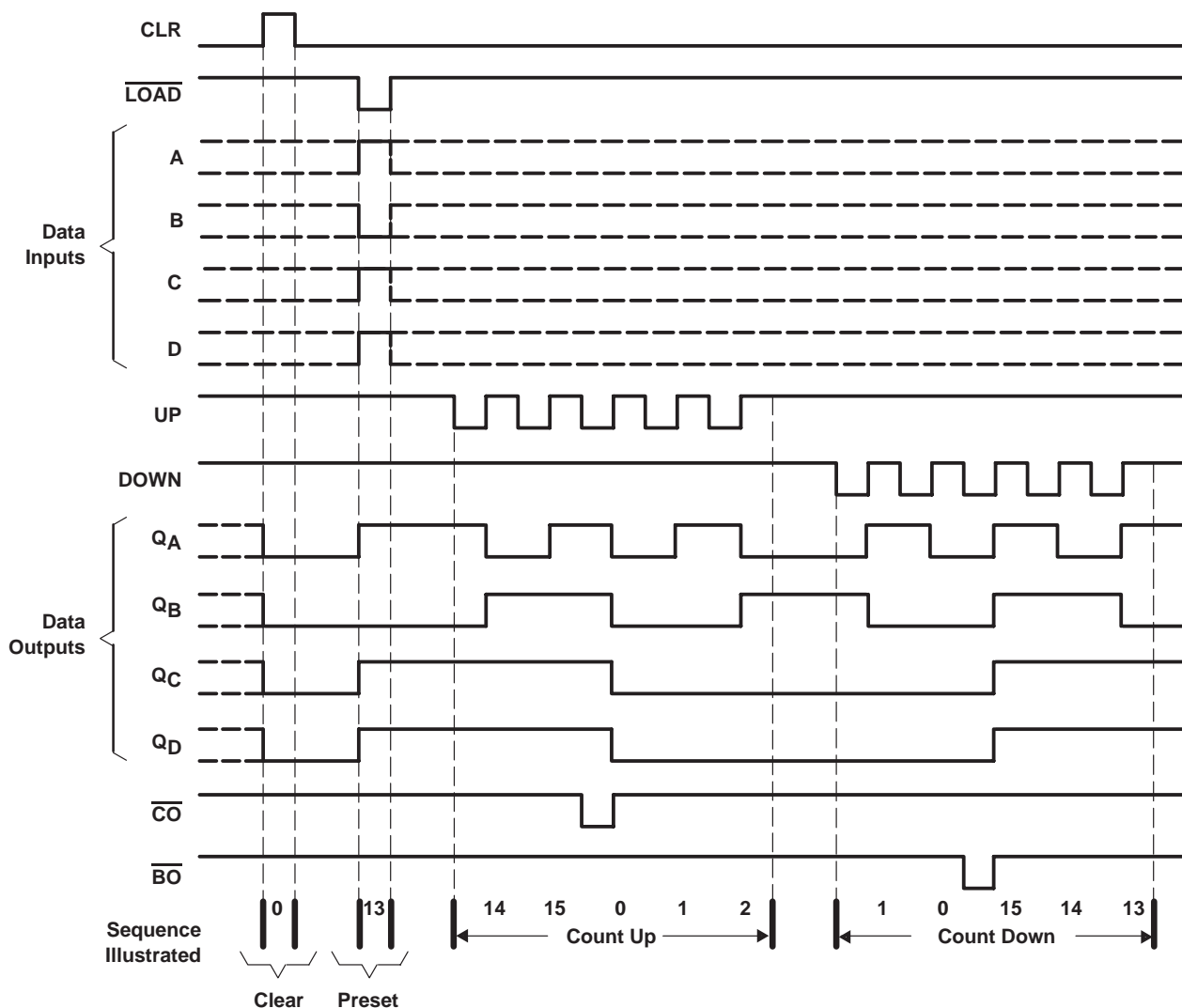
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## typical clear, load, and count sequence

the following sequence is illustrated below:

1. Clear outputs to zero
2. Load (preset) to binary 13
3. Count up to 14, 15 (carry), 0, 1, and 2
4. Count down to 1, 0 (borrow), 15, 14, and 13



NOTES: A. Clear overrides load, data, and count inputs.  
 B. When counting up, count-down input must be high; when counting down, count-up input must be high.



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ .....	7 V
Operating free-air temperature range, $T_A$ : SN54ALS193A .....	–55°C to 125°C
SN74ALS193A .....	0°C to 70°C
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN54ALS193A			SN74ALS193A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			–0.4			–0.4	mA
$I_{OL}$	Low-level output current			4			8	mA
$f_{clock}$	Clock frequency	0		20	0		30	MHz
$t_w$	Pulse duration	CLR high		10		10		ns
		LOAD low		25		20		
		UP or DOWN high or low		30		16.5		
$t_{su}$	Setup time	Data before LOAD↑		25		20		ns
		CLR inactive before UP or DOWN		20		20		
		LOAD inactive before UP or DOWN		20		20		
$t_h$	Hold time	Data after LOAD↑		5		5		ns
		UP high after DOWN↑		5		0		
		DOWN high after UP↑		5		0		
$T_A$	Operating free-air temperature	–55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS193A		SN74ALS193A		UNIT	
				MIN	TYP‡	MAX	MIN		TYP‡
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			–1.5	–1.5	V	
$V_{OH}$		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,	$I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$	V	
$V_{OL}$		$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$	0.25	0.4	0.25	0.4	V	
			$I_{OL} = 8\text{ mA}$			0.35	0.5		
$I_I$		$V_{CC} = 5.5\text{ V}$ ,	$V_I = 7\text{ V}$			0.1	0.35	0.1	mA
$I_{IH}$		$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			20	20	$\mu\text{A}$	
$I_{IL}$	UP or DOWN	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$			–0.2	–0.2	mA	
	All others					–0.1	–0.1		
$I_{O}^{\S}$		$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.25\text{ V}$	–20	–112	–30	–112	mA	
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ ,	See Note 1	12	22	12	22	mA	

‡ All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with the clear and load inputs grounded and all other inputs at 4.5 V.



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## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54ALS193A		SN74ALS193A		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			25		30		MHz
t <sub>PLH</sub>	UP	$\overline{CO}$	3	20	3	16	ns
t <sub>PHL</sub>			3	21	5	18	
t <sub>PLH</sub>	DOWN	$\overline{BO}$	4	20	4	16	ns
t <sub>PHL</sub>			5	22	5	18	
t <sub>PLH</sub>	UP or DOWN	Any Q	3	27	3	19	ns
t <sub>PHL</sub>			4	23	4	17	
t <sub>PLH</sub>	$\overline{LOAD}$	Any Q	7	38	7	30	ns
t <sub>PHL</sub>			8	37	8	28	
t <sub>PHL</sub>	CLR	Any Q	5	20	5	17	ns

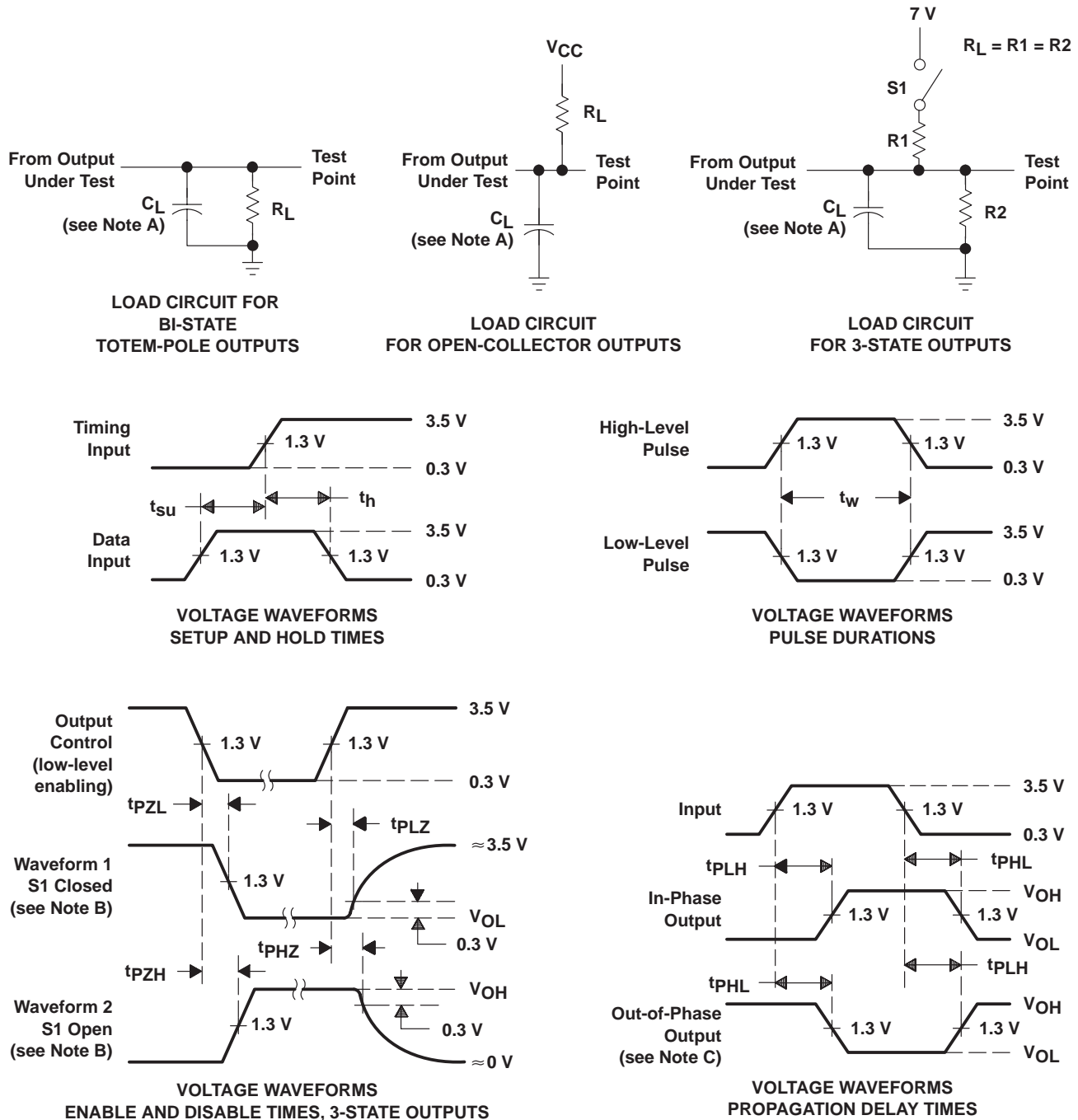
† For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.



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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
  - D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.
  - E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8869801EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8869801EA SNJ54ALS193AJ	<a href="#">Samples</a>
5962-8869801FA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8869801FA SNJ54ALS193AW	<a href="#">Samples</a>
SN54ALS193AJ	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54ALS193AJ	<a href="#">Samples</a>
SN74ALS193AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS193A	<a href="#">Samples</a>
SN74ALS193AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS193AN	<a href="#">Samples</a>
SN74ALS193ANE4	ACTIVE	PDIP	N	16	25	TBD	Call TI	Call TI	0 to 70		<a href="#">Samples</a>
SNJ54ALS193AJ	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8869801EA SNJ54ALS193AJ	<a href="#">Samples</a>
SNJ54ALS193AW	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8869801FA SNJ54ALS193AW	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ALS193A, SN74ALS193A :**

- Catalog : [SN74ALS193A](#)
- Military : [SN54ALS193A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

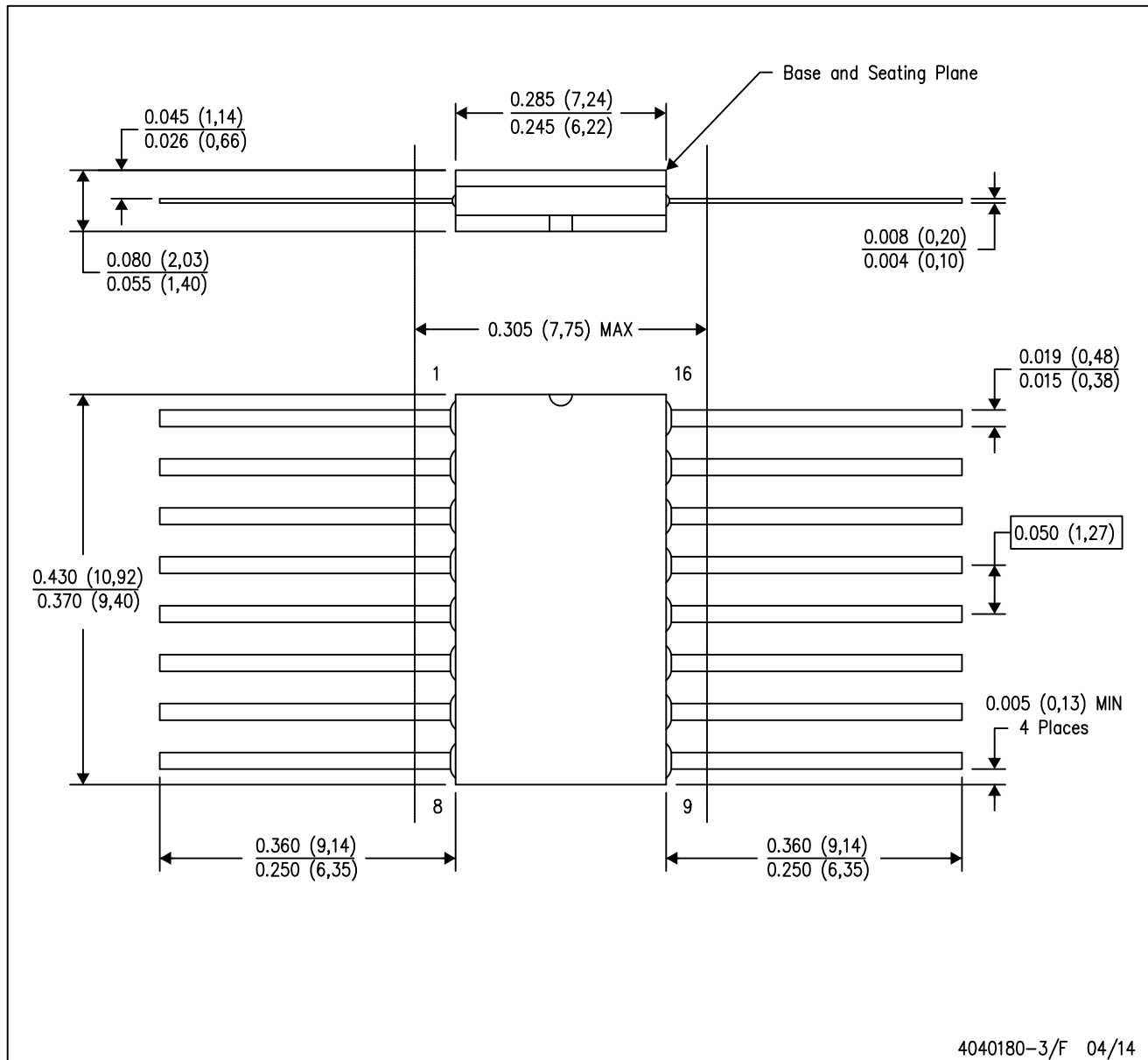
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-8869801FA	W	CFP	16	1	506.98	26.16	6220	NA
SN74ALS193AD	D	SOIC	16	40	507	8	3940	4.32
SN74ALS193AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74ALS193AN	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54ALS193AW	W	CFP	16	1	506.98	26.16	6220	NA

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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