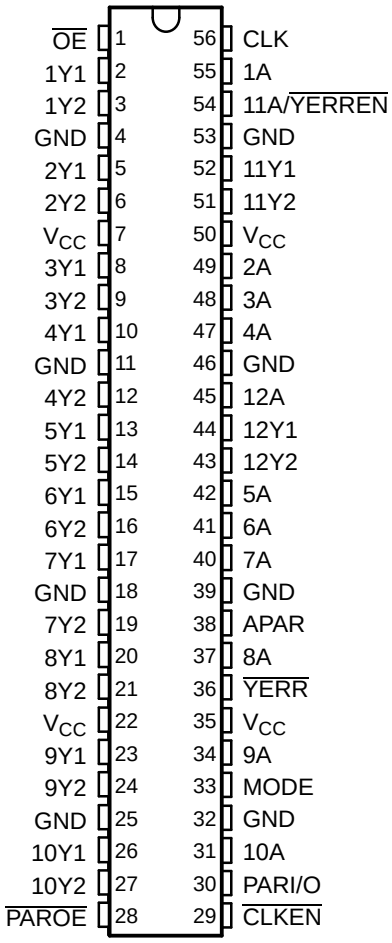
SN74ALVCH16903
3.3-V 12-BIT UNIVERSAL BUS DRIVER WITH PARITY CHECKER AND DUAL 3-STATE OUTPUTS

SCES095D – MARCH 1997 – REVISED SEPTEMBER 2004

FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Checks Parity**
- **Able to Cascade With a Second SN74ALVCH16903**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



DESCRIPTION

This 12-bit universal bus driver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16903 has dual outputs and can operate as a buffer or an edge-triggered register. In both modes, parity is checked on APAR, which arrives one cycle after the data to which it applies. The $\overline{YERR}$ output, which is produced one cycle after APAR, is open drain.

MODE selects one of the two data paths. When MODE is low, the device operates as an edge-triggered register. On the positive transition of the clock (CLK) input and when the clock-enable ($\overline{CLKEN}$) input is low, data set up at the A inputs is stored in the internal registers. On the positive transition of CLK and when $\overline{CLKEN}$ is high, only data set up at the 9A–12A inputs is stored in their internal registers. When MODE is high, the device operates as a buffer and data at the A inputs passes directly to the outputs. 11A/$\overline{YERREN}$ serves a dual purpose; it acts as a normal data bit and also enables $\overline{YERR}$ data to be clocked into the $\overline{YERR}$ output register.

When used as a single device, parity output enable ($\overline{PAROE}$) must be tied high; when parity input/output (PARI/O) is low, even parity is selected and when PARI/O is high, odd parity is selected. When used in pairs and $\overline{PAROE}$ is low, the parity sum is output on PARI/O for cascading to the second SN74ALVCH16903. When used in pairs and $\overline{PAROE}$ is high, PARI/O accepts a partial parity sum from the first SN74ALVCH16903.

A buffered output-enable ($\overline{OE}$) input can be used to place the 24 outputs and $\overline{YERR}$ in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operation of the device. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

DESCRIPTION (CONTINUED)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16903 is characterized for operation from 0°C to 70°C.

FUNCTION TABLES

FUNCTION

INPUTS					OUTPUTS	
$\overline{OE}$	MODE	$\overline{CLKEN}$	CLK	A	1Yn(1)–8Yn(1)	9Yn(1)–12Yn(1)
L	L	L	↑	H	H	H
L	L	L	↑	L	L	L
L	L	H	↑	H	Y_0	H
L	L	H	↑	L	Y_0	L
L	H	X	X	H	H	H
L	H	X	X	L	L	L
H	X	X	X	X	Z	Z

(1) n = 1 or 2

PARITY FUNCTION

INPUTS						OUTPUT $\overline{YERR}$
$\overline{OE}$	$\overline{PAROE}$ (1)	11A/$\overline{YERREN}$(2)	PARI/O	Σ OF INPUTS 1A–10A = H	APAR	
L	H	L	L	0, 2, 4, 6, 8, 10	L	H
L	H	L	L	1, 3, 5, 7, 9	L	L
L	H	L	L	0, 2, 4, 6, 8, 10	H	L
L	H	L	L	1, 3, 5, 7, 9	H	H
L	H	L	H	0, 2, 4, 6, 8, 10	L	L
L	H	L	H	1, 3, 5, 7, 9	L	H
L	H	L	H	0, 2, 4, 6, 8, 10	H	H
L	H	L	H	1, 3, 5, 7, 9	H	L
H	X	X	X	X	X	H
L	X	H	X	X	X	H

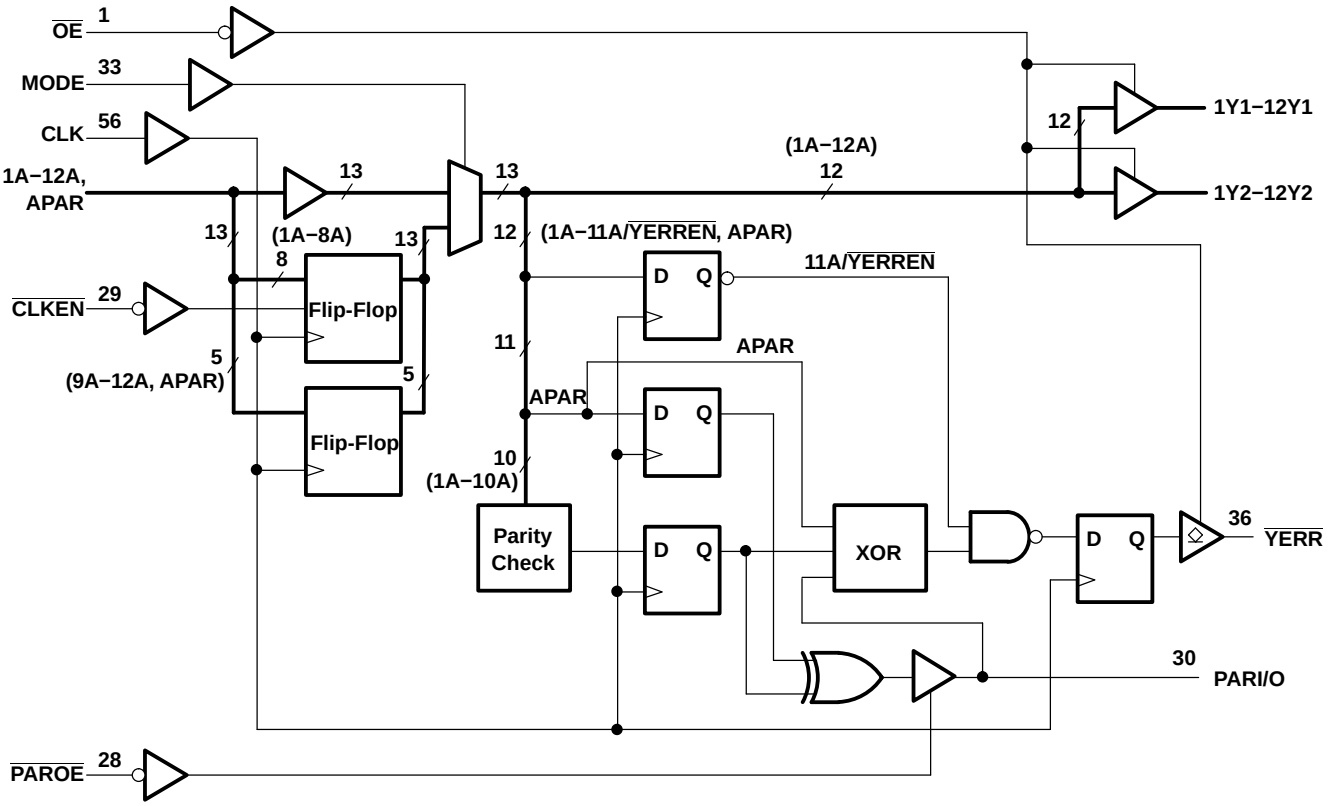
(1) When used as a single device, $\overline{PAROE}$ must be tied high.
(2) Valid after appropriate number of clock pulses have set internal register

PARI/O FUNCTION(1)

INPUTS			OUTPUT PARI/O
$\overline{PAROE}$	Σ OF INPUTS 1A–10A = H	APAR	
L	0, 2, 4, 6, 8, 10	L	L
L	1, 3, 5, 7, 9	L	H
L	0, 2, 4, 6, 8, 10	H	H
L	1, 3, 5, 7, 9	H	L
H	X	X	Z

(1) This table applies to the first device of a cascaded pair of SN74ALVCH16903 devices.

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
V_I	Input voltage range(2)		-0.5	4.6	V
V_O	Output voltage range(2)(3)		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		-50	mA
I_{OK}	Output clamp current	V_O < 0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(4)	DGG package		81	°C/W
		DGV package		86	
		DL package		74	
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS(1)

				MIN	MAX	UNIT
V_{CC}	Supply voltage			2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V		1.7		V
		V_{CC} = 2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V			0.7	V
		V_{CC} = 2.7 V to 3.6 V			0.8	
V_I	Input voltage			0	V_{CC}	V
V_O	Output voltage			0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V	Y port		-12	mA
		V_{CC} = 2.7 V			-12	
		V_{CC} = 3 V	PARI/O		-12	
			Y port		-24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V	Y port		12	mA
		V_{CC} = 2.7 V			12	
		V_{CC} = 3 V	PARI/O		12	
			Y port		24	
			$\overline{YERR}$ output		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			0	10	ns/V
T_A	Operating free-air temperature			0	70	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}	Y port	I_{OH} = -100 μA		2.3 V to 3.6 V	V_{CC} - 0.2			V
		I_{OH} = -6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = -12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
				3 V	2.4			
		I_{OH} = -24 mA,	V_{IH} = 2 V	3 V	2			
	PARI/O	I_{OH} = -12 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}	Y port	I_{OL} = 100 μA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
	PARI/O	I_{OL} = 12 mA,	V_{IL} = 0.8 V	3 V			0.55	
	$\overline{YERR}$ output	I_{OL} = 24 mA		3 V			0.5	
I_I		V_I = V_{CC} or GND		3.6 V			±5	μA
$I_{I(hold)}$		V_I = 0.7 V		2.3 V	45			μA
		V_I = 1.7 V		2.3 V	-45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V		3 V	-75			
		V_I = 0 to 3.6 V(2)		3.6 V			±500	
I_{OH}	$\overline{YERR}$ output	V_O = V_{CC}		0 to 3.6 V			±10	μA
I_{OZ}(3)		V_O = V_{CC} or GND		3.6 V			±10	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	μA
ΔI_{CC}		One input at V_{CC} - 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		5.5		pF
	Data inputs					5.5		
C_o	$\overline{YERR}$ output	V_O = V_{CC} or GND		3.3 V		5		pF
	Data outputs					6		
C_{io}	PARI/O	V_O = V_{CC} or GND		3.3 V		7		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1 and Figure 4)

				V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency				125		125		125	MHz
t_w	Pulse duration, CLK↑			3		3		3		ns
t_{su}	Setup time	1A–12A before CLK↑	Register mode	1.7		1.9		1.45		ns
		1A–10A before CLK↑	Buffer mode	5.9		5.2		4.4		
		APAR before CLK↑	Register mode	1.2		1.5		1.3		
			Buffer mode	4.6		3.6		3.1		
		PARI/O before CLK↑	Both modes	2.4		2		1.7		
		11A/$\overline{\text{YERREN}}$ before CLK↑	Buffer mode	2		1.9		1.6		
		$\overline{\text{CLKEN}}$ before CLK↑	Register mode	2.5		2.6		2.2		
t_h	Hold time	1A–12A after CLK↑	Register mode	0.4		0.25		0.55		ns
		1A–10A after CLK↑	Buffer mode	0.25		0.25		0.25		
		APAR after CLK↑	Register mode	0.7		0.4		0.7		
			Buffer mode	0.25		0.25		0.25		
		PARI/O after CLK↑	Register mode	0.25		0.25		0.4		
			Buffer mode	0.25		0.25		0.5		
		11A/$\overline{\text{YERREN}}$ after CLK↑	Buffer mode	0.25		0.25		0.4		
		$\overline{\text{CLKEN}}$ after CLK↑	Register mode	0.25		0.5		0.4		

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 and Figure 4)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}				125		125		125		MHz
t_{pd}	Buffer mode	A	Y	1	4.4		4.2	1.1	3.8	ns
	Both modes	CLK	$\overline{\text{YERR}}$	1	5.7		4.9	1.4	4.4	
			PARI/O	1.2	8.6		7.9	1.7	6.6	
t_{pd} (1)	Both modes	CLK	PARI/O	1	6.8		5.2	1.3	4.5	ns
t_{pd}	Both modes	MODE	Y	1	5.9		5.8	1.3	4.9	ns
t_{PLH}	Register mode	CLK	Y	1	6.1		5.5	1.2	4.8	ns
t_{PHL}				1	5.9		4.9	1.2	4.6	
t_{en}	Both modes	$\overline{\text{OE}}$	Y	1.1	6.5		6.4	1.4	5.4	ns
		$\overline{\text{PAROE}}$	PARI/O	1	5.6		6	1	4.8	
t_{dis}	Both modes	$\overline{\text{OE}}$	Y	1	6.4		5.2	1.7	5	ns
		$\overline{\text{PAROE}}$	PARI/O	1	3.2		3.8	1.2	3.8	
t_{PLH}	Both modes	$\overline{\text{OE}}$	$\overline{\text{YERR}}$	1	3.6		4.2	1.9	4	ns
t_{PHL}				1.2	5.1		4.9	1.5	4.2	

(1) See Figure 2 and Figure 5 for the load specification.

SIMULTANEOUS SWITCHING CHARACTERISTICS(1)

(see Figure 3 and Figure 6)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Register mode	CLK	Y	1.8	6.5		6.1	1.8	5	ns
t_{PHL}				1.4	5.9		5.1	1.7	4.5	

(1) All outputs switching

OPERATING CHARACTERISTICS FOR BUFFER MODE

T_A = 25°C

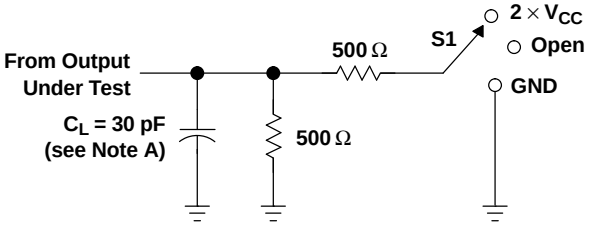
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 0, f = 10 MHz	57.5	65	pF
		Outputs disabled		15	17.5	

OPERATING CHARACTERISTICS FOR REGISTER MODE

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 0, f = 10 MHz	57	87.5	pF
		Outputs disabled		16.5	34	

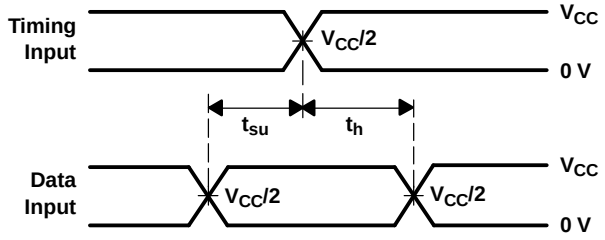
PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V



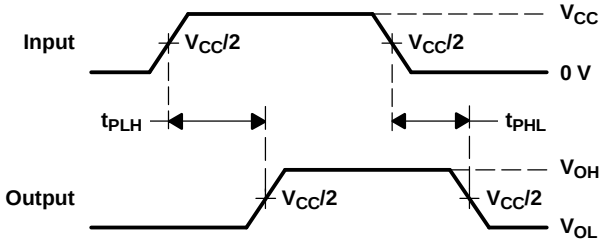
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

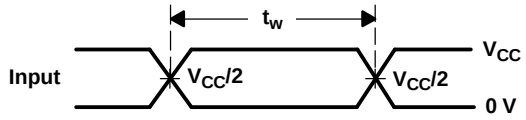
$\overline{YERR}$	S1
t_{PHL} (see Note H)	2 × V_{CC}
t_{PLH} (see Note I)	2 × V_{CC}



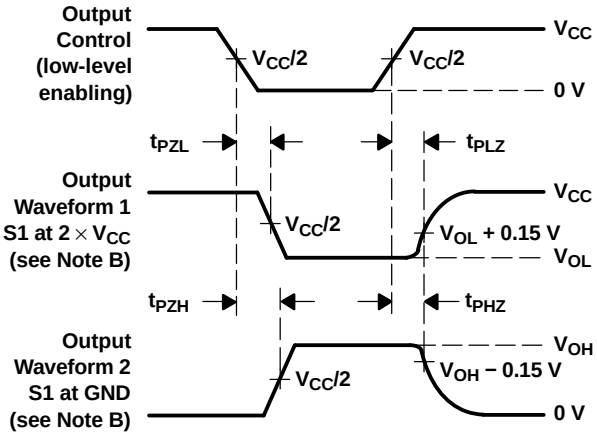
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

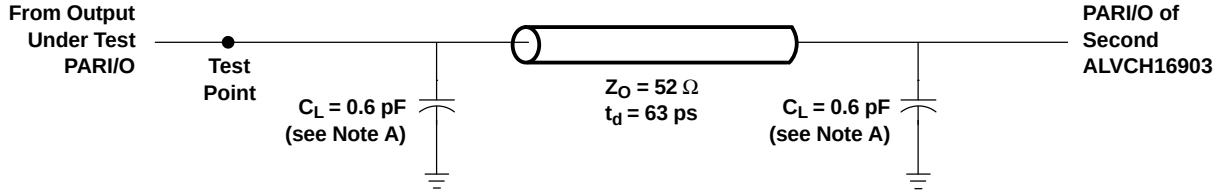


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

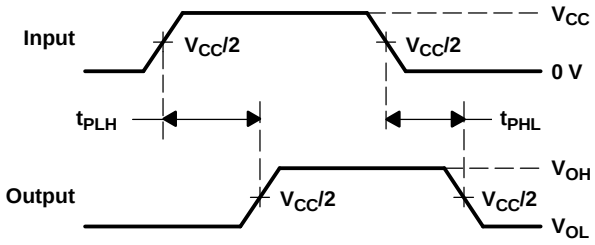
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. t_{PHL} is measured at $V_{CC}/2$.
I. t_{PLH} is measured at V_{OL} + 0.15 V.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V



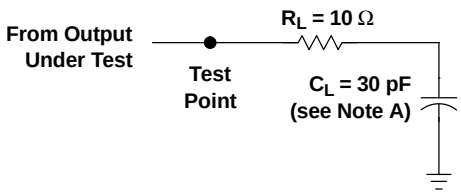
LOAD CIRCUIT



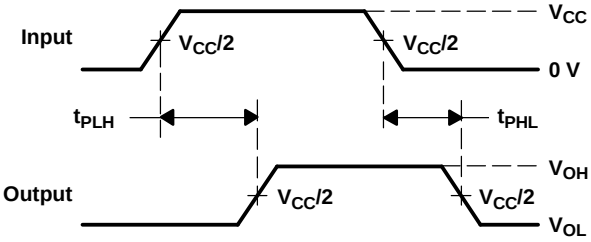
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms



LOAD CIRCUIT

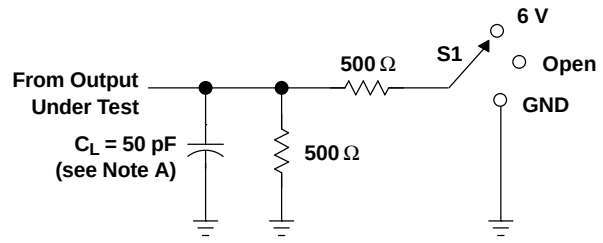


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.

Figure 3. Load Circuit and Voltage Waveforms

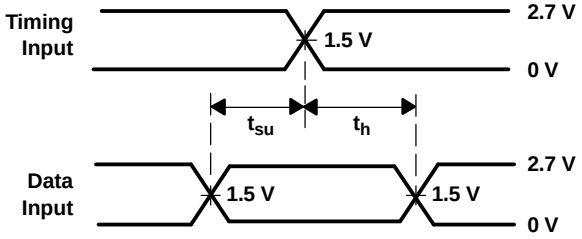
PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V



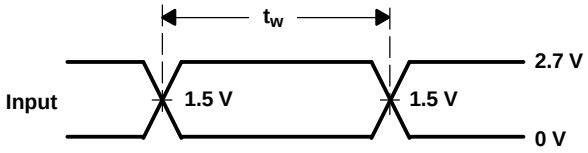
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

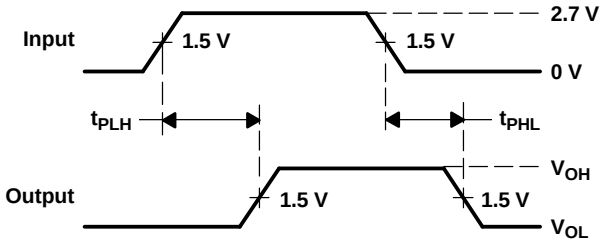
$\overline{YERR}$	S1
t_{PHL} (see Note H)	6 V
t_{PLH} (see Note I)	6 V



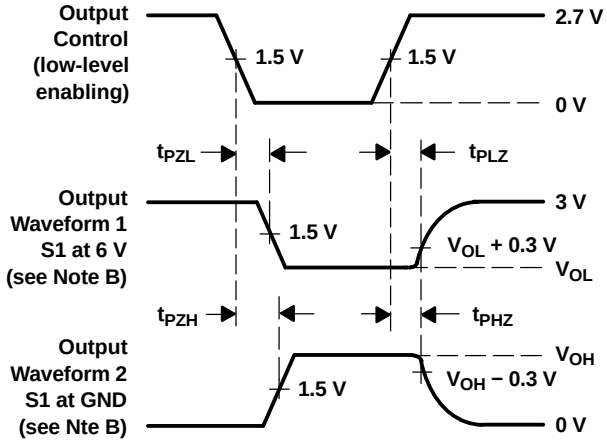
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

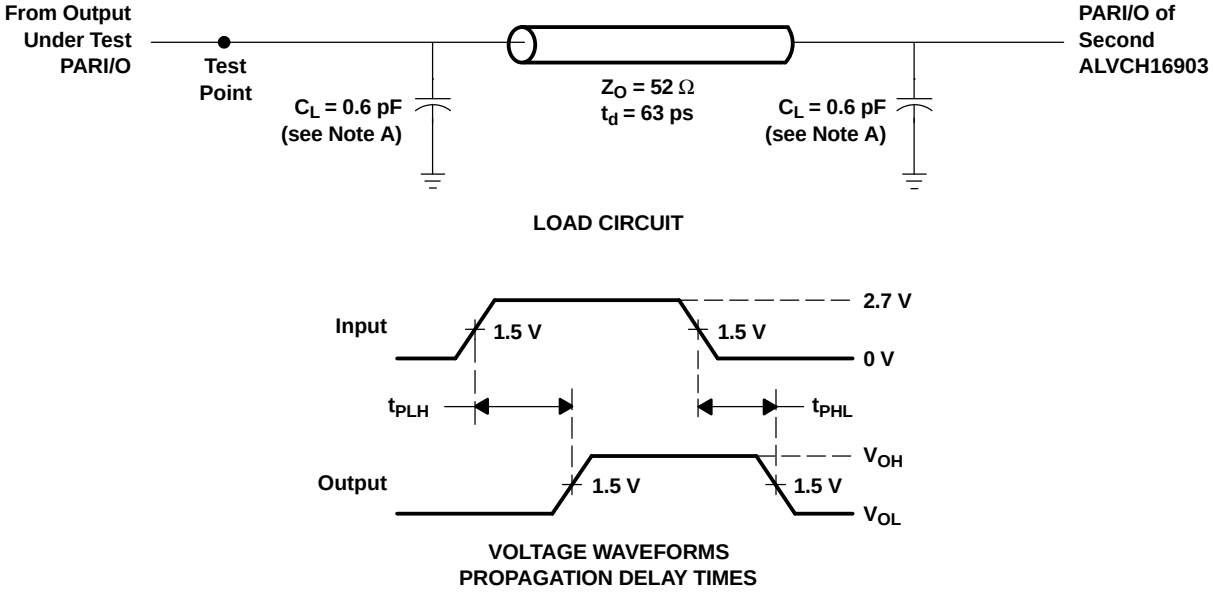


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. t_{PHL} is measured at 1.5 V.
I. t_{PLH} is measured at V_{OL} + 0.3 V.

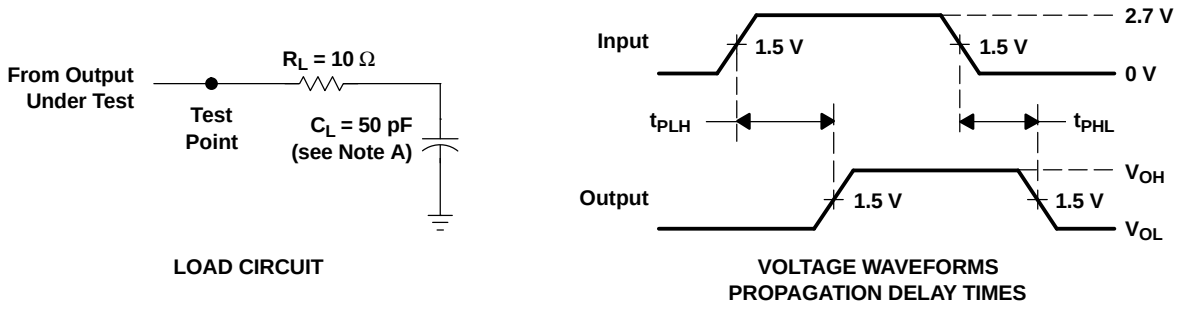
Figure 4. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 5. Load Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 6. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALVCH16903DL	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16903
SN74ALVCH16903DL.B	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16903

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

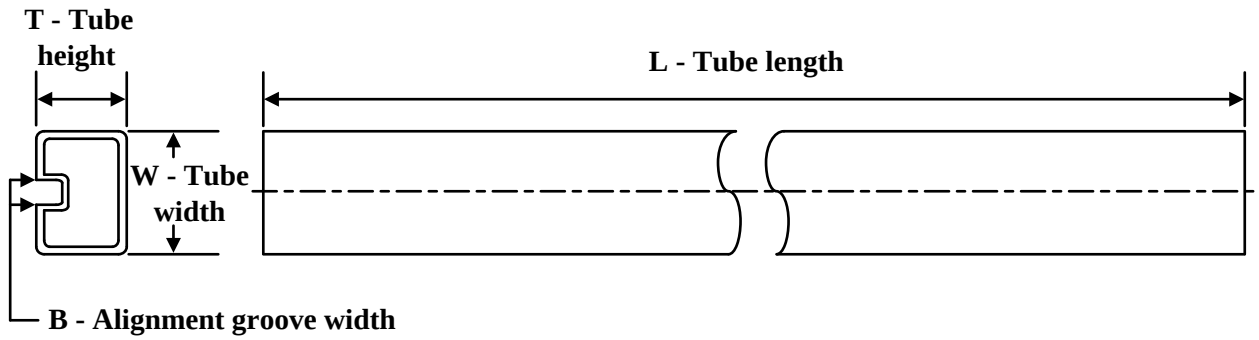
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

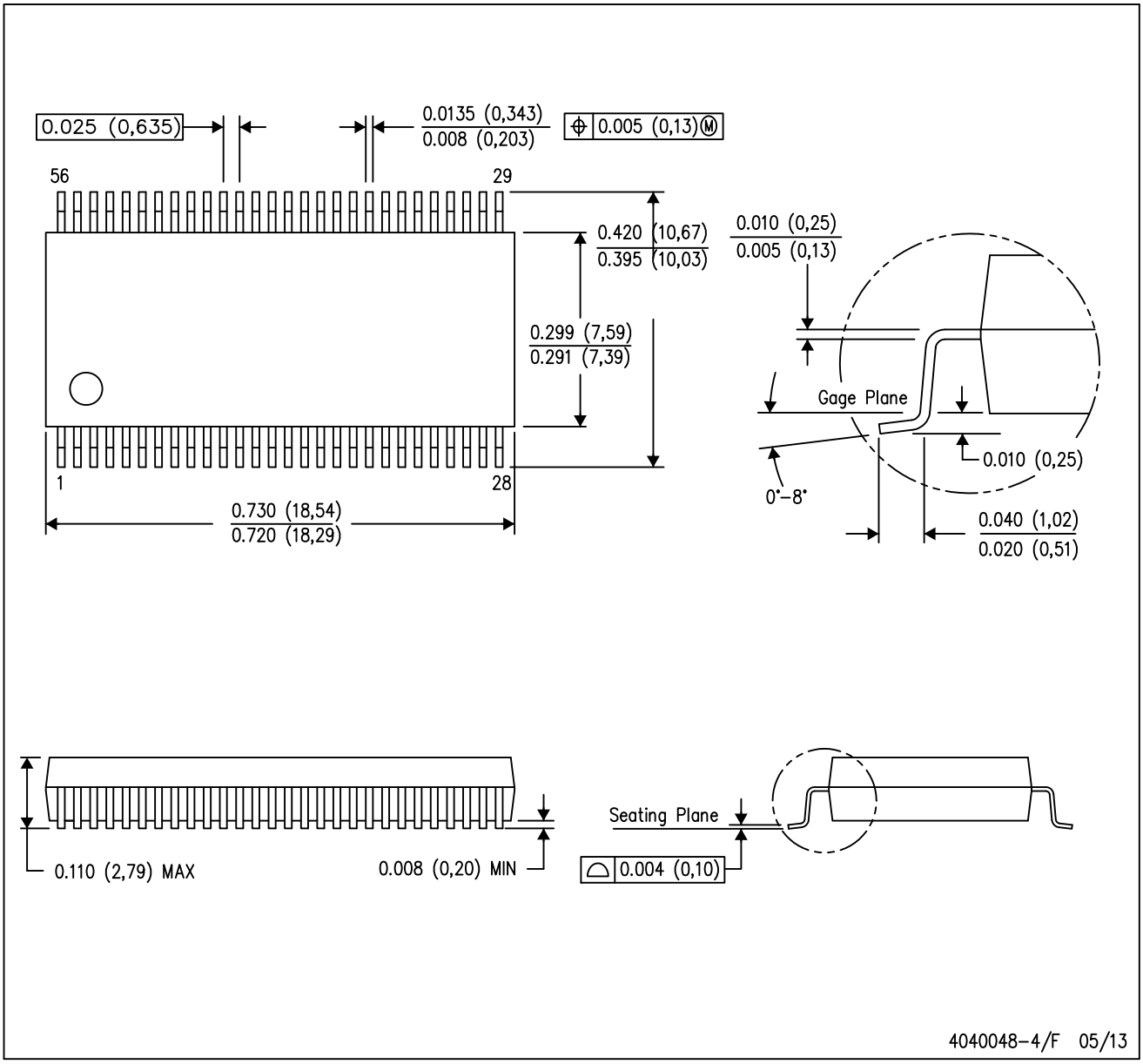
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ALVCH16903DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ALVCH16903DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025