

# SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

- Internal Look-Ahead Circuitry for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N) and Ceramic (J) DIPs

## description

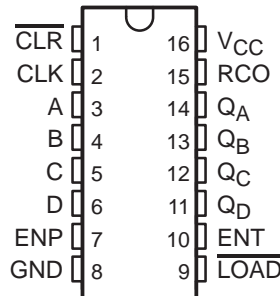
These synchronous, presettable, 4-bit decade and binary counters feature an internal carry look-ahead circuitry for application in high-speed counting designs. The SN54ALS162B is a 4-bit decade counter. The 'ALS161B, 'ALS163B, 'AS161, and 'AS163 devices are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; they can be preset to any number between 0 and 9 or 15. Because presetting is synchronous, setting up a low level at the load (LOAD) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

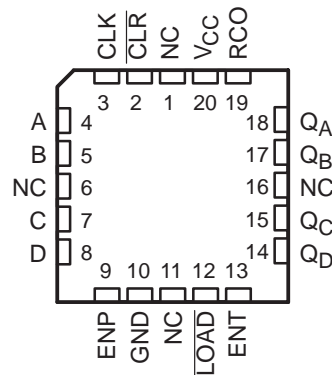
The clear function for the 'ALS161B and 'AS161 devices is asynchronous. A low level at the clear ( $\overline{\text{CLR}}$ ) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, LOAD, or enable inputs. The clear function for the SN54ALS162B, 'ALS163B, and 'AS163 devices is synchronous, and a low level at CLR sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to  $\overline{\text{CLR}}$  to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP and ENT inputs and a ripple-carry (RCO) output are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. RCO, thus enabled,

SN54ALS161B, SN54ALS162B, SN54ALS163B,  
SN54AS161, SN54AS163 . . . J PACKAGE  
SN74ALS161B, SN74AS161,  
SN74AS163 . . . D OR N PACKAGE  
SN74ALS163B . . . D, DB, OR N PACKAGE  
(TOP VIEW)



SN54ALS161B, SN54ALS162B, SN54ALS163B,  
SN54AS161, SN54AS163 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163  
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163  
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

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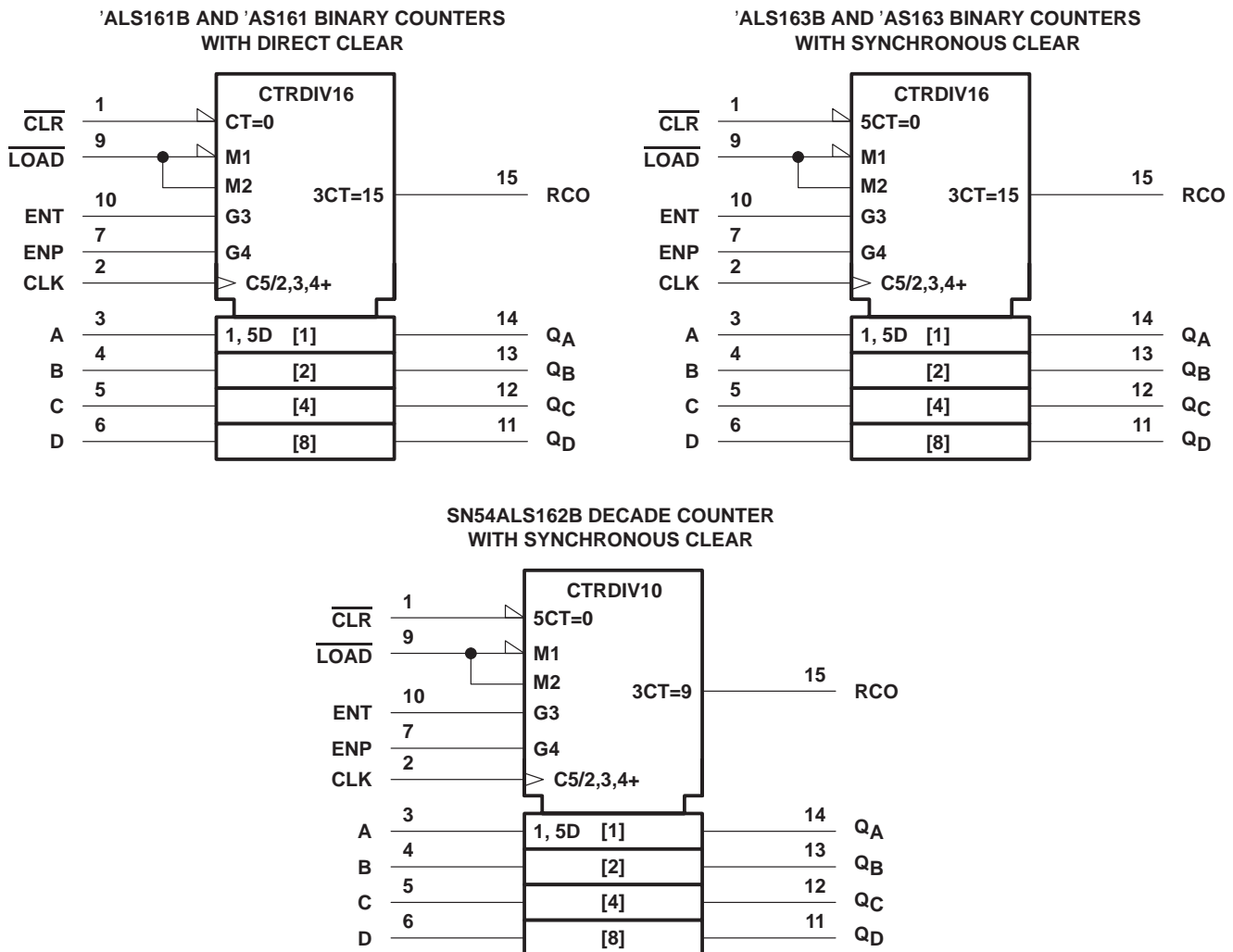
**description (continued)**

produces a high-level pulse while the count is maximum (9 or 15, with  $Q_A$  high). The high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or  $\overline{LOAD}$ ) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, and SN54AS163 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS161B, SN74ALS163B, SN74AS161, and SN74AS163 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**logic symbols†**

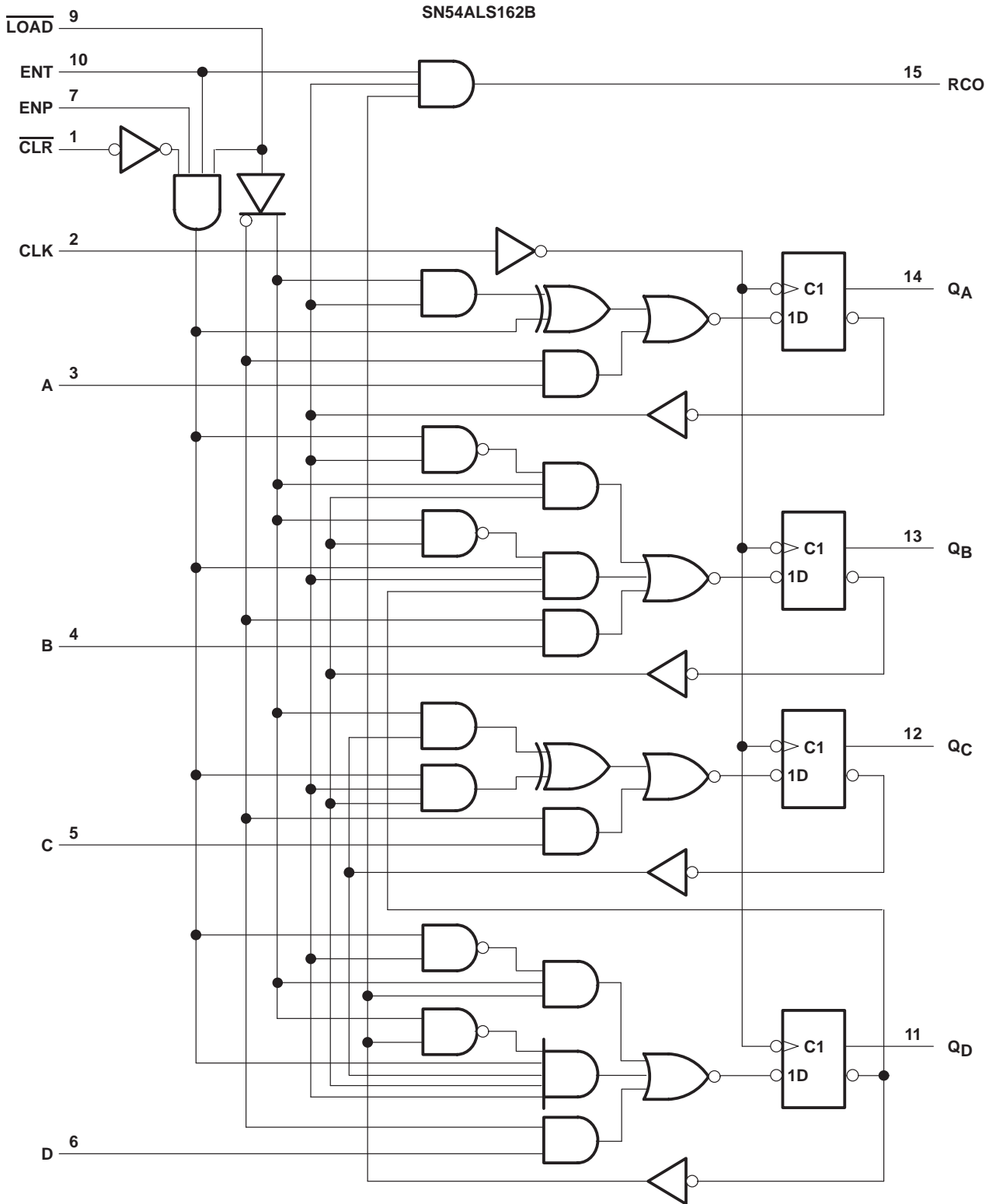


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, and N packages.

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163  
 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163  
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logic diagram (positive logic)



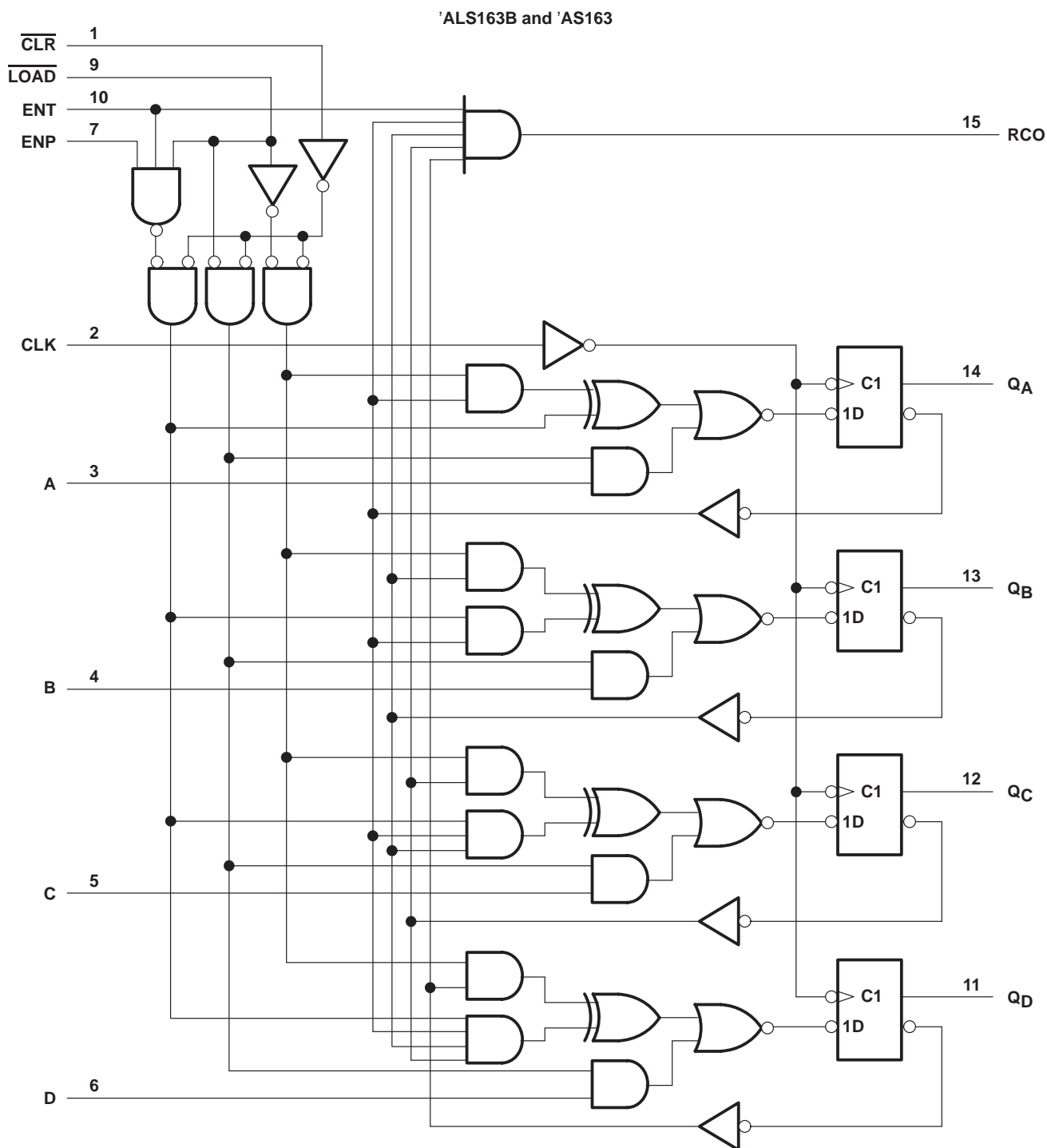
Pin numbers shown are for the J package.



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163  
 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163  
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**logic diagram (positive logic)**



Pin numbers shown are for the D, DB, J, and N packages.  
 'ALS161B and 'AS161 synchronous binary counters are similar; however,  $\overline{\text{CLR}}$  is asynchronous.



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 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

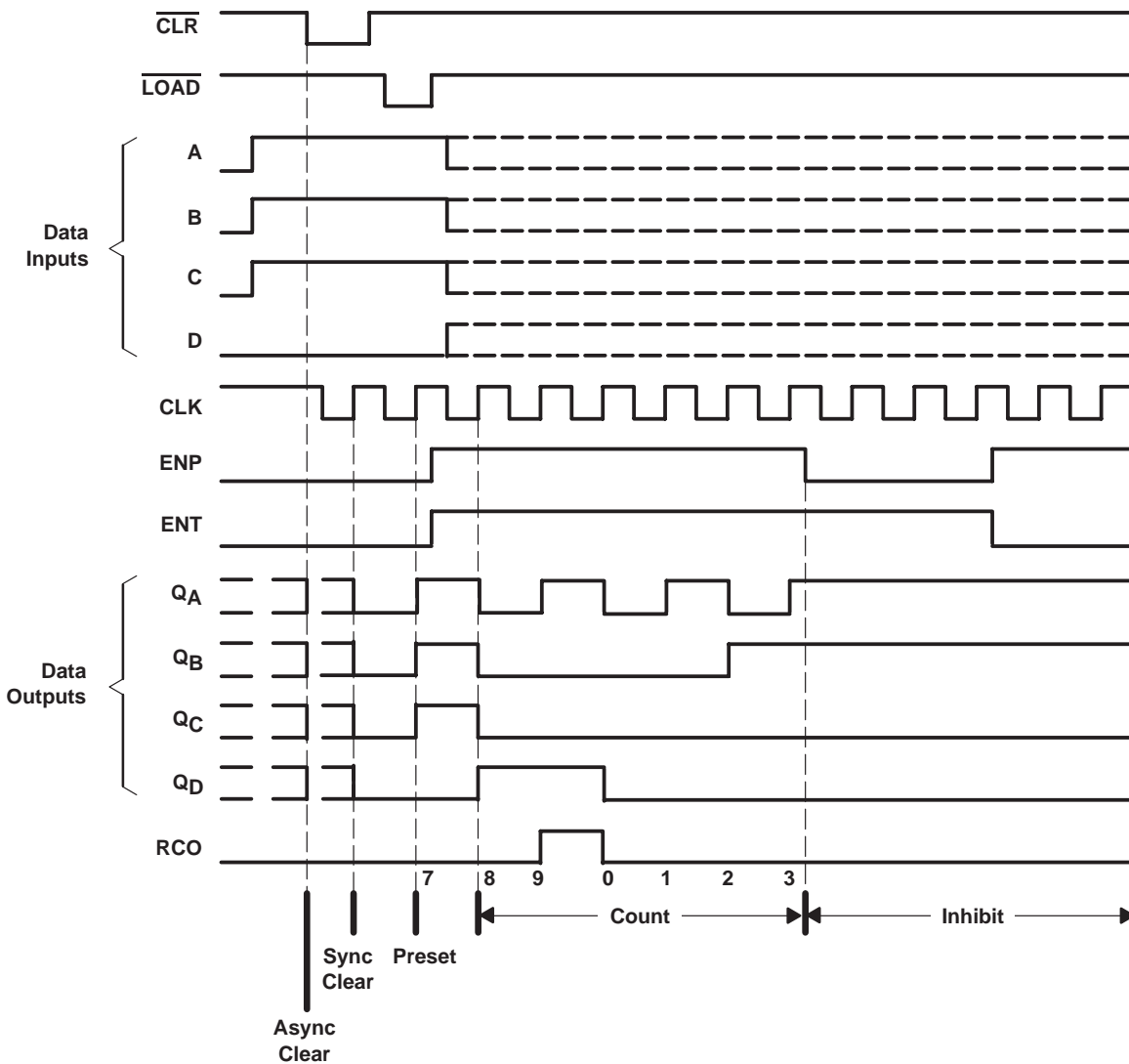
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typical clear, preset, count, and inhibit sequences

SN54ALS162B

The following sequence is illustrated below:

1. Clear outputs to zero (SN54ALS162B is synchronous)
2. Preset to BCD 7
3. Count to 8, 9, 0, 1, 2, and 3
4. Inhibit



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163  
 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163  
 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

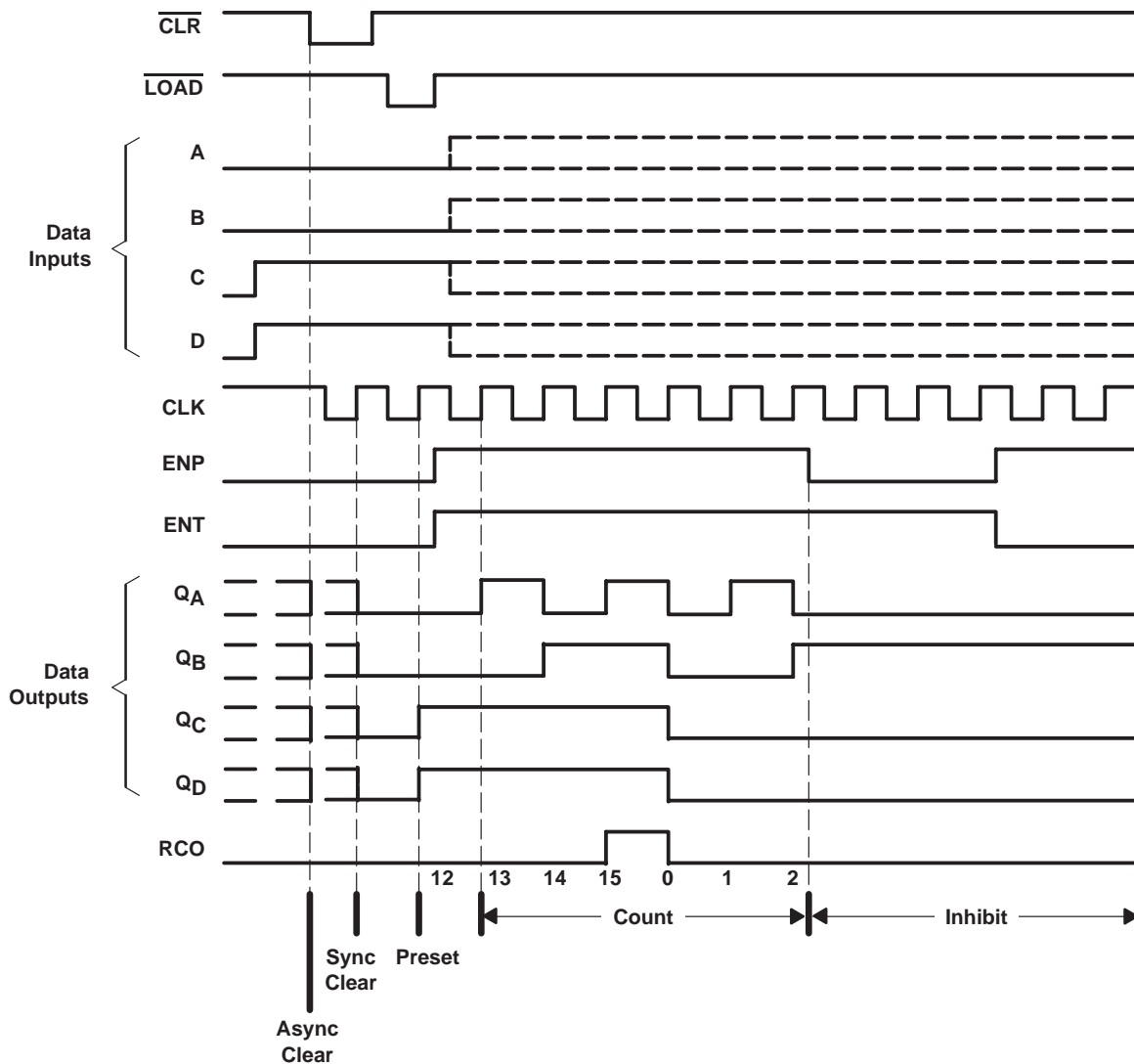
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**typical clear, preset, count, and inhibit sequences**

'ALS161B, 'AS161, 'ALS163B, and 'AS163

The following sequence is illustrated below:

1. Clear outputs to zero ('ALS161B and 'AS161 are asynchronous; 'ALS163B and 'AS163 are synchronous.)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



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**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163  
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163  
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V	
Input voltage range, $V_I$ .....	–0.5 V to 7 V	
Package thermal impedance, $\theta_{JA}$ (see Note 1):	D package .....	73°C/W
	DB package .....	82°C/W
	N package .....	67°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

**recommended operating conditions**

		SN54ALS161B SN54ALS162B SN54ALS163B			SN74ALS161B SN74ALS163B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			–0.4			–0.4	mA
$I_{OL}$	Low-level output current			4			8	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54ALS161B SN54ALS162B SN54ALS163B			SN74ALS161B SN74ALS163B			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			–1.5			–1.5	V
$V_{OH}$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$		0.25	0.4	$I_{OL} = 4\text{ mA}$		V
		$I_{OL} = 8\text{ mA}$				$I_{OL} = 8\text{ mA}$		
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$			20			20	μA
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$			–0.2			–0.2	mA
$I_{O}^{\S}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	–20		–112	–30		–112	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$			12			21	mA

‡ All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current,  $I_{OS}$ .



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163  
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163  
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**timing requirements over recommended operating conditions (unless otherwise noted) (see Figure 1)**

			SN54ALS161B SN54ALS162B SN54ALS163B		SN74ALS161B SN74ALS163B		UNIT	
			MIN	MAX	MIN	MAX		
$f_{clock}$	Clock frequency		22		40		MHz	
$t_w$	Pulse duration	$\overline{CLR}$ high or low	20		12.5		ns	
		'ALS161B	CLR low		15			
$t_{su}$	Setup time, before CLK $\uparrow$	A, B, C, D	50		15		ns	
		$\overline{LOAD}$	20		15			
		'ALS161B	ENP, ENT		25			15
		SN54ALS162B, 'ALS163B			20			
		'ALS161B	CLR inactive		10			10
		SN54ALS162B, 'ALS163B	CLR low		20			
SN54ALS162B, 'ALS163B	CLR high		20		10			
$t_h$	Hold time, all synchronous inputs after CLK $\uparrow$		0		0		ns	

**switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALS161B		SN74ALS161B		UNIT
			MIN	MAX	MIN	MAX	
$f_{max}$			22		40		MHz
$t_{PLH}$	CLK	RCO	5	34	5	20	ns
$t_{PHL}$			5	27	5	20	
$t_{PLH}$	CLK	Any Q	4	19	4	15	ns
$t_{PHL}$			6	25	6	20	
$t_{PLH}$	ENT	RCO	3	18	3	13	ns
$t_{PHL}$			3	17	3	13	
$t_{PHL}$	$\overline{CLR}$	Any Q	8	27	8	24	ns
		RCO	11	32	11	23	

**switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALS162B SN54ALS163B		SN74ALS163B		UNIT
			MIN	MAX	MIN	MAX	
$f_{max}$			22		40		MHz
$t_{PLH}$	CLK	RCO	5	25	5	20	ns
$t_{PHL}$			5	25	5	20	
$t_{PLH}$	CLK	Any Q	4	18	4	15	ns
$t_{PHL}$			6	25	6	20	
$t_{PLH}$	ENT	RCO	3	16	3	13	ns
$t_{PHL}$			3	16	3	13	





**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163  
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163  
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**recommended operating conditions**

		SN54AS161 SN54AS163			SN74AS161 SN74AS163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-2			-2	mA
I <sub>OL</sub>	Low-level output current			20			20	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN54AS161 SN54AS163			SN74AS161 SN74AS163			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.2			-1.2	V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V,	I <sub>OH</sub> = -2 mA	V <sub>CC</sub> - 2			V <sub>CC</sub> - 2			V
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 20 mA	0.25	0.5		0.25	0.5		V
I <sub>I</sub>	LOAD	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V			0.3			0.3	mA
	ENT					0.2		0.2		
	All others					0.1		0.1		
I <sub>IH</sub>	LOAD	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			60			60	μA
	ENT					40		40		
	All others					20		20		
I <sub>IL</sub>	LOAD	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V			-1.5			-1.5	mA
	ENT					-1		-1		
	All others					-0.5		-0.5		
I <sub>O</sub> ‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-30		-112	-30		-112	mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V		35	53		35	53		mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163  
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163  
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**timing requirements over recommended operating conditions (see Figure 1)**

		SN54AS161 SN54AS163		SN74AS161 SN74AS163		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	65		75		MHz
$t_w$	Pulse duration	$\overline{\text{CLR}}$ high or low		7.7	6.7	ns
		'AS161	$\overline{\text{CLR}}$ low	10	8	
$t_{\text{su}}$	Setup time, before CLK $\uparrow$	A, B, C, D		10	8	ns
		$\overline{\text{LOAD}}$		10	8	
		ENP, ENT		10	8	
		'AS161	$\overline{\text{CLR}}$ inactive	10	8	
		'AS163	$\overline{\text{CLR}}$ low	14	12	
			$\overline{\text{CLR}}$ high (inactive)	10	9	
$t_h$	Hold time, all synchronous inputs after CLK $\uparrow$	2		0		ns

**switching characteristics over recommended operating conditions (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54AS161		SN74AS161		UNIT
			MIN	MAX	MIN	MAX	
$f_{\text{max}}$			65*		75		MHz
$t_{\text{PLH}}$	CLK	RCO (with $\overline{\text{LOAD}}$ high)	1	8.5	1	8	ns
		RCO (with $\overline{\text{LOAD}}$ low)	3	17.5	3	16.5	
$t_{\text{PHL}}$	CLK	RCO	2	14	2	12.5	ns
$t_{\text{PLH}}$	CLK	Any Q	1	7.5	1	7	ns
$t_{\text{PHL}}$			2	14	2	13	
$t_{\text{PLH}}$	ENT	RCO	1.5	10	1.5	9	ns
$t_{\text{PHL}}$			1	9.5	1	8.5	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Any Q	2	14	2	13	ns
		RCO	2	14	2	12.5	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating conditions (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54AS163		SN74AS163		UNIT
			MIN	MAX	MIN	MAX	
$f_{\text{max}}$			65*		75		MHz
$t_{\text{PLH}}$	CLK	RCO (with $\overline{\text{LOAD}}$ high)	1	8.5	1	8	ns
		RCO (with $\overline{\text{LOAD}}$ low)	3	17.5	3	16.5	
$t_{\text{PHL}}$	CLK	RCO	2	14	2	12.5	ns
$t_{\text{PLH}}$	CLK	Any Q	1	7.5	1	7	ns
$t_{\text{PHL}}$			2	14	2	13	
$t_{\text{PLH}}$	ENT	RCO	1.5	10	1.5	9	ns
$t_{\text{PHL}}$			1	9.5	1	8.5	

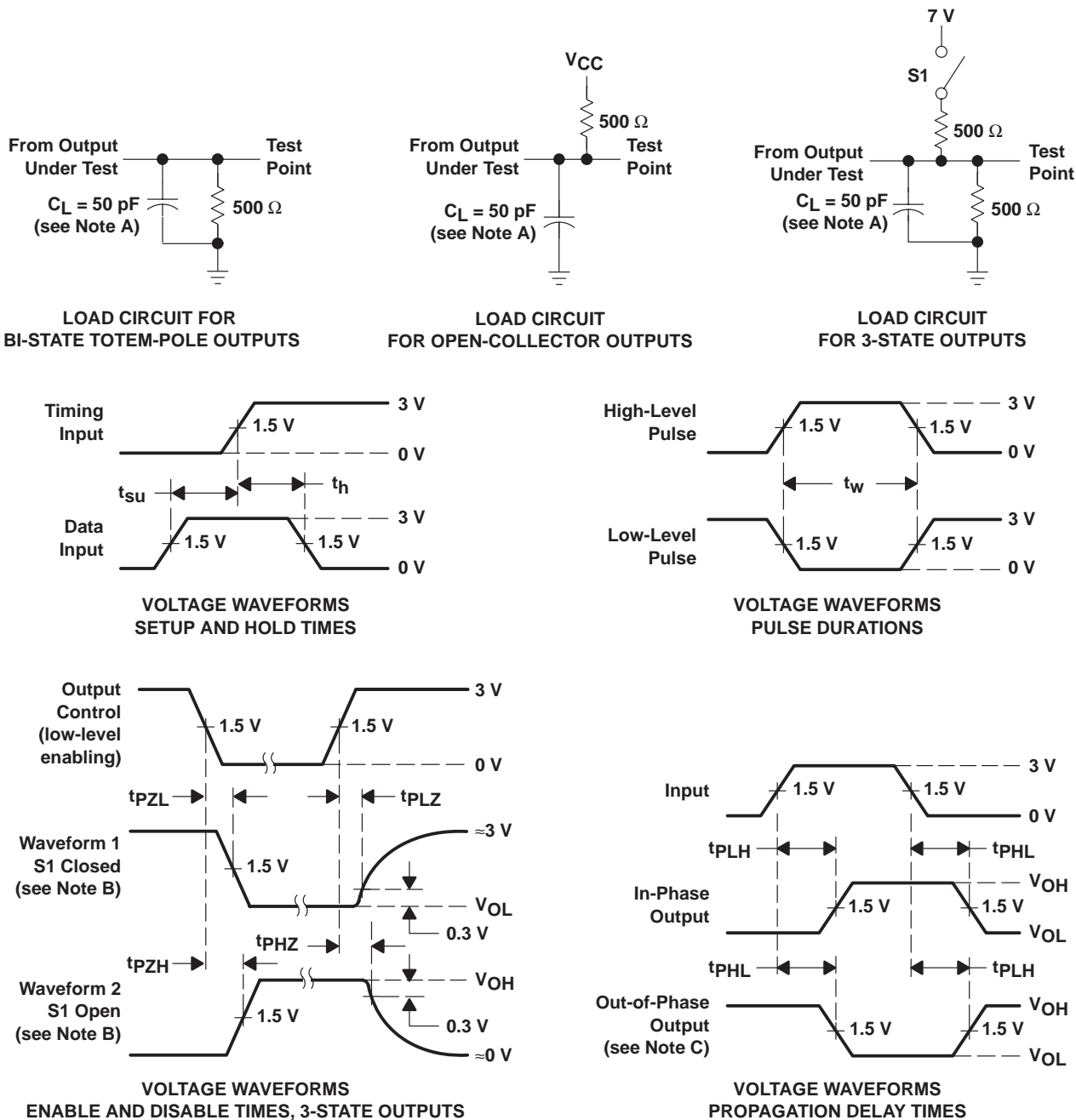
\* On products compliant to MIL-PRF-38535, this parameter is not production tested.



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PARAMETER MEASUREMENT INFORMATION  
 SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

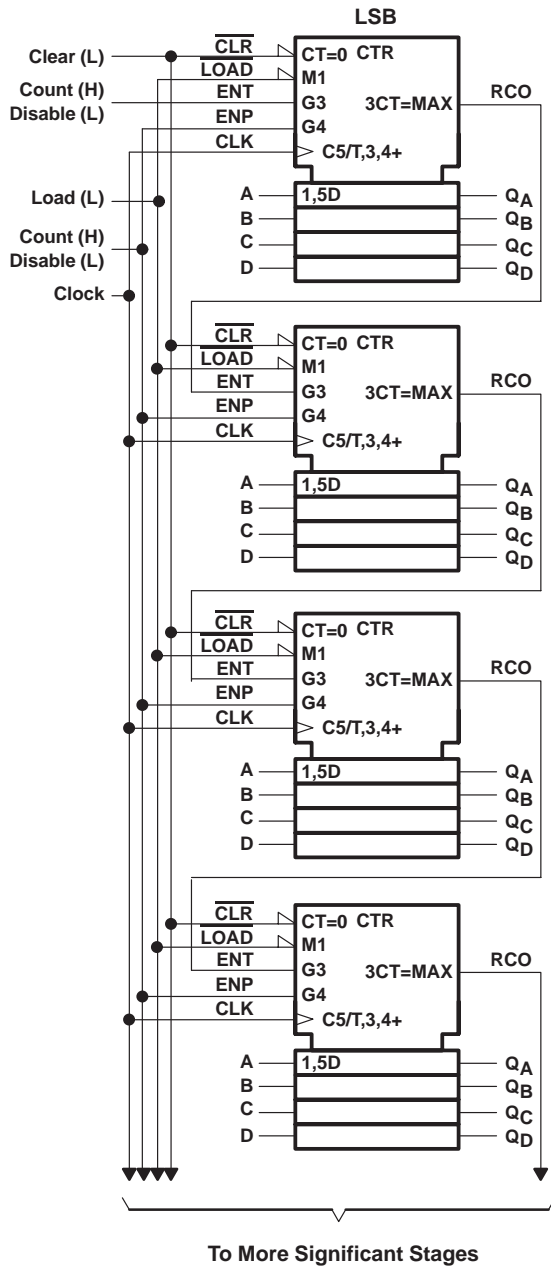
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APPLICATION INFORMATION

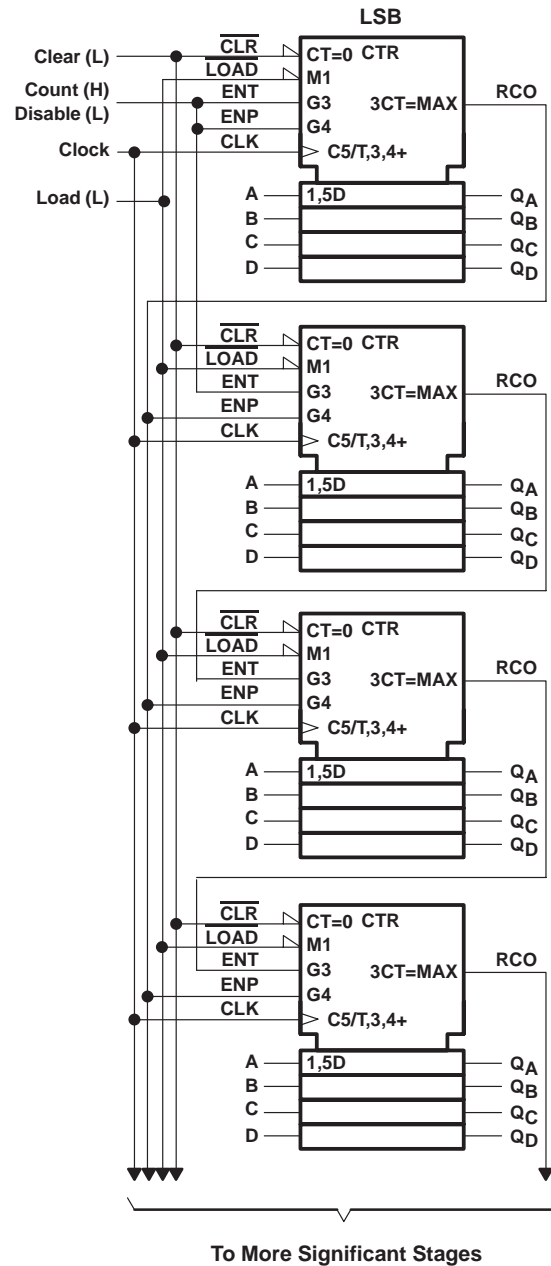
n-bit synchronous counters

This application demonstrates how the ripple-mode carry circuit (see Figure 2) and the carry look-ahead circuit (see Figure 3) can be used to implement a high-speed n-bit counter. The SN54ALS162B counts in BCD. The 'ALS161B, 'AS161, 'ALS163B, and 'AS163 devices count in binary. When additional stages are added, the  $f_{max}$  decreases in Figure 2, but remains unchanged in Figure 3.



$$f_{max} = 1/(\text{CLK to RCO } t_{PLH}) + (\text{ENT to RCO } t_{PLH}) (N - 2) + (\text{ENT } t_{su})$$

Figure 2. Ripple-Mode Carry Circuit



$$f_{max} = 1/(\text{CLK to RCO } t_{PLH}) + (\text{ENP } t_{su})$$

Figure 3. Carry Look-Ahead Circuit



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
83022012A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83022012A SNJ54ALS 161BFK
8302201EA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302201EA SNJ54ALS161BJ
8302201FA	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302201FA SNJ54ALS161BW
83022022A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83022022A SNJ54ALS 163BFK
8302202EA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302202EA SNJ54ALS163BJ
JM38510/38001B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 38001B2A
JM38510/38001BEA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 38001BEA
JM38510/38002B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 38002B2A
JM38510/38002BEA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 38002BEA
SN54ALS161BJ	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS161BJ
SN54ALS163BJ	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS163BJ
SN74ALS161BD	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	0 to 70	ALS161B
SN74ALS161BDR	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS161B
SN74ALS161BN	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS161BN
SN74ALS161BNSR	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS161B
SN74ALS163BD	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	0 to 70	ALS163B
SN74ALS163BDR	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS163B
SN74ALS163BN	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS163BN
SN74ALS163BNSR	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS163B
SN74AS161N	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS161N
SN74AS161NSR	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS161

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74AS163D</a>	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS163
<a href="#">SN74AS163N</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS163N
<a href="#">SNJ54ALS161BFK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83022012A SNJ54ALS 161BFK
<a href="#">SNJ54ALS161BJ</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302201EA SNJ54ALS161BJ
<a href="#">SNJ54ALS161BW</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302201FA SNJ54ALS161BW
<a href="#">SNJ54ALS163BFK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83022022A SNJ54ALS 163BFK
<a href="#">SNJ54ALS163BJ</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302202EA SNJ54ALS163BJ
<a href="#">SNJ54AS161J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54AS161J

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54ALS161B, SN54ALS163B, SN54AS161, SN74ALS161B, SN74ALS163B, SN74AS161 :**

- Catalog : [SN74ALS161B](#), [SN74ALS163B](#), [SN74AS161](#)
- Military : [SN54ALS161B](#), [SN54ALS163B](#), [SN54AS161](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS161BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74ALS161BNSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74ALS163BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74ALS163BNSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AS161NSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS161BDR	SOIC	D	16	2500	353.0	353.0	32.0
SN74ALS161BNSR	SOP	NS	16	2000	356.0	356.0	35.0
SN74ALS163BDR	SOIC	D	16	2500	340.5	336.1	32.0
SN74ALS163BNSR	SOP	NS	16	2000	356.0	356.0	35.0
SN74AS161NSR	SOP	NS	16	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
83022012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8302201FA	W	CFP	16	25	506.98	26.16	6220	NA
83022022A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/38001B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/38002B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/38001B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/38002B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ALS161BN	N	PDIP	16	25	506	13.97	11230	4.32
SN74ALS161BN	N	PDIP	16	25	506	13.97	11230	4.32
SN74ALS163BN	N	PDIP	16	25	506	13.97	11230	4.32
SN74ALS163BN	N	PDIP	16	25	506	13.97	11230	4.32
SN74AS161N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AS161N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AS163D	D	SOIC	16	40	507	8	3940	4.32
SN74AS163N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AS163N	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54ALS161BFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS161BW	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54ALS163BFK	FK	LCCC	20	55	506.98	12.06	2030	NA



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



4220735/A 12/2021

#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

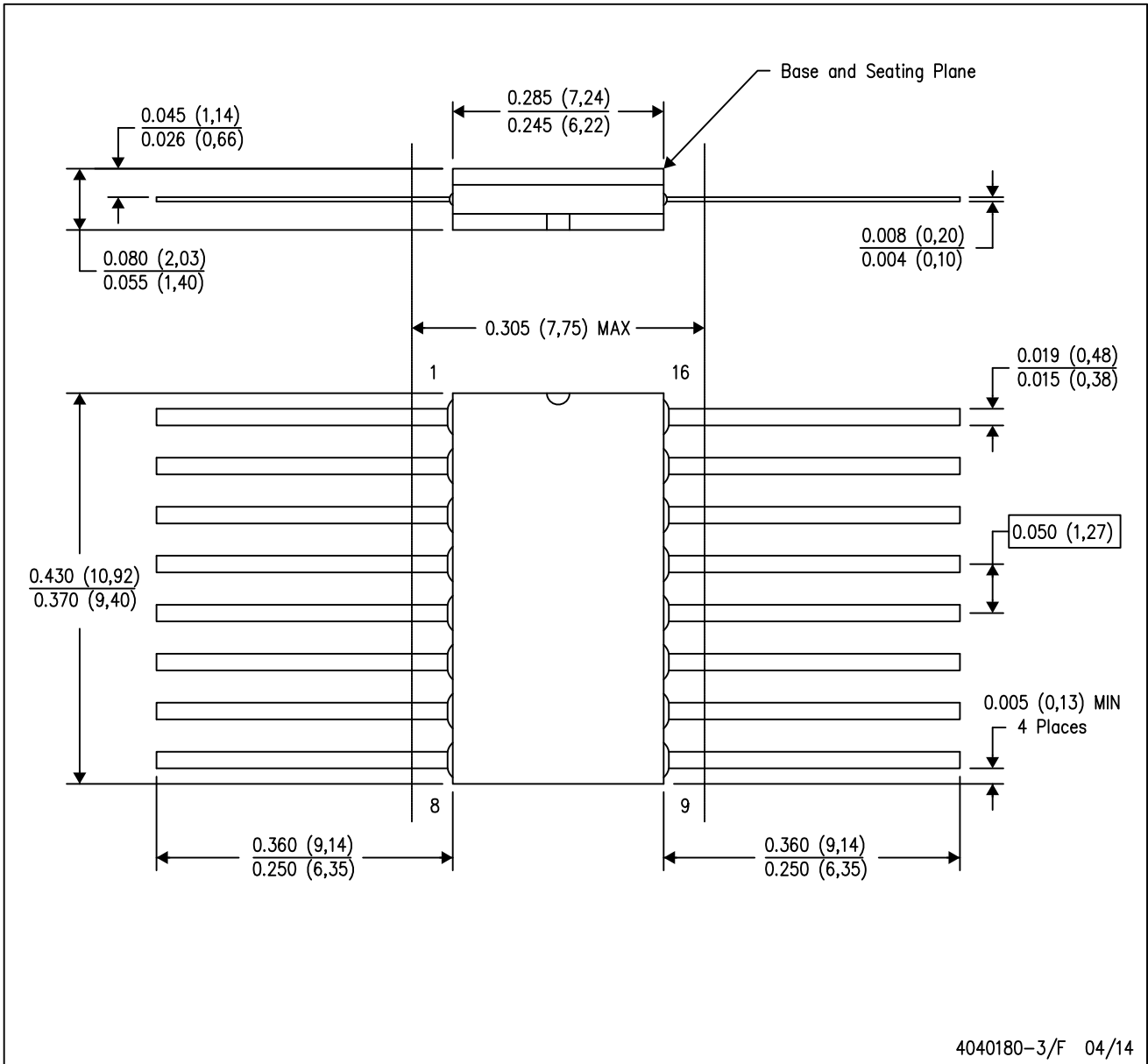
**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16



## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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