2-BIT UNDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR

Check for Samples: SN74AVC2T244

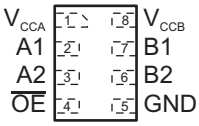
FEATURES

- **Wide Operating V_{CC} Range of 0.9 V to 3.6 V**
- **Low Static-Power Consumption, 6-µA Max I_{CC}**
- **Output Enable Feature Allows User to Disable Outputs to Reduce Power Consumption**
- **±24-mA Output Drive at 3.0 V**
- **I_{off} Supports Partial Power-Down-Mode Operation**
- **Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input**
- **Maximum Data Rates**
  - **380 Mbps (1.8-V to 3.3-V Translation)**
  - **200 Mbps (<1.8-V to 3.3-V Translation)**
  - **200 Mbps (Translate to 2.5 V or 1.8 V)**
  - **150 Mbps (Translate to 1.5 V)**
  - **100 Mbps (Translate to 1.2 V)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **5000-V Human-Body Model (A114-A)**

APPLICATIONS

- **Handset, Smartphone, Tablet, Server**

DQE/DQM PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 2-bit unidirectional translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 0.9 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 0.9 V to 3.6 V. This allows for low-voltage translation between 0.9-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V and 3.6-V voltage nodes. For the SN74AVC2T244, when the output-enable ($\overline{OE}$) input is high, all outputs are placed in the high-impedance state. The SN74AVC2T244 is designed so that the $\overline{OE}$ input circuit is referenced to V_{CCA}. This device is fully specified for partial-power-down applications using Ioff. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	DQE – MicroQFN	SN74AVC2T244DQER	VA
	DQM – MicroQFN	SN74AVC2T244DQMR	VAH

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

PIN DESCRIPTION

PIN	FUNCTION
VCCA	Input Port DC Power Supply
VCCB	Output Port DC Power Supply
GND	Ground
An	Input Port
Bn	Output Port
OE	Output Enable

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
Voltage	DC Supply voltage, V_{CCA} V_{CCB}			–0.5	4.6	V
	DC Input voltage, V_I		A_n	–0.5	4.6	V
	Control Input, V_C		$\overline{OE}$	–0.5	4.6	V
	DC Output voltage, V_O, $V_{CCA} = V_{CCB} = 0$	(Power Down)	B_n	–0.5	4.6	V
		(Active Mode)	B_n	–0.5	4.6	
		3-State Mode	B_n	–0.5	4.6	
	DC Input Diode current, I_{IK}	V_I < GND			–20	mA
	DC Output Diode current, I_{OK}	V_O < GND			–50	mA
	DC Output Source/Sink current, I_O				±50	mA
	DC Supply current per supply pin, I_{CCA}, I_{CCB}				±100	mA
I_{GND}	DC Ground current per ground pin				±100	mA
T_{stg}	Storage temperature range			–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

				MIN	MAX	UNIT
V_{CCA}, V_{CCB}	Positive DC Supply voltage			0.9	3.6	V
V_I	Bus input voltage			GND	3.6	V
V_I	Input voltage			GND	3.6	V
V_C	Control input		$\overline{OE}$	GND	3.6	V
V_O	Bus output voltage	(Power Down Mode)	B_n	GND	3.6	V
		(Active Mode)	B_n	GND	V_{CCB}	V
		3-State Mode	B_n	GND	3.6	V
T_A	Operating free-air temperature			–40	85	°C
$\Delta t/\Delta v$	Input transition rise or fall rate V_I from 30% to 70% of V_{CC}; V_{CC} = 3.3 V ±0.3 V			0	10	nS

ELECTRICAL CHARACTERISTICS(1) (2)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA} (V)	V_{CCB} (V)	–40°C to 85°C		UNIT
					MIN	MAX	
V_{IH}	Input HIGH Voltage (An, $\overline{OE}$)		2.7 – 3.6	0.9 – 3.6	2.0	–	V
			2.3 – 2.7		1.6	–	
			1.4 – 2.3		0.65 × V_{CCA}	–	
			0.9 – 1.4		0.9 × V_{CCA}	–	
V_{IL}	Input LOW voltage (An, $\overline{OE}$)		2.7 – 3.6	0.9 – 3.6	–	0.8	V
			2.3 – 2.7		–	0.7	
			1.4 – 2.3		–	0.35 × V_{CCA}	
			0.9 – 1.5		–	0.1 × V_{CCA}	
V_{OH}	Output HIGH voltage	I_{OH} = –100 µA; V_I = V_H	0.9 – 3.6	0.9 – 3.6	V_{CCB} – 0.2	–	V
		I_{OH} = –0.5 mA; V_I = V_H	0.9	0.9	0.75 × V_{CCB}	–	
		I_{OH} = –2 mA; V_I = V_H	1.4	1.4	1.05	–	
		I_{OH} = –6 mA; V_I = V_H	1.65	1.65	1.25	–	
			2.3	2.3	2.0	–	
		I_{OH} = –12 mA; V_I = V_H	2.3	2.3	1.8	–	
			2.7	2.7	2.2	–	
		I_{OH} = –18 mA; V_I = V_H	2.3	2.3	1.7	–	
			3.0	3.0	2.4	–	
		I_{OH} = –24 mA; V_I = V_H	3.0	3.0	2.2	–	
V_{OL}	Output LOW voltage	I_{OH} = 100 µA; V_I = V_H	0.9 – 3.6	0.9 – 3.6	–	0.2	V
		I_{OH} = 0.5 mA; V_I = V_H	1.1	1.1	–	0.3	
		I_{OH} = 2 mA; V_I = V_H	1.4	1.4	–	0.35	
		I_{OH} = 6 mA; V_I = V_H	1.65	1.65	–	0.3	
		I_{OH} = 12 mA; V_I = V_H	2.3	2.3	–	0.4	
			2.7	2.7	–	0.4	
		I_{OH} = 18 mA; V_I = V_H	2.3	2.3	–	0.6	
			3.0	3.0	–	0.4	
		I_{OH} = 24 mA; V_I = V_H	3.0	3.0	–	0.55	
I_I	Input Leakage Current	V_I = V_{CCA} or GND	0.9 – 3.6	0.9 – 3.6	–1.0	1.5	µA
I_{OFF}	Power-Off Leakage Current	$\overline{OE}$ = 0V	0	0.9 – 3.6	–1.0	1.3	µA
			0.9 – 3.6	0	–1.0	1.5	
I_{CCA}	Quiescent Supply Current	V_I = V_{CCA} or GND; I_O = 0	0.9 – 3.6	0.9 – 3.6	–	3.0	µA
I_{CCB}	Quiescent Supply Current	V_I = V_{CCA} or GND; I_O = 0	0.9 – 3.6	0.9 – 3.6	–	3.0	µA
I_{CCA} + I_{CCB}	Quiescent Supply Current	V_I = V_{CCA} or GND; I_O = 0	0.9 – 3.6	0.9 – 3.6	–	6.0	µA
ΔI_{CCA}	Increase in I_{CC} per Input Voltage, Other inputs at V_{CCA} or GND	V_I = V_{CCA} – 0.3 V; V_I = V_{CCA} or GND	3.6	3.6	–	5.0	µA

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.

ELECTRICAL CHARACTERISTICS(1) (2) (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA} (V)	V_{CCB} (V)	–40°C to 85°C		UNIT
					MIN	MAX	
ΔI_{CCB}	Increase in I_{CC} per Input Voltage, Other inputs at V_{CCA} or GND	$V_I = V_{CCA} - 0.3$ V; $V_I = V_{CCA}$ or GND	3.6	3.6	–	5.0	µA
I_{OZ}	I/O Tri-State Output Leakage Current	TA = 25°C, $\overline{OE}$ = 0 V	0.9 – 3.6	0.9 – 3.6	–1.0	1.0	µA

AC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	V_{CCA} (V)	VCCB (V)	MIN	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation Delay, A_n to B_n	0.9 – 3.6	0.9 – 3.6		20	nS
		1.2 – 3.6	1.2 – 3.6		7	
		1.8 – 3.6	1.8 – 3.6		3.5	
t_{PZH}, t_{PZL}	Output Enable, $\overline{OE}$ to B_n	0.9 – 3.6	0.9 – 3.6		23	nS
		1.2 – 3.6	1.2 – 3.6		6.5	
		1.8 – 3.6	1.8 – 3.6		4.1	
t_{PHZ}, t_{PLZ}	Output Disable, $\overline{OE}$ to B_n	0.9 – 3.6	0.9 – 3.6		17	nS
		1.2 – 3.6	1.2 – 3.6		7	
		1.8 – 3.6	1.8 – 3.6		4.3	
t_{OSHL}, t_{OSLH}	Output to Output Skew, Time	0.9 – 3.6	0.9 – 3.6		0.15	nS
		1.2 – 3.6	1.2 – 3.6		0.15	
		1.8 – 3.6	1.8 – 3.6		0.15	

Table 1. CAPACITANCE(1)

Symbol	Parameter	Test Conditions	TYP(2)	Unit
C_{IN}	Control Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$	3.5	pF
$C_{I/O}$	I/O Pin Input capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$	5.0	pF
C_{PD}	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$, f = 10 MHz	33	pF

(1) C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from: $I_{CC(operating)} \approx C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$ where $I_{CC} = I_{CCA} + I_{CCB}$ and N_{SW} = total number of outputs switching.
(2) Typical values are at TA = +25°C.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AVC2T244DQER	ACTIVE	X2SON	DQE	8	5000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VA	Samples
SN74AVC2T244DQMR	ACTIVE	X2SON	DQM	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

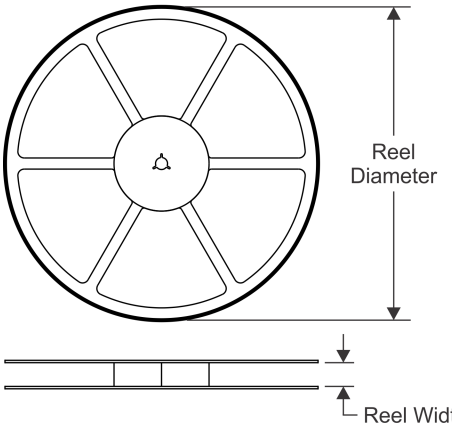
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

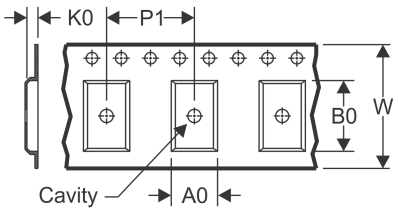
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

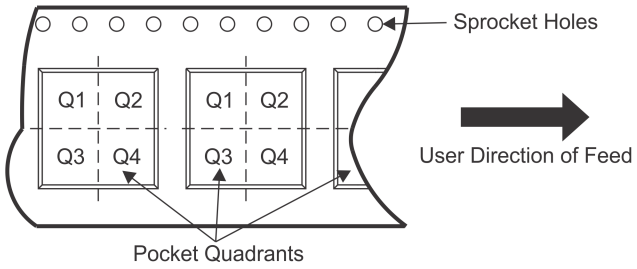


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

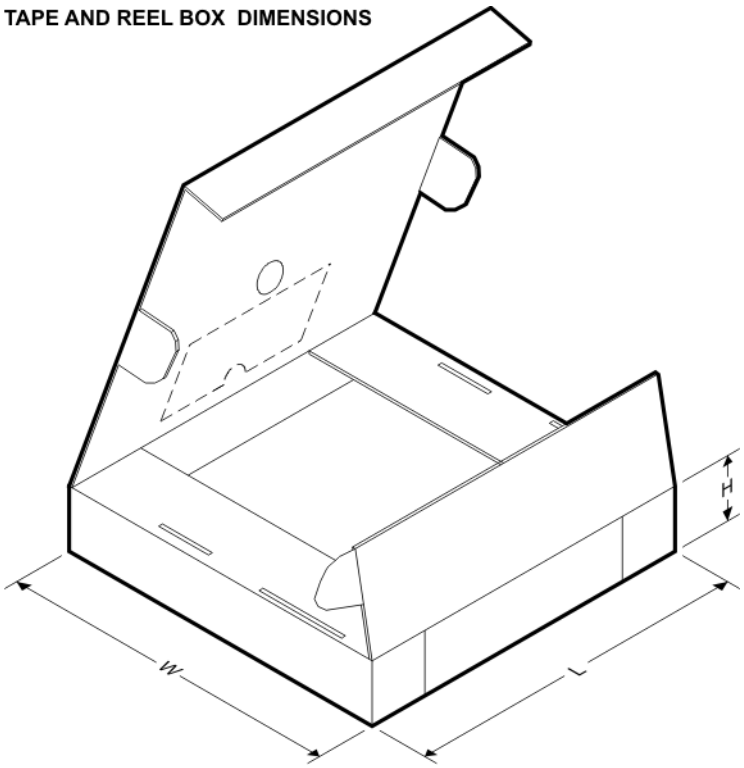
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC2T244DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
SN74AVC2T244DQMR	X2SON	DQM	8	3000	180.0	8.4	1.57	2.21	0.59	4.0	8.0	Q1

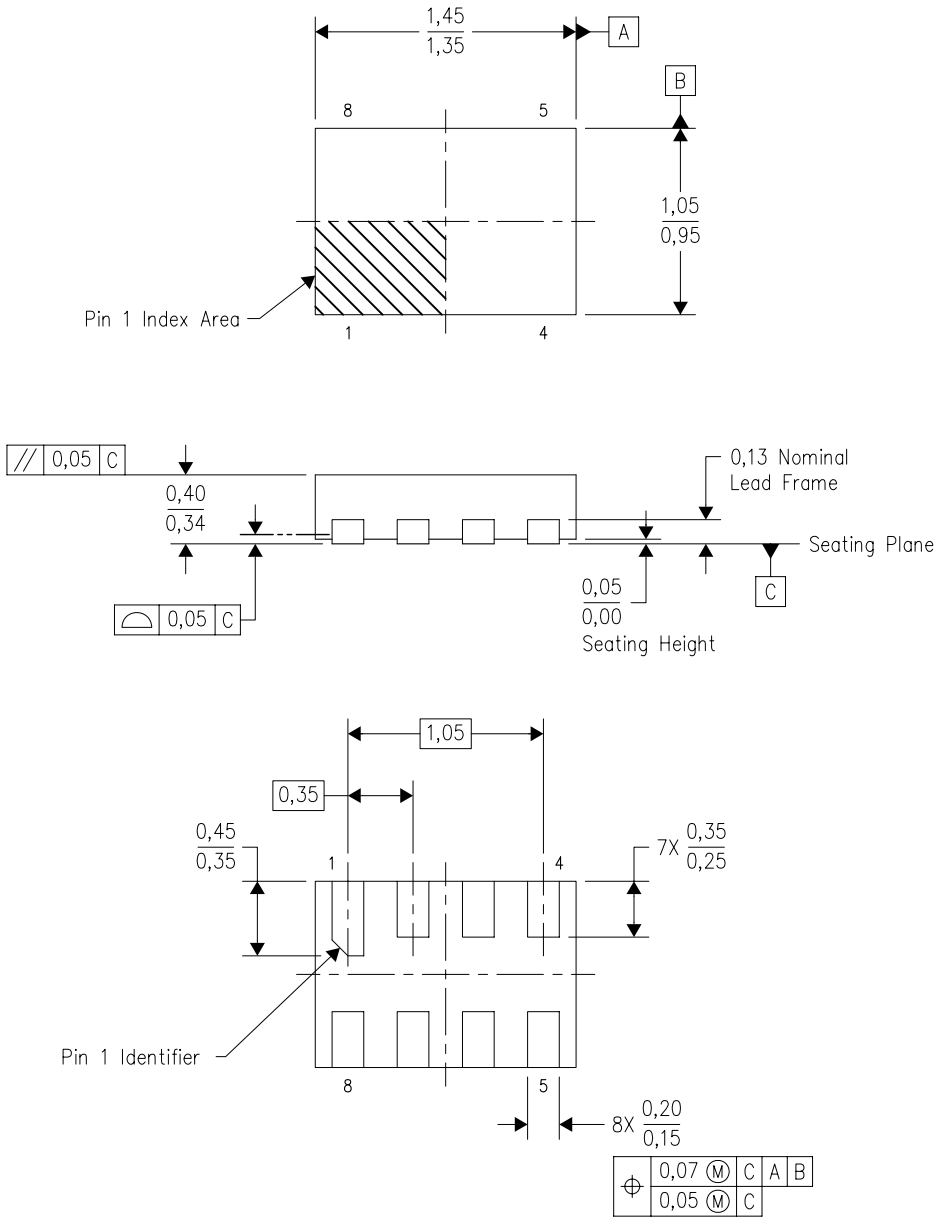
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC2T244DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
SN74AVC2T244DQMR	X2SON	DQM	8	3000	202.0	201.0	28.0

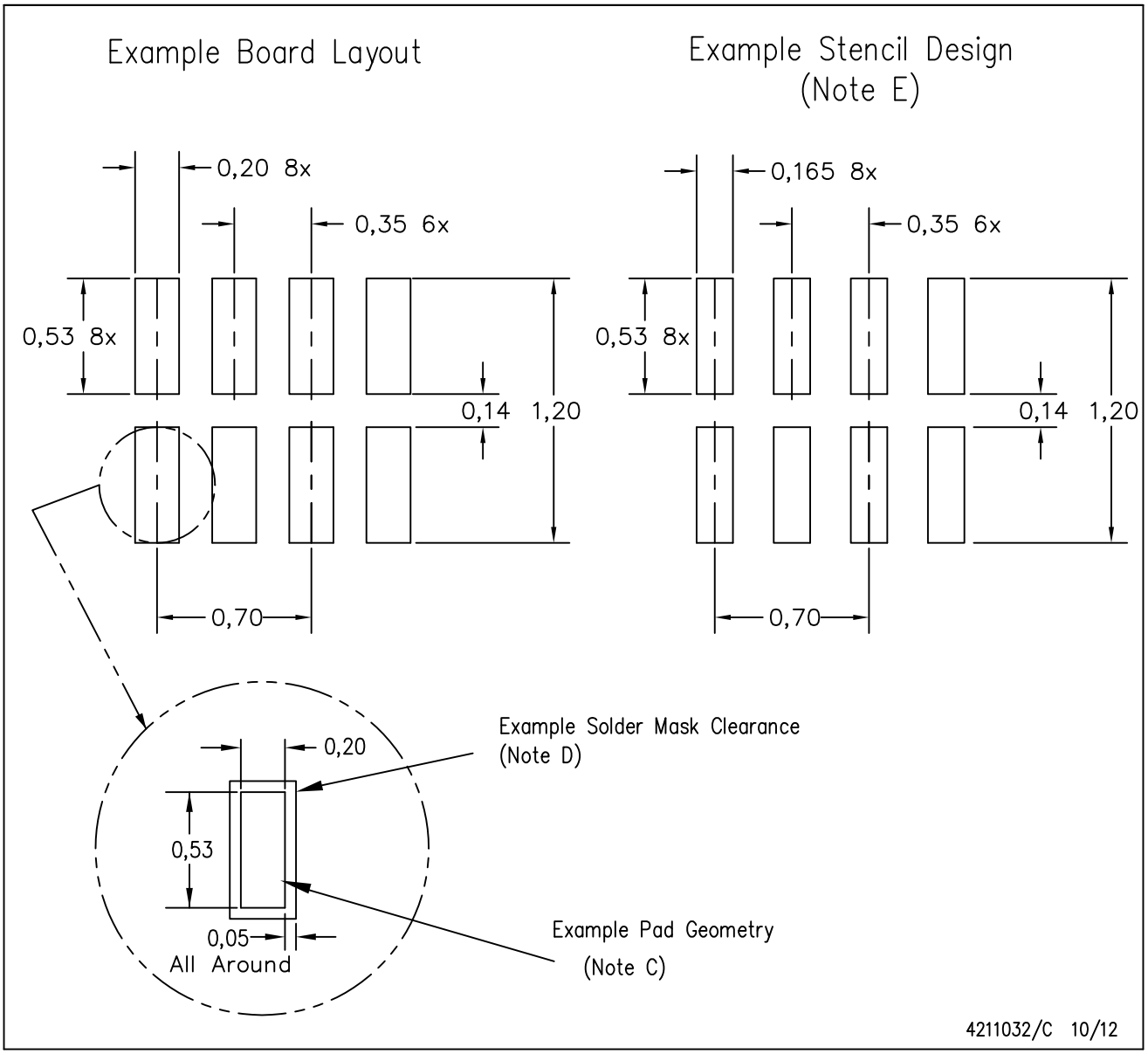
DQE (R–PX2SON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4209779/B 10/2008

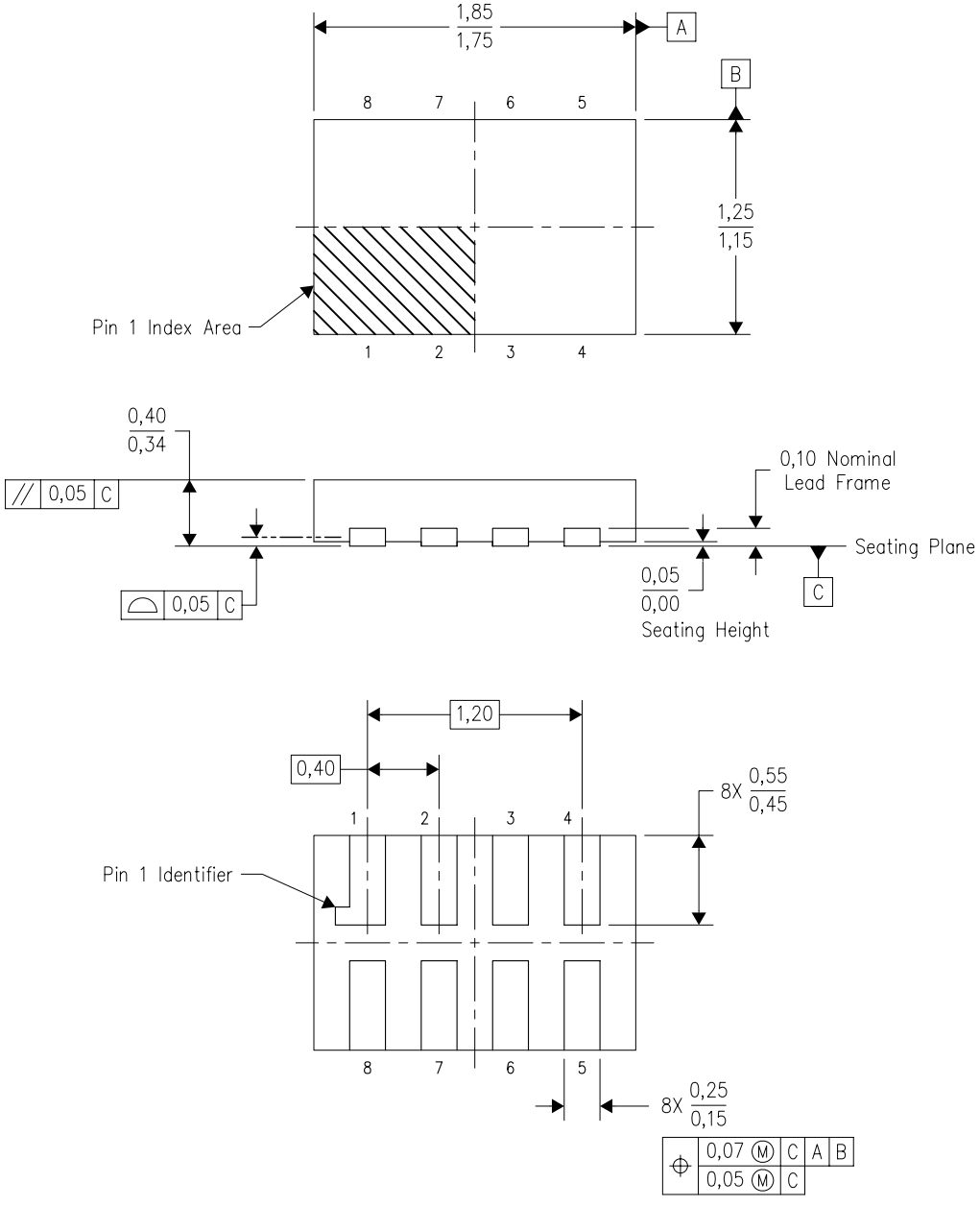
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. This package complies to JEDEC MO–287 variation X2EAF.

DQE (R–PX2SON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Over–printing land for acceptable area ratio is not viable due to land width and bridging potential. Customer may further reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
I. Component placement force should be minimized to prevent excessive paste block deformation.

DQM (R–PX2SON–N8) PLASTIC SMALL OUTLINE NO–LEAD

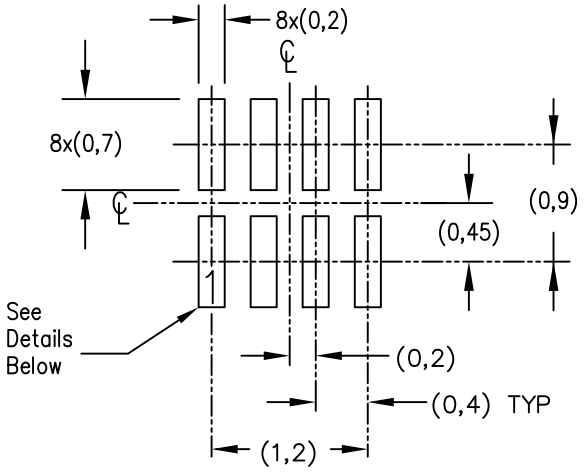


4210302/A 06/2009

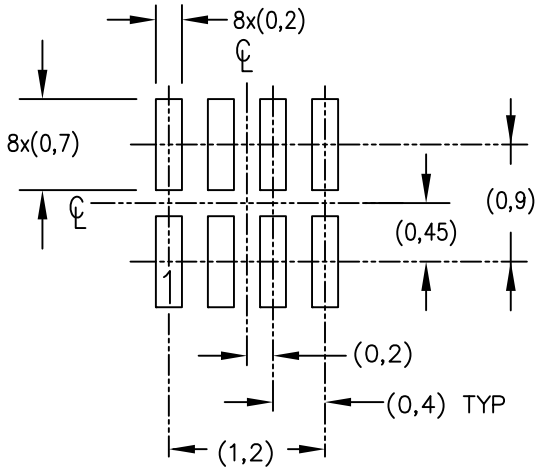
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

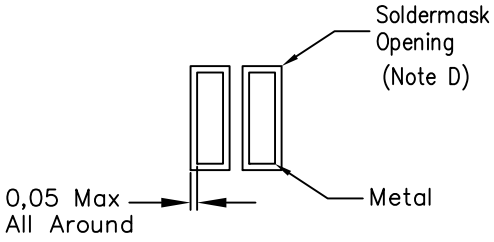
DQM (R–PX2SON–N8) PLASTIC SMALL OUTLINE NO–LEAD

Example Board Layout

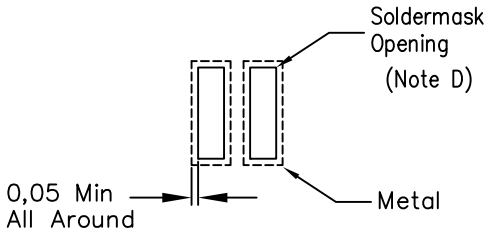


Example Stencil Design
0.1mm Thick Stencil
(Note C)





Non Solder Mask Defined Pad



Solder Mask Defined Pad

Solder Mask Details

4218746/A 07/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
D. Customers should contact their board fabrication site for recommended solder mask tolerances.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265