SN74AXC4T774-Q1 Automotive 4-Bit Dual-Supply Bus Transceiver with Independent Direction, Configurable-Voltage Translation, and Tri-State Outputs

1 Features

- AEC-Q100 qualified for automotive applications
- Fully configurable dual-rail design allows each port to operate with a power supply range from 0.65V to 3.6V
- Operating temperature from –40°C to +125°C
- Independent direction control pins to allow configurable up and down translation
- Glitch-free power supply sequencing
- Up to 310Mbps support when translating from 1.8V to 3.3V
- V_{CC} Isolation Feature:
  - If either V_{CC} input is below 100mV, all I/Os outputs are disabled and become high-impedance
- I_{off} supports partial-power-down mode operation
- Compatible with AVC family level shifters
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD protection exceeds JEDEC JS-001
  - 8000-V Human-Body Model
  - 1000-V Charged-Device Model

2 Applications

- Infotainment head unit
- ADAS fusion
- ADAS front camera
- HEV/EV battery management
- Telematics control unit

3 Description

The SN74AXC4T774-Q1 is a four-bit non-inverting bus transceiver that uses two individually configurable power-supply rails. The device is operational with both V_{CCA} and V_{CCB} supplies as low as 0.65V. The A port is designed to track V_{CCA}, which accepts any supply voltage from 0.65V to 3.6V. The B port is designed to track V_{CCB}, which also accepts any supply voltage from 0.65V to 3.6V. Additionally the SN74AXC4T774-Q1 is compatible with a single-supply system.

The SN74AXC4T774-Q1 device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level of the direction-control inputs (DIRx). The output-enable input ($\overline{OE}$) is used to disable the outputs so the buses are effectively isolated. The SN74AXC4T774-Q1 device is designed so the control pins (DIRx and $\overline{OE}$) are referenced to V_{CCA}.

To put the level shifter I/Os in the high-impedance state during power up or power down, tie the $\overline{OE}$ pin to V_{CCA} through a pullup resistor.

This device is fully specified for partial-power-down applications using the I_{off} current. The I_{off} protection circuitry is designed so that no excessive current is drawn from or to an input, output, or combined I/O that is biased to a specific voltage while the device is powered down.

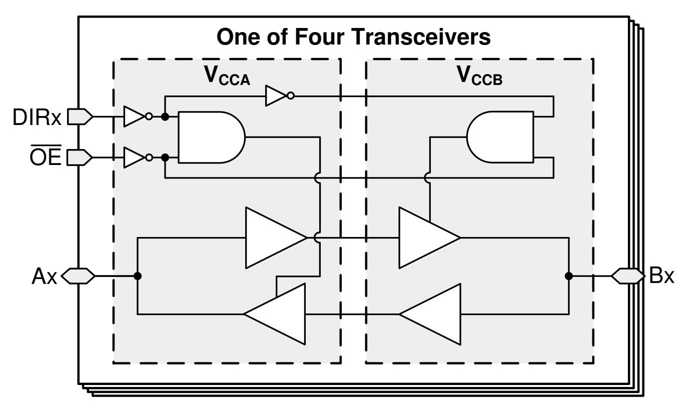
The V_{CC} isolation feature is designed so that if either V_{CCA} or V_{CCB} is less than 100mV, both I/O ports are set to the high-impedance state by disabling their outputs.

Glitch-free power supply sequencing allows either supply rail to be powered on or off in any order while providing robust power sequencing performance.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN74AXC4T774-Q1	PW (TSSOP, 16)	5mm × 6.4mm
	BQB (WQFN, 16)	3.5mm × 2.5mm
	RSV (UQFN, 16)	2.6mm × 1.8mm

(1) For more information, see Section 11
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram

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4 Pin Configuration and Functions

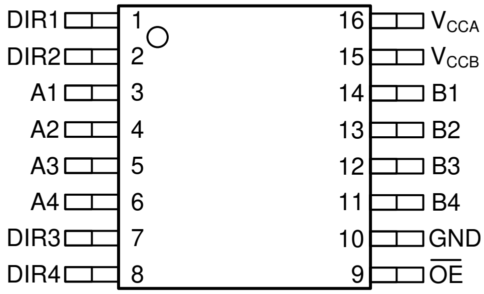


Figure 4-1. PW Package 16-Pin TSSOP Top View

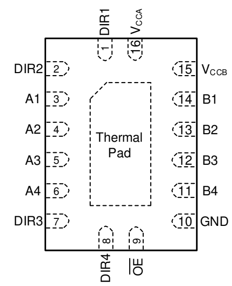


Figure 4-2. BQB Package 16-Pin WQFN Transparent Top View

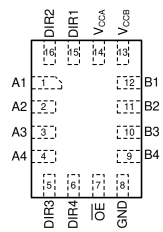


Figure 4-3. RSV Package 16-Pin UQFN Transparent Top View

Pin Functions

PIN	NO.			TYPE	DESCRIPTION
NAME	PW	RSV	BQB		
A1	3	1	3	I/O	Input/output A1. Referenced to V_{CCA}.
A2	4	2	4	I/O	Input/output A2. Referenced to V_{CCA}.
A3	5	3	5	I/O	Input/output A3. Referenced to V_{CCA}.
A4	6	4	6	I/O	Input/output A4. Referenced to V_{CCA}.
B1	14	12	14	I/O	Input/output B1. Referenced to V_{CCB}.
B2	13	11	13	I/O	Input/output B2. Referenced to V_{CCB}.
B3	12	10	12	I/O	Input/output B3. Referenced to V_{CCB}.
B4	11	9	11	I/O	Input/output B4. Referenced to V_{CCB}.
DIR1	1	15	1	I	Direction-control input for port 1. Referenced to V_{CCA}.
DIR2	2	16	2	I	Direction-control input for port 2. Referenced to V_{CCA}.
DIR3	7	5	7	I	Direction-control input for port 3. Referenced to V_{CCA}.
DIR4	8	6	8	I	Direction-control input for port 4. Referenced to V_{CCA}.
$\overline{OE}$	9	7	9	I	Tri-state output enable. Pull $\overline{OE}$ high to place all outputs in tri-state mode. Referenced to V_{CCA}.
GND	10	8	10	—	Ground
V_{CCA}	16	14	16	—	A-port power supply voltage. $0.65V \le V_{CCA} \le 3.6V$
V_{CCB}	15	13	15	—	B-port power supply voltage. $0.65V \le V_{CCB} \le 3.6V$

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	4.2	V
V_{CCB}	Supply voltage B		–0.5	4.2	V
V_I	Input Voltage[(2)]	I/O Ports (A Port)	–0.5	4.2	V
		I/O Ports (B Port)	–0.5	4.2	
		Control Inputs	–0.5	4.2	
V_O	Voltage applied to any output in the high-impedance or power-off state[(2)]	A Port	–0.5	4.2	V
		B Port	–0.5	4.2	
V_O	Voltage applied to any output in the high or low state[(2)] [(3)]	A Port	–0.5	V_{CCA} + 0.2	V
		B Port	–0.5	V_{CCB} + 0.2	
I_{IK}	Input clamp current	V_I < 0	–50		mA
I_{OK}	Output clamp current	V_O < 0	–50		mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions.* Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.2V maximum if the output current rating is observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]	±8000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1] [2]

				MIN	MAX	UNIT
V_{CCA}	Supply voltage A			0.65	3.6	V
V_{CCB}	Supply voltage B			0.65	3.6	V
V_{IH}	High-level input voltage	Data Inputs	V_{CCI} = 0.65V - 0.75V	V_{CCI} x 0.70		
			V_{CCI} = 0.76V - 1V	V_{CCI} x 0.70		
			V_{CCI} = 1.1V - 1.95V	V_{CCI} x 0.65		
			V_{CCI} = 2.3V - 2.7V	1.6		
			V_{CCI} = 3V - 3.6V	2		
		Control Inputs(DIRx, $\overline{OE}$), Referenced to V_{CCA}	V_{CCA} = 0.65V - 0.75V	V_{CCA} x 0.70		
			V_{CCA} = 0.76V - 1V	V_{CCA} x 0.70		
			V_{CCA} = 1.1V - 1.95V	V_{CCA} x 0.65		
			V_{CCA} = 2.3V - 2.7V	1.6		
			V_{CCA} = 3V - 3.6V	2		
V_{IL}	Low-level input voltage	Data Inputs	V_{CCI} = 0.65V - 0.75V		V_{CCI} x 0.30	V
			V_{CCI} = 0.76V - 1V		V_{CCI} x 0.30	
			V_{CCI} = 1.1V - 1.95V		V_{CCI} x 0.35	
			V_{CCI} = 2.3V - 2.7V		0.7	
			V_{CCI} = 3V - 3.6V		0.8	
		Control Inputs(DIRx, $\overline{OE}$), Referenced to V_{CCA}	V_{CCA} = 0.65V - 0.75V		V_{CCA} x 0.30	
			V_{CCA} = 0.76V - 1V		V_{CCA} x 0.30	
			V_{CCA} = 1.1V - 1.95V		V_{CCA} x 0.35	
			V_{CCA} = 2.3V - 2.7V		0.7	
			V_{CCA} = 3V - 3.6V		0.8	
V_I	Input voltage[1]			0	3.6	V
V_O	Output voltage	Active State		0	V_{CCO}	V
		Tri-State		0	3.6	
$\Delta t/\Delta v$[2]	Input transition rise and fall time				10	ns/V
T_A	Operating free-air temperature			–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.V_{CCO} is the V_{CC} associated with the output port.
(2) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, SCBA004.

5.4 Thermal Information

THERMAL METRIC[1]		SN74AXC4T774-Q1			UNIT
		PW (TSSOP)	RSV (UQFN)	BQB (WQFN)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.2	130.8	73.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.6	69.1	70.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.5	59.9	43.5	°C/W
Y_{JT}	Junction-to-top characterization parameter	7.3	3.9	4.9	°C/W
Y_{JB}	Junction-to-board characterization parameter	63.9	58.3	43.5	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	NA	NA	21.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1) (2) (4)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A) –40°C to 85°C MIN	TYP	MAX	–40°C to 125°C MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$V_I = V_{IH}$	I_{OH} = –100µA	0.7V - 3.6V	0.7V - 3.6V	V_{CCO} – 0.1			V_{CCO} – 0.1			V
			I_{OH} = –50µA	0.65V	0.65V	0.55			0.55			
			I_{OH} = –200µA	0.76V	0.76V	0.58			0.58			
			I_{OH} = –500µA	0.85V	0.85V	0.65			0.65			
			I_{OH} = –3mA	1.1V	1.1V	0.85			0.85			
			I_{OH} = –6mA	1.4V	1.4V	1.05			1.05			
			I_{OH} = –8mA	1.65V	1.65V	1.2			1.2			
			I_{OH} = –9mA	2.3V	2.3V	1.75			1.75			
			I_{OH} = –12mA	3V	3V	2.3			2.3			
V_{OL}	Low-level output voltage	$V_I = V_{IL}$	I_{OL} = 100µA	0.7V - 3.6V	0.7V - 3.6V			0.1			0.1	V
			I_{OL} = 50µA	0.65V	0.65V			0.1			0.1	
			I_{OL} = 200µA	0.76V	0.76V			0.18			0.18	
			I_{OL} = 500µA	0.85V	0.85V			0.2			0.2	
			I_{OL} = 3mA	1.1V	1.1V			0.25			0.25	
			I_{OL} = 6mA	1.4V	1.4V			0.35			0.35	
			I_{OL} = 8mA	1.65V	1.65V			0.45			0.45	
			I_{OL} = 9mA	2.3V	2.3V			0.55			0.55	
			I_{OL} = 12mA	3V	3V			0.7			0.7	
I_I	Input leakage current	Control inputs (DIRx, $\overline{OE}$):V_I = V_{CCA} or GND		0.65V- 3.6V	0.65V- 3.6V	–0.5		0.5	–1		1	µA
		Data Inputs (Ax, Bx),V_I = V_{CCI} or GND		0.65V- 3.6V	0.65V- 3.6V	–4		4	–8		8	µA
I_{off}	Partial power down current	A Port: V_I or V_O = 0V - 3.6V		0V	0V - 3.6V	–4		4	–8		8	µA
		B Port: V_I or V_O = 0V - 3.6V		0V - 3.6V	0V	–4		4	–8		8	
I_{OZ}	Tri-state output current (3)	A or B Port, V_I = V_{CCI} or GND, V_O = V_{CCO} or GND, $\overline{OE}$ = V_{IH}		3.6V	3.6V	–4		4	–8		8	µA
I_{CCA}	V_{CCA} supply current	V_I = V_{CCI} or GND	I_O = 0	0.65V- 3.6V	0.65V- 3.6V			15			27	µA
				0V	3.6V	–2			–12			
				3.6V	0V			10			18	
I_{CCB}	V_{CCB} supply current	V_I = V_{CCI} or GND	I_O = 0	0.65V- 3.6V	0.65V- 3.6V			15			27	µA
				0V	3.6V			10			18	
				3.6V	0V	–2			–12			
I_{CCA} + I_{CCB}	Combined supply current	V_I = V_{CCI} or GND	I_O = 0	0.65V- 3.6V	0.65V- 3.6V			21			40	µA
C_i	Control Input Capacitance	V_I = 3.3V or GND		3.3V	3.3V		4.5			4.5		pF
C_{io}	Data I/O Capacitance	$\overline{OE}$ = V_{CCA}, V_O = 1.65V DC +1MHz -16dBm sine wave		3.3V	3.3V		6.5			6.5		pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) All typical data is taken at 25°C.

5.6 Switching Characteristics, V_{CCA} = 0.7 ± 0.05V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B–Port Supply Voltage (V_{CCB})																UNIT
					0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V		3.3 ± 0.3V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	172	0.5	120	0.5	88	0.5	51	0.5	46	0.5	56	0.5	78	0.5	221	ns
				–40°C to 125°C	0.5	172	0.5	120	0.5	88	0.5	51	0.5	46	0.5	56	0.5	78	0.5	221	
		B	A	–40°C to 85°C	0.5	172	0.5	141	0.5	109	0.5	51	0.5	16	0.5	12	0.5	9	0.5	9	
				–40°C to 125°C	0.5	172	0.5	141	0.5	109	0.5	51	0.5	16	0.5	12	0.5	9	0.5	9	
t_{dis}	Disable time	$\overline{OE}$	A	–40°C to 85°C	0.5	205	0.5	205	0.5	205	0.5	205	0.5	205	0.5	205	0.5	205	0.5	205	ns
				–40°C to 125°C	0.5	205	0.5	205	0.5	205	0.5	205	0.5	205	0.5	205	0.5	205	0.5	205	
		$\overline{OE}$	B	–40°C to 85°C	0.5	189	0.5	161	0.5	145	0.5	102	0.5	99	0.5	102	0.5	113	0.5	176	
				–40°C to 125°C	0.5	189	0.5	161	0.5	145	0.5	102	0.5	99	0.5	102	0.5	113	0.5	176	
t_{en}	Enable time	$\overline{OE}$	A	–40°C to 85°C	0.5	287	0.5	287	0.5	287	0.5	287	0.5	287	0.5	287	0.5	287	0.5	287	ns
				–40°C to 125°C	0.5	287	0.5	287	0.5	287	0.5	287	0.5	287	0.5	287	0.5	287	0.5	287	
		$\overline{OE}$	B	–40°C to 85°C	0.5	309	0.5	219	0.5	177	0.5	133	0.5	127	0.5	132	0.5	165	0.5	418	
				–40°C to 125°C	0.5	309	0.5	219	0.5	177	0.5	133	0.5	127	0.5	132	0.5	165	0.5	418	

5.7 Switching Characteristics, V_{CCA} = 0.8 ± 0.04V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB}) 0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V		3.3 ± 0.3V		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	141	0.5	96	0.5	73	0.5	39	0.5	29	0.5	28	0.5	29	0.5	40	ns
				–40°C to 125°C	0.5	141	0.5	96	0.5	73	0.5	39	0.5	29	0.5	28	0.5	29	0.5	40	
		B	A	–40°C to 85°C	0.5	120	0.5	96	0.5	76	0.5	39	0.5	16	0.5	11	0.5	9	0.5	9	
				–40°C to 125°C	0.5	120	0.5	96	0.5	76	0.5	39	0.5	16	0.5	12	0.5	9	0.5	9	
t_{dis}	Disable time	$\overline{OE}$	A	–40°C to 85°C	0.5	114	0.5	114	0.5	114	0.5	114	0.5	114	0.5	114	0.5	114	0.5	114	ns
				–40°C to 125°C	0.5	114	0.5	114	0.5	114	0.5	114	0.5	114	0.5	114	0.5	114	0.5	114	
		$\overline{OE}$	B	–40°C to 85°C	0.5	156	0.5	131	0.5	116	0.5	71	0.5	67	0.5	68	0.5	70	0.5	84	
				–40°C to 125°C	0.5	156	0.5	131	0.5	116	0.5	71	0.5	67	0.5	68	0.5	70	0.5	84	
t_{en}	Enable time	$\overline{OE}$	A	–40°C to 85°C	0.5	161	0.5	161	0.5	161	0.5	161	0.5	161	0.5	161	0.5	161	0.5	161	ns
				–40°C to 125°C	0.5	161	0.5	161	0.5	161	0.5	161	0.5	161	0.5	161	0.5	161	0.5	161	
		$\overline{OE}$	B	–40°C to 85°C	0.5	258	0.5	174	0.5	137	0.5	90	0.5	73	0.5	71	0.5	77	0.5	106	
				–40°C to 125°C	0.5	258	0.5	174	0.5	137	0.5	90	0.5	73	0.5	71	0.5	77	0.5	106	

5.8 Switching Characteristics, V_{CCA} = 0.9 ± 0.045V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																UNIT
					0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V		3.3 ± 0.3V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	109	0.5	76	0.5	60	0.5	33	0.5	23	0.5	21	0.5	21	0.5	24	ns
				–40°C to 125°C	0.5	109	0.5	76	0.5	60	0.5	33	0.5	23	0.5	21	0.5	21	0.5	24	
		B	A	–40°C to 85°C	0.5	88	0.5	73	0.5	60	0.5	33	0.5	16	0.5	11	0.5	9	0.5	9	
				–40°C to 125°C	0.5	88	0.5	73	0.5	60	0.5	33	0.5	16	0.5	12	0.5	9	0.5	9	
t_{dis}	Disable time	$\overline{OE}$	A	–40°C to 85°C	0.5	83	0.5	83	0.5	83	0.5	83	0.5	83	0.5	83	0.5	83	0.5	83	ns
				–40°C to 125°C	0.5	83	0.5	83	0.5	83	0.5	83	0.5	83	0.5	83	0.5	83	0.5	83	
		$\overline{OE}$	B	–40°C to 85°C	0.5	138	0.5	112	0.5	97	0.5	51	0.5	46	0.5	46	0.5	46	0.5	54	
				–40°C to 125°C	0.5	138	0.5	112	0.5	97	0.5	51	0.5	46	0.5	46	0.5	46	0.5	54	
t_{en}	Enable time	$\overline{OE}$	A	–40°C to 85°C	0.5	94	0.5	94	0.5	94	0.5	94	0.5	94	0.5	94	0.5	94	0.5	94	ns
				–40°C to 125°C	0.5	94	0.5	94	0.5	94	0.5	94	0.5	94	0.5	94	0.5	94	0.5	94	
		$\overline{OE}$	B	–40°C to 85°C	0.5	203	0.5	140	0.5	110	0.5	70	0.5	52	0.5	45	0.5	43	0.5	51	
				–40°C to 125°C	0.5	203	0.5	140	0.5	110	0.5	74	0.5	54	0.5	47	0.5	43	0.5	51	

5.9 Switching Characteristics, V_{CCA} = 1.2 ± 0.1V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																UNIT
					0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V		3.3 ± 0.3V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	50	0.5	39	0.5	33	0.5	20	0.5	14	0.5	12	0.5	10	0.5	12	ns
				–40°C to 125°C	0.5	50	0.5	39	0.5	33	0.5	20	0.5	14	0.5	12	0.5	10	0.5	12	
		B	A	–40°C to 85°C	0.5	51	0.5	39	0.5	33	0.5	20	0.5	15	0.5	11	0.5	8	0.5	7	
				–40°C to 125°C	0.5	51	0.5	39	0.5	33	0.5	20	0.5	15	0.5	12	0.5	8	0.5	7	
t_{dis}	Disable time	$\overline{OE}$	A	–40°C to 85°C	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	0.5	28	ns
				–40°C to 125°C	0.5	29	0.5	29	0.5	29	0.5	29	0.5	29	0.5	29	0.5	29	0.5	29	
		$\overline{OE}$	B	–40°C to 85°C	0.5	123	0.5	95	0.5	78	0.5	33	0.5	26	0.5	25	0.5	23	0.5	26	
				–40°C to 125°C	0.5	124	0.5	95	0.5	79	0.5	34	0.5	27	0.5	26	0.5	24	0.5	26	
t_{en}	Enable time	$\overline{OE}$	A	–40°C to 85°C	0.5	39	0.5	39	0.5	39	0.5	39	0.5	39	0.5	39	0.5	39	0.5	39	ns
				–40°C to 125°C	0.5	40	0.5	40	0.5	40	0.5	40	0.5	40	0.5	40	0.5	40	0.5	40	
		$\overline{OE}$	B	–40°C to 85°C	0.5	124	0.5	87	0.5	70	0.5	51	0.5	38	0.5	33	0.5	26	0.5	25	
				–40°C to 125°C	0.5	124	0.5	87	0.5	70	0.5	55	0.5	42	0.5	36	0.5	28	0.5	26	

5.10 Switching Characteristics, V_{CCA} = 1.5 ± 0.1V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																UNIT
					0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V		3.3 ± 0.3V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	16	0.5	16	0.5	16	0.5	15	0.5	11	0.5	10	0.5	8	0.5	10	ns
				–40°C to 125°C	0.5	16	0.5	16	0.5	16	0.5	15	0.5	11	0.5	10	0.5	8	0.5	10	
		B	A	–40°C to 85°C	0.5	47	0.5	29	0.5	23	0.5	14	0.5	11	0.5	9	0.5	7	0.5	6	
				–40°C to 125°C	0.5	47	0.5	29	0.5	23	0.5	14	0.5	11	0.5	9	0.5	7	0.5	6	
t_{dis}	Disable time	$\overline{OE}$	A	–40°C to 85°C	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	ns
				–40°C to 125°C	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	
		$\overline{OE}$	B	–40°C to 85°C	0.5	120	0.5	91	0.5	74	0.5	29	0.5	22	0.5	20	0.5	20	0.5	20	
				–40°C to 125°C	0.5	120	0.5	92	0.5	75	0.5	30	0.5	23	0.5	22	0.5	19	0.5	20	
t_{en}	Enable time	$\overline{OE}$	A	–40°C to 85°C	0.5	24	0.5	24	0.5	24	0.5	24	0.5	24	0.5	24	0.5	24	0.5	24	ns
				–40°C to 125°C	0.5	25	0.5	25	0.5	25	0.5	25	0.5	25	0.5	25	0.5	25	0.5	25	
		$\overline{OE}$	B	–40°C to 85°C	0.5	28	0.5	29	0.5	33	0.5	41	0.5	31	0.5	27	0.5	22	0.5	19	
				–40°C to 125°C	0.5	29	0.5	30	0.5	33	0.5	42	0.5	33	0.5	29	0.5	24	0.5	21	

5.11 Switching Characteristics, V_{CCA} = 1.8 ± 0.15V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																UNIT
					0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V		3.3 ± 0.3V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	12	0.5	11	0.5	11	0.5	11	0.5	9	0.5	8	0.5	7	0.5	7	ns
				–40°C to 125°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	9	0.5	9	0.5	7	0.5	7	
		B	A	–40°C to 85°C	0.5	56	0.5	28	0.5	21	0.5	12	0.5	10	0.5	8	0.5	6	0.5	5	
				–40°C to 125°C	0.5	56	0.5	28	0.5	21	0.5	12	0.5	10	0.5	9	0.5	7	0.5	6	
t_{dis}	Disable time	$\overline{OE}$	A	–40°C to 85°C	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	ns
				–40°C to 125°C	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	
		$\overline{OE}$	B	–40°C to 85°C	0.5	117	0.5	90	0.5	73	0.5	28	0.5	21	0.5	19	0.5	16	0.5	18	
				–40°C to 125°C	0.5	119	0.5	90	0.5	74	0.5	29	0.5	22	0.5	20	0.5	17	0.5	18	
t_{en}	Enable time	$\overline{OE}$	A	–40°C to 85°C	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	ns
				–40°C to 125°C	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	
		$\overline{OE}$	B	–40°C to 85°C	0.5	21	0.5	20	0.5	20	0.5	32	0.5	27	0.5	24	0.5	20	0.5	18	
				–40°C to 125°C	0.5	22	0.5	22	0.5	22	0.5	34	0.5	29	0.5	26	0.5	22	0.5	19	

5.12 Switching Characteristics, V_{CCA} = 2.5 ± 0.2V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})																UNIT
					0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V		3.3 ± 0.3V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	10	0.5	10	0.5	9	0.5	8	0.5	7	0.5	6	0.5	6	0.5	6	ns
				–40°C to 125°C	0.5	10	0.5	10	0.5	9	0.5	8	0.5	7	0.5	7	0.5	6	0.5	6	
		B	A	–40°C to 85°C	0.5	78	0.5	30	0.5	21	0.5	10	0.5	8	0.5	7	0.5	6	0.5	5	
				–40°C to 125°C	0.5	78	0.5	30	0.5	21	0.5	10	0.5	8	0.5	7	0.5	6	0.5	5	
t_{dis}	Disable time	$\overline{OE}$	A	–40°C to 85°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	ns
				–40°C to 125°C	0.5	14	0.5	14	0.5	14	0.5	14	0.5	14	0.5	14	0.5	14	0.5	14	
		$\overline{OE}$	B	–40°C to 85°C	0.5	115	0.5	89	0.5	72	0.5	26	0.5	19	0.5	18	0.5	14	0.5	17	
				–40°C to 125°C	0.5	117	0.5	89	0.5	72	0.5	28	0.5	21	0.5	19	0.5	15	0.5	17	
t_{en}	Enable time	$\overline{OE}$	A	–40°C to 85°C	0.5	14	0.5	14	0.5	14	0.5	14	0.5	14	0.5	14	0.5	14	0.5	14	ns
				–40°C to 125°C	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	
		$\overline{OE}$	B	–40°C to 85°C	0.5	15	0.5	14	0.5	13	0.5	14	0.5	15	0.5	16	0.5	15	0.5	15	
				–40°C to 125°C	0.5	16	0.5	15	0.5	15	0.5	16	0.5	17	0.5	18	0.5	17	0.5	16	

5.13 Switching Characteristics, V_{CCA} = 3.3 ± 0.3V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

PARAMETER		FROM	TO	Test Condtions	B-Port Supply Voltage (V_{CCB})																UNIT
					0.7 ± 0.05V		0.8 ± 0.04V		0.9 ± 0.045V		1.2 ± 0.1V		1.5 ± 0.1V		1.8 ± 0.15V		2.5 ± 0.2V		3.3 ± 0.3V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	–40°C to 85°C	0.5	10	0.5	9	0.5	9	0.5	8	0.5	6	0.5	6	0.5	5	0.5	5	ns
				–40°C to 125°C	0.5	10	0.5	9	0.5	9	0.5	8	0.5	6	0.5	6	0.5	5	0.5	5	
		B	A	–40°C to 85°C	0.5	221	0.5	40	0.5	24	0.5	12	0.5	10	0.5	7	0.5	6	0.5	5	
				–40°C to 125°C	0.5	221	0.5	40	0.5	24	0.5	12	0.5	10	0.5	7	0.5	6	0.5	5	
t_{dis}	Disable time	$\overline{OE}$	A	–40°C to 85°C	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	ns
				–40°C to 125°C	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	
		$\overline{OE}$	B	–40°C to 85°C	0.5	115	0.5	89	0.5	72	0.5	26	0.5	19	0.5	17	0.5	14	0.5	16	
				–40°C to 125°C	0.5	117	0.5	89	0.5	72	0.5	27	0.5	20	0.5	18	0.5	14	0.5	16	
t_{en}	Enable time	$\overline{OE}$	A	–40°C to 85°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	ns
				–40°C to 125°C	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	0.5	13	
		$\overline{OE}$	B	–40°C to 85°C	0.5	13	0.5	12	0.5	11	0.5	11	0.5	11	0.5	12	0.5	12	0.5	12	
				–40°C to 125°C	0.5	14	0.5	12	0.5	12	0.5	12	0.5	12	0.5	13	0.5	13	0.5	13	

5.14 Operating Characteristics: T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
C_{pdA}	Power Dissipation Capacitance per transceiver (A to B: outputs enabled)	C_L = 0, R_L = Open f = 1MHz t_{rise} = t_{fall} = 1ns	0.7V	0.7V		2.4		pF
			0.8V	0.8V		2.3		
			0.9V	0.9V		2.2		
			1.2V	1.2V		2.2		
			1.5V	1.5V		2.2		
			1.8V	1.8V		2.2		
			2.5V	2.5V		2.4		
			3.3V	3.3V		3.0		
	Power Dissipation Capacitance per transceiver (A to B: outputs disabled)	C_L = 0, R_L = Open f = 1MHz t_{rise} = t_{fall} = 1ns	0.7V	0.7V		1.5		pF
			0.8V	0.8V		1.5		
			0.9V	0.9V		1.5		
			1.2V	1.2V		1.5		
			1.5V	1.5V		1.5		
			1.8V	1.8V		1.5		
			2.5V	2.5V		1.6		
			3.3V	3.3V		2.0		
	Power Dissipation Capacitance per transceiver (B to A: outputs enabled)	C_L = 0, R_L = Open f = 1MHz t_{rise} = t_{fall} = 1ns	0.7V	0.7V		13.4		pF
			0.8V	0.8V		15.0		
			0.9V	0.9V		14.0		
			1.2V	1.2V		20.7		
			1.5V	1.5V		29.6		
			1.8V	1.8V		40.2		
			2.5V	2.5V		65.8		
			3.3V	3.3V		91.7		
	Power Dissipation Capacitance per transceiver (B to A: outputs disabled)	C_L = 0, R_L = Open f = 1MHz t_{rise} = t_{fall} = 1ns	0.7V	0.7V		1.3		pF
			0.8V	0.8V		1.1		
			0.9V	0.9V		1.1		
			1.2V	1.2V		1.0		
			1.5V	1.5V		1.0		
			1.8V	1.8V		1.0		
			2.5V	2.5V		1.0		
			3.3V	3.3V		1.0		

5.14 Operating Characteristics: T_A = 25°C (continued)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
C_{pdB}	Power Dissipation Capacitance per transceiver (A to B: outputs enabled)	C_L = 0, R_L = Open f = 1MHz t_{rise} = t_{fall} = 1ns	0.7V	0.7V		13.4		pF
			0.8V	0.8V		13.8		
			0.9V	0.9V		14.9		
			1.2V	1.2V		20.6		
			1.5V	1.5V		29.6		
			1.8V	1.8V		40.3		
			2.5V	2.5V		66.2		
			3.3V	3.3V		92.5		
	Power Dissipation Capacitance per transceiver (A to B: outputs disabled)	C_L = 0, R_L = Open f = 1MHz t_{rise} = t_{fall} = 1ns	0.7V	0.7V		1.3		pF
			0.8V	0.8V		1.2		
			0.9V	0.9V		1.1		
			1.2V	1.2V		1.1		
			1.5V	1.5V		1.1		
			1.8V	1.8V		1.1		
			2.5V	2.5V		1.1		
			3.3V	3.3V		1.1		
	Power Dissipation Capacitance per transceiver (B to A: outputs enabled)	C_L = 0, R_L = Open f = 1MHz t_{rise} = t_{fall} = 1ns	0.7V	0.7V		2.5		pF
			0.8V	0.8V		2.4		
			0.9V	0.9V		2.3		
			1.2V	1.2V		2.2		
			1.5V	1.5V		2.3		
			1.8V	1.8V		2.3		
			2.5V	2.5V		2.5		
			3.3V	3.3V		3.0		
	Power Dissipation Capacitance per transceiver (B to A: outputs disabled)	C_L = 0, R_L = Open f = 1MHz t_{rise} = t_{fall} = 1ns	0.7V	0.7V		1.6		pF
			0.8V	0.8V		1.5		
			0.9V	0.9V		1.5		
			1.2V	1.2V		1.5		
			1.5V	1.5V		1.5		
			1.8V	1.8V		1.5		
			2.5V	2.5V		1.6		
			3.3V	3.3V		2.0		

5.15 Typical Characteristics

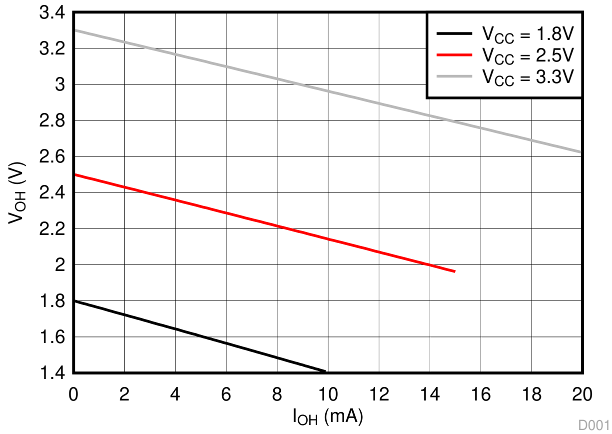


Figure 5-1. Typical (T_A=25°C) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

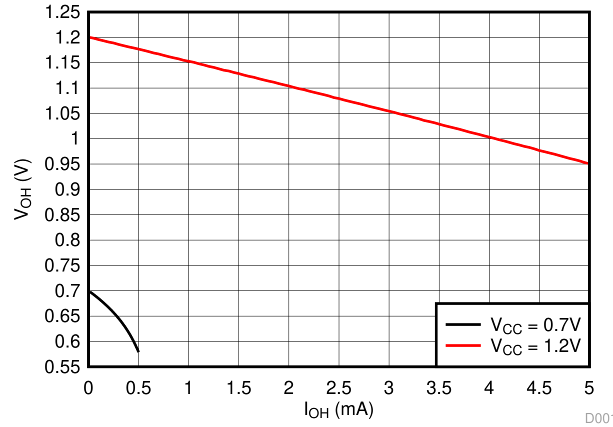


Figure 5-2. Typical (T_A=25°C) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

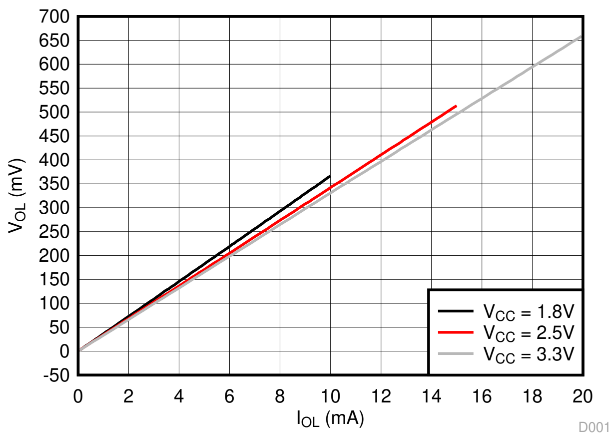


Figure 5-3. Typical (T_A=25°C) Output High Voltage (V_{OL}) vs Sink Current (I_{OL})

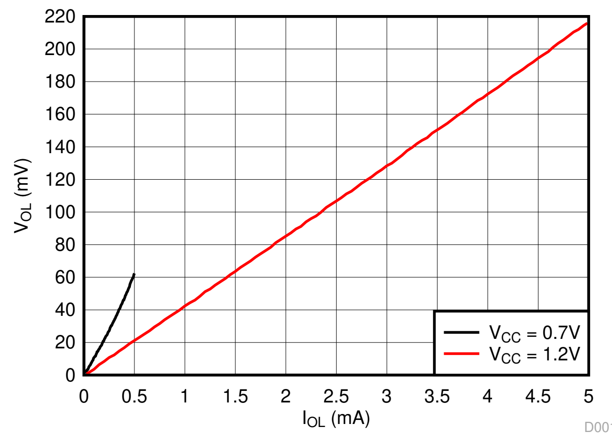


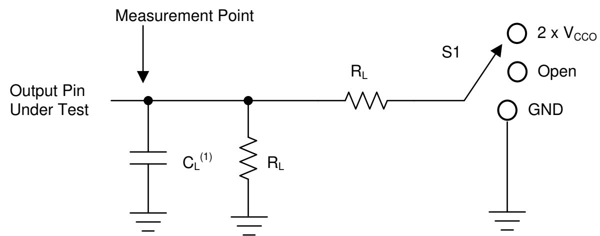
Figure 5-4. Typical (T_A=25°C) Output High Voltage (V_{OL}) vs Sink Current (I_{OL})

6 Parameter Measurement Information

6.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1MHz
- Z_O = 50Ω
- dv/dt ≤ 1ns/V

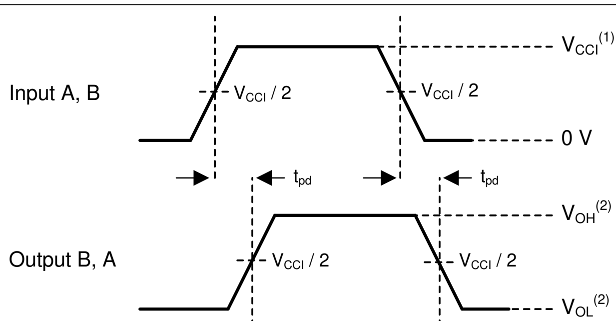


A. C_L includes probe and jig capacitance.

Figure 6-1. Load Circuit

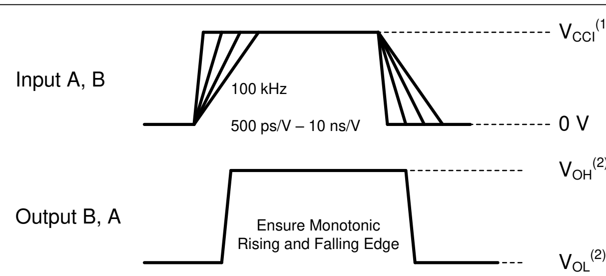
Table 6-1. Load Circuit Conditions

Parameter	V_{CCO}	R_L	C_L	S_1	V_{TP}
Δt/Δv Input transition rise or fall rate	0.65V – 3.6V	1MΩ	15pF	Open	N/A
t_{pd} Propagation (delay) time	1.1V – 3.6V	2kΩ	15pF	Open	N/A
	0.65V – 0.95V	20kΩ	15pF	Open	N/A
t_{en}, t_{dis} Enable time, disable time	3V – 3.6V	2kΩ	15pF	2 × V_{CCO}	0.3V
	1.65V – 2.7V	2kΩ	15pF	2 × V_{CCO}	0.15V
	1.1V – 1.6V	2kΩ	15pF	2 × V_{CCO}	0.1V
	0.65V – 0.95V	20kΩ	15pF	2 × V_{CCO}	0.1V
t_{en}, t_{dis} Enable time, disable time	3V – 3.6V	2kΩ	15pF	GND	0.3V
	1.65V – 2.7V	2kΩ	15pF	GND	0.15V
	1.1V – 1.6V	2kΩ	15pF	GND	0.1V
	0.65V – 0.95V	20kΩ	15pF	GND	0.1V



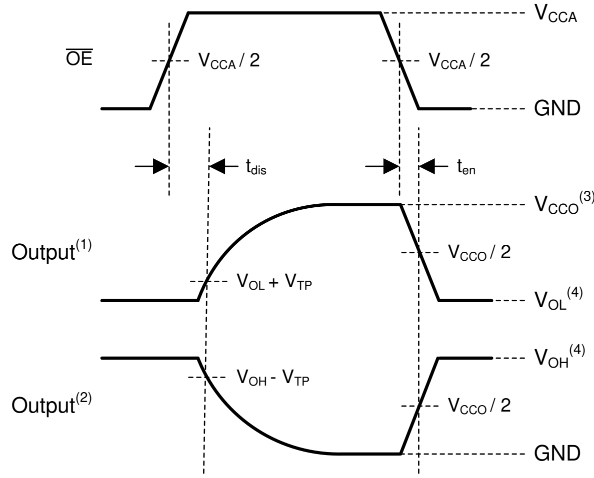
1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

Figure 6-2. Propagation Delay



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

Figure 6-3. Input Transition Rise or Fall Rate



A. Output waveform on the condition that input is driven to a valid Logic Low.

B. Output waveform on the condition that input is driven to a valid Logic High.

C. V_{CCO} is the supply pin associated with the output port.

D. V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

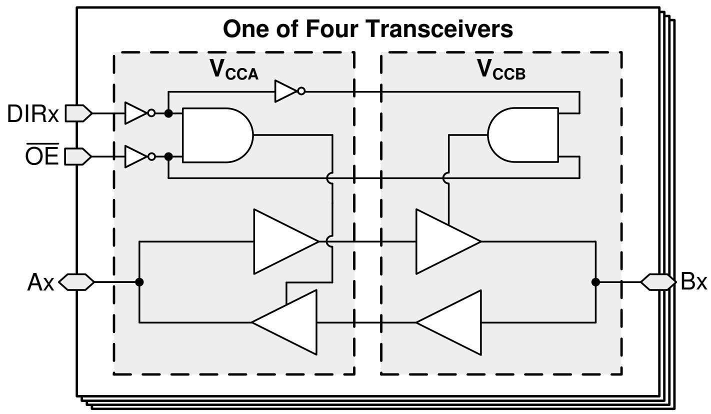
Figure 6-4. Enable Time And Disable Time

7 Detailed Description

7.1 Overview

The SN74AXC4T774-Q1 is a 4-bit, dual-supply noninverting bidirectional voltage level translation device. Ax pins and control pins (DIRx and $\overline{OE}$) are reference to V_{CCA} logic levels, and Bx pins are referenced to V_{CCB} logic levels. The A port is able to accept I/O voltages ranging from 0.65V to 3.6V, while the B port can accept I/O voltages from 0.65V to 3.6V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both Ax and Bx pins are in the high-impedance state. See Section 7.4 for a summary of the operation of the control logic.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

7.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

7.3.3 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

7.3.4 V_{CC} Isolation

The inputs and outputs for this device enter a high-impedance state when either supply is <100mV.

7.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

7.3.6 Glitch-free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the I/Os (that is, where the output erroneously transitions to VCC when it should be held low). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Glitch Free Power Sequencing With AXC Level Translators* application report

7.3.7 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in Figure 7-1.

> **CAUTION**
>
> Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

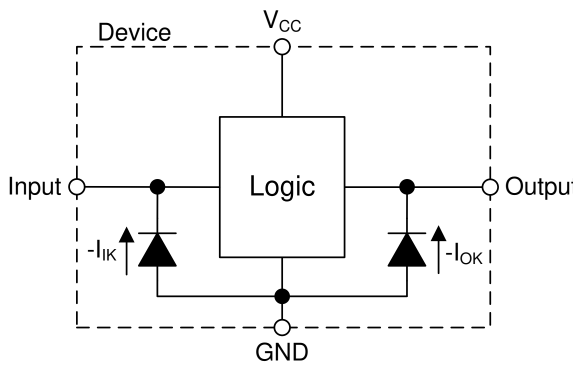


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.8 Fully Configurable Dual-Rail Design

The V_{CCA} and V_{CCB} pins can be supplied at any voltage from 0.65V to 3.6V, making the device suitable for translating between any of the voltage nodes (0.7V, 0.8V, 0.9V, 1.2V, 1.8V, 2.5V, and 3.3V).

7.3.9 I/Os with Integrated Static Pull-Down Resistors

To help avoid floating inputs on the I/Os, this device has 71kΩ typical integrated weak pull-downs on all data I/Os. This feature allows all inputs to be left floating without the concern for unstable outputs or increased current consumption. This also helps to reduce external component count for applications where not all channels are used or need to be fixed low. If an external pull-up is required, it should be no larger than 7kΩ to avoid contention with the 71kΩ internal pull-down.

7.3.10 Supports High-Speed Translation

The SN74AXC4T774-Q1 device can support high data-rate applications. The translated signal data rate can be up to 310Mbps when the signal is translated from 1.8V to 3.3V.

7.4 Device Functional Modes

Table 7-1. Function Table (Each Transceiver)

CONTROL INPUTS[(1)] [(2)]		Port Status		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Output (Enabled)	Input (Hi-Z)	B data to A bus
L	H	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	X	Input (Hi-Z)	Input (Hi-Z)	Isolation

(1) Input circuits of the data I/Os are always active.
(2) Pins configured as inputs should not be left floating.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AXC4T774-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AXC4T774-Q1 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The max data rate can be up to 310Mbps when device translates a signal from 1.8V to 3.3V.

One example application is shown in Figure 8-1, where the SN74AXC4T774-Q1 device is used to translate a low voltage SPI signal from an SoC to a higher voltage signal to properly drive the inputs of a GPS module, and vice versa.

8.2 Typical Application

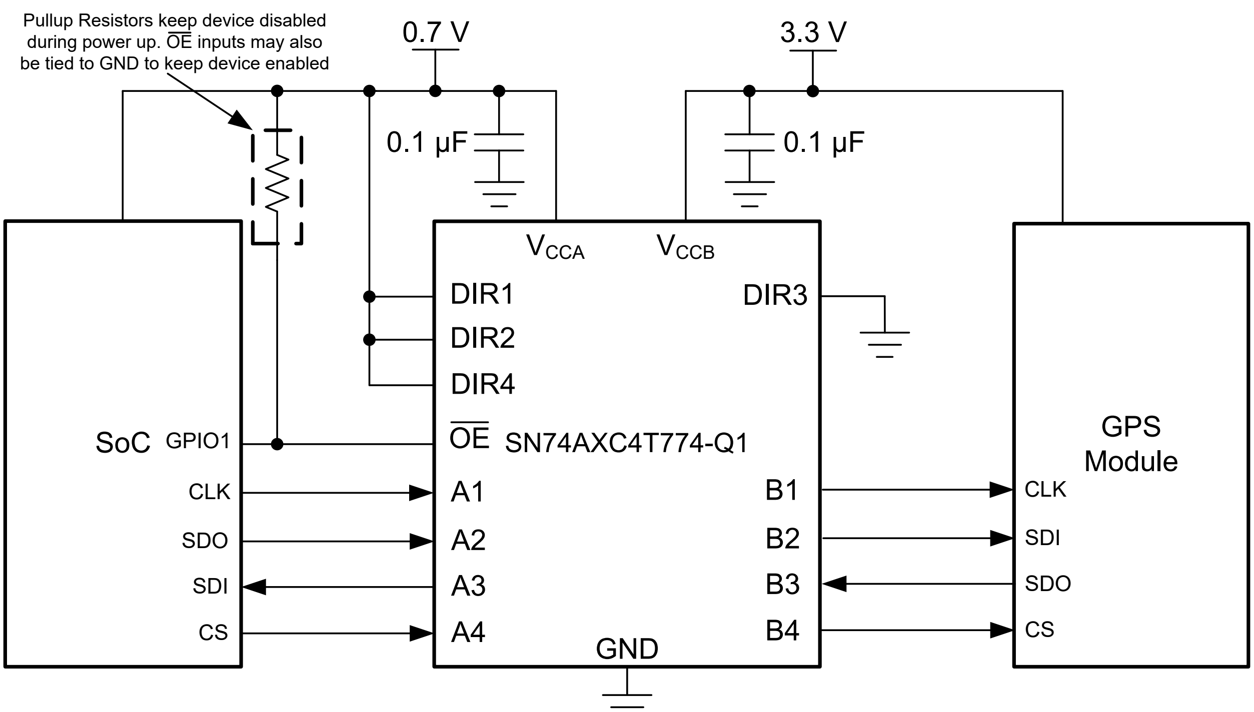


Figure 8-1. Serial Peripheral Interface (SPI) Application

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	0.65V to 3.6V
Output voltage range	0.65V to 3.6V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  – Use the supply voltage of the device that is driving the SN74AXC4T774-Q1 device to determine the input voltage range. For a valid logic-high, the value must exceed the high-level input voltage (V_{IH}) of the input port. For a valid logic low the value must be less than the low-level input voltage (V_{IL}) of the input port.
- Output voltage range
  – Use the supply voltage of the device that the SN74AXC4T774-Q1 device is driving to determine the output voltage range.

8.2.3 Application Curve

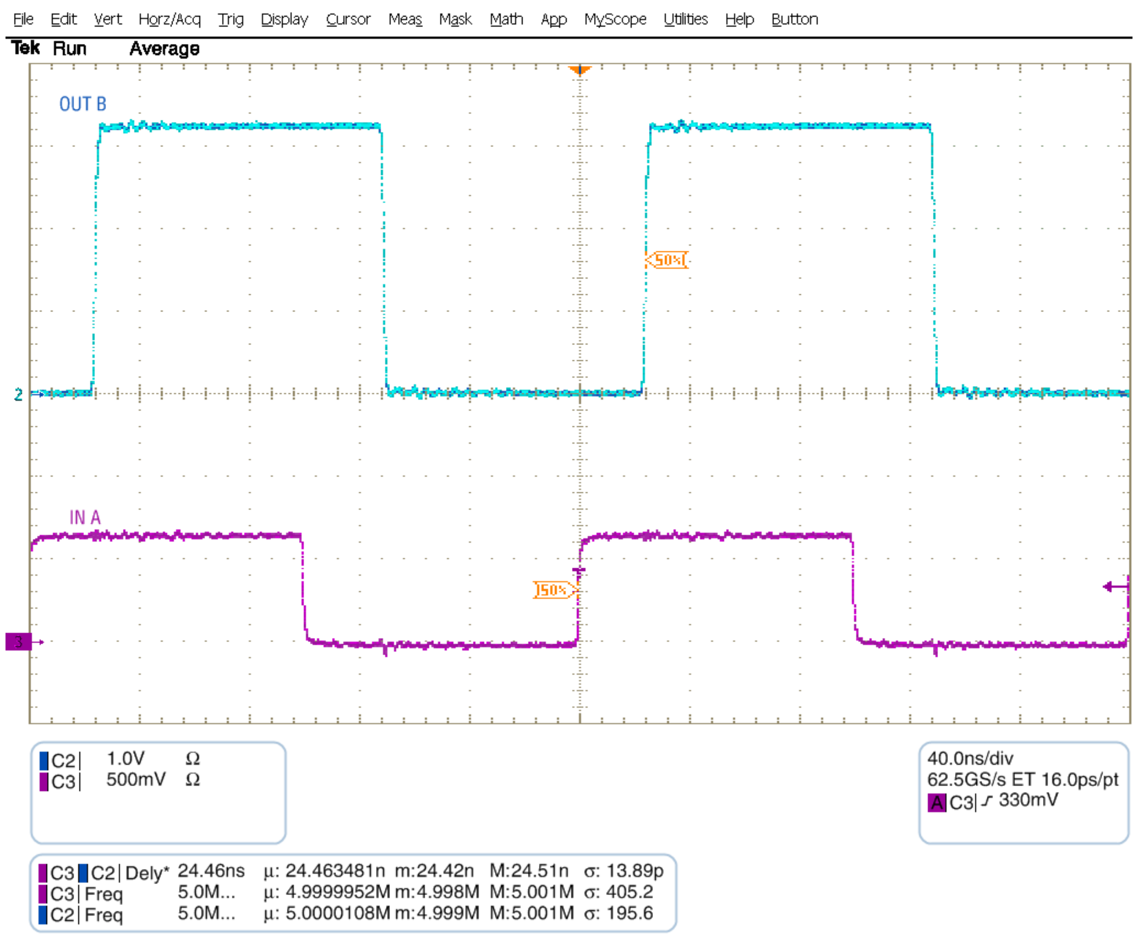


Figure 8-2. Up Translation at 2.5MHz (0.7V to 3.3V)

8.3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Glitch Free Power Sequencing With AXC Level Translators* application report

8.4 Layout

8.4.1 Layout Guidelines

For device reliability, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1 μF capacitor is recommended, but transient performance can be improved by having both 1 μF and 0.1 μF capacitors in parallel as bypass capacitors.
- The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.4.2 Layout Example

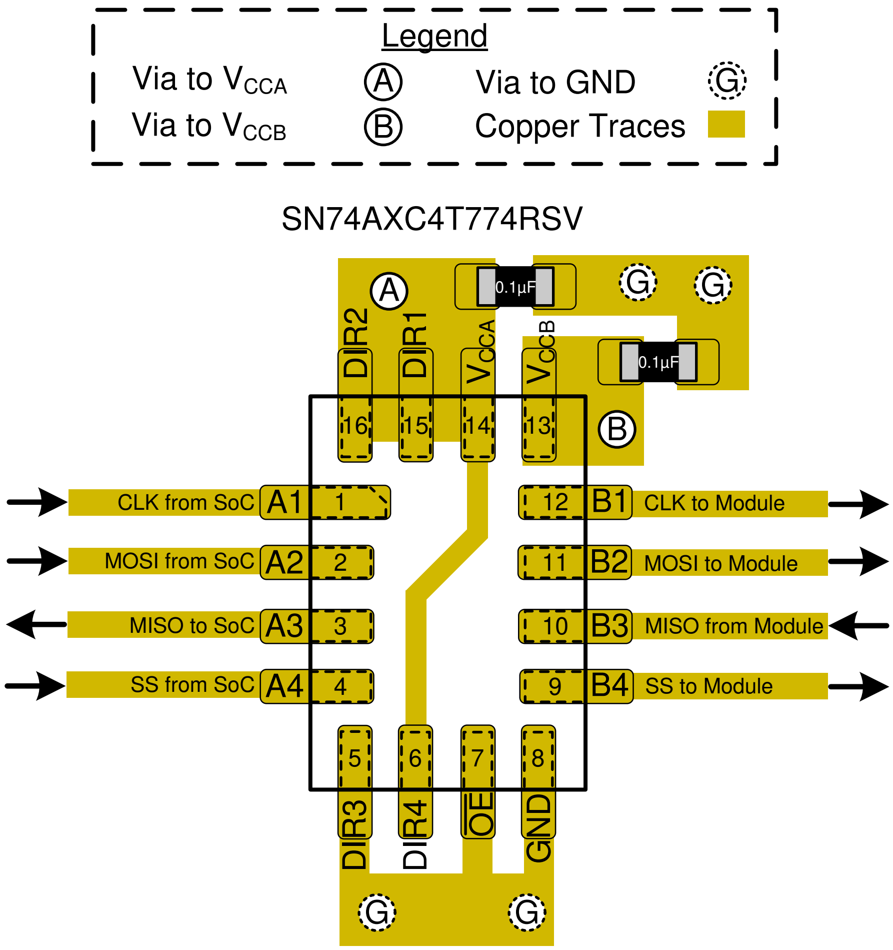


Figure 8-3. Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report
- Texas Instruments, *Power Sequencing for AXC Family of Devices*application report application report
- Texas Instruments, *SN74AXC4T774 Evaluation Module Tool Folder*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2021) to Revision E (January 2024) — **Page**

- Added the *I/Os with Integrated Static Pull-Down Resistors* section...20

Changes from Revision C (July 2020) to Revision D (March 2021) — **Page**

- Changed the status of the BQB (WQFN) package option from *preview* to *production*.......................................1

Changes from Revision B (June 2020) to Revision C (July 2020) — **Page**

- Added BQB (WQFN) package option to *Device Information* table...1
- Updated the numbering format for tables, figures and cross-references throughout the document.................. 1

Changes from Revision A (April 2020) to Revision B (June 2020)	Page
• Changed RSV device status from Preview to Active	1

Changes from Revision * (February 2020) to Revision A (April 2020)	Page
• Changed device status from Advance Information to Production Data	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CAXC4T774QBQBRQ1	ACTIVE	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4T774Q	Samples
CAXC4T774QRSVRQ1	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25ZR	Samples
SN74AXC4T774QPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4T774Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AXC4T774-Q1 :

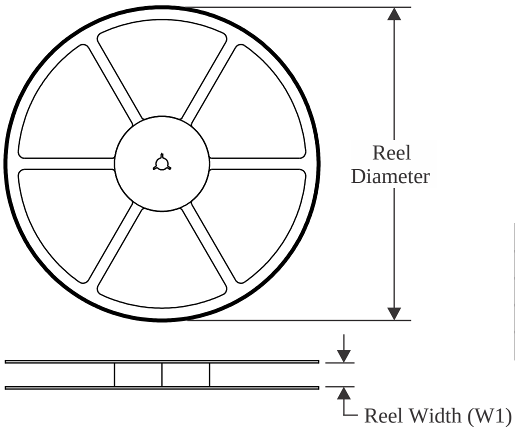
- Catalog : SN74AXC4T774

NOTE: Qualified Version Definitions:

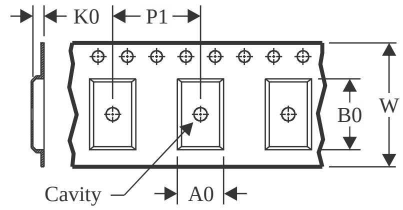
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

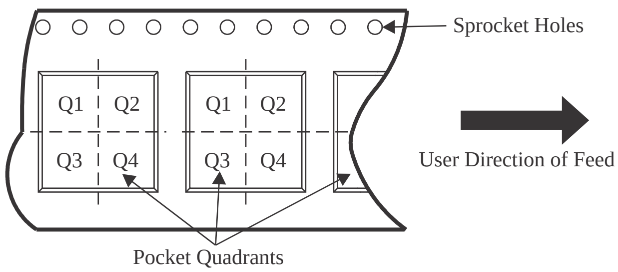


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

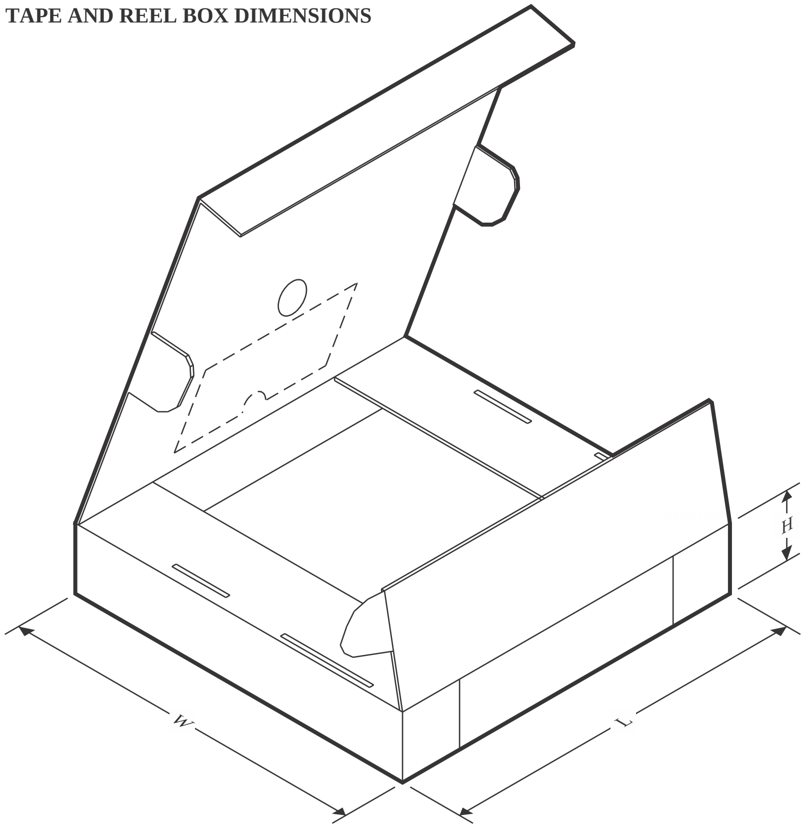
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

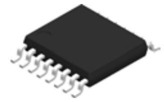
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAXC4T774QBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
CAXC4T774QRSVRQ1	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
SN74AXC4T774QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

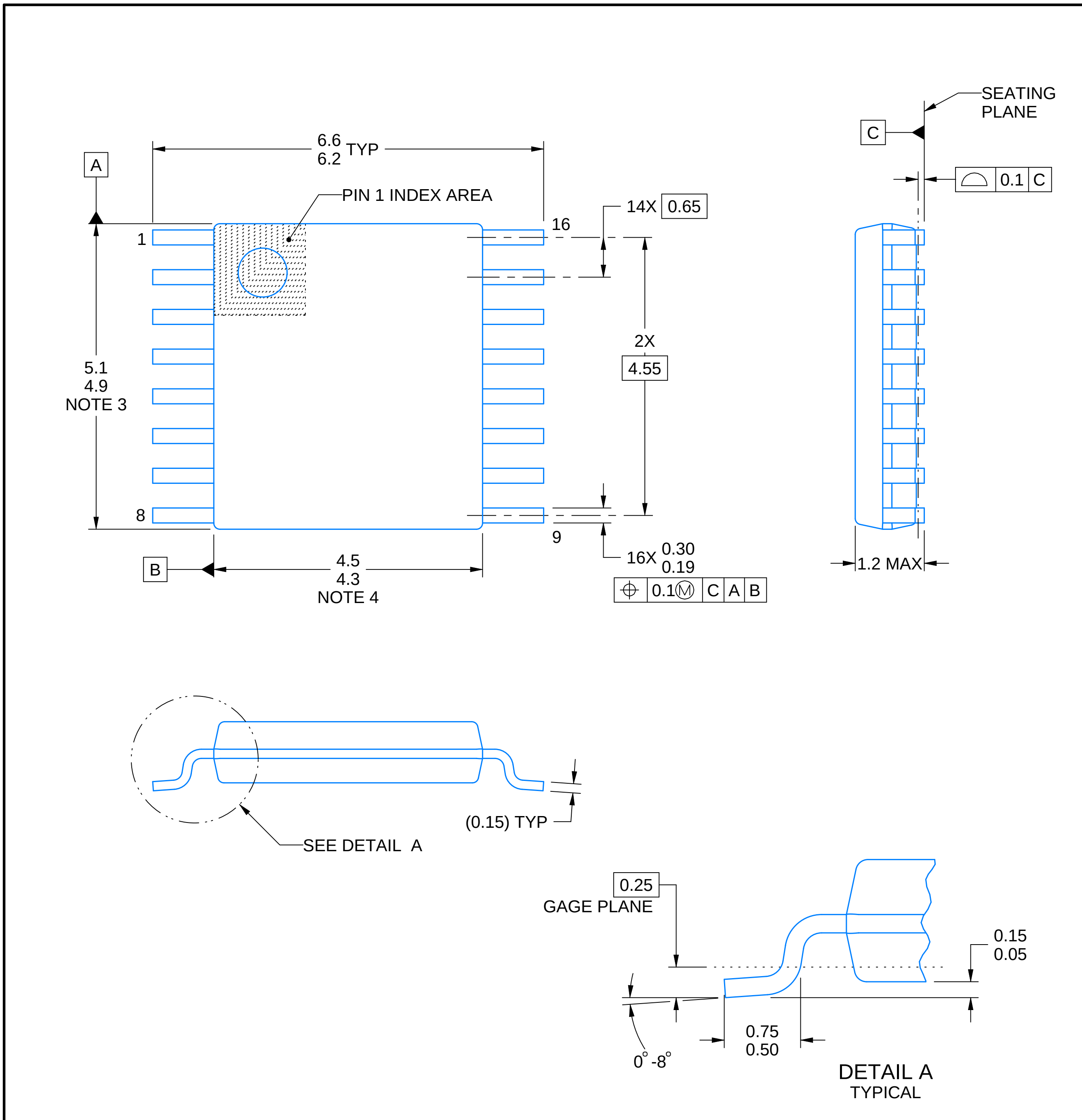
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAXC4T774QBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0
CAXC4T774QRSVRQ1	UQFN	RSV	16	3000	189.0	185.0	36.0
SN74AXC4T774QPWRQ1	TSSOP	PW	16	2000	356.0	356.0	35.0



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

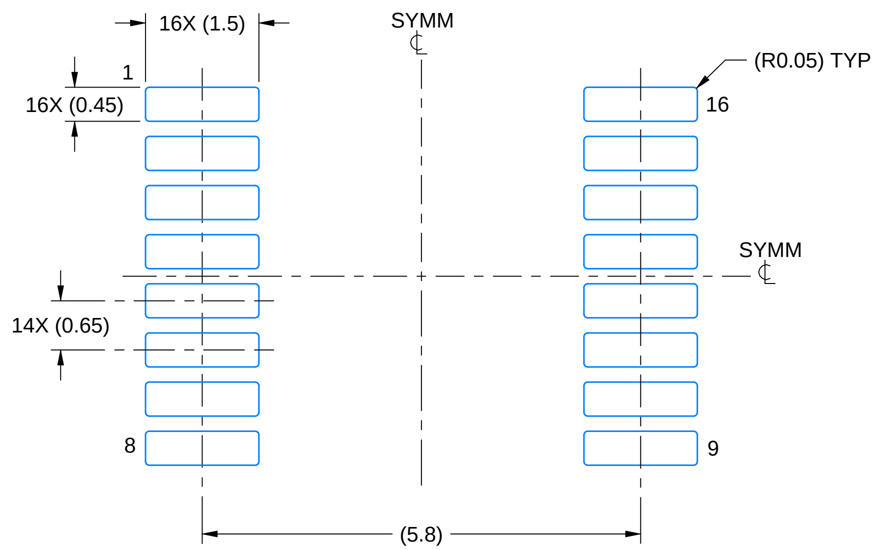
SMALL OUTLINE PACKAGE



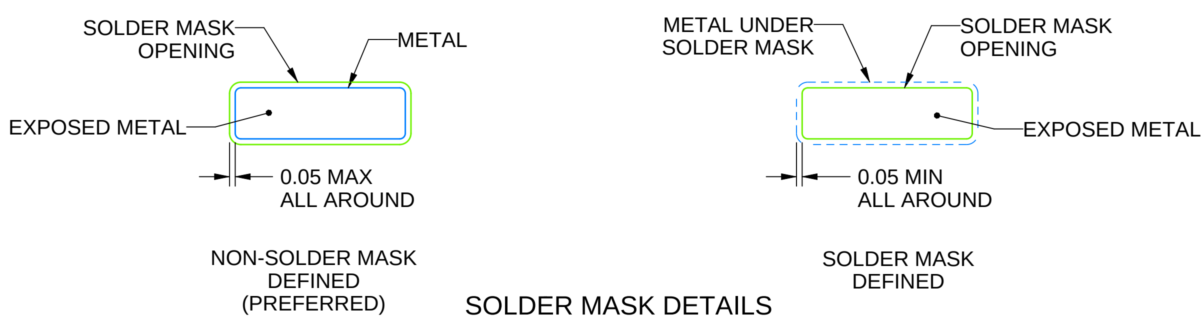
4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

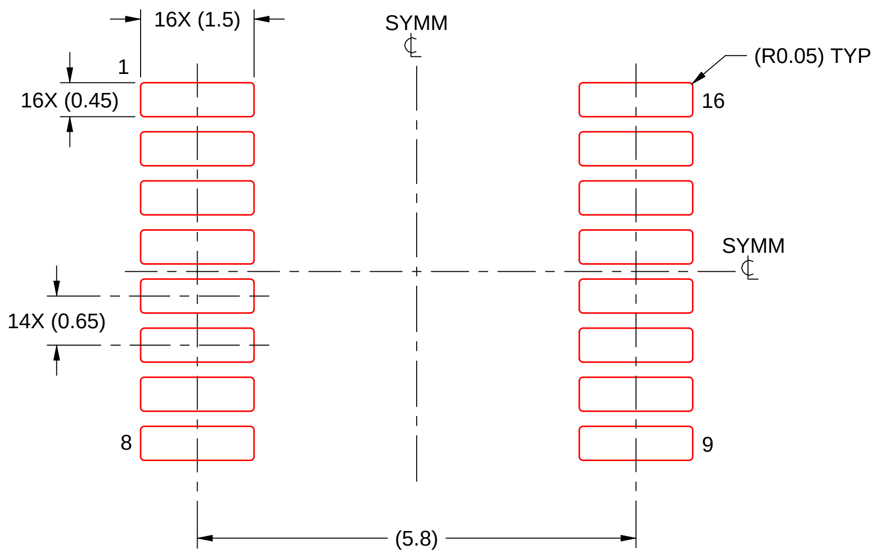


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



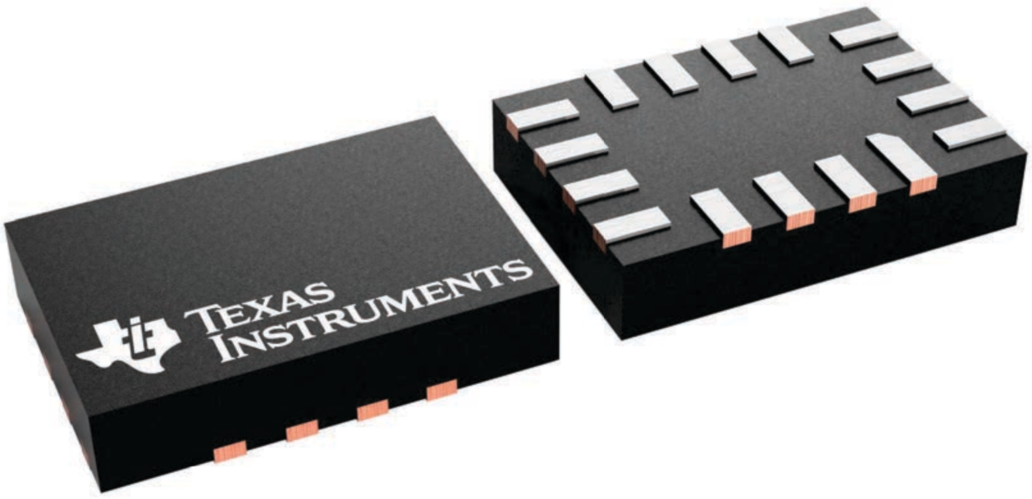
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

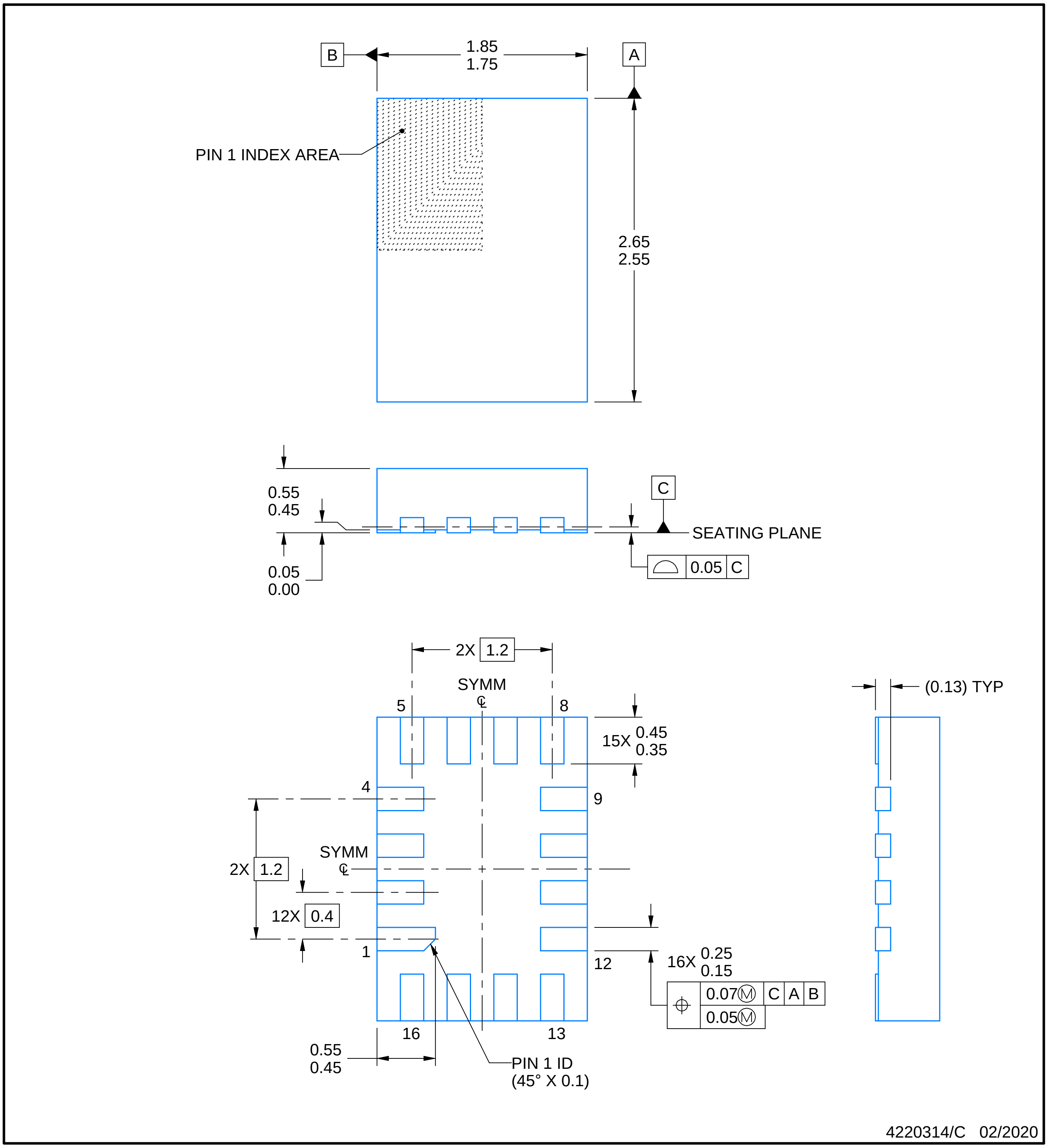
4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

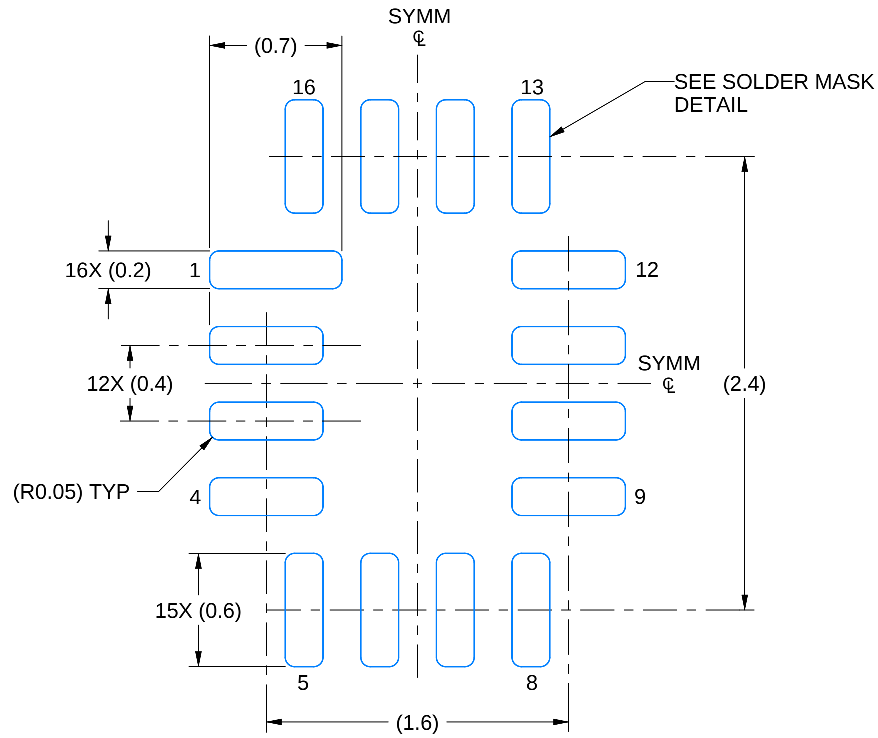
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



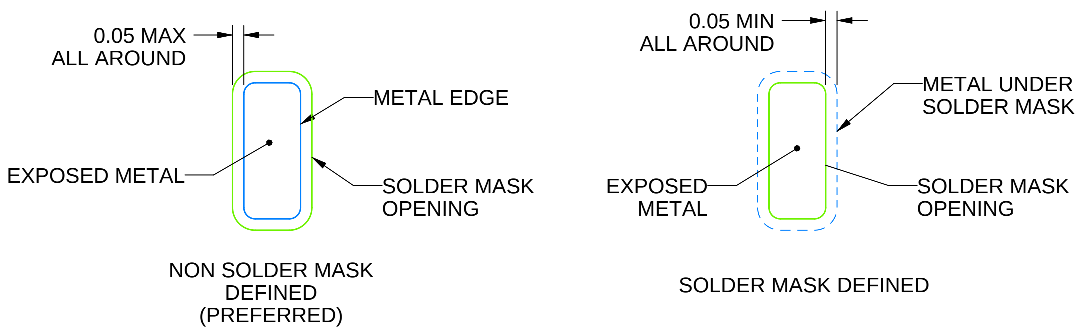


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

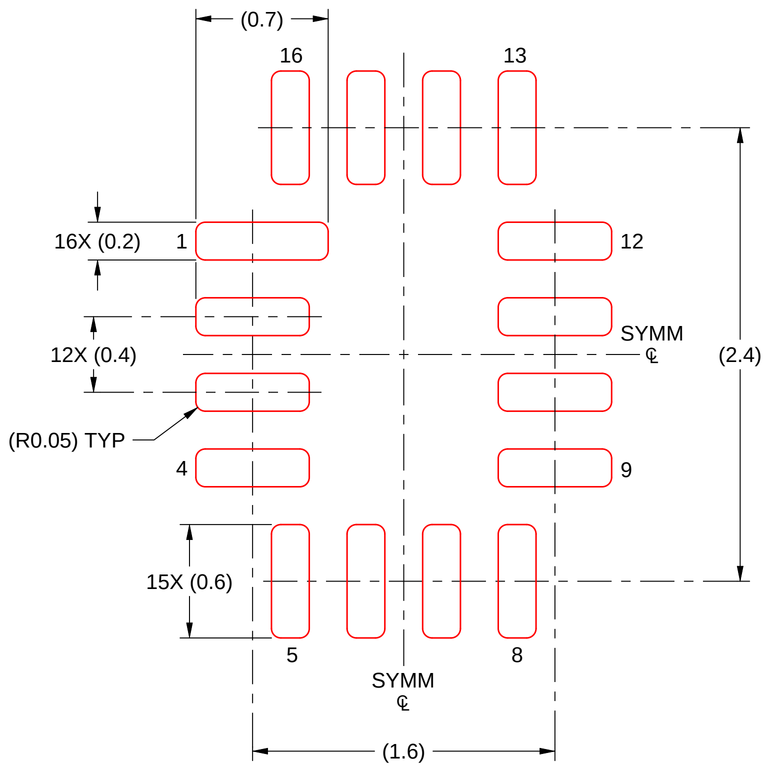


SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



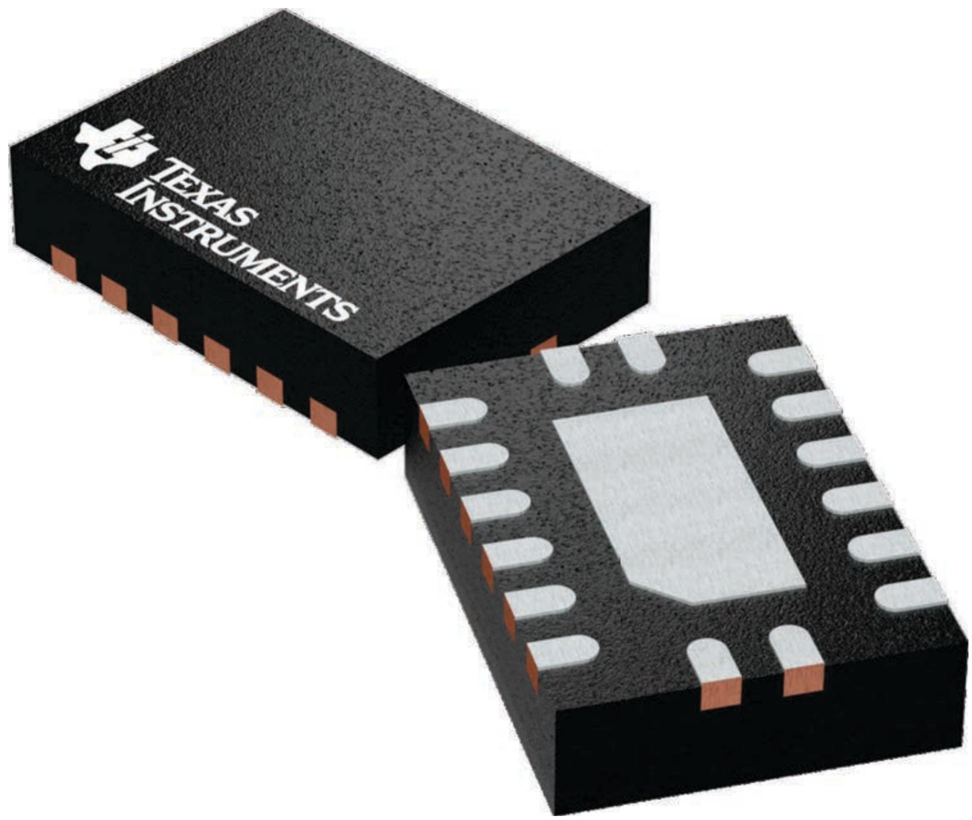
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

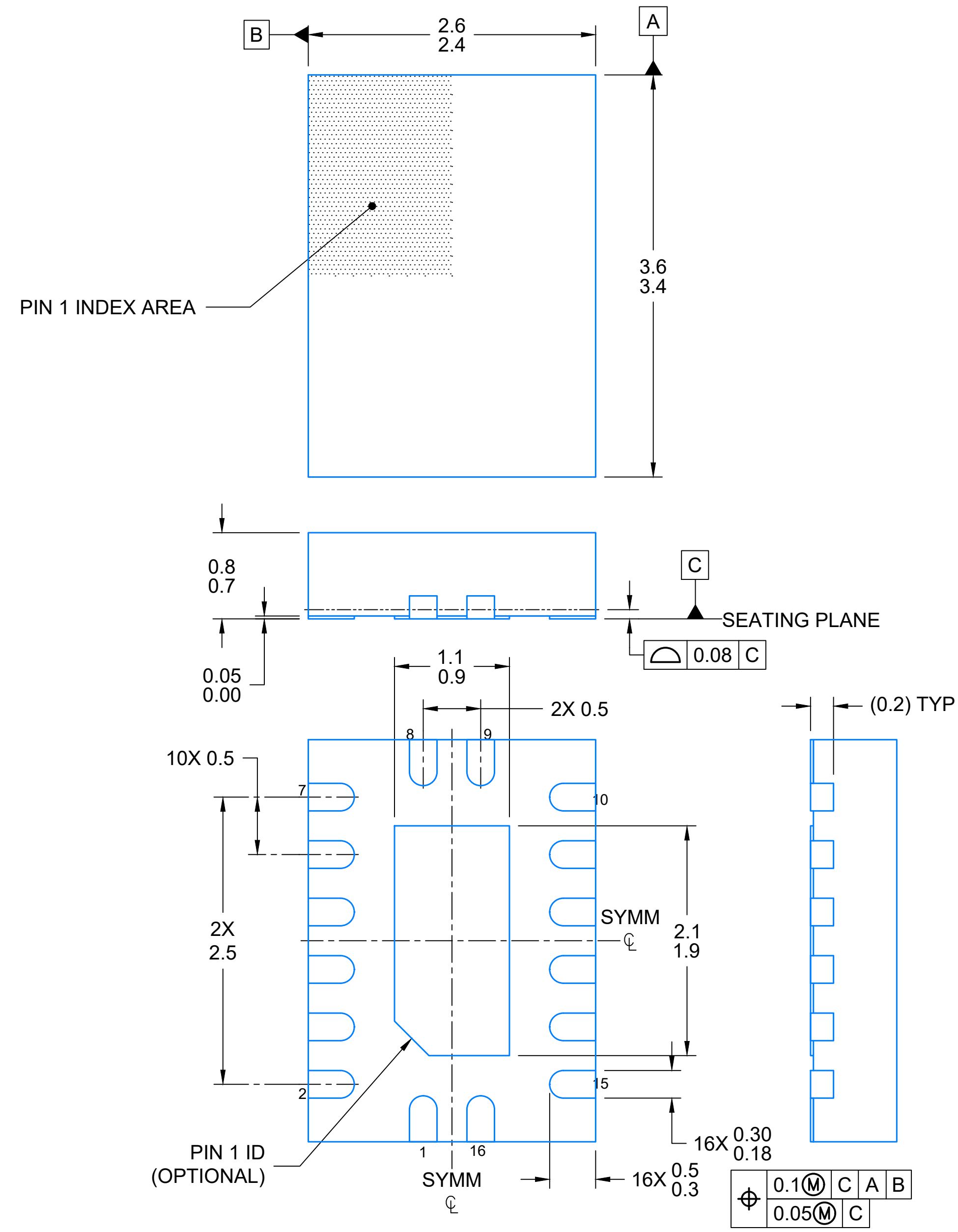
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



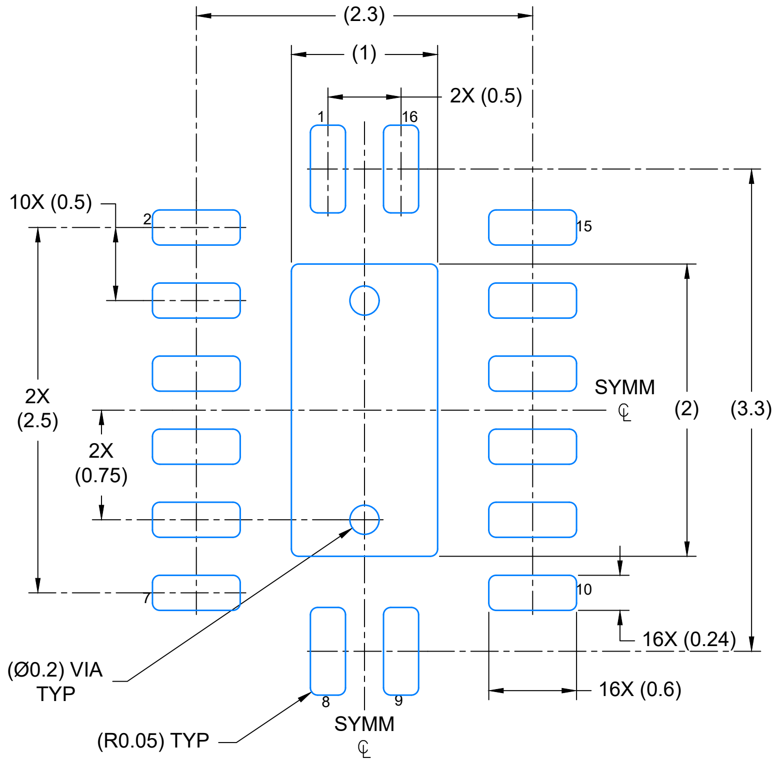
4226161/A



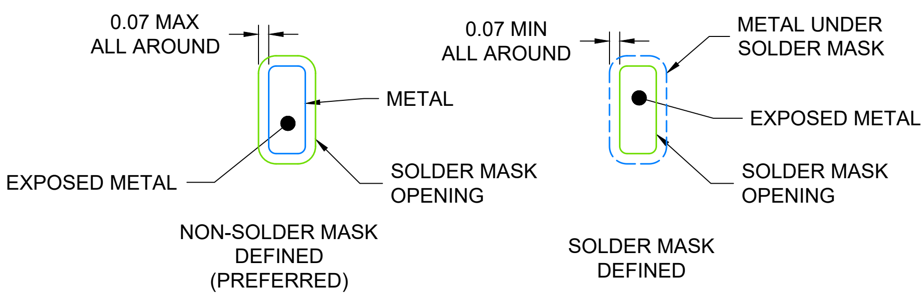
4224640/A 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



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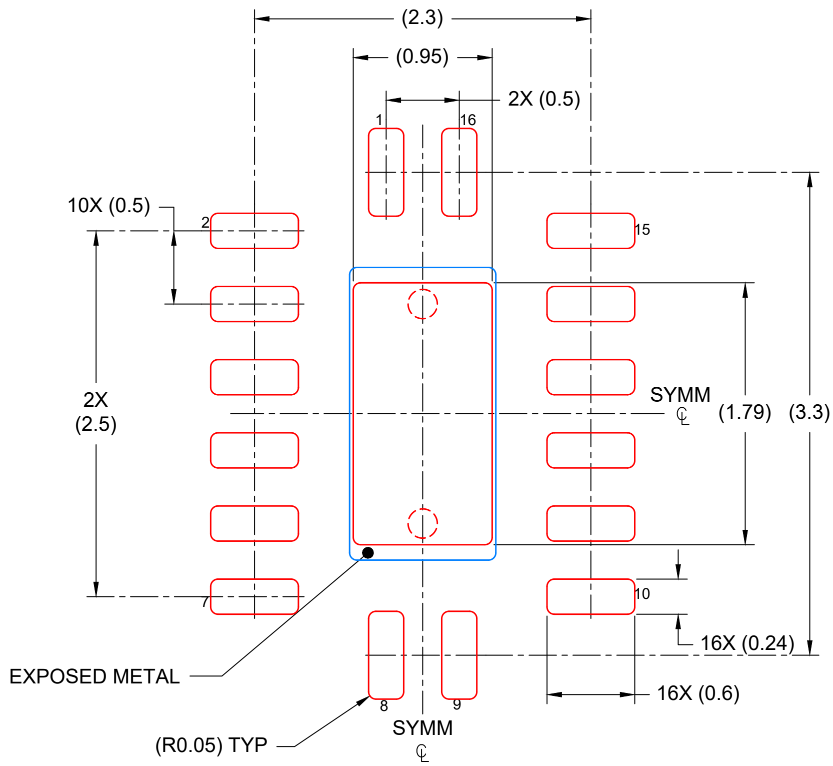
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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