

# SN74AXCH8T245 8-Bit Dual-Supply Bus Transceiver with Configurable Voltage Translation, Tri-State Outputs, and Bus-Hold Circuitry

## 1 Features

- Qualified Fully Configurable Dual-Rail Design Allows Each Port to Operate With a Power Supply Range From 0.65 V to 3.6 V
- Operating Temperature From  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Bus-hold on Data Inputs Eliminates the Need for External Pullup or Pulldown Resistors
- Multiple Direction Control Pins to Allow Simultaneous Up and Down Translation
- Up to 380 Mbps support when translating from 1.8 V to 3.3 V
- $V_{CC}$  Isolation Feature to Effectively Isolate Both Buses in a Power-Down Scenario
- Partial Power-Down Mode to Limit Backflow Current in a Power-Down Scenario
- Compatible With SN74AVCH8T245 and 74AVCH8T245 Level Shifters
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 8000-V Human-Body Model
  - 1000-V Charged-Device Model

## 2 Applications

- Enterprise and Communications
- Wireless Infrastructure
- Building Automation
- Data Center Switches
- Enterprise-Solid State Drive
- Rack Server
- EPOS

## 3 Description

The SN74AXCH8T245 device is an 8-bit non-inverting bus transceiver that resolves voltage level mismatch between devices operating at the latest voltage nodes (0.7 V, 0.8 V, and 0.9 V) and devices operating at industry standard voltage nodes (1.8 V, 2.5 V, 3.3 V) and vice versa.

The device operates by using two independent power-supply rails ( $V_{CCA}$  and  $V_{CCB}$ ). Data pins A1 through A8 are designed to track  $V_{CCA}$ , which accepts any supply voltage from 0.65 V to 3.6 V. Data pins B1 through B8 are designed to track  $V_{CCB}$ , which accepts any supply voltage from 0.65 V to 3.6 V. Additionally the SN74AXCH8T245 is compatible with a single-supply system.

The SN74AXCH8T245 device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level of the direction-control inputs (DIR1 and DIR2). The output-enable ( $\overline{OE}$ ) input is used to disable the outputs so the buses are effectively isolated.

The SN74AXCH8T245 device is designed so the control pins (DIR and  $\overline{OE}$ ) are referenced to  $V_{CCA}$ .

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pull-up or pull-down resistors with the bus-hold circuitry is not recommended. If a supply is present for  $V_{CCA}$  or  $V_{CCB}$ , the bus-hold circuitry always remains active on all A and B ports respectively, independent of the direction control or output enable.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

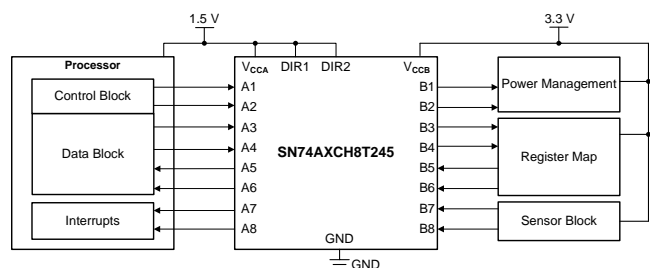
The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input supply is below 100 mV, all level shifter outputs are disabled and placed into a high-impedance state. To ensure the high-impedance state of the level shifter I/Os during power up or power down,  $\overline{OE}$  should be tied to  $V_{CCA}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AXCH8T245PW	TSSOP (24)	7.80 mm x 4.40 mm
SN74AXCH8T245RHL	VQFN (24)	5.50 mm x 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Typical Application Schematic



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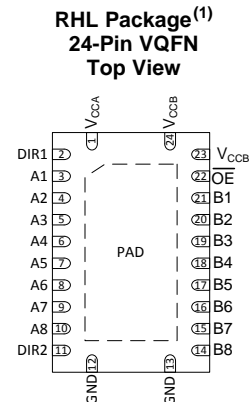
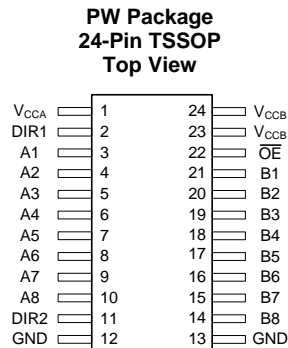
## 4 Revision History

### Changes from Original (August 2018) to Revision A

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•	Added RHL package pinout .....	3
•	Added RHL package to Thermal Information table .....	5

## 5 Pin Configuration and Functions



(1) PAD - may be grounded (recommended) or left floating.

### Pin Functions

PIN		I/O	DESCRIPTION
NAME	PW, RHL		
A1	3	I/O	Input/output A1. Referenced to V <sub>CCA</sub> .
A2	4	I/O	Input/output A2. Referenced to V <sub>CCA</sub> .
A3	5	I/O	Input/output A3. Referenced to V <sub>CCA</sub> .
A4	6	I/O	Input/output A4. Referenced to V <sub>CCA</sub> .
A5	7	I/O	Input/output A5. Referenced to V <sub>CCA</sub> .
A6	8	I/O	Input/output A6. Referenced to V <sub>CCA</sub> .
A7	9	I/O	Input/output A7. Referenced to V <sub>CCA</sub> .
A8	10	I/O	Input/output A8. Referenced to V <sub>CCA</sub> .
B1	21	I/O	Input/output B1. Referenced to V <sub>CCB</sub> .
B2	20	I/O	Input/output B2. Referenced to V <sub>CCB</sub> .
B3	19	I/O	Input/output B3. Referenced to V <sub>CCB</sub> .
B4	18	I/O	Input/output B4. Referenced to V <sub>CCB</sub> .
B5	17	I/O	Input/output B5. Referenced to V <sub>CCB</sub> .
B6	16	I/O	Input/output B6. Referenced to V <sub>CCB</sub> .
B7	15	I/O	Input/output B7. Referenced to V <sub>CCB</sub> .
B8	14	I/O	Input/output B8. Referenced to V <sub>CCB</sub> .
DIR1	2	I	Direction-control signal. Referenced to V <sub>CCA</sub> .
DIR2	11	I	Direction-control signal. Referenced to V <sub>CCA</sub> . See <a href="#">Multiple Direction Control Pins</a> for additional details. Tie to GND to maintain backwards compatibility with the SN74AVCH8T245 device.
GND	12	—	Ground
	13	—	Ground
OE	22	I	Output Enable. Pull to GND to enable all outputs. Pull to V <sub>CCA</sub> to place all outputs in high-impedance mode. Referenced to V <sub>CCA</sub> .
V <sub>CCA</sub>	1	—	A-port supply voltage. 0.65 V ≤ V <sub>CCA</sub> ≤ 3.6 V
V <sub>CCB</sub>	23	—	B-port supply voltage. 0.65 V ≤ V <sub>CCB</sub> ≤ 3.6 V
	24	—	B-port supply voltage. 0.65 V ≤ V <sub>CCB</sub> ≤ 3.6 V

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage, $V_{CCA}$		-0.5	4.2	V
Supply voltage, $V_{CCB}$		-0.5	4.2	V
Input voltage, $V_I$ <sup>(2)</sup>	I/O ports (A port)	-0.5	4.2	V
	I/O ports (B port)	-0.5	4.2	
	Control inputs	-0.5	4.2	
Voltage applied to any output in the high-impedance or power-off state, $V_O$ <sup>(2)</sup>	A port	-0.5	4.2	V
	B port	-0.5	4.2	
Voltage applied to any output in the high or low state, $V_O$ <sup>(2) (3)</sup>	A port	-0.5	$V_{CCA} + 0.2$	V
	B port	-0.5	$V_{CCB} + 0.2$	
Input clamp current, $I_{IK}$	$V_I < 0$	-50		mA
Output clamp current, $I_{OK}$	$V_O < 0$	-50		mA
Continuous output current, $I_O$		-50	50	mA
Continuous current through $V_{CCA}$ , $V_{CCB}$ , or GND		-100	100	mA
Junction Temperature, $T_J$			150	°C
Storage temperature, $T_{stg}$		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current rating is observed.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±8000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted) <sup>(1)(2)(3)</sup>

		MIN	MAX	UNIT	
V <sub>CCA</sub>	Supply voltage	0.65	3.6	V	
V <sub>CCB</sub>	Supply voltage	0.65	3.6	V	
V <sub>IH</sub>	High-level input voltage	Data inputs	V <sub>CCI</sub> = 0.65 V - 0.75 V	V <sub>CCI</sub> × 0.70	V
			V <sub>CCI</sub> = 0.76 V - 1 V	V <sub>CCI</sub> × 0.70	
			V <sub>CCI</sub> = 1.1 V - 1.95 V	V <sub>CCI</sub> × 0.65	
			V <sub>CCI</sub> = 2.3 V - 2.7 V	1.6	
			V <sub>CCI</sub> = 3 V - 3.6 V	2	
	Control inputs (DIR, $\overline{OE}$ ) Referenced to V <sub>CCA</sub>	V <sub>CCA</sub> = 0.65 V - 0.75 V	V <sub>CCA</sub> × 0.70		
		V <sub>CCA</sub> = 0.76 V - 1 V	V <sub>CCA</sub> × 0.70		
		V <sub>CCA</sub> = 1.1 V - 1.95 V	V <sub>CCA</sub> × 0.65		
		V <sub>CCA</sub> = 2.3 V - 2.7 V	1.6		
		V <sub>CCA</sub> = 3 V - 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	Data inputs	V <sub>CCI</sub> = 0.65 V - 0.75 V	V <sub>CCI</sub> × 0.30	V
			V <sub>CCI</sub> = 0.76 V - 1 V	V <sub>CCI</sub> × 0.30	
			V <sub>CCI</sub> = 1.1 V - 1.95 V	V <sub>CCI</sub> × 0.35	
			V <sub>CCI</sub> = 2.3 V - 2.7 V	0.7	
			V <sub>CCI</sub> = 3 V - 3.6 V	0.8	
	Control inputs (DIR, $\overline{OE}$ ) Referenced to V <sub>CCA</sub>	V <sub>CCA</sub> = 0.65 V - 0.75 V	V <sub>CCA</sub> × 0.30		
		V <sub>CCA</sub> = 0.76 V - 1 V	V <sub>CCA</sub> × 0.30		
		V <sub>CCA</sub> = 1.1 V - 1.95 V	V <sub>CCA</sub> × 0.35		
		V <sub>CCA</sub> = 2.3 V - 2.7 V	0.7		
		V <sub>CCA</sub> = 3 V - 3.6 V	0.8		
V <sub>I</sub>	Input voltage <sup>(3)</sup>	0	3.6	V	
V <sub>O</sub>	Output voltage	Active state	0	V <sub>CCO</sub> <sup>(2)</sup>	V
		Tri-state	0	3.6	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V	
T <sub>A</sub>	Operating free-air temperature	-40	125	°C	

(1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.

(2) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

(3) All unused data inputs of the device must be held at V<sub>CCI</sub> or GND to ensure proper device operation. See the [Implications of Slow or Floating CMOS Inputs](#) application report.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74AXCH8T245		UNIT	
	PW (TSSOP)	RHL (VQFN)		
	24 PINS	24 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	101.7	35	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	45.4	39.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	56.9	13.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	7.0	0.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	56.4	13.8	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	1.4	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

 Over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS		V <sub>CCA</sub>	V <sub>CCB</sub>	–40°C to 85°C			–40°C to 125°C			UNIT
					MIN	TYP <sup>(2)</sup>	MAX	MIN	TYP <sup>(2)</sup>	MAX	
V <sub>OH</sub> High-level output voltage	V <sub>I</sub> = V <sub>IH</sub>	I <sub>OH</sub> = –100 μA	0.7 V - 3.6 V	0.7 V - 3.6 V	V <sub>CCO</sub> – 0.1			V <sub>CCO</sub> – 0.1			V
		I <sub>OH</sub> = –50 μA	0.65 V	0.65 V	0.55			0.55			
		I <sub>OH</sub> = –200 μA	0.76 V	0.76 V	0.58			0.58			
		I <sub>OH</sub> = –500 μA	0.85 V	0.85 V	0.65			0.65			
		I <sub>OH</sub> = –3 mA	1.1 V	1.1 V	0.85			0.85			
		I <sub>OH</sub> = –6 mA	1.4 V	1.4 V	1.05			1.05			
		I <sub>OH</sub> = –8 mA	1.65 V	1.65 V	1.2			1.2			
		I <sub>OH</sub> = –9 mA	2.3 V	2.3 V	1.75			1.75			
		I <sub>OH</sub> = –12 mA	3 V	3 V	2.3			2.3			
V <sub>OL</sub> Low-level output voltage	V <sub>I</sub> = V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	0.7 V - 3.6 V	0.7 V - 3.6 V				0.1			V
		I <sub>OL</sub> = 50 μA	0.65 V	0.65 V				0.1			
		I <sub>OL</sub> = 200 μA	0.76 V	0.76 V				0.18			
		I <sub>OL</sub> = 500 μA	0.85 V	0.85 V				0.2			
		I <sub>OL</sub> = 3 mA	1.1 V	1.1 V				0.25			
		I <sub>OL</sub> = 6 mA	1.4 V	1.4 V				0.35			
		I <sub>OL</sub> = 8 mA	1.65 V	1.65 V				0.45			
		I <sub>OL</sub> = 9 mA	2.3 V	2.3 V				0.55			
		I <sub>OL</sub> = 12 mA	3 V	3 V				0.7			
I <sub>BHL</sub> Bus-hold low sustaining current <sup>(3)</sup>	V <sub>I</sub> = 0.20 V		0.65 V	0.65 V	4			4			μA
	V <sub>I</sub> = 0.23 V		0.76 V	0.76 V	8			7			
	V <sub>I</sub> = 0.26 V		0.85 V	0.85 V	10			10			
	V <sub>I</sub> = 0.39 V		1.1 V	1.1 V	20			20			
	V <sub>I</sub> = 0.49 V		1.4 V	1.4 V	40			30			
	V <sub>I</sub> = 0.58 V		1.65 V	1.65 V	55			45			
	V <sub>I</sub> = 0.7 V		2.3 V	2.3 V	90			80			
	V <sub>I</sub> = 0.8 V		3 V	3 V	145			135			
I <sub>BHH</sub> Bus-hold high sustaining current <sup>(4)</sup>	V <sub>I</sub> = 0.45 V		0.65 V	0.65 V	–4			–4			μA
	V <sub>I</sub> = 0.53 V		0.76 V	0.76 V	–8			–7			
	V <sub>I</sub> = 0.59 V		0.85 V	0.85 V	–10			–10			
	V <sub>I</sub> = 0.71 V		1.1 V	1.1 V	–20			–20			
	V <sub>I</sub> = 0.91 V		1.4 V	1.4 V	–40			–30			
	V <sub>I</sub> = 1.07 V		1.65 V	1.65 V	–55			–45			
	V <sub>I</sub> = 1.6 V		2.3 V	2.3 V	–90			–80			
	V <sub>I</sub> = 2.0 V		3 V	3 V	–145			–135			
I <sub>BHLO</sub> Bus-hold low overdrive current <sup>(5)</sup>	V <sub>I</sub> = 0 to V <sub>CC</sub>		0.75 V	0.75 V	40			40			μA
			0.84 V	0.84 V	50			50			
			0.95 V	0.95 V	65			65			
			1.3 V	1.3 V	105			105			
			1.6 V	1.6 V	150			150			
			1.95 V	1.95 V	205			205			
			2.7 V	2.7 V	335			335			
			3.6V	3.6V	480			480			

 (1) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

 (2) All typical values are for T<sub>A</sub> = 25°C.

 (3) The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub>(MAX). I<sub>BHL</sub> should be measured after lowering V<sub>I</sub> to GND and then raising it to V<sub>IL</sub>(MAX).

 (4) The bus-hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub>(MIN). I<sub>BHH</sub> should be measured after raising V<sub>I</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub>(MIN).

 (5) An external driver must source at least I<sub>BHLO</sub> to switch this node from low to high.

**Electrical Characteristics (continued)**

Over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	–40°C to 85°C			–40°C to 125°C			UNIT
				MIN	TYP <sup>(2)</sup>	MAX	MIN	TYP <sup>(2)</sup>	MAX	
I <sub>BHHO</sub>	Bus-hold high overdrive current <sup>(6)</sup> V <sub>I</sub> = 0 to V <sub>CC</sub>	0.75 V	0.75 V	–40			–40			μA
		0.84 V	0.84 V	–50			–50			
		0.95 V	0.95 V	–65			–65			
		1.3 V	1.3 V	–105			–105			
		1.6 V	1.6 V	–150			–150			
		1.95 V	1.95 V	–205			–205			
		2.7 V	2.7 V	–335			–335			
		3.6V	3.6V	–480			–480			
I <sub>I</sub>	Input leakage current Control Inputs (DIR, $\overline{OE}$ ): V <sub>I</sub> = V <sub>CCA</sub> or GND	0.65 V - 3.6 V	0.65 V - 3.6 V	–0.5		0.5	–1		1	μA
I <sub>off</sub>	Partial power down current A Port: V <sub>I</sub> or V <sub>O</sub> = 0 V - 3.6 V	0 V	0 V - 3.6 V	–8		8	–12		12	μA
	B Port: V <sub>I</sub> or V <sub>O</sub> = 0 V - 3.6 V	0 V - 3.6 V	0 V	–8		8	–12		12	
I <sub>OZ</sub>	High-impedance state output current A Port: V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>I</sub> = V <sub>CCI</sub> or GND, $\overline{OE}$ = V <sub>IH</sub>	3.6 V	3.6 V	–8		8	–12		12	μA
	B Port: V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>I</sub> = V <sub>CCI</sub> or GND, $\overline{OE}$ = V <sub>IH</sub>	3.6 V	3.6 V	–8		8	–12		12	
I <sub>CCA</sub>	V <sub>CCA</sub> supply current V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0 mA	0.65 V - 3.6 V	0.65 V - 3.6 V			20			42	μA
		0 V	3.6 V	–2			–12			
		3.6 V	0 V			13			27	
I <sub>CCB</sub>	V <sub>CCB</sub> supply current V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0 mA	0.65 V - 3.6 V	0.65 V - 3.6 V			20			40	μA
		0 V	3.6 V			13			27	
		3.6 V	0 V	–2			–12			
I <sub>CCA</sub> + I <sub>CCB</sub>	Combined supply current V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0 mA	0.65 V - 3.6 V	0.65 V - 3.6 V			30			60	μA
C <sub>i</sub>	Input capacitance Control Inputs (DIR, $\overline{OE}$ ): V <sub>I</sub> = 3.3 V or GND	3.3 V	3.3 V		4.5			4.5		pF
C <sub>io</sub>	Data I/O capacitance Ports A and B: $\overline{OE}$ = V <sub>CCA</sub> , V <sub>O</sub> = 1.65V DC + 1 MHz -16 dBm sine wave	3.3 V	3.3 V		7.3			7.3		pF

(6) An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.

## 6.6 Switching Characteristics, $V_{CCA} = 0.7\text{ V}$

See [Figure 1](#) and [Figure 2](#) for test circuit and loading conditions. See [Figure 3](#) and [Figure 4](#) for measurement waveforms.

PARAMETER		TEST CONDITION	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )								UNIT	
			0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$t_{pd}$	Propagation delay	A input to B output	-40°C to 85°C	0.5	178	0.5	115	0.5	83	0.5	49	ns
			-40°C to 125°C	0.5	178	0.5	115	0.5	83	0.5	49	
	B input to A output	-40°C to 85°C	0.5	178	0.5	159	0.5	132	0.5	94		
		-40°C to 125°C	0.5	178	0.5	159	0.5	132	0.5	94		
$t_{dis}$	Disable time	$\overline{OE}$ input to A output	-40°C to 85°C	0.5	194	0.5	194	0.5	194	0.5	194	ns
			-40°C to 125°C	0.5	194	0.5	194	0.5	194	0.5	194	
	$\overline{OE}$ input to B output	-40°C to 85°C	0.5	216	0.5	179	0.5	158	0.5	78		
		-40°C to 125°C	0.5	216	0.5	179	0.5	158	0.5	78		
$t_{en}$	Enable time	$\overline{OE}$ input to A output	-40°C to 85°C	0.5	240	0.5	240	0.5	240	0.5	240	ns
			-40°C to 125°C	0.5	240	0.5	240	0.5	240	0.5	240	
	$\overline{OE}$ input to B output	-40°C to 85°C	0.5	292	0.5	180	0.5	125	0.5	76		
		-40°C to 125°C	0.5	292	0.5	180	0.5	125	0.5	76		

PARAMETER		TEST CONDITION	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )								UNIT	
			1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$t_{pd}$	Propagation delay	A input to B output	-40°C to 85°C	0.5	47	0.5	50	0.5	62	0.5	151	ns
			-40°C to 125°C	0.5	47	0.5	50	0.5	62	0.5	151	
	B input to A output	-40°C to 85°C	0.5	89	0.5	88	0.5	87	0.5	86		
		-40°C to 125°C	0.5	89	0.5	88	0.5	87	0.5	86		
$t_{dis}$	Disable time	$\overline{OE}$ input to A output	-40°C to 85°C	0.5	194	0.5	194	0.5	194	0.5	194	ns
			-40°C to 125°C	0.5	194	0.5	194	0.5	194	0.5	194	
	$\overline{OE}$ input to B output	-40°C to 85°C	0.5	70	0.5	69	0.5	67	0.5	101		
		-40°C to 125°C	0.5	70	0.5	69	0.5	67	0.5	101		
$t_{en}$	Enable time	$\overline{OE}$ input to A output	-40°C to 85°C	0.5	240	0.5	240	0.5	240	0.5	240	ns
			-40°C to 125°C	0.5	240	0.5	240	0.5	240	0.5	240	
	$\overline{OE}$ input to B output	-40°C to 85°C	0.5	69	0.5	69	0.5	84	0.5	552		
		-40°C to 125°C	0.5	69	0.5	69	0.5	84	0.5	552		



## 6.7 Switching Characteristics, $V_{CCA} = 0.8\text{ V}$

See [Figure 1](#) and [Figure 2](#) for test circuit and loading conditions. See [Figure 3](#) and [Figure 4](#) for measurement waveforms.

PARAMETER		TEST CONDITION	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )								UNIT		
			0.7 V $\pm$ 0.05 V		0.8 V $\pm$ 0.04 V		0.9 V $\pm$ 0.045 V		1.2 V $\pm$ 0.1 V				
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{pd}$	Propagation delay	A input to B output	–40°C to 85°C		0.5	159	0.5	96	0.5	64	0.5	33	ns
			–40°C to 125°C		0.5	159	0.5	96	0.5	64	0.5	33	
	B input to A output	–40°C to 85°C		0.5	117	0.5	97	0.5	79	0.5	54		
		–40°C to 125°C		0.5	117	0.5	97	0.5	79	0.5	54		
$t_{dis}$	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	154	0.5	154	0.5	154	0.5	154	ns
			–40°C to 125°C		0.5	154	0.5	154	0.5	154	0.5	154	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	202	0.5	165	0.5	144	0.5	65		
		–40°C to 125°C		0.5	202	0.5	165	0.5	144	0.5	65		
$t_{en}$	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	137	0.5	137	0.5	137	0.5	137	ns
			–40°C to 125°C		0.5	137	0.5	137	0.5	137	0.5	137	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	270	0.5	160	0.5	104	0.5	55		
		–40°C to 125°C		0.5	270	0.5	160	0.5	104	0.5	55		

PARAMETER		TEST CONDITION	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )								UNIT		
			1.5 V $\pm$ 0.1 V		1.8 V $\pm$ 0.15 V		2.5 V $\pm$ 0.2 V		3.3 V $\pm$ 0.3 V				
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{pd}$	Propagation delay	A input to B output	–40°C to 85°C		0.5	27	0.5	26	0.5	26	0.5	35	ns
			–40°C to 125°C		0.5	27	0.5	26	0.5	26	0.5	35	
	B input to A output	–40°C to 85°C		0.5	44	0.5	43	0.5	42	0.5	41		
		–40°C to 125°C		0.5	44	0.5	43	0.5	42	0.5	41		
$t_{dis}$	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	154	0.5	154	0.5	154	0.5	154	ns
			–40°C to 125°C		0.5	154	0.5	154	0.5	154	0.5	154	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	57	0.5	55	0.5	50	0.5	52		
		–40°C to 125°C		0.5	57	0.5	55	0.5	50	0.5	52		
$t_{en}$	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	137	0.5	137	0.5	137	0.5	137	ns
			–40°C to 125°C		0.5	137	0.5	137	0.5	137	0.5	137	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	46	0.5	44	0.5	46	0.5	59		
		–40°C to 125°C		0.5	46	0.5	44	0.5	46	0.5	59		

## 6.8 Switching Characteristics, $V_{CCA} = 0.9\text{ V}$

See [Figure 1](#) and [Figure 2](#) for test circuit and loading conditions. See [Figure 3](#) and [Figure 4](#) for measurement waveforms.

PARAMETER		TEST CONDITION	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )								UNIT	
			0.7 V $\pm$ 0.05 V		0.8 V $\pm$ 0.04 V		0.9 V $\pm$ 0.045 V		1.2 V $\pm$ 0.1 V			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$t_{pd}$	Propagation delay	A input to output	-40°C to 85°C	0.5	133	0.5	79	0.5	53	0.5	23	ns
			-40°C to 125°C	0.5	133	0.5	79	0.5	53	0.5	23	
	B input to A output	-40°C to 85°C	0.5	84	0.5	64	0.5	53	0.5	41		
		-40°C to 125°C	0.5	84	0.5	64	0.5	53	0.5	41		
$t_{dis}$	Disable time	$\overline{OE}$ input to A output	-40°C to 85°C	0.5	130	0.5	130	0.5	130	0.5	130	ns
			-40°C to 125°C	0.5	130	0.5	130	0.5	130	0.5	130	
	$\overline{OE}$ input to B output	-40°C to 85°C	0.5	193	0.5	157	0.5	137	0.5	57		
		-40°C to 125°C	0.5	193	0.5	157	0.5	137	0.5	57		
$t_{en}$	Enable time	$\overline{OE}$ input to A output	-40°C to 85°C	0.5	128	0.5	128	0.5	128	0.5	128	ns
			-40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	
	$\overline{OE}$ input to B output	-40°C to 85°C	0.5	257	0.5	149	0.5	94	0.5	45		
		-40°C to 125°C	0.5	257	0.5	149	0.5	94	0.5	45		

PARAMETER		TEST CONDITION	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )								UNIT	
			1.5 V $\pm$ 0.1 V		1.8 V $\pm$ 0.15 V		2.5 V $\pm$ 0.2 V		3.3 V $\pm$ 0.3 V			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$t_{pd}$	Propagation delay	A input to B output	-40°C to 85°C	0.5	18	0.5	16	0.5	15	0.5	18	ns
			-40°C to 125°C	0.5	18	0.5	16	0.5	15	0.5	18	
	B input to A output	-40°C to 85°C	0.5	29	0.5	25	0.5	23	0.5	22		
		-40°C to 125°C	0.5	29	0.5	25	0.5	23	0.5	22		
$t_{dis}$	Disable time	$\overline{OE}$ input to A output	-40°C to 85°C	0.5	130	0.5	130	0.5	130	0.5	130	ns
			-40°C to 125°C	0.5	130	0.5	130	0.5	130	0.5	130	
	$\overline{OE}$ input to B output	-40°C to 85°C	0.5	50	0.5	48	0.5	42	0.5	43		
		-40°C to 125°C	0.5	50	0.5	48	0.5	42	0.5	43		
$t_{en}$	Enable time	$\overline{OE}$ input to A output	-40°C to 85°C	0.5	128	0.5	128	0.5	128	0.5	128	ns
			-40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	
	$\overline{OE}$ input to B output	-40°C to 85°C	0.5	37	0.5	34	0.5	32	0.5	36		
		-40°C to 125°C	0.5	37	0.5	34	0.5	32	0.5	36		

## 6.9 Switching Characteristics, $V_{CCA} = 1.2\text{ V}$

See [Figure 1](#) and [Figure 2](#) for test circuit and loading conditions. See [Figure 3](#) and [Figure 4](#) for measurement waveforms.

PARAMETER		TEST CONDITION	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )								UNIT	
			0.7 V $\pm$ 0.05 V		0.8 V $\pm$ 0.04 V		0.9 V $\pm$ 0.045 V		1.2 V $\pm$ 0.1 V			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$t_{pd}$	Propagation delay	A input to B output	-40°C to 85°C	0.5	95	0.5	54	0.5	40	0.5	15	ns
			-40°C to 125°C	0.5	95	0.5	54	0.5	40	0.5	15	
	B input to A output	-40°C to 85°C	0.5	49	0.5	33	0.5	23	0.5	15		
		-40°C to 125°C	0.5	49	0.5	33	0.5	23	0.5	15		
$t_{dis}$	Disable time	$\overline{OE}$ input to A output	-40°C to 85°C	0.5	47	0.5	47	0.5	47	0.5	47	ns
			-40°C to 125°C	0.5	47	0.5	47	0.5	47	0.5	47	
	$\overline{OE}$ input to B output	-40°C to 85°C	0.5	181	0.5	147	0.5	127	0.5	49		
		-40°C to 125°C	0.5	181	0.5	147	0.5	127	0.5	49		
$t_{en}$	Enable time	$\overline{OE}$ input to A output	-40°C to 85°C	0.5	40	0.5	40	0.5	40	0.5	40	ns
			-40°C to 125°C	0.5	40	0.5	40	0.5	40	0.5	40	
	$\overline{OE}$ input to B output	-40°C to 85°C	0.5	221	0.5	132	0.5	81	0.5	34		
		-40°C to 125°C	0.5	221	0.5	132	0.5	81	0.5	34		

PARAMETER		TEST CONDITION	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )								UNIT	
			1.5 V $\pm$ 0.1 V		1.8 V $\pm$ 0.15 V		2.5 V $\pm$ 0.2 V		3.3 V $\pm$ 0.3 V			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$t_{pd}$	Propagation delay	A input to B output	-40°C to 85°C	0.5	11	0.5	9	0.5	8	0.5	8	ns
			-40°C to 125°C	0.5	11	0.5	9	0.5	8	0.5	8	
	B input to A output	-40°C to 85°C	0.5	12	0.5	10	0.5	8	0.5	8		
		-40°C to 125°C	0.5	12	0.5	10	0.5	8	0.5	8		
$t_{dis}$	Disable time	$\overline{OE}$ input to A output	-40°C to 85°C	0.5	47	0.5	47	0.5	47	0.5	47	ns
			-40°C to 125°C	0.5	47	0.5	47	0.5	47	0.5	47	
	$\overline{OE}$ input to B output	-40°C to 85°C	0.5	42	0.5	40	0.5	34	0.5	34		
		-40°C to 125°C	0.5	42	0.5	40	0.5	34	0.5	34		
$t_{en}$	Enable time	$\overline{OE}$ input to A output	-40°C to 85°C	0.5	39	0.5	40	0.5	40	0.5	40	ns
			-40°C to 125°C	0.5	39	0.5	40	0.5	40	0.5	40	
	$\overline{OE}$ input to B output	-40°C to 85°C	0.5	25	0.5	22	0.5	20	0.5	19		
		-40°C to 125°C	0.5	25	0.5	22	0.5	20	0.5	19		

**6.10 Switching Characteristics,  $V_{CCA} = 1.5\text{ V}$** 

 See [Figure 1](#) and [Figure 2](#) for test circuit and loading conditions. See [Figure 3](#) and [Figure 4](#) for measurement waveforms.

PARAMETER		TEST CONDITION	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )								UNIT		
			0.7 V $\pm$ 0.05 V		0.8 V $\pm$ 0.04 V		0.9 V $\pm$ 0.045 V		1.2 V $\pm$ 0.1 V				
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{pd}$	Propagation delay	A input to B output	–40°C to 85°C		0.5	90	0.5	44	0.5	29	0.5	12	ns
			–40°C to 125°C		0.5	90	0.5	44	0.5	29	0.5	12	
	B input to A output	–40°C to 85°C		0.5	47	0.5	27	0.5	18	0.5	11		
		–40°C to 125°C		0.5	47	0.5	27	0.5	18	0.5	11		
$t_{dis}$	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	37	0.5	37	0.5	37	0.5	37	ns
			–40°C to 125°C		0.5	37	0.5	37	0.5	37	0.5	37	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	176	0.5	142	0.5	122	0.5	44		
		–40°C to 125°C		0.5	176	0.5	142	0.5	122	0.5	44		
$t_{en}$	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	25	0.5	25	0.5	25	0.5	25	ns
			–40°C to 125°C		0.5	25	0.5	25	0.5	25	0.5	25	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	214	0.5	114	0.5	71	0.5	29		
		–40°C to 125°C		0.5	214	0.5	114	0.5	71	0.5	29		

PARAMETER		TEST CONDITION	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )								UNIT		
			1.5 V $\pm$ 0.1 V		1.8 V $\pm$ 0.15 V		2.5 V $\pm$ 0.2 V		3.3 V $\pm$ 0.3 V				
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{pd}$	Propagation delay	A input to B output	–40°C to 85°C		0.5	9	0.5	8	0.5	6	0.5	6	ns
			–40°C to 125°C		0.5	9	0.5	8	0.5	6	0.5	6	
	B input to A output	–40°C to 85°C		0.5	9	0.5	8	0.5	6	0.5	5		
		–40°C to 125°C		0.5	9	0.5	8	0.5	6	0.5	5		
$t_{dis}$	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	37	0.5	37	0.5	37	0.5	37	ns
			–40°C to 125°C		0.5	37	0.5	37	0.5	37	0.5	37	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	38	0.5	37	0.5	31	0.5	31		
		–40°C to 125°C		0.5	38	0.5	37	0.5	31	0.5	31		
$t_{en}$	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	25	0.5	25	0.5	25	0.5	25	ns
			–40°C to 125°C		0.5	25	0.5	25	0.5	25	0.5	25	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	21	0.5	18	0.5	15	0.5	13		
		–40°C to 125°C		0.5	21	0.5	18	0.5	15	0.5	13		

## 6.11 Switching Characteristics, $V_{CCA} = 1.8\text{ V}$

See [Figure 1](#) and [Figure 2](#) for test circuit and loading conditions. See [Figure 3](#) and [Figure 4](#) for measurement waveforms.

PARAMETER		TEST CONDITION	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )								UNIT		
			0.7 V $\pm$ 0.05 V		0.8 V $\pm$ 0.04 V		0.9 V $\pm$ 0.045 V		1.2 V $\pm$ 0.1 V				
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{pd}$	Propagation delay	A input to B output	–40°C to 85°C		0.5	88	0.5	43	0.5	25	0.5	10	ns
			–40°C to 125°C		0.5	88	0.5	43	0.5	25	0.5	10	
	B input to A output	–40°C to 85°C		0.5	50	0.5	26	0.5	16	0.5	9		
		–40°C to 125°C		0.5	50	0.5	26	0.5	16	0.5	9		
$t_{dis}$	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	35	0.5	35	0.5	35	0.5	35	ns
			–40°C to 125°C		0.5	35	0.5	35	0.5	35	0.5	35	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	174	0.5	139	0.5	119	0.5	42		
		–40°C to 125°C		0.5	174	0.5	139	0.5	119	0.5	42		
$t_{en}$	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	20	0.5	20	0.5	20	0.5	20	ns
			–40°C to 125°C		0.5	20	0.5	20	0.5	20	0.5	20	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	213	0.5	111	0.5	67	0.5	27		
		–40°C to 125°C		0.5	213	0.5	111	0.5	67	0.5	27		

PARAMETER		TEST CONDITION	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )								UNIT		
			1.5 V $\pm$ 0.1 V		1.8 V $\pm$ 0.15 V		2.5 V $\pm$ 0.2 V		3.3 V $\pm$ 0.3 V				
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{pd}$	Propagation delay	A input to B output	–40°C to 85°C		0.5	8	0.5	7	0.5	6	0.5	5	ns
			–40°C to 125°C		0.5	8	0.5	7	0.5	6	0.5	5	
	B input to A output	–40°C to 85°C		0.5	7	0.5	6	0.5	5	0.5	4		
		–40°C to 125°C		0.5	7	0.5	7	0.5	5	0.5	4		
$t_{dis}$	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	35	0.5	35	0.5	35	0.5	35	ns
			–40°C to 125°C		0.5	35	0.5	35	0.5	35	0.5	35	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	36	0.5	35	0.5	30	0.5	29		
		–40°C to 125°C		0.5	36	0.5	35	0.5	30	0.5	29		
$t_{en}$	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	20	0.5	20	0.5	20	0.5	20	ns
			–40°C to 125°C		0.5	20	0.5	20	0.5	20	0.5	20	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	19	0.5	16	0.5	13	0.5	11		
		–40°C to 125°C		0.5	19	0.5	16	0.5	13	0.5	11		

## 6.12 Switching Characteristics, $V_{CCA} = 2.5\text{ V}$

See [Figure 1](#) and [Figure 2](#) for test circuit and loading conditions. See [Figure 3](#) and [Figure 4](#) for measurement waveforms.

PARAMETER		TEST CONDITION	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )								UNIT		
			0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V				
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{pd}$	Propagation delay	A input to B output	–40°C to 85°C		0.5	87	0.5	42	0.5	23	0.5	8	ns
			–40°C to 125°C		0.5	87	0.5	42	0.5	23	0.5	8	
	B input to A output	–40°C to 85°C		0.5	62	0.5	26	0.5	15	0.5	8		
		–40°C to 125°C		0.5	62	0.5	26	0.5	15	0.5	8		
$t_{dis}$	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	28	0.5	28	0.5	28	0.5	28	ns
			–40°C to 125°C		0.5	28	0.5	28	0.5	28	0.5	28	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	173	0.5	137	0.5	117	0.5	40		
		–40°C to 125°C		0.5	173	0.5	137	0.5	117	0.5	40		
$t_{en}$	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	13	0.5	13	0.5	13	0.5	13	ns
			–40°C to 125°C		0.5	13	0.5	13	0.5	13	0.5	13	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	211	0.5	107	0.5	63	0.5	24		
		–40°C to 125°C		0.5	211	0.5	107	0.5	63	0.5	24		

PARAMETER		TEST CONDITION	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )								UNIT		
			1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V				
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{pd}$	Propagation delay	A input to B output	–40°C to 85°C		0.5	6	0.5	6	0.5	5	0.5	5	ns
			–40°C to 125°C		0.5	6	0.5	6	0.5	5	0.5	5	
	B input to A output	–40°C to 85°C		0.5	6	0.5	6	0.5	5	0.5	4		
		–40°C to 125°C		0.5	6	0.5	6	0.5	5	0.5	4		
$t_{dis}$	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	28	0.5	28	0.5	28	0.5	28	ns
			–40°C to 125°C		0.5	28	0.5	28	0.5	28	0.5	28	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	34	0.5	33	0.5	28	0.5	28		
		–40°C to 125°C		0.5	34	0.5	33	0.5	28	0.5	28		
$t_{en}$	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	13	0.5	13	0.5	13	0.5	13	ns
			–40°C to 125°C		0.5	13	0.5	13	0.5	13	0.5	13	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	16	0.5	14	0.5	10	0.5	9		
		–40°C to 125°C		0.5	16	0.5	14	0.5	10	0.5	9		

### 6.13 Switching Characteristics, $V_{CCA} = 3.3\text{ V}$

See [Figure 1](#) and [Figure 2](#) for test circuit and loading conditions. See [Figure 3](#) and [Figure 4](#) for measurement waveforms.

PARAMETER		TEST CONDITION	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )								UNIT		
			0.7 V $\pm$ 0.05 V		0.8 V $\pm$ 0.04 V		0.9 V $\pm$ 0.045 V		1.2 V $\pm$ 0.1 V				
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{pd}$	Propagation delay	A input to B output	–40°C to 85°C		0.5	87	0.5	41	0.5	22	0.5	8	ns
			–40°C to 125°C		0.5	87	0.5	41	0.5	22	0.5	8	
	B input to A output	–40°C to 85°C		0.5	151	0.5	36	0.5	18	0.5	8		
		–40°C to 125°C		0.5	151	0.5	36	0.5	18	0.5	8		
$t_{dis}$	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	27	0.5	27	0.5	27	0.5	27	ns
			–40°C to 125°C		0.5	27	0.5	27	0.5	27	0.5	27	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	172	0.5	136	0.5	116	0.5	39		
		–40°C to 125°C		0.5	172	0.5	136	0.5	116	0.5	39		
$t_{en}$	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	11	0.5	11	0.5	11	0.5	11	ns
			–40°C to 125°C		0.5	11	0.5	11	0.5	11	0.5	11	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	210	0.5	106	0.5	62	0.5	23		
		–40°C to 125°C		0.5	210	0.5	106	0.5	62	0.5	23		

PARAMETER		TEST CONDITION	B-PORT SUPPLY VOLTAGE ( $V_{CCB}$ )								UNIT		
			1.5 V $\pm$ 0.1 V		1.8 V $\pm$ 0.15 V		2.5 V $\pm$ 0.2 V		3.3 V $\pm$ 0.3 V				
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$t_{pd}$	Propagation delay	A input to B output	–40°C to 85°C		0.5	5	0.5	5	0.5	4	0.5	4	ns
			–40°C to 125°C		0.5	5	0.5	5	0.5	4	0.5	4	
	B input to A output	–40°C to 85°C		0.5	6	0.5	5	0.5	5	0.5	4		
		–40°C to 125°C		0.5	6	0.5	5	0.5	5	0.5	4		
$t_{dis}$	Disable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	27	0.5	27	0.5	27	0.5	27	ns
			–40°C to 125°C		0.5	27	0.5	27	0.5	27	0.5	27	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	33	0.5	32	0.5	27	0.5	27		
		–40°C to 125°C		0.5	33	0.5	32	0.5	27	0.5	27		
$t_{en}$	Enable time	$\overline{OE}$ input to A output	–40°C to 85°C		0.5	11	0.5	11	0.5	11	0.5	11	ns
			–40°C to 125°C		0.5	11	0.5	11	0.5	11	0.5	11	
	$\overline{OE}$ input to B output	–40°C to 85°C		0.5	15	0.5	13	0.5	10	0.5	8		
		–40°C to 125°C		0.5	15	0.5	13	0.5	10	0.5	8		

**6.14 Operating Characteristics:  $T_A = 25^\circ\text{C}$** 

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{pdA}$ Power dissipation capacitance per transceiver (A to B: outputs enabled)	$C_L = 0$ , $R_L = \text{Open}$ $f = 1 \text{ MHz}$ , $t_r = t_f = 1 \text{ ns}$	$V_{CCA} = V_{CCB} = 0.7 \text{ V}$		3.0	pF
		$V_{CCA} = V_{CCB} = 0.8 \text{ V}$		3.0	
		$V_{CCA} = V_{CCB} = 0.9 \text{ V}$		3.0	
		$V_{CCA} = V_{CCB} = 1.2 \text{ V}$		3.1	
		$V_{CCA} = V_{CCB} = 1.5 \text{ V}$		3.0	
		$V_{CCA} = V_{CCB} = 1.8 \text{ V}$		3.2	
		$V_{CCA} = V_{CCB} = 2.5 \text{ V}$		3.7	
		$V_{CCA} = V_{CCB} = 3.3 \text{ V}$		4.4	
$C_{pdA}$ Power dissipation capacitance per transceiver (A to B: outputs disabled)	$C_L = 0$ , $R_L = \text{Open}$ $f = 1 \text{ MHz}$ , $t_r = t_f = 1 \text{ ns}$	$V_{CCA} = V_{CCB} = 0.7 \text{ V}$		2.5	pF
		$V_{CCA} = V_{CCB} = 0.8 \text{ V}$		2.5	
		$V_{CCA} = V_{CCB} = 0.9 \text{ V}$		2.6	
		$V_{CCA} = V_{CCB} = 1.2 \text{ V}$		2.6	
		$V_{CCA} = V_{CCB} = 1.5 \text{ V}$		2.6	
		$V_{CCA} = V_{CCB} = 1.8 \text{ V}$		2.7	
		$V_{CCA} = V_{CCB} = 2.5 \text{ V}$		3.2	
		$V_{CCA} = V_{CCB} = 3.3 \text{ V}$		3.9	
$C_{pdA}$ Power dissipation capacitance per transceiver (B to A: outputs enabled)	$C_L = 0$ , $R_L = \text{Open}$ $f = 1 \text{ MHz}$ , $t_r = t_f = 1 \text{ ns}$	$V_{CCA} = V_{CCB} = 0.7 \text{ V}$		12.6	pF
		$V_{CCA} = V_{CCB} = 0.8 \text{ V}$		12.3	
		$V_{CCA} = V_{CCB} = 0.9 \text{ V}$		12.4	
		$V_{CCA} = V_{CCB} = 1.2 \text{ V}$		12.4	
		$V_{CCA} = V_{CCB} = 1.5 \text{ V}$		12.7	
		$V_{CCA} = V_{CCB} = 1.8 \text{ V}$		13.6	
		$V_{CCA} = V_{CCB} = 2.5 \text{ V}$		17.4	
		$V_{CCA} = V_{CCB} = 3.3 \text{ V}$		20.9	
$C_{pdA}$ Power dissipation capacitance per transceiver (B to A: outputs disabled)	$C_L = 0$ , $R_L = \text{Open}$ $f = 1 \text{ MHz}$ , $t_r = t_f = 1 \text{ ns}$	$V_{CCA} = V_{CCB} = 0.7 \text{ V}$		1.2	pF
		$V_{CCA} = V_{CCB} = 0.8 \text{ V}$		1.1	
		$V_{CCA} = V_{CCB} = 0.9 \text{ V}$		1.1	
		$V_{CCA} = V_{CCB} = 1.2 \text{ V}$		1.0	
		$V_{CCA} = V_{CCB} = 1.5 \text{ V}$		1.0	
		$V_{CCA} = V_{CCB} = 1.8 \text{ V}$		0.9	
		$V_{CCA} = V_{CCB} = 2.5 \text{ V}$		0.9	
		$V_{CCA} = V_{CCB} = 3.3 \text{ V}$		0.9	



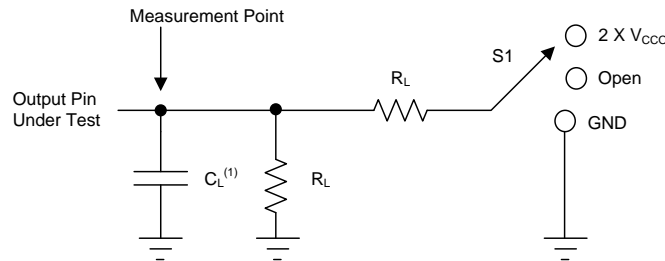
**Operating Characteristics:  $T_A = 25^\circ\text{C}$  (continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{pdB}$ Power dissipation capacitance per transceiver (A to B: outputs enabled)	$C_L = 0$ , $R_L = \text{Open}$ $f = 1 \text{ MHz}$ , $t_r = t_f = 1 \text{ ns}$	$V_{CCA} = V_{CCB} = 0.7 \text{ V}$		12.6	pF
		$V_{CCA} = V_{CCB} = 0.8 \text{ V}$		12.4	
		$V_{CCA} = V_{CCB} = 0.9 \text{ V}$		12.4	
		$V_{CCA} = V_{CCB} = 1.2 \text{ V}$		12.4	
		$V_{CCA} = V_{CCB} = 1.5 \text{ V}$		12.6	
		$V_{CCA} = V_{CCB} = 1.8 \text{ V}$		13.6	
		$V_{CCA} = V_{CCB} = 2.5 \text{ V}$		17.2	
		$V_{CCA} = V_{CCB} = 3.3 \text{ V}$		20.8	
$C_{pdB}$ Power dissipation capacitance per transceiver (A to B: outputs disabled)	$C_L = 0$ , $R_L = \text{Open}$ $f = 1 \text{ MHz}$ , $t_r = t_f = 1 \text{ ns}$	$V_{CCA} = V_{CCB} = 0.7 \text{ V}$		1.4	pF
		$V_{CCA} = V_{CCB} = 0.8 \text{ V}$		1.3	
		$V_{CCA} = V_{CCB} = 0.9 \text{ V}$		1.3	
		$V_{CCA} = V_{CCB} = 1.2 \text{ V}$		1.2	
		$V_{CCA} = V_{CCB} = 1.5 \text{ V}$		1.1	
		$V_{CCA} = V_{CCB} = 1.8 \text{ V}$		1.1	
		$V_{CCA} = V_{CCB} = 2.5 \text{ V}$		1.1	
		$V_{CCA} = V_{CCB} = 3.3 \text{ V}$		1.0	
$C_{pdB}$ Power dissipation capacitance per transceiver (B to A: outputs enabled)	$C_L = 0$ , $R_L = \text{Open}$ $f = 1 \text{ MHz}$ , $t_r = t_f = 1 \text{ ns}$	$V_{CCA} = V_{CCB} = 0.7 \text{ V}$		3.3	pF
		$V_{CCA} = V_{CCB} = 0.8 \text{ V}$		3.3	
		$V_{CCA} = V_{CCB} = 0.9 \text{ V}$		3.3	
		$V_{CCA} = V_{CCB} = 1.2 \text{ V}$		3.2	
		$V_{CCA} = V_{CCB} = 1.5 \text{ V}$		3.2	
		$V_{CCA} = V_{CCB} = 1.8 \text{ V}$		3.3	
		$V_{CCA} = V_{CCB} = 2.5 \text{ V}$		3.6	
		$V_{CCA} = V_{CCB} = 3.3 \text{ V}$		4.4	
$C_{pdB}$ Power dissipation capacitance per transceiver (B to A: outputs disabled)	$C_L = 0$ , $R_L = \text{Open}$ $f = 1 \text{ MHz}$ , $t_r = t_f = 1 \text{ ns}$	$V_{CCA} = V_{CCB} = 0.7 \text{ V}$		2.8	pF
		$V_{CCA} = V_{CCB} = 0.8 \text{ V}$		2.8	
		$V_{CCA} = V_{CCB} = 0.9 \text{ V}$		2.8	
		$V_{CCA} = V_{CCB} = 1.2 \text{ V}$		2.8	
		$V_{CCA} = V_{CCB} = 1.5 \text{ V}$		2.7	
		$V_{CCA} = V_{CCB} = 1.8 \text{ V}$		2.8	
		$V_{CCA} = V_{CCB} = 2.5 \text{ V}$		3.1	
		$V_{CCA} = V_{CCB} = 3.3 \text{ V}$		3.9	

## 7 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- $f = 1$  MHz
- $Z_0 = 50 \Omega$
- $dv / dt \leq 1$  ns/V



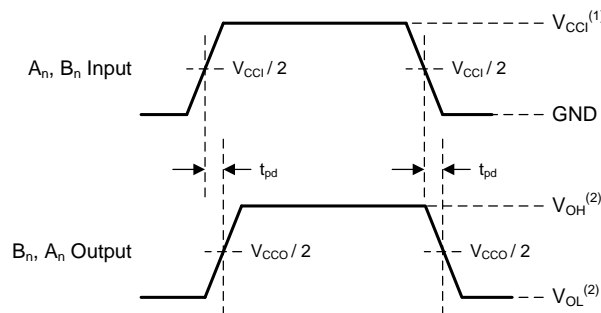
(1)  $C_L$  includes probe and jig capacitance.

Figure 1. Load Circuit

Parameter	$V_{CC0}$	$R_L$	$C_L$	S1	$V_{TP}$
$t_{pd}$	1.1 V - 3.6 V	2 k $\Omega$	15 pF	Open	N/A
	0.65 V - 0.95 V	20 k $\Omega$	15 pF	Open	N/A
$t_{en}^{(1)}, t_{dis}^{(1)}$	3 V - 3.6 V	2 k $\Omega$	15 pF	2 X $V_{CC0}$	0.3 V
	1.65 V - 2.7 V	2 k $\Omega$	15 pF	2 X $V_{CC0}$	0.15 V
	1.1 V - 1.6 V	2 k $\Omega$	15 pF	2 X $V_{CC0}$	0.1 V
	0.65 V - 0.95 V	20 k $\Omega$	15 pF	2 X $V_{CC0}$	0.1 V
$t_{en}^{(2)}, t_{dis}^{(2)}$	3 V - 3.6 V	2 k $\Omega$	15 pF	GND	0.3 V
	1.65 V - 2.7 V	2 k $\Omega$	15 pF	GND	0.15 V
	1.1 V - 1.6 V	2 k $\Omega$	15 pF	GND	0.1 V
	0.65 V - 0.95 V	20 k $\Omega$	15 pF	GND	0.1 V

- (1) Output waveform on the conditions that input is driven to a valid Logic Low.  
 (2) Output waveform on the condition that input is driven to a valid Logic High.

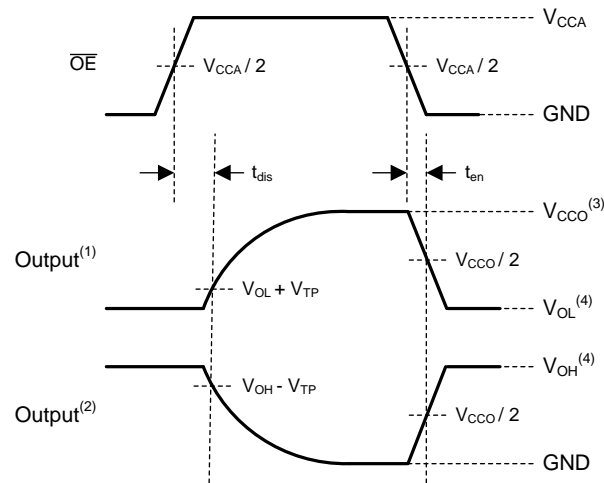
Figure 2. Load Circuit Conditions



- (1)  $V_{CC1}$  is the supply pin associated with the input port.  
 (2)  $V_{OH}$  and  $V_{OL}$  are typical output voltage levels with specified  $R_L$ ,  $C_L$ , and  $S_1$ .

Figure 3. Propagation Delay

**Parameter Measurement Information (continued)**



- (1) Output waveform on the condition that input is driven to a valid Logic Low.
- (2) Output waveform on the condition that input is driven to a valid Logic High.
- (3)  $V_{CCO}$  is the supply pin associated with the output port.
- (4)  $V_{OH}$  and  $V_{OL}$  are typical output voltage levels with specified  $R_L$ ,  $C_L$ , and  $S_1$ .

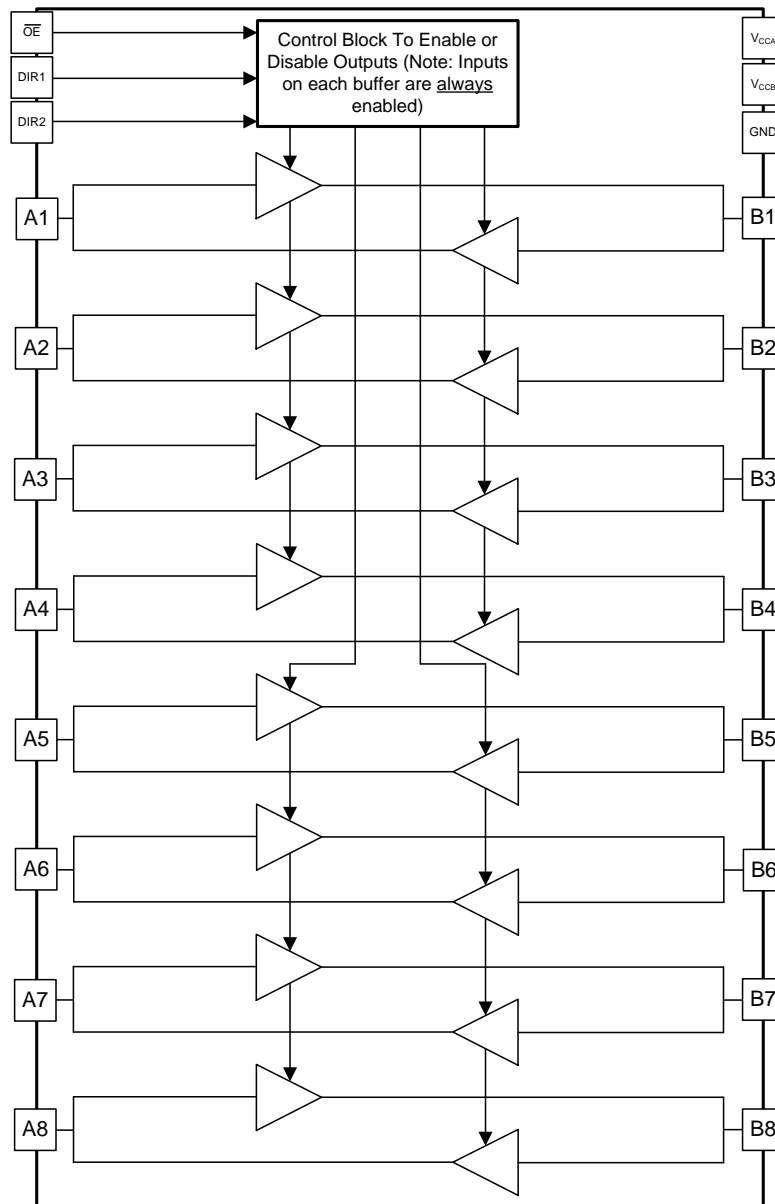
**Figure 4. Enable Time And Disable Time**

## 8 Detailed Description

### 8.1 Overview

The SN74AXCH8T245 device is an 8-bit, dual-supply non-inverting transceiver with bidirectional voltage level translation. The I/O pins labeled with A and the control pins (DIR1, DIR2, and  $\overline{OE}$ ) are supported by  $V_{CCA}$ , and the I/O pins labeled with B are supported by  $V_{CCB}$ . Both the A port and the B port are able to accept I/O voltages ranging from 0.65 V to 3.6 V.

### 8.2 Functional Block Diagram



**Figure 5. Functional Block Diagram**

## 8.3 Feature Description

### 8.3.1 Up-Translation and Down-Translation From 0.65 V to 3.6 V

Both supply pins are configurable over the full 0.65 V to 3.6 V voltage range, which makes the device suitable for translating between any of the low voltage nodes (0.7 V, 0.8 V, 0.9 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V).

### 8.3.2 Multiple Direction Control Pins

Two control pins are used to configure the 8 data I/Os. I/O channels 1 through 4 are grouped together and I/O channels 5 through 8 are banked together. The benefit of this is to permit simultaneous up-translation and down-translation within one device. This eliminates the need for multiple devices, where each device can only provide up-translation or down-translation sequentially. Simultaneous up and down translation is supported when both  $V_{CCA}$  and  $V_{CCB}$  are at least 1.40 V.

### 8.3.3 Bus-Hold Circuitry

Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state, which helps with board space savings and reduced component costs. Use of pull-up or pull-down resistors with the bus-hold circuitry is not recommended. See the Bus-Hold Circuit application note for more details. ([SCLA015](#)).

Note that the bus-hold circuitry always remains active when the corresponding supply is present (i.e. B port bus-hold circuits are active when  $V_{CCB}$  is present, and A port bus-hold circuits are active when  $V_{CCA}$  is present). The bus hold circuitry is also active even when the device is in a partial power down state or when the output enable pin is used to place all outputs into high impedance.

### 8.3.4 $I_{off}$ Supports Partial-Power-Down Mode Operation

This feature is to limit the leakage current of an I/O pin being driven to a voltage as large as 3.6 V while having its corresponding power supply rail powered down. This is represented by the  $I_{off}$  parameter in the [Electrical Characteristics](#) table.

## 8.4 Device Functional Modes

All control inputs are referenced to  $V_{CCA}$  and must be driven to a valid Logic High or Logic Low (that is, not floating) to assure proper device operation and to prevent excessive power consumption. [Table 1](#) summarizes the possible modes of device operation based on the configuration of the control inputs.

**Table 1. Function Table<sup>(1)</sup>**

CONTROL INPUTS			Signal Direction	
$\overline{OE}$	DIR1	DIR2	Bits 1:4	Bits 5:8
H	X	X	Disabled (Hi-Z)	
L	L	L	B to A	
L	L	H	B to A	A to B
L	H	L	A to B	
L	H	H	A to B	B to A

(1) Input circuits of the data I/Os are always active and must be driven to a valid logic level.

## 9 Application and Implementation

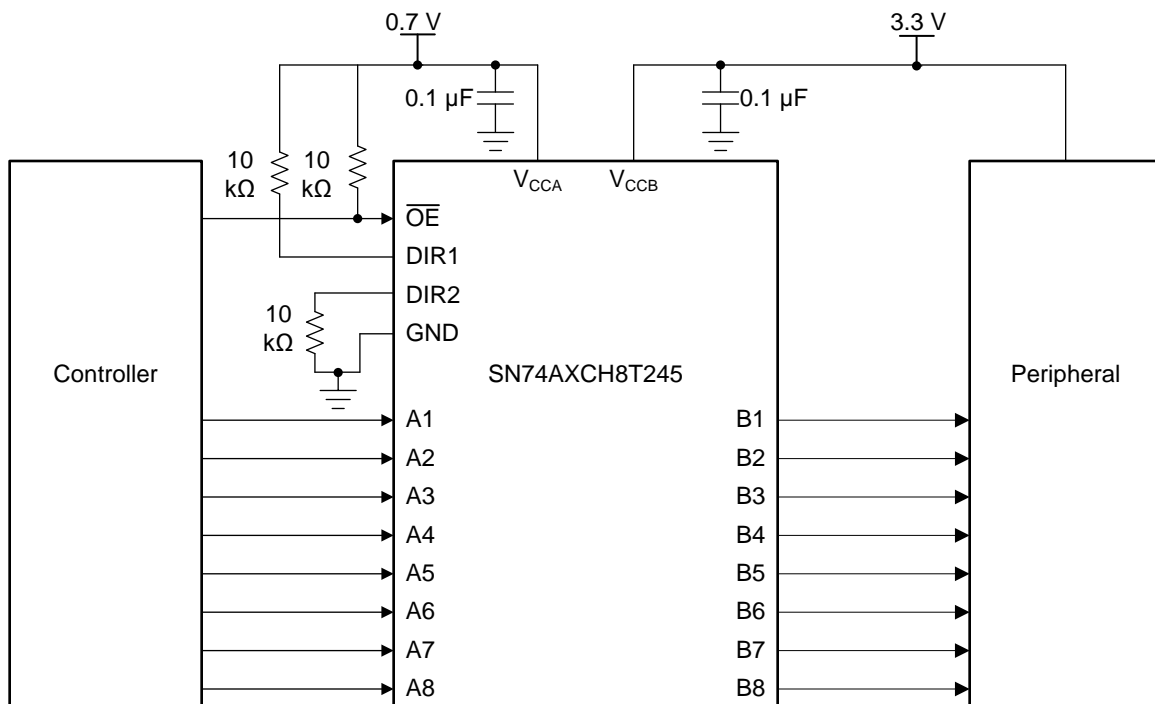
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74AXCH8T245 device can be used in level-translation applications for interfacing devices or systems operating at different voltage nodes. Figure 6 depicts an application in which the SN74AXCH8T245 device is up-translating a 0.7 V input to a 3.3 V output to interface between a system controller and a peripheral device.

### 9.2 Typical Application



**Figure 6. Typical Application Schematic**

## Typical Application (continued)

### 9.2.1 Design Requirements

For this design example, use the parameters listed in [Table 2](#).

**Table 2. Design Parameters**

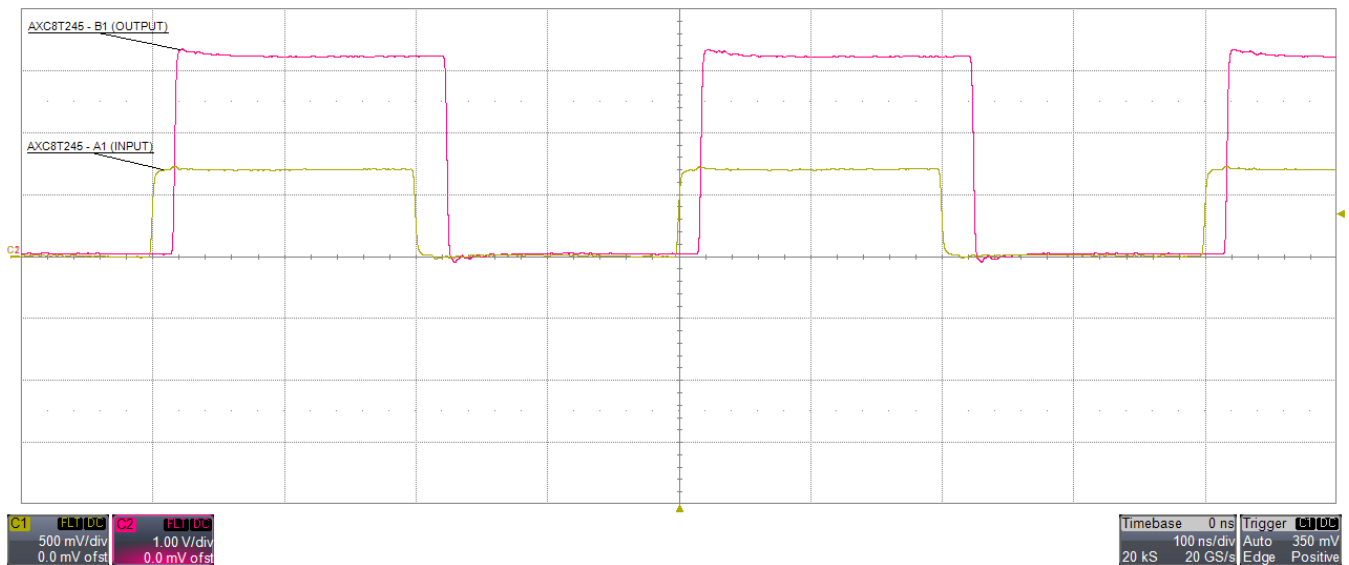
DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	0.65 V to 3.6 V
Output voltage range	0.65 V to 3.6 V

### 9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AXCH8T245 device to determine the input voltage range. For a valid logic high the value must exceed the  $V_{IH}$  of the input port. For a valid logic low the value must be less than the  $V_{IL}$  of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AXCH8T245 device is driving to determine the output voltage range.

### 9.2.3 Application Curve



**Figure 7. Translation Up (0.7 V to 3.3 V) at 2.5 MHz**

## 10 Power Supply Recommendations

Always apply a ground reference to the GND pins first. However, there are no additional requirements for power supply sequencing.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of the AXC family of level translators, see the [Power Sequencing for AXC Family of Devices](#) application report.

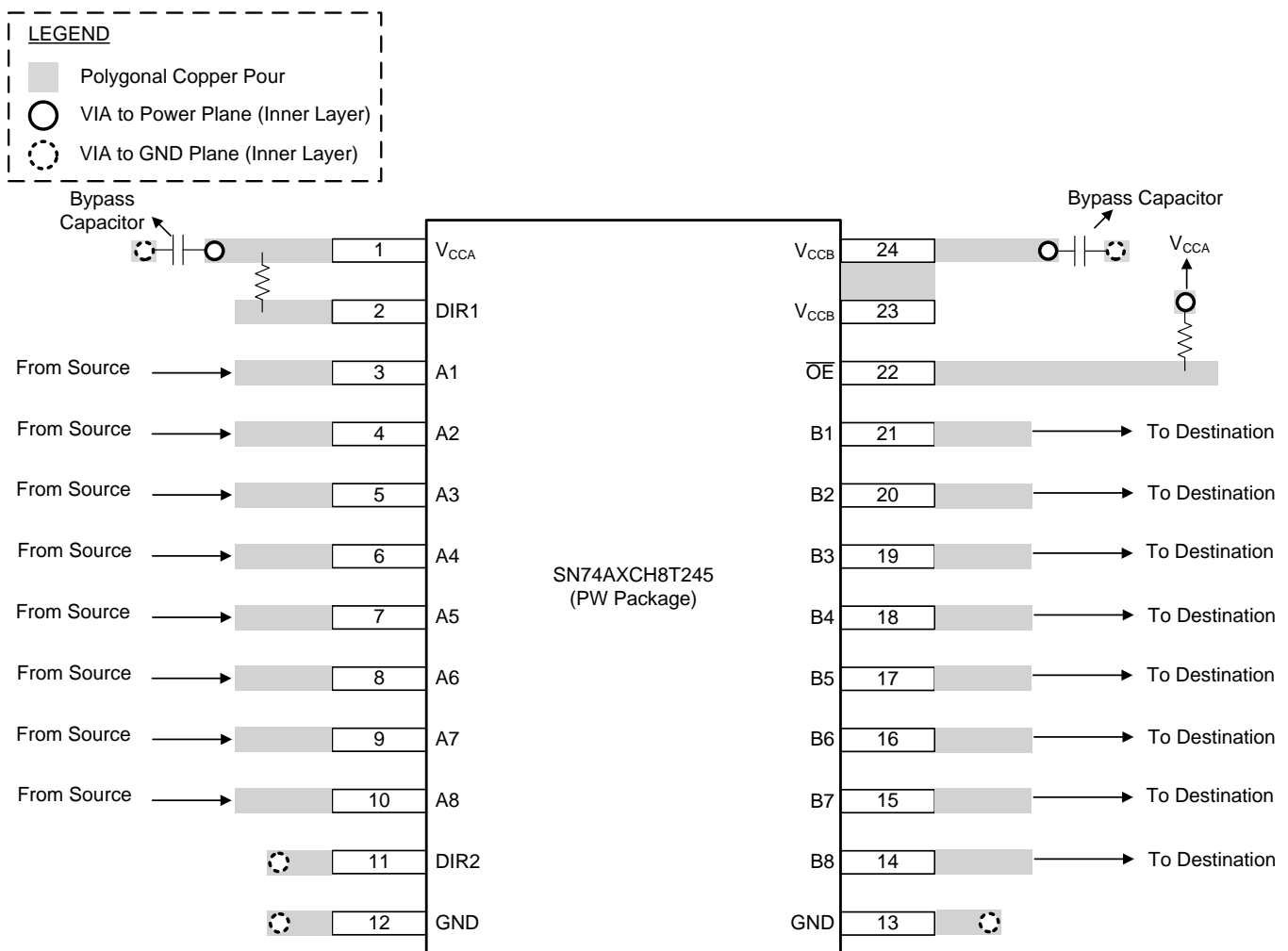
## 11 Layout

### 11.1 Layout Guidelines

To assure reliability of the device, follow common printed-circuit board layout guidelines.

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

### 11.2 Layout Example





## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#) application report
- Texas Instruments, [Power Sequencing for AXC Family of Devices](#) application report

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.

### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

### 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74AXCH8T245RHRLRG4.Z	Active	Production	VQFN (RHL)   24	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH8T245
<a href="#">SN74AXCH8T245PWR</a>	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH8T245
SN74AXCH8T245PWR.Z	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH8T245
SN74AXCH8T245PWRG4.Z	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH8T245
<a href="#">SN74AXCH8T245RHRLR</a>	Active	Production	VQFN (RHL)   24	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH8T245
SN74AXCH8T245RHRLR.Z	Active	Production	VQFN (RHL)   24	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH8T245

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AXCH8T245PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74AXCH8T245RHLR	VQFN	RHL	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AXCH8T245PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
SN74AXCH8T245RHLR	VQFN	RHL	24	3000	367.0	367.0	35.0

PW0024A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220208/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

PW0024A

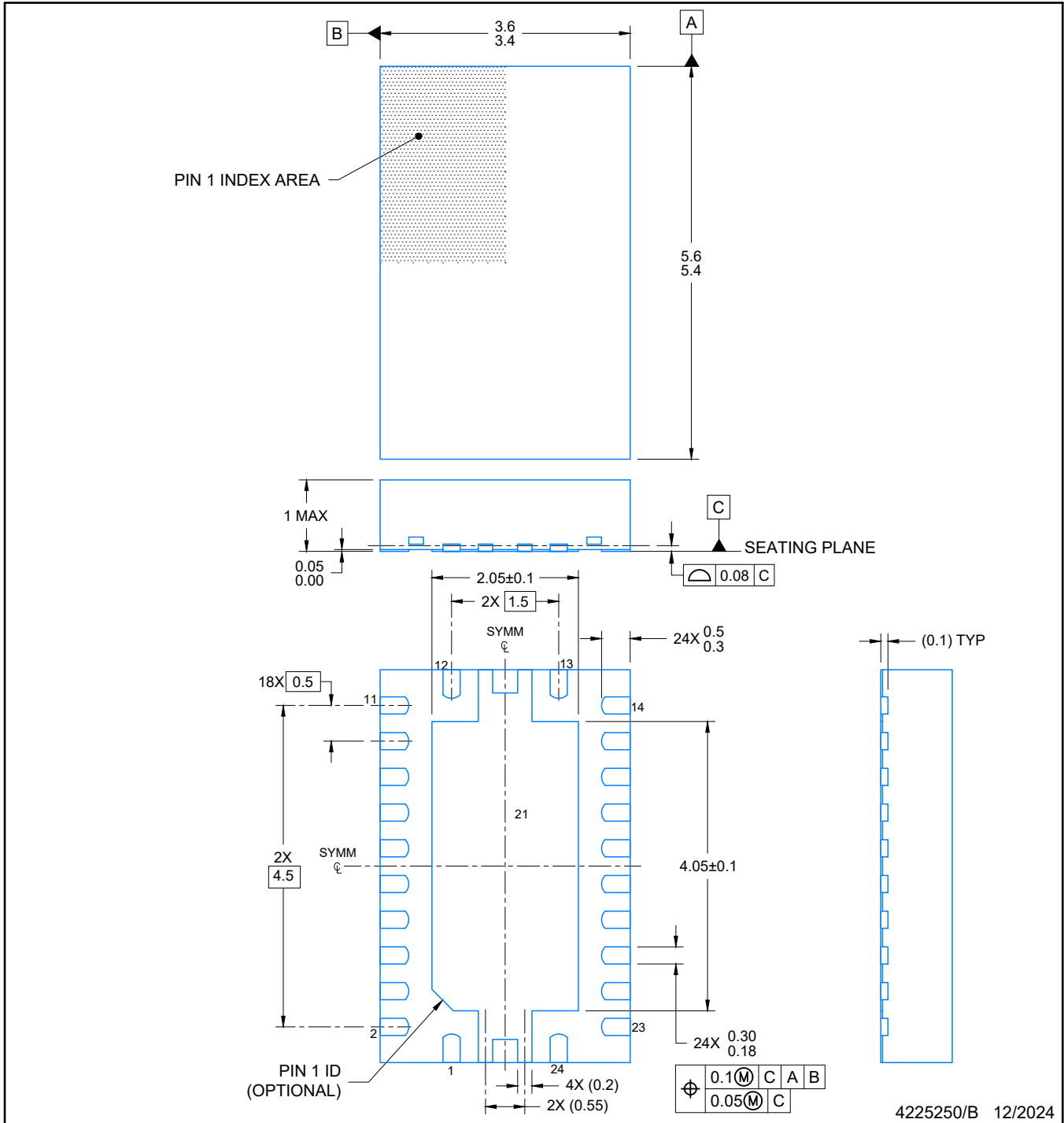
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

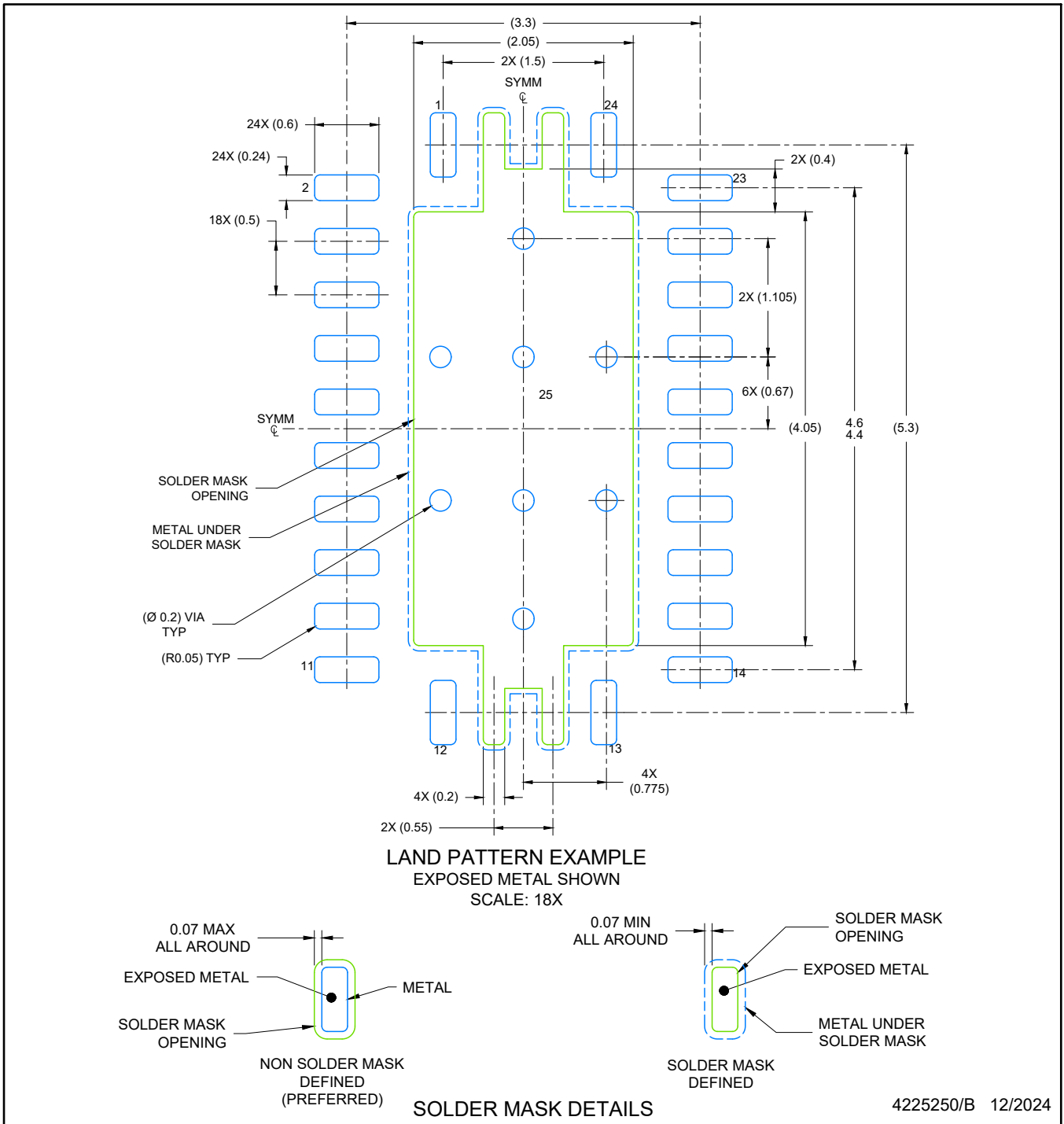
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4225250/B 12/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

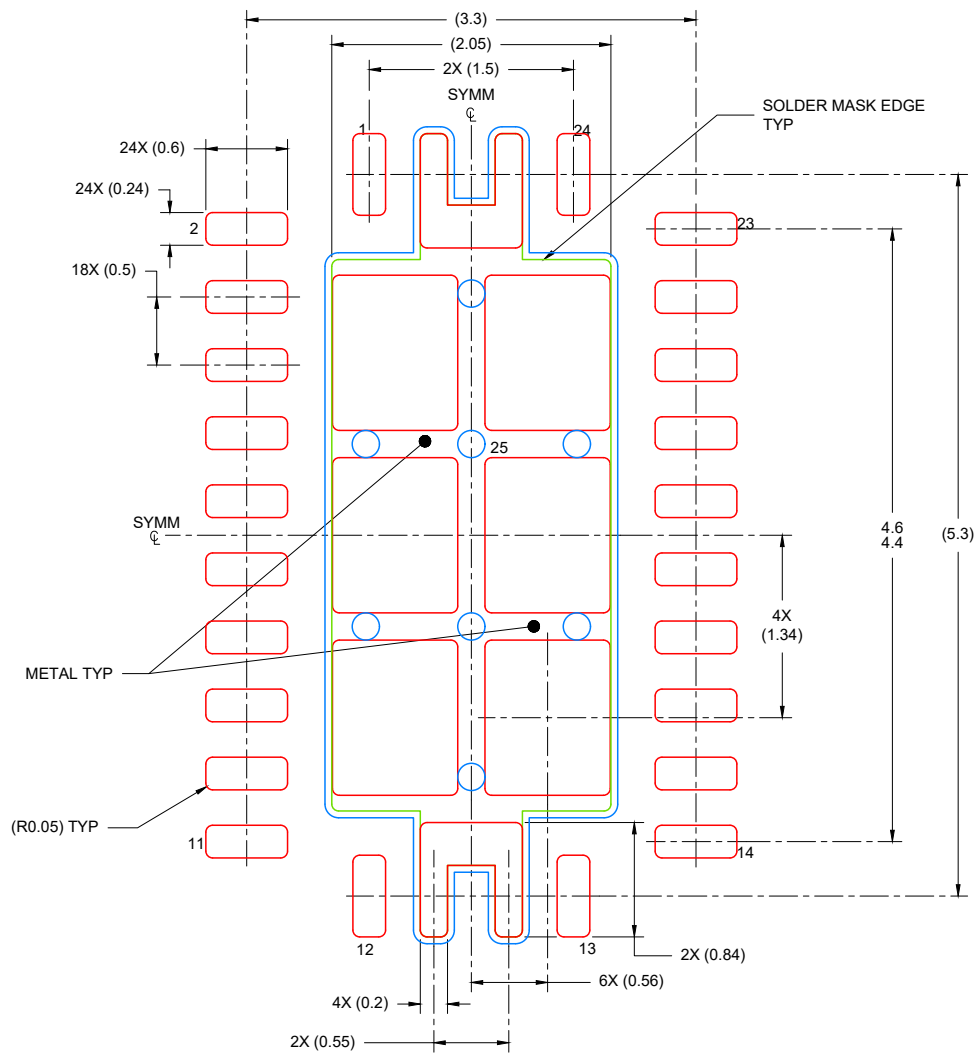
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

RHL0024A

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
80% PRINTED COVERAGE BY AREA  
SCALE: 18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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