- High-Bandwidth Data Path
  (Up To 500 MHz†)
- 5-V-Tolerant I/Os with Device Powered Up
  or Powered Down
- Low and Flat ON-State Resistance ($r_{on}$)
  Characteristics Over Operating Range
  ($r_{on} = 4 \, \Omega$ Typical)
- Rail-to-Rail Switching on Data I/O Ports
  - 0- to 5-V Switching With 3.3-V $V_{CC}$
  - 0- to 3.3-V Switching With 2.5-V $V_{CC}$
- Bidirectional Data Flow, With Near-Zero
  Propagation Delay
- Low Input/Output Capacitance Minimizes
  Loading and Signal Distortion
  ($C_{io(OFF)} = 3.5 \, pF$ Typical)
- Fast Switching Frequency
  ($f_{OE} = 20 \, MHz$ Max)

† For additional information regarding the performance
characteristics of the CB3Q family, refer to the TI
application report, CBT-C, CB3T, and CB3Q
Signal-Switch Families, literature number SCDA008.

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description/ordering information

The SN74CB3Q3244 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage
of the pass transistor, providing a low and flat ON-state resistance ($r_{on}$). The low and flat ON-state resistance
allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The
device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data
bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3244 provides an optimized
interface solution ideally suited for broadband communications, networking, and data-intensive computing
systems.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of
Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
The SN74CB3Q3244 is organized as two 4-bit bus switches with separate output-enable (1OE, 2OE) inputs. It can be used as two 4-bit bus switches or as one 8-bit bus switch. When OE is low, the associated 4-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is high, the associated 4-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The terminal assignments and function table are provided for each 4-bit bus switch.
logic diagram (positive logic)

simplified schematic, each FET switch (SW)

† EN is the internal enable signal applied to the switch.
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, \( V_{CC} \) .................................................. −0.5 V to 4.6 V
Control input voltage range, \( V_{IN} \) (see Notes 1 and 2) .................................. −0.5 V to 7 V
Switch I/O voltage range, \( V_{I/O} \) (see Notes 1, 2, and 3) ................................ −0.5 V to 7 V
Control input clamp current, \( I_{IK} \) (\( V_{IN} < 0 \)) .................................... −50 mA
I/O port clamp current, \( I_{I/OK} \) (\( V_{I/O} < 0 \)) ........................................ −50 mA
ON-state switch current, \( I_{I/O} \) (see Note 4) .............................................. ±64 mA
Continuous current through \( V_{CC} \) or GND terminals .................................. ±100 mA
Package thermal impedance, \( \theta_{JA} \) (see Note 5): DB package .................. 70°C/W
(see Note 5): DBQ package ............................................................... 68°C/W
(see Note 5): DGV package ............................................................. 92°C/W
(see Note 5): DW package .............................................................. 58°C/W
(see Note 5): GQN package ............................................................ 78°C/W
(see Note 5): PW package ............................................................... 83°C/W
(see Note 6): RGY package ............................................................ 37°C/W
Storage temperature range, \( T_{stg} \) .................................................. −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. \( V_I \) and \( V_O \) are used to denote specific conditions for \( V_{I/O} \).
4. \( I_I \) and \( I_O \) are used to denote specific conditions for \( I_{I/O} \).
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

<table>
<thead>
<tr>
<th>( V_{CC} )</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>2.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>High-level control input voltage</td>
<td>( V_{CC} = 2.3 ) V to 2.7 V</td>
<td>1.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{CC} = 2.7 ) V to 3.6 V</td>
<td>2</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Low-level control input voltage</td>
<td>( V_{CC} = 2.3 ) V to 2.7 V</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{CC} = 2.7 ) V to 3.6 V</td>
<td>0</td>
</tr>
<tr>
<td>( V_{I/O} )</td>
<td>Data input/output voltage</td>
<td>( V_{CC} = 2.3 ) V to 2.7 V</td>
<td>0</td>
</tr>
<tr>
<td>( T_A )</td>
<td>Operating free-air temperature</td>
<td>−40</td>
<td>85</td>
</tr>
</tbody>
</table>

NOTE 7: All unused control inputs of the device must be held at \( V_{CC} \) or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.
### Electrical Characteristics

**Over Recommended Operating Free-Air Temperature Range (unless otherwise noted)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP†</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>$V_{IK}$</strong></td>
<td>$V_{CC} = 3.6$ V, $I_I = −18$ mA</td>
<td></td>
<td></td>
<td>−1.8</td>
<td>V</td>
</tr>
<tr>
<td><strong>$I_{IN}$</strong></td>
<td>$V_{CC} = 3.6$ V, $V_{IN} = 0$ to $5.5$ V</td>
<td></td>
<td></td>
<td>±1</td>
<td>$\mu$A</td>
</tr>
<tr>
<td><strong>$I_{OZ}$‡</strong></td>
<td>$V_{CC} = 3.6$ V, $V_{O} = 0$ to $5.5$ V, $V_I = 0$, $V_{IN} = V_{CC}$ or GND</td>
<td></td>
<td></td>
<td>±1</td>
<td>$\mu$A</td>
</tr>
<tr>
<td><strong>$I_{off}$</strong></td>
<td>$V_{CC} = 0$, $V_{O} = 0$ to $5.5$ V, $V_I = 0$</td>
<td></td>
<td></td>
<td>1</td>
<td>$\mu$A</td>
</tr>
<tr>
<td><strong>$I_{CC}$</strong></td>
<td>$V_{CC} = 3.6$ V, $I_{I/O} = 0$, Switch ON or OFF, $V_{IN} = V_{CC}$ or GND</td>
<td></td>
<td></td>
<td>0.7</td>
<td>2</td>
</tr>
<tr>
<td><strong>$\Delta I_{CC}$§</strong></td>
<td>Control inputs</td>
<td>$V_{CC} = 3.6$ V, One input at 3 V, Other inputs at $V_{CC}$ or GND</td>
<td></td>
<td></td>
<td>0.14</td>
</tr>
<tr>
<td><strong>$C_{in}$</strong></td>
<td>Control inputs</td>
<td>$V_{CC} = 3.3$ V, $V_{IN} = 5.5$ V, $3.3$ V, or $0$</td>
<td></td>
<td></td>
<td>2.5</td>
</tr>
<tr>
<td><strong>$C_{io(OFF)}$</strong></td>
<td>$V_{CC} = 3.3$ V, Switch OFF, $V_{IN} = V_{CC}$ or GND, $V_{I/O} = 5.5$ V, $3.3$ V, or $0$</td>
<td></td>
<td></td>
<td>3.5</td>
<td>5</td>
</tr>
<tr>
<td><strong>$C_{io(ON)}$</strong></td>
<td>$V_{CC} = 3.3$ V, Switch ON, $V_{IN} = V_{CC}$ or GND, $V_{I/O} = 5.5$ V, $3.3$ V, or $0$</td>
<td></td>
<td></td>
<td>9</td>
<td>11</td>
</tr>
<tr>
<td><strong>$r_{on}$#</strong></td>
<td></td>
<td>$V_{CC} = 2.3$ V, TYP at $V_{CC} = 2.5$ V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{I} = 0$, $I_O = 30$ mA</td>
<td></td>
<td></td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{I} = 1.7$ V, $I_O = −15$ mA</td>
<td></td>
<td></td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{I} = 2.4$ V, $I_O = −15$ mA</td>
<td></td>
<td></td>
<td>5</td>
</tr>
</tbody>
</table>

$V_{IN}$ and $I_{IN}$ refer to control inputs. $V_I$, $V_O$, $I_I$, and $I_O$ refer to data pins.

† All typical values are at $V_{CC} = 3.3$ V (unless otherwise noted), $T_A = 25^\circ$C.

‡ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}$ or GND.

¶ This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

# Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

### Switching Characteristics

**Over Recommended Operating Free-Air Temperature Range (unless otherwise noted) (see Figure 3)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>$V_{CC} = 2.5$ V ± $0.2$ V</th>
<th>$V_{CC} = 3.3$ V ± $0.3$ V</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN</td>
<td>MAX</td>
<td>MIN</td>
</tr>
<tr>
<td><strong>$f_{OE}$¶</strong></td>
<td>$OE$</td>
<td>A or B</td>
<td>10</td>
<td>20</td>
<td>MHz</td>
</tr>
<tr>
<td><strong>$t_{pd}$‡</strong></td>
<td>A or B</td>
<td>B or A</td>
<td>0.12</td>
<td>0.2</td>
<td>ns</td>
</tr>
<tr>
<td><strong>$t_{en}$</strong></td>
<td>$OE$</td>
<td>A or B</td>
<td>2.8</td>
<td>7.1</td>
<td>ns</td>
</tr>
<tr>
<td><strong>$t_{dis}$</strong></td>
<td>$OE$</td>
<td>A or B</td>
<td>1</td>
<td>5.8</td>
<td>ns</td>
</tr>
</tbody>
</table>

¶ Maximum switching frequency for control input ($V_O > V_{CC}$, $V_I = 5$ V, $R_L \geq 1$ M$\Omega$, $C_L = 0$)

‡ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
Figure 1. Typical \( r_{\text{on}} \) vs \( V_I \), \( V_{\text{CC}} = 3.3 \) V and \( I_O = -15 \) mA

Figure 2. Typical \( I_{\text{CC}} \) vs OE Switching Frequency, \( V_{\text{CC}} = 3.3 \) V
PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

<table>
<thead>
<tr>
<th>TEST</th>
<th>VCC (V)</th>
<th>S1</th>
<th>RL (Ω)</th>
<th>VI (V)</th>
<th>CL (pF)</th>
<th>VΔ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>tpd(s)</td>
<td>2.5 V ± 0.2 V</td>
<td>Open</td>
<td>500 Ω</td>
<td>VCC or GND</td>
<td>30 pF</td>
<td>0 V</td>
</tr>
<tr>
<td></td>
<td>3.3 V ± 0.3 V</td>
<td>Open</td>
<td>500 Ω</td>
<td>VCC or GND</td>
<td>50 pF</td>
<td>0.15 V</td>
</tr>
<tr>
<td>tplz/tplz</td>
<td>2.5 V ± 0.2 V</td>
<td>2 × VCC</td>
<td>500 Ω</td>
<td>GND</td>
<td>30 pF</td>
<td>0.15 V</td>
</tr>
<tr>
<td></td>
<td>3.3 V ± 0.3 V</td>
<td>2 × VCC</td>
<td>500 Ω</td>
<td>GND</td>
<td>50 pF</td>
<td>0.15 V</td>
</tr>
<tr>
<td>tphz/tphz</td>
<td>2.5 V ± 0.2 V</td>
<td>GND</td>
<td>500 Ω</td>
<td>VCC</td>
<td>30 pF</td>
<td>0.15 V</td>
</tr>
<tr>
<td></td>
<td>3.3 V ± 0.3 V</td>
<td>GND</td>
<td>500 Ω</td>
<td>VCC</td>
<td>50 pF</td>
<td>0.15 V</td>
</tr>
</tbody>
</table>

NOTES:
A. CL includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50 Ω, tr ≤ 2.5 ns, tf ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. tPLZ and tPHZ are the same as tDIS.
F. tPZL and tPZH are the same as tEN.
G. tPLH and tPHL are the same as tpd(s). The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74CB3Q3244DBGQ</td>
<td>ACTIVE</td>
<td>SSOP</td>
<td>DBQ</td>
<td>20</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>CB3Q3244</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74CB3Q3244DGVR</td>
<td>ACTIVE</td>
<td>TVSOP</td>
<td>DGV</td>
<td>20</td>
<td>2000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>BU244</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74CB3Q3244PW</td>
<td>LIFEBUY</td>
<td>TSSOP</td>
<td>PW</td>
<td>20</td>
<td>70</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>BU244</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74CB3Q3244PWR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>20</td>
<td>2000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>BU244</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74CB3Q3244RGYR</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGY</td>
<td>20</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>BU244</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**
- Reel Diameter
- Reel Width (W1)

**TAPE DIMENSIONS**
- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**
- Pocket Quadrants
- Sprocket Holes
- User Direction of Feed

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74CB3Q3244DBQR</td>
<td>SSOP</td>
<td>DBQ</td>
<td>20</td>
<td>2500</td>
<td>330.0</td>
<td>16.4</td>
<td>6.5</td>
<td>9.0</td>
<td>2.1</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>SN74CB3Q3244DGVR</td>
<td>TVSOP</td>
<td>DGV</td>
<td>20</td>
<td>2000</td>
<td>330.0</td>
<td>12.4</td>
<td>6.9</td>
<td>5.6</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
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<td>6.95</td>
<td>7.0</td>
<td>1.4</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
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<td>SN74CB3Q3244RGYR</td>
<td>VQFN</td>
<td>RGY</td>
<td>20</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>3.8</td>
<td>4.8</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
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</table>
**TAPE AND REEL BOX DIMENSIONS**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74CB3Q3244DBQR</td>
<td>SSOP</td>
<td>DBQ</td>
<td>20</td>
<td>2500</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
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<tr>
<td>SN74CB3Q3244DGVR</td>
<td>TVSOP</td>
<td>DGV</td>
<td>20</td>
<td>2000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
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<td>TSSOP</td>
<td>PW</td>
<td>20</td>
<td>2000</td>
<td>356.0</td>
<td>356.0</td>
<td>35.0</td>
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<tr>
<td>SN74CB3Q3244RGYR</td>
<td>VQFN</td>
<td>RGY</td>
<td>20</td>
<td>3000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
TUBE

- **T** - Tube height
- **L** - Tube length
- **W** - Tube width
- **B** - Alignment groove width

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Name</th>
<th>Package Type</th>
<th>Pins</th>
<th>SPQ</th>
<th>L (mm)</th>
<th>W (mm)</th>
<th>T (µm)</th>
<th>B (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74CB3Q3244PW</td>
<td>PW</td>
<td>TSSOP</td>
<td>20</td>
<td>70</td>
<td>530</td>
<td>10.2</td>
<td>3600</td>
<td>3.5</td>
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</tbody>
</table>
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO-137 variation AD.
MECHANICAL DATA

DGV (R-PDSO-G**) PLASTIC SMALL-OUTLINE

24 PINS SHOWN

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
   14/16/20/56 Pins – MO-194

<table>
<thead>
<tr>
<th>PINS **</th>
<th>14</th>
<th>16</th>
<th>20</th>
<th>24</th>
<th>38</th>
<th>48</th>
<th>56</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIM A MAX</td>
<td>3.70</td>
<td>3.70</td>
<td>5.10</td>
<td>5.10</td>
<td>7.90</td>
<td>9.80</td>
<td>11.40</td>
</tr>
<tr>
<td>A MIN</td>
<td>3.50</td>
<td>3.50</td>
<td>4.90</td>
<td>4.90</td>
<td>7.70</td>
<td>9.60</td>
<td>11.20</td>
</tr>
</tbody>
</table>

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
   14/16/20/56 Pins – MO-194
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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